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Testing of leakage current failure in ASIC devices exposed to total ionizing dose environment using design for testability techniques

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TESTING OF LEAKAGE CURRENT FAILURE IN ASIC DEVICES EXPOSED TO TOTAL IONIZING DOSE ENVIRONMENT USING DESIGN FOR TESTABILITY TECHNIQUES

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Abstract

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Testing of Leakage Current Failure in ASIC Devices Exposed to Total Ionizing Dose Environment Using Design for Testability Techniques

By Assem Mohamed

Due to the advancements in technology, electronic devices have been relied upon to operate under harsh conditions. Radiation is one of the main causes of different failures of the electronics devices. According to the operation environment, the sources of the radiation can be terrestrial or extra-terrestrial. For terrestrial the devices can be used in nuclear reactors or biomedical devices where the radiation is man-made. While for the extra- terrestrial, the devices can be used in satellites, the international space station or spaceships, where the radiation comes from various sources like the Sun. According to the operation environment the effects of radiation differ. These effects falls under two categories, total ionizing dose effect (TID) and single event effects (SEEs).

TID effects can be affect the delay and leakage current of CMOS circuits negatively. The affects can therefore hinder the integrated circuits' operation. Before the circuits are used, particularly in critical radiation heavy applications like military and space, testing under radiation must be done to avoid any failures during operation. The standard in testing electronic devices is generating worst case test vectors (WCTVs) and under radiation using these vectors the circuits are tested. However, the generation of these WCTVs have been very challenging so this approach is rarely used for TIDs effects.

Design for testability (DFT) have been widely used in the industry for digital circuits testing applications. DFT is usually used with automatic test patterns generation software to generate test vectors against fault models of manufacturer defects for application specific integrated circuit (ASIC.) However, it was never used to generate test vectors for leakage current testing induced in ASICs exposed to TID radiation environment.

The purpose of the thesis is to use DFT to identify WCTVs for leakage current failures in sequential circuits for ASIC devices exposed to TID. A novel methodology was devised to identify these test vectors. The methodology is validated and compared to previous non DFT methods. The methodology is proven to overcome the limitation of previous methodologies.

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LIST OF ABBREVIATIONS

ASIC	Application Specific Integrated Circuits
ATE	Automatic Test Equipment
BIST	Built-In Self-Test

CMOS	Complementary Metal Oxide Semiconductor
CUT	Circuit Under Test
DFT	Design For Testability
EDA	Electronic Design Automation
IC	Integrated Circuit
LFSR	Linear Feedback Shift Register
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
NMOS	N-type metal-oxide-semiconductor logic
ORA	Output Response Analyzer
PMOS	P-type metal-oxide-semiconductor logic
RILC	Radiation Induced Leakage Current
SEE	Single Event Effect
SEGR	Single Event Gate Rupture
SEL	Single Event Latch up
SEU	Single Event Upset
SSI	Small Scale Integration
TID	Total Ionizing Dose
VLSI	Very Large Scale Integration
WCTV	Worst-Case Test Vector

1. Summary

Electronic devices are used everywhere, from space to the hands of almost every person on earth. Some of these places have high doses of ionizing radiation. The radiation sources can be extra-terrestrial, terrestrial and man-made. For example, some particles are trapped around Earth's atmosphere. The sources of these particles can be the sun or high energy galactic cosmic rays. While on Earth these sources can range from neutrons found in the atmosphere to alpha particles emitted from the decay of some elements on the devices. While man-made radiation is found mainly in nuclear reactors, biomedical devices and high energy particles physics experiments.

The radiation affects the electronic devices in many ways which may damage the device and hence hinder normal operations. According to the environment and the radiation source the effects are different. The effects can be permanent; like total ionizing dose, or temporary; like single even upset, gate rapture and latch up.

Design for testability (DFT) has been around for many years. The field is saturated with ideas and well established in the industry. This field was developed due to the limitations of controllability and observability of large sequential electronic circuits. DFT replaces normal memory elements with scan cells, which increases the controllability and observability of the circuits. However, it was never used to test the effects of TID on ASIC chips leakage current.

To ensure proper operations of the devices, a standard procedure to test the effects of radiation on electronic circuits must be implemented. MIL-STD-883, method 1019 highlights the use of worst case test vectors (WCTV) to test the circuits. However, these vectors are very hard to generate in complex circuits.

Fault modeling is a very important field in testing VLSI devices, due to the fact that simulations is one of the main cores of the field. Multiple fault models for leakage current were introduced in [1]–[4] and used to generate WCTV. However, these models had their limitations. As these models couldn't generate WCTV for large sequential circuits due to the complexity of their design. Previous effort [4] uses a genetic algorithm instead of searching exhaustively to generate the WCTV of leakage current failures.

In this thesis a new methodology to model sequential circuit is introduced. The methodology combines the modeling done in [2], [3] while using DFT and [4] to solve the limitations of the model introduced in [3]. It introduces a new methodology to model cyclic and cyclic free sequential circuits so they can be used to generate WCTV, while using [4] to generate the WCTV.

The methodology then was validated using the simulation of 8 designs. Multiple simulations were made to verify the compatibility of the methodology. Like simulations to verify the genetic algorithm introduced in [4]. Then modelling of [2], [3]. Then new simulation to explore the limits of [3] were made . Last but not least an enhanced model was introduced in the special case of cyclic free pipelined sequential circuits was also introduced and verified against a model introduced in [3].

The thesis is divided as follow. Section two explains the sources of radiation and the radiation intense electronic devices environments. Section three deals with the effect of radiation on the electronic device. Section four introduces DFT and its importance. Section five discuss the current field of leakage current testing and fault modelling. Section six introduces the proposed methodology and discusses the simulation results. Finally, Section seven discusses the conclusions and future work.

2. Radiations sources and effects on CMOS

When electronic devices are subjected to radiation, during operation in harsh environments with radiation sources, the devices can be damaged in different ways. This damage may result in improper operation of said devices. There are many sources of radiation an electronic device can be subjected to, these sources depend on the physical place of operation of the devices. There are three main sources; terrestrial, extra-terrestrial and man-made radiation. The terrestrial radiation can be due to alpha particles in the devices or neutrons in the atmosphere. While the extra-terrestrial radiation can originate from many sources like, the sun, high energy galactic cosmic rays or particles trapped under the Earth's atmosphere. Electronic devices can be subjected to man-made radiation mainly in three places; nuclear reactors, biomedical devices and high energy physics experiments. When the devices are subjected to ionizing radiation some of the radiation's energy is transferred to the devices which may cause many different effects of said devices. These effects can affect the devices in many ways like increasing the delay or leakage current and it even causes faults in the memory. In the end these effects can cause functional failure to the electronic devices.

2.1 Radiation sources

Nowadays electronic devices are used everywhere on or outside Earth. Thus, some of these devices will be subjected to Terrestrial, Extra-terrestrial or man-made radiation. Usually the environments that contains radiation sources are highly critical, so the devices must be capable to operate under these conditions.

2.1.1 Terrestrial environment Radiation

There are two main sources of terrestrial radiation, Alpha particles radiated from the integrated circuits (IC) defects and Neutrons inside the Earth's atmosphere.

Due to the radioactive decay of some on-chip defected material, alpha particles are produced. These materials can be categorized into four elements Platinum, Uranium, Thorium and Hafnium. These elements are used during the fabrication process of the integrated circuits. These elements emit alpha particles which cause soft

errors during the operation of the ICs. As the feature size of the devices gets shorter the alpha particles induced soft errors increases. Beside the alpha particles, Muons particles are being investigated due to their increased effects on the devices as the devices are getting smaller[5].

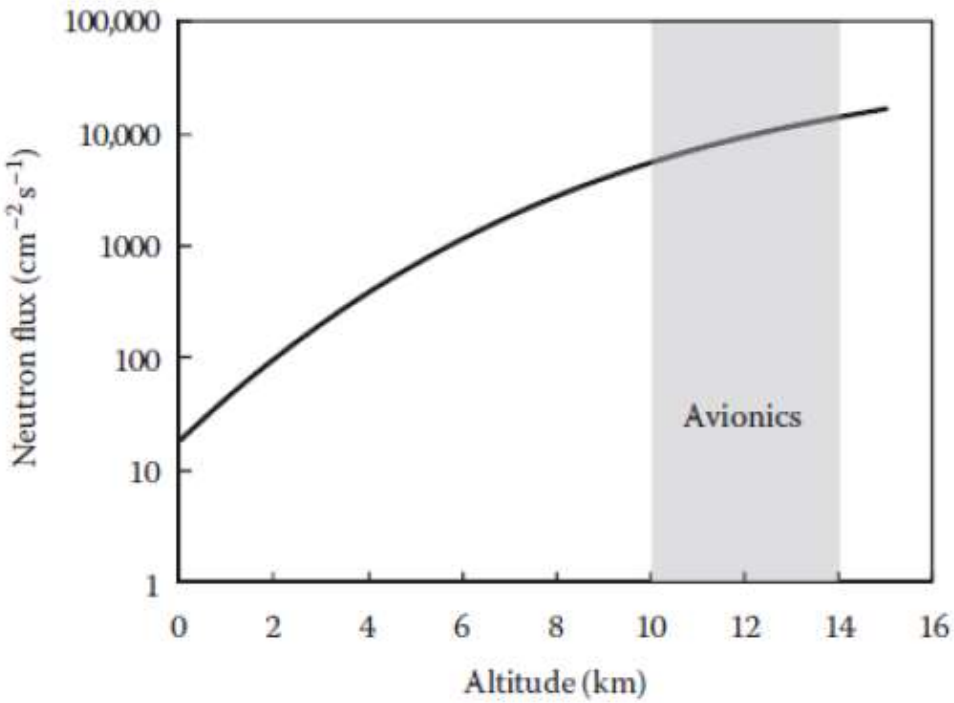

Figure 1 Terrestrial environment flux (neutron flux per cm-2s-1) vs the altitude (Km) [2]

Due to the interaction of the galactic cosmic rays and the outer layers of the Earth's atmosphere Neutrons are produced. These uncharged Neutrons have high energy so when they hit the devices they can transmit energy to them and thus a nuclear reaction may occur. When the cosmic rays hit the Earth's atmosphere gases, oxygen and nitrogen, particles are produced. These particles include neutrons, protons, ions and muons. Due to the multiplication effect of the atmosphere's shielding, as the rays further penetrate the Earth's atmosphere the number of these particles decreases. Figure 1 shows the relationship between the neutron flux and the altitude. The neutron flux is very high in the altitude in which the Avionics operates thus Avionic electronic devices operating in a must be capable of withstanding these effects[6].

2.1.2 Extra-terrestrial environment Radiation

Due to the many sources of radiation in the extra-terrestrial environment is very challenging for an electronic device to operate in. There are three main sources of radiation in space; solar events, Galactic and extra-galactic cosmic rays and magnetosphere trapped particles.

The sun ionizing particles energy can reach over 10 MeV which depends on the solar cycles. The solar activity have two phase; high and low. The high activity phase lasts for seven years while the low for four and then the cycle repeats. The events during the cycle can be classified into two classifications, solar particle events and loss of Sun's mass. The solar particles events can be solar flares or coronal mass ejections. While the loss of mass from the sun is due to protons or electrons escaping the Sun's gravity. These particles interact with the Earth's manganic field as the have their own.

Galactic and extra-galactic cosmic rays emit a lot of energy when it hits the devices. The sources of these rays are external to the solar system. These rays are of unknown sources and acceleration methods. They travelled through the galaxy repeatedly for millions of years as they reached the speed of light. They can consist of many elements however they're mostly protons. They have energy over 10^{11} GeV which makes it very easy for them to penetrate objects and very hard to economically shield the devices from them.

The interaction between the earth's magnetic field and the solar wind's causes the formation of objects called magnetospheres. These objects have to components one from the solar winds and the other from the Earth's magnetic failed. Electrons are trapped inside the magnetospheres due to the barrier the Earth's magnetic fields forms against the solar winds and flares while protons are trapped due to the barrier from the Galactic cosmic rays. The energy of the particles varies from 5 MeV to 800 MeV. These particles, trapped inside the magnetosphere, spirals between the two poles, thus forming a radiation belt surrounding the earth called Van Allen radiation belt. The belt is divided into two layers, the outer layer containing electrons and the inner layer consisting of both electrons and protons. While the outer layer's electrons have energy that reaches 10 MeV the inner layer particle's energy ranges in the hundreds of KeV.

Modeling space's ionizing radiation has proven to be very challenging for many reasons. Some of them are due to the dependency on the cycles of the solar activity.

Also the amount is very dependent on the location of the device both inside its carrier, due to shielding, and among which layer of space. It's not economically viable to overdesign components sent into space as it's very expensive to increase weight to space-carriers; satellites of space-crafts. Also due to the shortage of power, the devices complexity can't be a viable solution[6].

2.1.3 Artificially Man-Made Radiation

The last source of radiation is the man-made radiation. It can be found in places like biomedical devices and equipment of high energy particle colliders. For example, inside the Large Hadron Collider the radiation exceeds 100 Mrad(SI) Compared to the 100 Krad(Si) that most space missions are exposed to. Therefore, these devices have their own libraries (rad-hard) that avoid normal standard designs layouts, so it can endure the high level of radiation. Another source of radiation is Nuclear power plants. For example, the ITER neural beam facility have fluxes with energy reaching 14 MeV with the does reaching 50 Rad(SI) per operating hour[7].

2.2 Radiation

2.2.1 Mechanisms

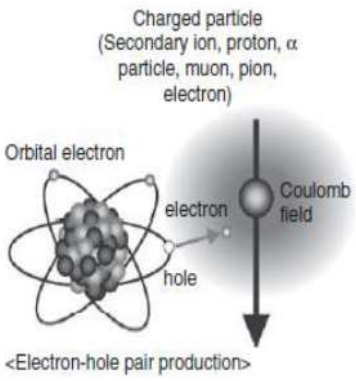

Figure 2: Charged particle interaction with an atom

The radiation effects must be studied to design electronic devices that can operate under radiation. When a charged particle approaches an atom some of the atom's electrons gets extracted due to the secondary particle's Coulomb force thus creating an electron-hole pair as shown in Figure 2. If the material is metal the electrons

recombine with the protons without any radiation effect due to the lack of band gap between the electrons and the holes and thus their high mobility. However for dielectric materials like SiO_2, according to the field applied on the devices, holes can accumulate resulting in parasitic energy level either on the surface or inside the dielectric oxide and therefore it result in effects called Total Ionization Does (TID) as Figure 3 shows[8].

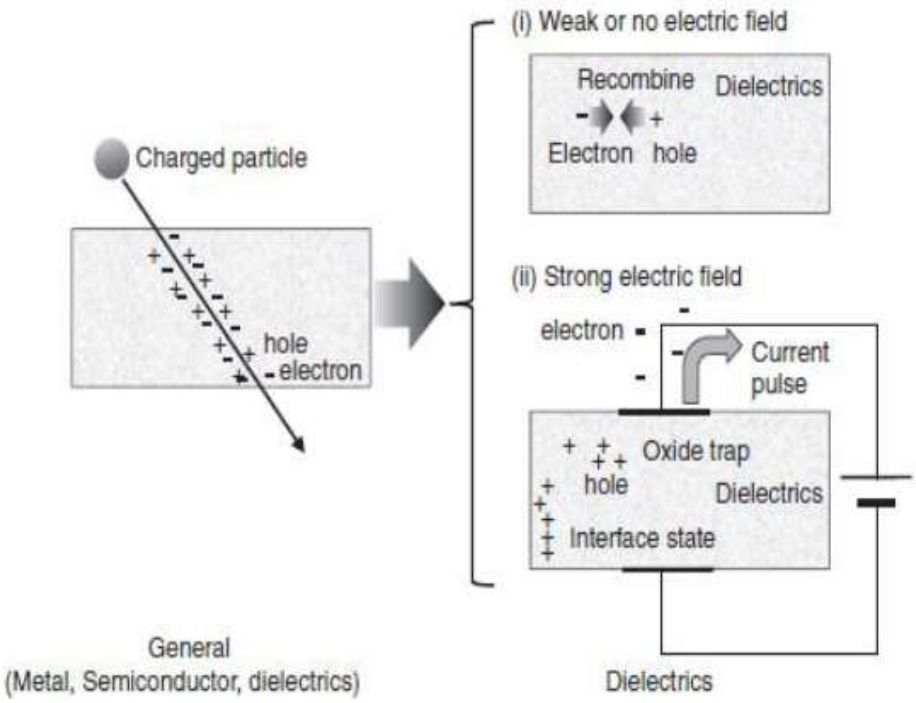

Figure 3: High energy charged particle effects on metal and dielectric material ***[8]***

As shown in Figure 4, radiaction can affect the material by dispalcing its lattice. This effect is due to the collsion of photons and neutrons and it causes dislocation loops and interstitials which affects the material charataristics [8].

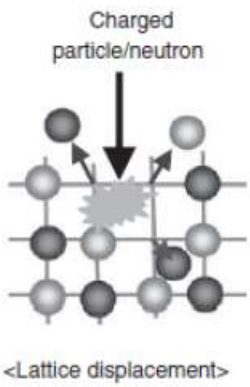

*Figure 4: Radiation effect on lattice displacement****[8]***

2.2.2 Effects

The effects of radiation depend on the mechanism mentioned in the previous section more than the source of the radiation itself or the environments of the operating device. The effects can be divided into two categories; total ionization dose effects and single even effects

2.2.2.1 Total Ionization Dose

The definition of Total Ionization Dose (TID) is the value of energy that us transferred from the source of ionization radiation to the radiation exposed material. TID is measured in rad. One rad is equal to 100 ergs transferred per target material gram. When talking about radiation the amount of radiated dose is usually followed with the target material. Gray (Gy) is another way to measure TID, 100 Gy make one rad. TID affects the electronic devices mainly in two ways inside the insulation layer; generating interface states and trapping positive charges (holes)[6]. TID occurs mainly in two places; Extra-terrestrial environment and man-made radiation environments like nuclear reactors and high energy particle accelerators.

Silicon dioxide (SiO_2) is very sensitive to TID. Due to the importance of SiO_2 in the metal oxide semiconductor (MOS) device structure, the TID affects the electronic devices gravely. As shown in Figure 5, the band diagram of a positive biased n-Mos device with p-substrate and the effect of TID on the device.

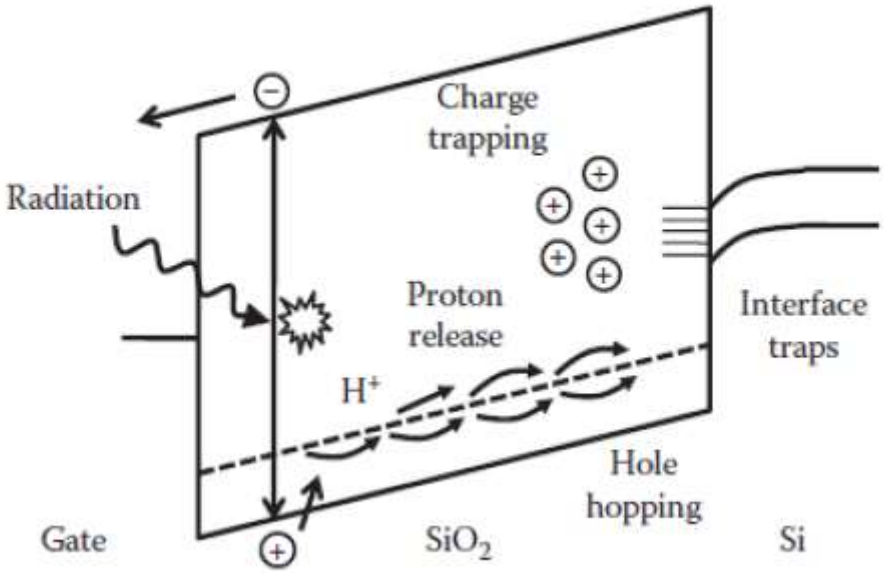

Figure 5: TID effects on n-MOS ***[6]***

When energy is transferred to the SiO_2, pairs of electron-holes are created. Initial recombination is the process when the electrons-hole pairs are recommended immediately in the oxide layer. According to the applied electric field the energy transferred from the source to the particles and the charge to the particle; the number of pairs that go through the initial recombination change. Charge yield is defined as the pairs didn't recombine in the initial recombination. Due to the electrons high mobility these electrons are attracted to the biased gate, which is positive. However, the heavier low mobility holes are slower, in comparison to the electrons, to get attracted to the silicon substrate. Due to the fact that the holes remain in their position or close to it, negative voltage shift is created in the threshold voltage which affects the characteristics of the device[9].

According to the applied electric field and the temperature of the device the holes that don't combine during the initial recombination move to the silicon substrate in different speeds. The holes move in a hopping matter which is called Polaron hopping. It can take a hole 10^{-17} seconds to move to the substrate at room temperature with longer time at lower temperatures. If the gate is biased positively the holes will reach the SiO_2 substrate. The holes either go into the SiO_2 substrate or get trapped in defected places that have similar density to the SiO_2 which causes a negative shift in the MOS device characteristics permanently. There for the threshold voltage of the

device is shifted and that inversion causes leakage current to increase when the device is off. The increase on leakage current causes the increase in the static power of the devices. These holes can also result in the release of the hydrogen ions. Interface traps is caused by these ions, thus exchanging the carriers with the channel. The Fermi level affects the occupancy of these ions at the interface. The interface traps creation takes longer time than the accumulation of charges because of the trapped holes. These traps result in positive change in the threshold voltage of the NMOS while having negative shit in the PMOS. Which in turn causes more delay to the devices thus decreasing its capability [9].

2.2.2.2 Single-Event

When high energy particles pass through a sensitive region it results in single-event effects (SEE). According to the effects of these particle the effects can be divided into two classes; soft and hard. When the damages to the device is temporary the effects is considered soft. These mainly happens in memory circuits. However, if the damage is permanent it's called hard errors like the rapture of the gate. These SEE can affect the operation of the device depending on the type of effect. There are three main types of SEE; single event gate rapture (SEGR), single-event upset (SEU) and single event latch-up (SEL). SEGR is when a rapture in the gate occurs and this is considered a hard SEE. SEU is when a soft SEE causes a flip in a bit inside the memory which is caused by one ionizing particle. However, when the bit in the memory is re-written the error will be corrected that's why it's considered a soft error. Last is the SEL, which happens when the parasitic bipolar structure was activated due to the radiation. This results in the surge of the current supplied to the device. The device can be damaged if it took a lot of time to cut off the power of the circuit.

3. Total Ionizing Dose effects on CMOS

Radiation result in a lot of effects on the operation of electronic devices. One of these effects is called Total Ionizing dose effects. The material of the devices are damaged due to TID and thus compromising the operation of the said devices. This chapter will highlight these TID effects furthermore while discussing some ways to test the devices.

3.1 TID effects on CMOS

When SiO_2 is exposed to TID, the high energy particles cause the generation of electron hole pairs when it interacts with the SiO_2 atoms. According to the energy transferred to the material, the density of the pairs changes proportionally. The loss of energy per unit length is defined by the linear energy transfer (LET) which has dE/dx as its units. When the energy that is transferred to the material can be defined as ΔE_E while the energy that leaves the material can be defined as ΔE_L in equation 1. While $\frac{\mu_{en}}{\rho}$ is the mass attenuation coefficient and ρ is the material density and finally Δx is the thickness of the material[10].

$$\Delta E_L(\gamma) = \Delta E_E(\gamma)\, e^{-\frac{\mu_{en}}{\rho}\rho\Delta x} \tag{1}$$

As shown Figure 6, the protons' LET, also known as the stopping power, is inversely proportional to their energy. However with the electrons it starts to decrease then increase again after the 1 MeV mark [11].

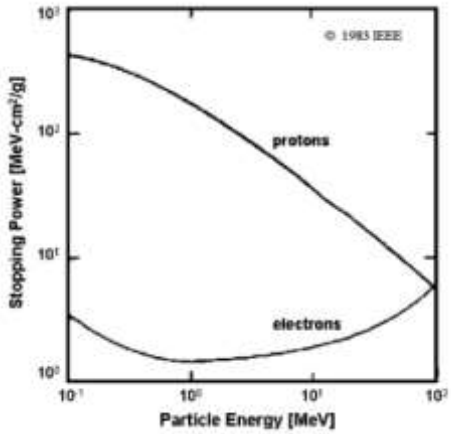

Figure 6: the effect of particle energy on the stopping power of the protons and electrons ***[11]***

Due to the electrons high mobility, the electrons that were generated from the radiation of the charged particles move towards the positive gate very fast. On the other hand, the holes move very slowly towards the silicon compared to the electrons. Some of the holes get trapped and thus forming positive oxide trap charges [12].

At the interface of the silicon some interface taps also occur. Hydrogen ions that drifts to the silicon interface interacts with each other causing the formation of these traps. However, these traps compared to the oxide traps are generated in a longer time. These traps cause an increase in the silicon's band gap energy levels. According to the location of the Fermi level the interface taps can be either positive or negative. When the Fermi lever is lower than the trap's energy level, it results in positively charged trap as it acts as a donor. While if the level is higher the traps accepts charges and thus becomes negatively charged. In NMOS devices the positive interface trap shifts the threshold voltage positively. While in PMOS devices the positive interface traps decrease the threshold voltage [9].

According to the interface traps and the oxide charges the effects of the radiation of the MOS transistor changes. There are three main effects; Threshold shifts, mobility degradation and leakage current.

3.1.1 Threshold voltage effects

The shift in the threshold voltage (ΔV_{th}) of the MOS transistor can be due to the effect of either the oxide traps (ΔV_{ot}) or the interface traps (ΔV_{it}) or both of them combined. The equation of the shift in threshold voltage can be expressed as

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \quad (2)$$

While calculating the ΔV_{ot} and the ΔV_{it} can be expressed by the following equation.

$$\Delta V_{ot,it} = \frac{-1}{C_{ox}\, t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x dx \quad (3)$$

$\rho_{ot,it}(x)$ Is the distribution of charges that was induced by the radiation as oxide charge traps or the interface traps. The threshold shit is positive for the negative charges while negative for the positive charges[9].

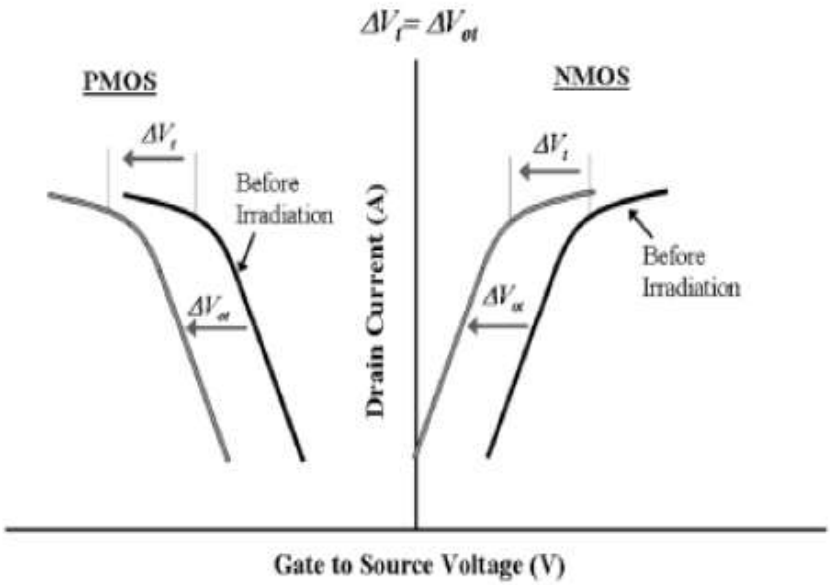

*Figure 7: oxide charge traps effect on the shift in Vth**[11]***

Figure 7 shows the effect the oxide traps have over both NMOS and PMOS devices. For NMOS devices the oxide-charge traps causes a decrease in the threshold value and therefore the biasing point of V_{gs} is shifted to the left (negative value) and thus increasing the current during the off state of the transistor. The same negative shift happens to the PMOS which increases the value of V_{th} and therefore decreases the drive and leakage current[11].

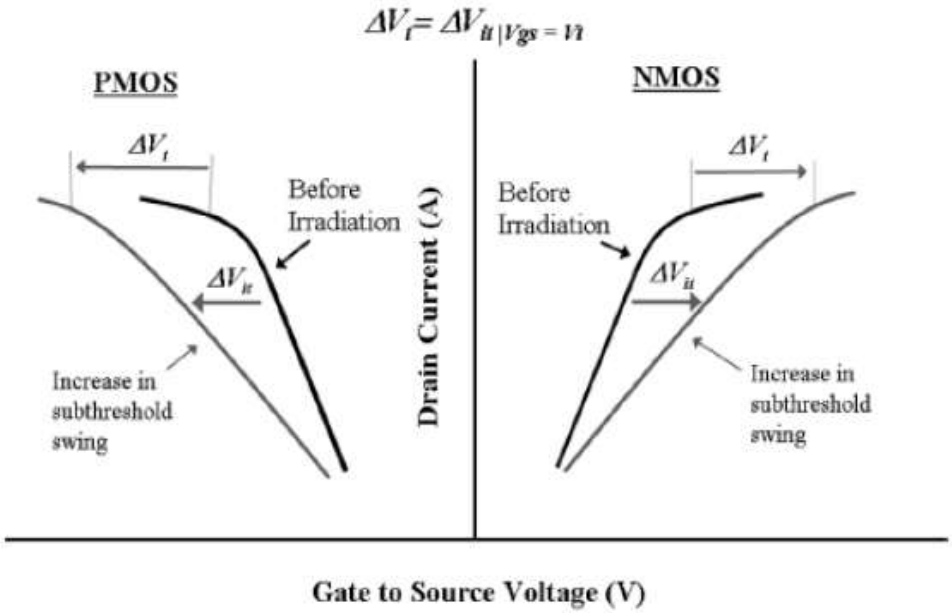

Figure 8: Interface traps effects on the shift in Vth

While Figure 8 shows the effects of interface traps on the threshold voltage. The radiation causes both the V_{th} swings of the NMOS and PMOS device to increase compared to the oxide charge traps. While the interface traps causes the V_{th} of the NMOS to increase it causes the PMOS V_{th} to decrease which affects the drive and leakage current of the transistors [11].

According to the duration of the radiation either the oxide-charge traps or the interface traps effects can be more dominant. If the radiation has high dose and sort time the oxide-charge traps will dominate as the interface traps won't be able to build up at such short time. Therefore, when the radiation is of a very high dose and very short time the V_{th} shifts to the negative in both the PMOS and NMOS. The effect of that shift in NMOS devices cause the increase in leakage current and therefore the static power of the devices which may compromise the operation of the device eventually [9].

If the dose was moderate and for a longer time both the effects of the oxide-charge traps and the interface traps affect the devices. For NMOS devices the effect of the oxide- charge traps is negative while the effect of interface traps are positive. In the end the effect on the threshold voltage cancels out or it may lead to a very small shift which may not affect the circuit. As for the PMOS both of them shifts the threshold to the left which will add up [9].

The relationship between the shift in threshold value due to the oxide-chare traps is directly proportional to the thickness of the oxide squared which means as the technology advances and the thickness decreases the effects decreases exponentially. However, as the thickness decreases a new phenomenon called shallow trench Isolation (STI) begins to take effect. Therefore in modern technologies TID is not a concern when designing the circuits because they have very low effects on the transistors with thinner gate oxide thickness as shown in Figure 9 [11].

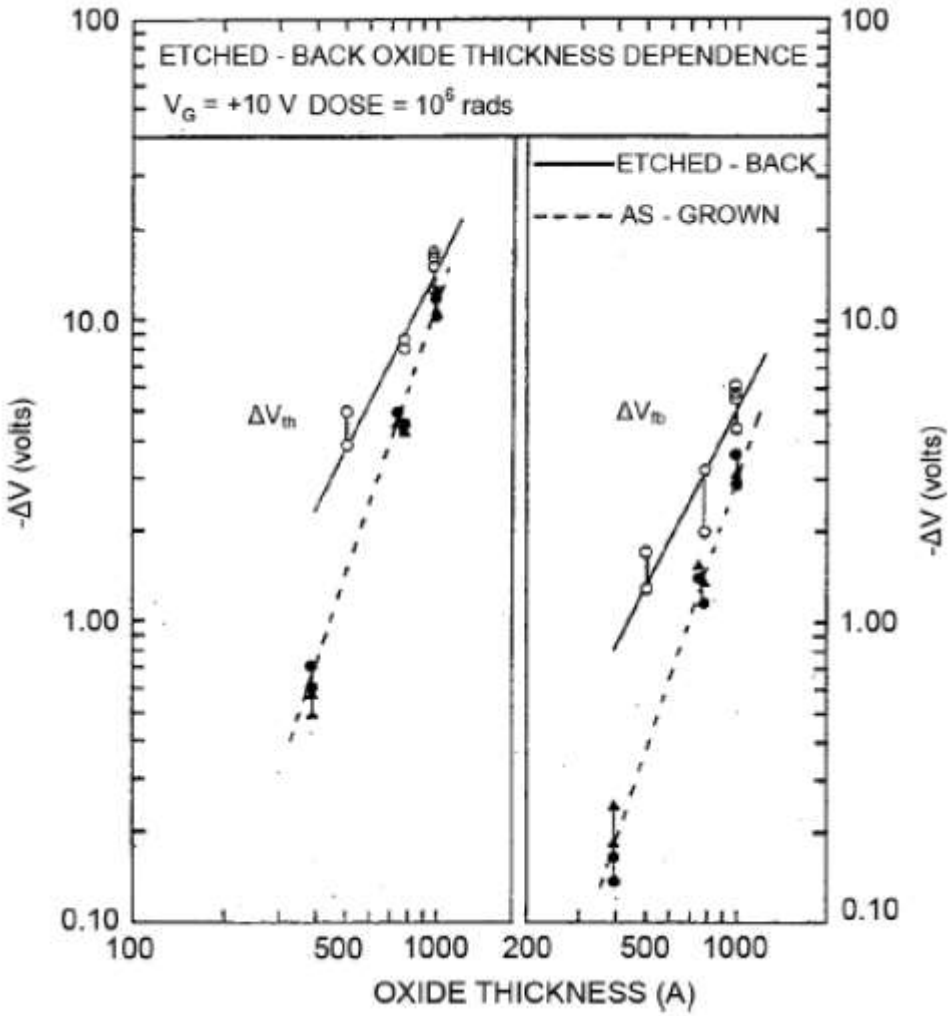

Figure 9: Vth vs oxide thickness [13]

Besides the thickness of the oxide layer, the width and length of the transistors affect the value of the threshold shift. For both the NMOS and PMOS transistor if the width is smaller the threshold shift increases. For long width devices the shift is not substantial and can be ignored. While for short channel devices (length) the value of the shift also increases as the sizes go down. This means that for devices with long

width and length the shift of the threshold voltage is not large and independent of the size of the transistor [14].

3.1.2 Carrier mobility degradation

Carrier mobility degradation of MOS transistors is the second effect of oxide charge and interface traps. When the mobility of carries decreases the drive of the MOS transistors decreases causing the decrease in the timing of the circuits and thus increasing the delay. If these effects are large timing failures may occur while the device is in the operation state.

Polaron hopping is a process that happen when the oxide–charge traps' holes that don't recombine during the initial recombination process get attracted to the substrate. The process is highly dependent on the applied field and temperature during the radiation process. The Polaron hopping also causes decrease in the mobility of the holes and increase in their mass [9]. As for the interface traps the charges that will be exchanged will happen only on the interface. Therefore, there is no barrier between that can trap the carriers at the interface of the silicon. Which means that interface traps can affect the mobility of the carriers significantly more than the oxide-charge traps [11].

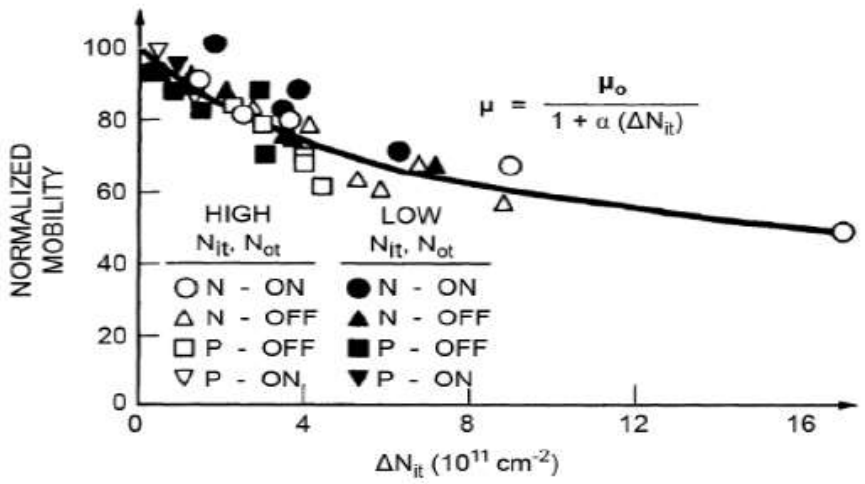

Figure 10: Normalized Mobility vs interface traps density[13]

Figure 10 shows the effects of interface traps on the mobility of the carriers. The effects of the interface traps are dominant over the oxide-charge traps because of its more efficient scattering of the carriers. Therefore it has first order effects on the carriers compared to the effects of the oxide-chare traps [13].

3.1.3 Leakage current effects

The last effect of TID radiation on CMOS technology is the radiation induced leakage current (RILC). Leakage current increases when the threshold voltage changes when the SiO_2 charges get trapped. Also, the buildup of charges in the field oxide p substrate affects the leakage currents.

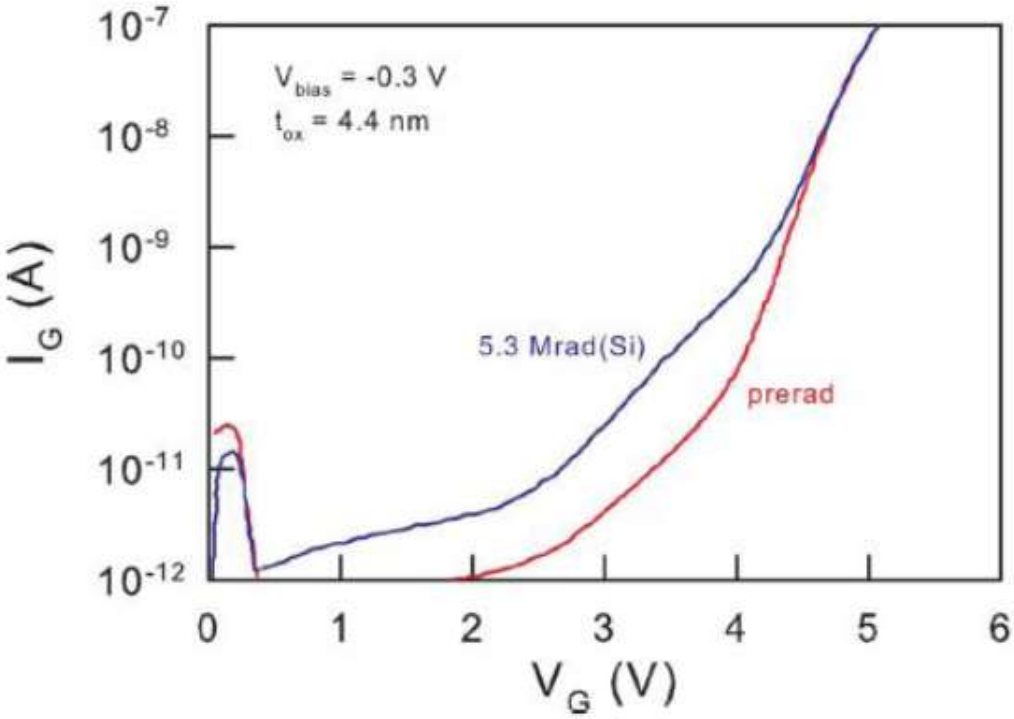

Figure 11: Gate voltage vs leakage current [12]

In Figure 11 the gate leakage currents are shown with respect to the voltage of the gate. The figure compares the leakage current of same transistor at two times, the first before getting exposed to radiation while the second after the transistor was exposed to 5.3 Mrad (Si) from gamma rays of Co-60 when the gate was biased with 0.3 volts [12].

Due to the ultra-thin gate oxide layer of the newer technologies, the modern devices are more immune to radiation damage. However, the field oxide of the modern technologies is significantly thicker than the gate oxide. Due to the proportionality of radiation response and oxide thickness the effect of TID on these modern devices is still a major concern [12].

Figure 12 shows common manufactured types of field oxides; local oxidation of silicon (LOCOS) field oxide and shallow trench field oxide. These types differ in their shape and formation method. The LOCOS field oxide was recently replaced by the fabrication manufactures with the shallow trench field oxide. As shown in (a) of the figure the charges on the LOCOS NMOS build up in the Bird's Beak area. While (b) shows where the charges accumulate in the shallow trench field oxide NMOS [12].

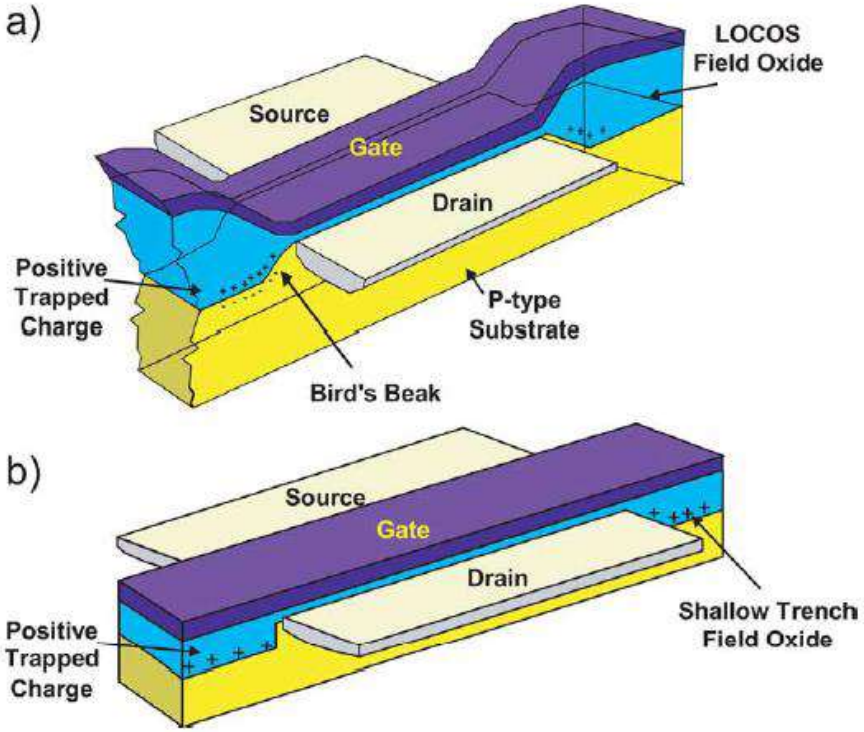

*Figure 12: Types of CMOS field oxides**[12]***

When Shallow trench isolation (STI) field oxide is exposed to high flux of ionized radiation it leakage current increases. Also, when single ions strike the substrate it damages it. Stand by current of the newer devices increases when the induced leakage current of the shallow tech isolation increases. Figure 13 shows the relationship between the standby current and the amount of radiation the devices are exposed to under a 130 nm commercial process [11].

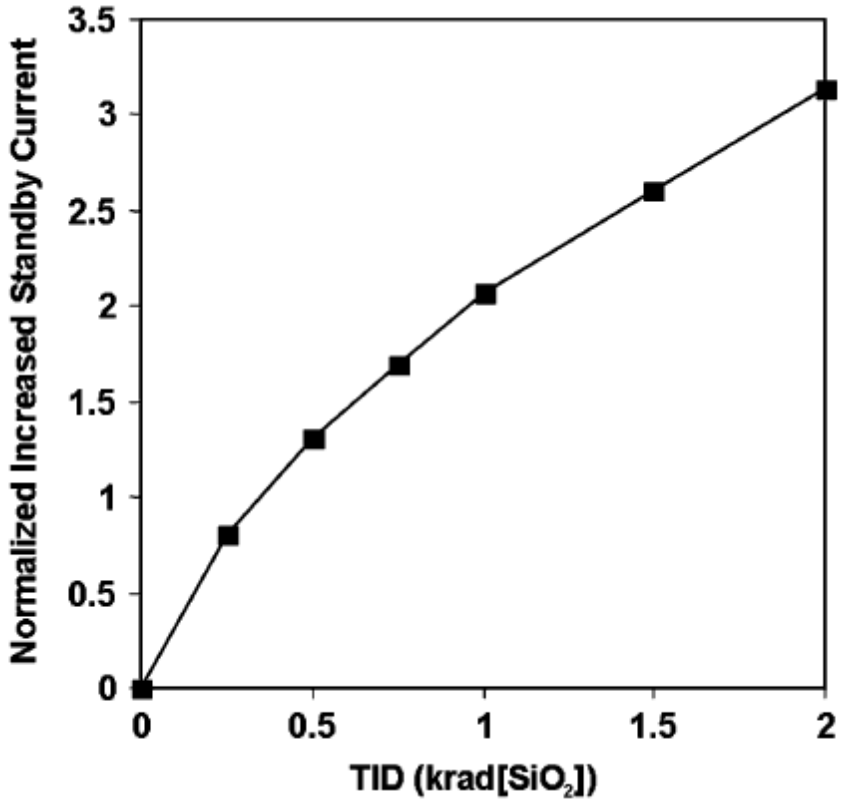

*Figure 13: Standby current vs TID under a 130 nm technology**[11]***

Leakage paths that are created when the STI devices are exposed to radiation as the charges are built-up due to the effects of TID. The leakage current hence increases the standby current of the devices. These paths are divided into two drain to source paths. One path is in a single NMOS transistor while the other path is between two NMOS transistors. The final leakage current is between the well and the source of different NMOS transistors. When the positive oxide charge traps hit p-type silicon they invert their polarity. Due to the inversion of p-type silicon layer current flows between isolated regions [11].

Built-up charges accumulate between the drain and the source to form a path for the current. These charges buildup on the side walls of the isolation oxide dielectric of the STI field oxide thus increasing the standby current of NMOS devices[11].

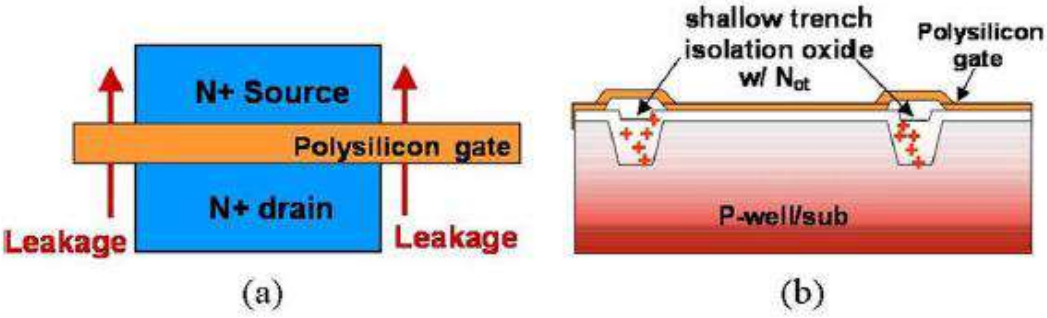

*Figure 14: a) shows the leakage path in NMOS and b) the built-up charges that causes the leakage currents**[11]***

Figure 14 shows the path of the leakage current because of the charges that buildup on the isolation oxide. While Figure 15 shows the effect of radiation on STI field TSMC 180 nm NMOS transistors. As shown in the figure as the radiation increases over 200 Krad(Si) the drain-source current increases significantly [11].

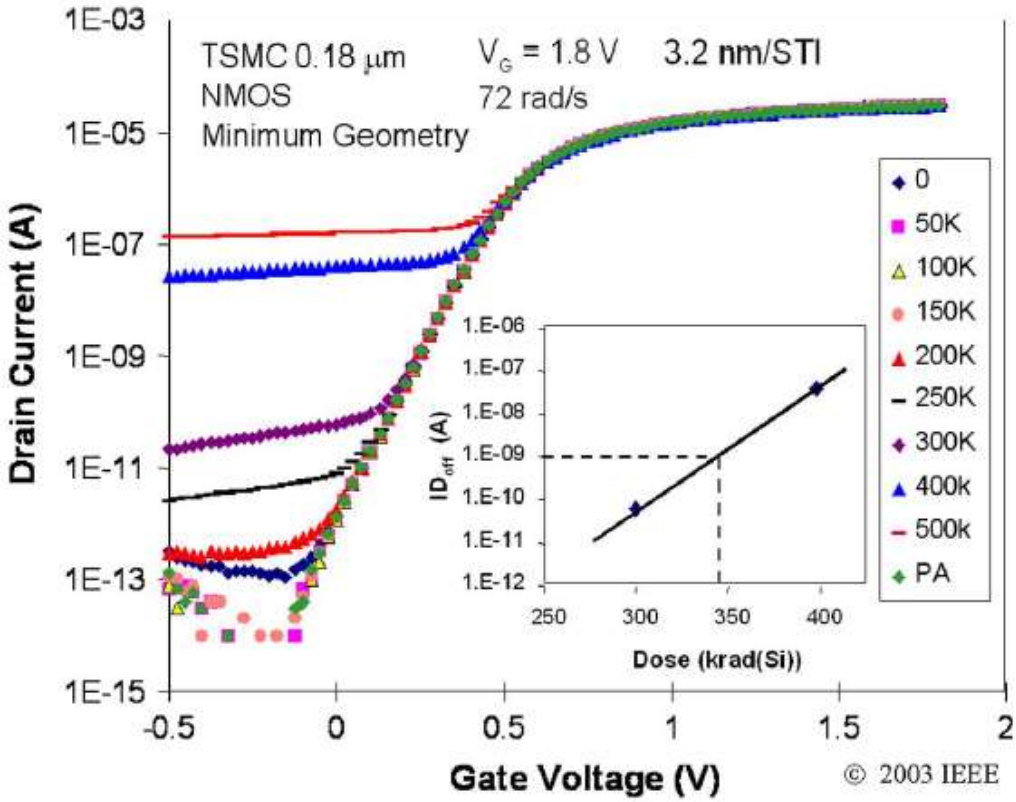

*Figure 15: Current-voltage characteristics of radiation exposed TSMC 180 nm NMOS device **[11]***

As for the well leakage current and the drain-source leakage current that happens between two NMOS devices, the path is either between two different devices of between the n^+ drain or the source as shown in Figure 16 or the source of a transistor and the n-well of the p channel of the transistor next to it shown in Figure 17 [11].

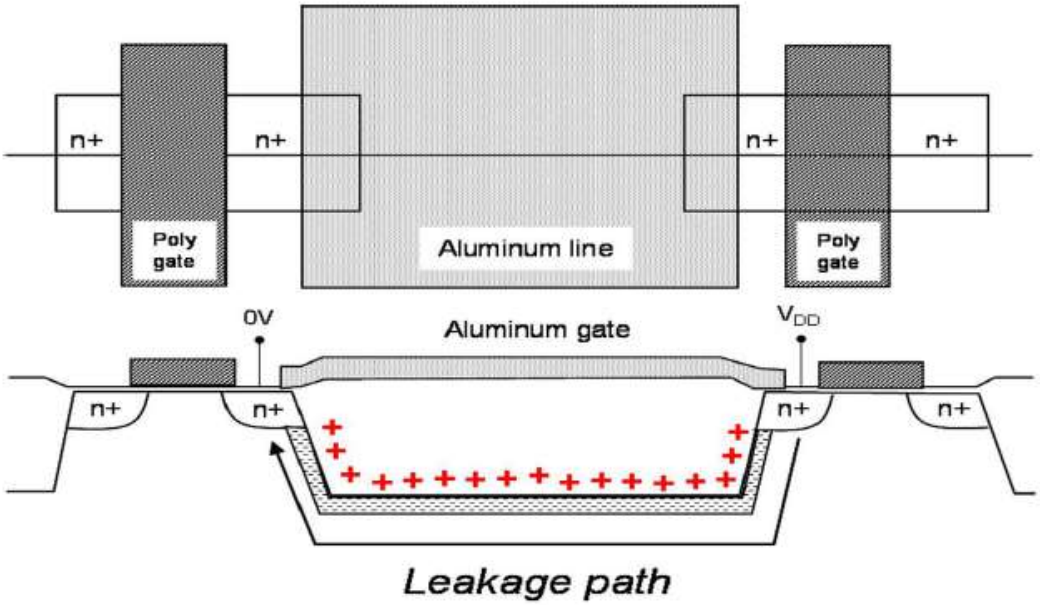

Figure 16: Leakage current between two different transistors next to each other ***[11]***

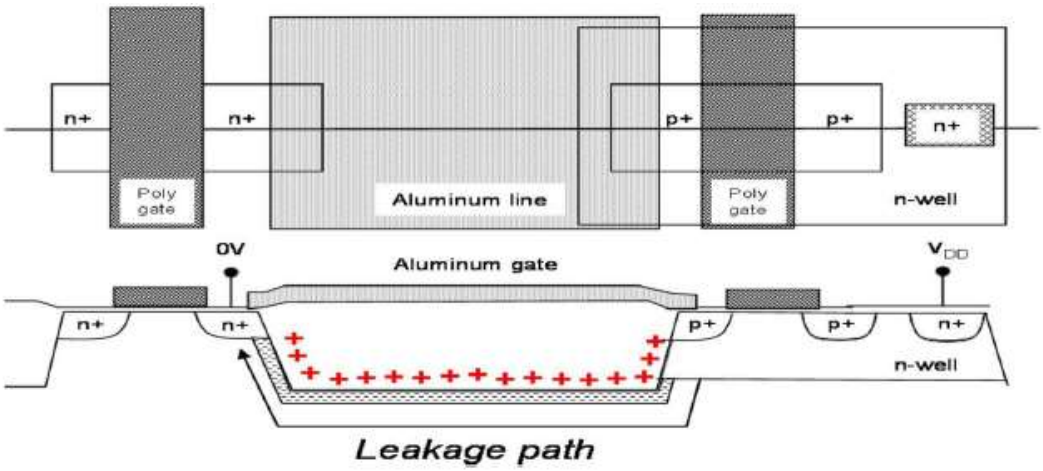

*Figure 17: Leakage current between source and the n-well of the p channel of the neighboring transistor****[11]***

Figure 18 shows the leakage current between two different transistors by taking two CMOS inverters as an example. Path (a) is the leakage of two neighboring NMOS transistors which drains current from the source to the ground due to the path between the drains of the transistors. Then the path between the PMOS of the second inverter and the NMOS of the first completes the path between VDD and ground. While path (b) drains current between the p-channel's n^+ well and the n-channel's drain of first NMOS transistor [11].

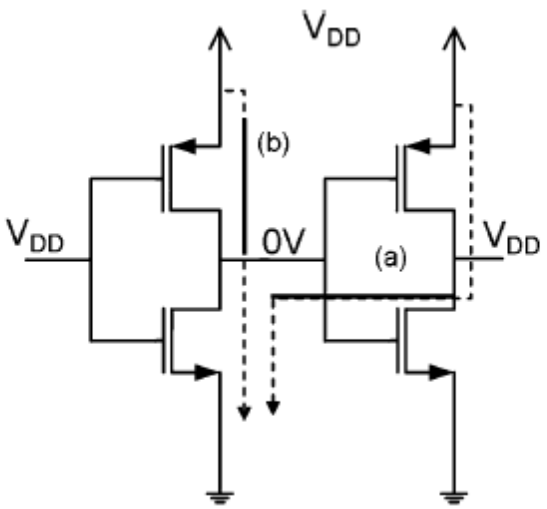

Figure 18: (a) leakage current between two adjacent NMOS transistors. (b) Leakage current between the channel and the p-channel's n^+ well ***[11]***

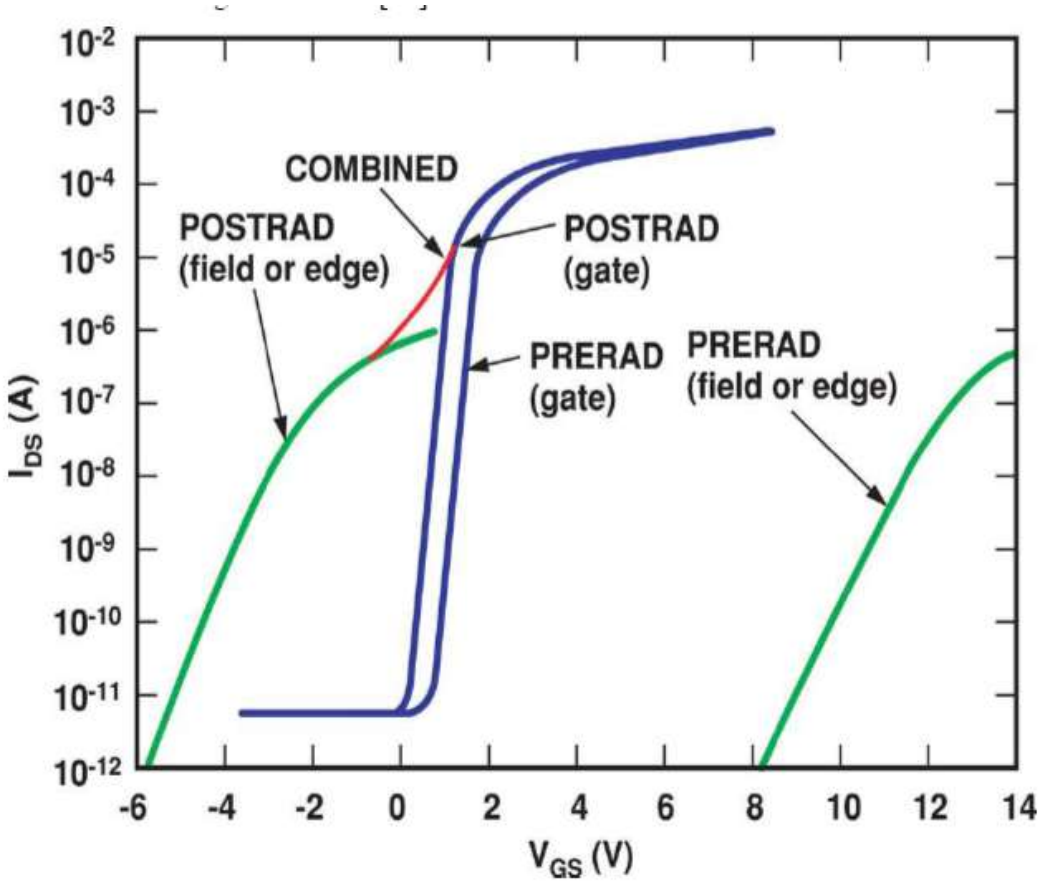

Figure 19: The effect of V_{th} shit in the leakage current of the devices vs the gate source voltage ***[9]***

Modeling the effects of the leakage current of the field oxides can be made by introducing, parallel to the gate oxide transistor, a field-oxide transistor. A formation of parasitic parallel field oxide transistor is formed at the parts where the field oxide overlaps with the gate polysilicon overlaps (the edges). Figure 19 shows that V_{th} before

radiation is larger than the post radiation V_{th}. As the charge built-up causes, a shift in V_{th} to the left (decreasing it) which results in more drain-source leakage current. If the shift in V_{th} if high enough the current will cause significant increase the standby current when the transistor should be in its off state [9].

3.2 TID Testing

To simulate radiation effects electronic devices, it's important to understand how the testing equipment work while knowing the environment that the circuit will be tested in. For reliability of the tests, testing techniques are standardized. MIL-STD-883 method 1019 while using gamma sources, like cobalt 60, is the standard for TID effects testing. MIL-STD-883 method 1019 stresses the importance of using test vectors that leads to the worst TID effects. These vectors called worst case test vector (WCTV) are very difficult to generate especially in complex circuits. Therefore very few attempts have been made to use WCTV in ASIC chips [15].

4. Design for testability

Due to the advances in electronic devices manufacturing technology, ICs now operate at frequencies in the range of GHz with effectively billions of transistors. These conditions make it harder to these the chips for many reasons. The first one is the need for the automatic testing equipment (ATE) to run at the same high frequency of the Circuit under test (CUT). The most used fault model is the stuck-at fault model. For it to work effectively the testing must be done at the maximum clock speed of the CUT. Using an ATE that operates at very high frequency is not always economically viable as they are very expensive. Due to the advancement in the technologies IC nowadays, like microprocessors, Have very high number of input and output ports which increases the complexity of their testing thus increasing the cost of the ATE while increasing the time of the test. As the numbers of transistors increase on the ICs the complexity of the test increases. Due to the increase of the modules on each chip, these modules become harder to reach thus increasing the complexity of generating test patterns that can effectively test the IC [16].

In manufacturing ICs, the design stage and test stage were considered separate stages done by different groups of engineers. The designer's job was very separate from the tester. The designer usually implements a functionality that was handed to him in the form of design specifications and that's where the design job ended, designers didn't think about other stages like the post manufacturing testing stage. On the other hand, the testing stage was only concerned with the effectiveness of testing the device in a rational time. Small scale integrated circuits (SSI) didn't pose any threat to that approach as they consisted of either combinational circuits or small finite state machines. However, as the technology advanced into very large scale integrated circuits (VLSI) the complexity of the circuit increased and therefor this approach was difficult to implement. In the 1980s a new approached began to surface, this approach depended on simulation the faults and measuring the patterns' fault coverage. The development of patterns was key during this stage. These patterns were generated to test large sequential circuits. The simulation included the states of the sequential circuits while detecting the manufacturing faults. However, the approached had its limits as it couldn't generate patterns that can reach more than 80 % fault coverage and thus the manufacturing output decreased in quality substantially. That's when the idea of having

the designing process separate from the testing process showed its limitations. Although functionality wise these circuits were fine they underperformed due to their high cost, testing wise, or low quality. Due to these limitations Design For Testability (DFT) made its way through the electronics industry [17].

DTF had a lot of problems to solve. The first one was how to access the internal states of a sequential circuit to increase the coverage. Many methods like ad hoc testability was introduced to increase the observability and controllability of the sequential circuits. Controllability in a circuit is defined by the level of difficulty in which a signal can be set in a circuit. While observability is how easy it is to observe internal signals of the circuits. Even with the introduction of these methods VLSI circuits' coverage didn't reach 90% because of the complexity of generating test patterns for large sequential circuits. This complexity stemmed from the large number of internal states in a sequential design which was difficult to control from the input pins or observe through the output ports. This lead to the new discoveries in the field of DFT which made controllability and observability easier thus controlling these internal states and observing them. This was done by directly accessing the memory elements of the sequential circuits from the outside. "Scan cells" were the modified version of the memory elements. This access to the internal states of a sequential circuit made generating test patterns similar to combinational circuits test pattern generation which already was a known field with many developed algorithms [17].

Due to its effectiveness the scan design became wildly used. The DFT technique removes the selected or all memory elements and inserts scan cell in their place. Each memory element has an extra input that is called scan input and an extra output called scan output. Each scan output is connected to the scan input of the memory element after it thus creating the scan chain. A lot of different designs were introduced each one has its own advantages and disadvantages. If all the memory elements were swapped with a scan cell the design is called "full-scan design". "Almost full-scan design" is when most elements but not all were changed to scan cell. The last type of scan cell design is "partial-scan design"; which is given to design that have few selected memory elements replaced with scan cells. Due to the increased complexity of the circuits in the submicron nanometer VLSI design even with scan cells the cost and coverage were challenged again. Therefore, a new approach was introduced, the approach uses scan designs while applying logic built in self-test to it. The new approach generates the test

patterns and check their outputs of the CUT on the chip itself without the need of applying inputs or checking outputs from outside the chip thus eliminating the ATE. Due to its high accuracy, logic BIST is used in testing sensitive applications like aerospace industry testing [17].

4.1 Ad-hoc DFT

A lot of ad-hoc techniques were suggested to improve the testability of the devices. Ad-hoc designs made local adjustments to the CUT for better testability. Although there was improvement in the testability of the CUT, the ad-hoc techniques weren't systematic and that was a major disadvantage as the design couldn't be generalized and with every CUT the technique must be implanted and that took a long time and resulted in unpredictable behaviors [17].

For ad-hoc designs to be effective some rules were implemented:

1- No asynchronous feedback; as asynchronous feedback in combination logic causes oscillations of the inputs and thus increases the complexity of generating test patterns.
2- Initializing flip-flops; adding clear or reset to the pins of the design will lead to the ease of initialization of the flip-flops
3- Limit the number of fan-in; large input fan-in gates are hard to observe while also being hard to control (their outputs) [18].

Test point insertion (TPI) is considered the most used ad-hoc design technique. Test points are introduced inside the CUT to be controlled and observed. Testability analysis is used to identify the test point [17].

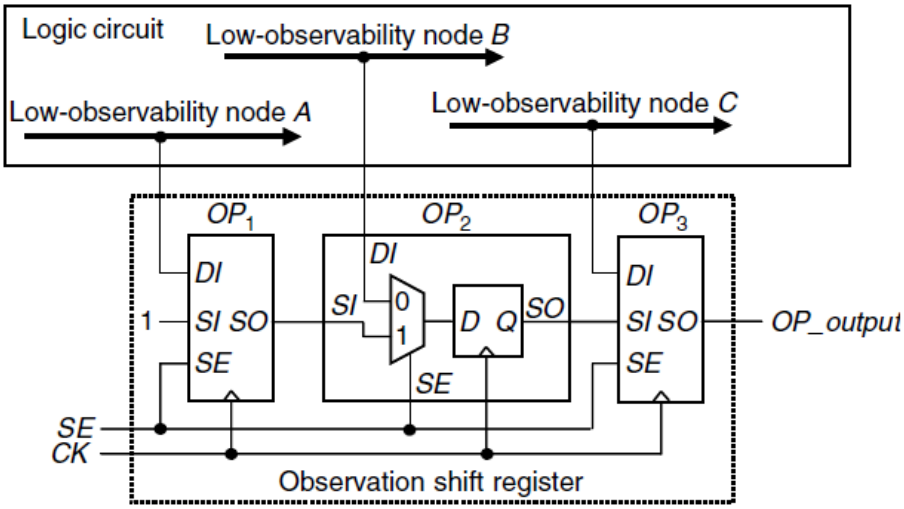

Figure 20: Ad-hoc observation point ***[17]***

In Figure 20 an observation point is shown. There are three points that are low in observability. The point OP_2 consists of multiplexer and a D flip-flop, the node is connected one of the inputs of the multiplexer and then the rest of the observation points are connected in a serial way to the shift register using the other input of the multiplexer. According to the value of the select of the multiplexer when the rising edge of the clock reaches the flip-flop either the low observability point's values are captured by the flip-flop when the select is zero or it acts as a shift register when the select value is one. In the end while the select of the multiplexer is one the observability nodes outputs can be observed as the end of the chain is a primary output [17].

On the other hand, the controllability nodes are shown in Figure 21. Point CP_2 is an example of the structure of a controllability node, although it's also made of a multiplexer and a flip-flop the connection is different from the observability nodes. As the multiplexer is inserted between the source and destination. The select signal of the multiplexer is called test mode signal. When the test mode signal is zero the CUT operates normally. However, when the test mode signal is 1 the destination value is derived from the flip-flop instead of the source and the low controllability nodes inputs acts as a shift register similar to the observability nodes however instead of the is primary output for the controllability a primary input is used to drive these nodes from the outside of the circuit. While designing the controllability nodes the critical path must be considered as the controllability nodes increase the delay. Some of the nodes

can benefit from combining both the controllability and observability node to form a "scan point" [17].

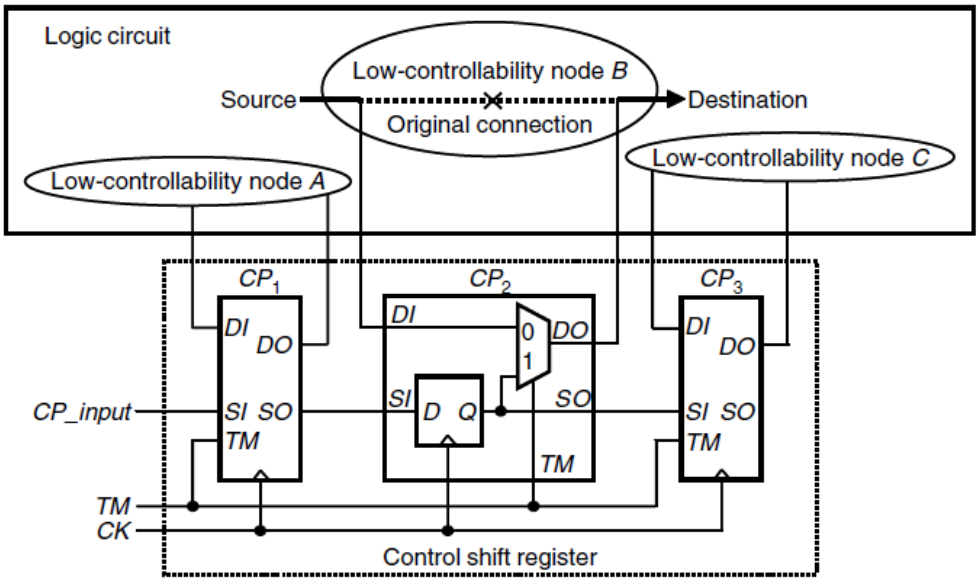

Figure 21: Ad-hoc control point example ***[17]***

4.2 Scan Design

Due to the limitations of the ad-hoc techniques; local and can't be generalized, A new techniques were introduced. These techniques focused on developing a generalized method for more efficient testing. This made the testing more structured as its flow can be added systematically to any design and this making the testing easier and more economically viable. To make these techniques easier to use and implement the electronic design automation (EDA) vendors provided accurate DTF tools. These tools are used to generate patterns quickly while maintaining a high fault coverage [17].

The scan design is the most used DTF technique due to its simplicity both in implementation and use. Every memory structure in a sequential logic circuit is replaced with a "scan cell". The scan cells usually have three additional ports, "scan input" (SI) as an input and "scan output" (SO) for the output and the last port is the control port which differs from one technique to another. The SI of each cell is connected to the SO of the previous cell. There are three modes for the scan cells; normal, shift and capture. The normal mode is when the cell operates normally to output the functionality of the given design. Both the shift and capture modes fall under the

test mode (TM) classification, to test and observe the internal the signals of the design. Muxed D scan, clocked scan and enhanced scan among the many architectures of the scan design [16].

4.2.1 Muxed D scan architecture

In this architecture every memory element is replaced with a D scan cell. Each D scan cell is composed of D flip-flop and s multiplexer as show in Figure 22. The select of the multiplex is called SE, this signals selects either the data input (DI), which is the normal input of the memory element, or the scan input (SI), which is the output of the previous scan cell [16].

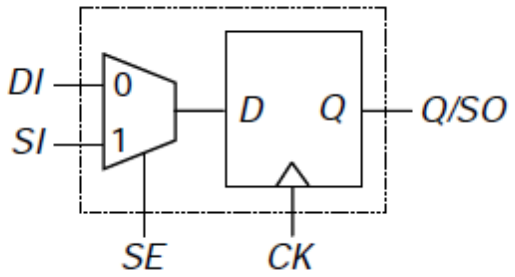

Figure 22: D scan cell [16]

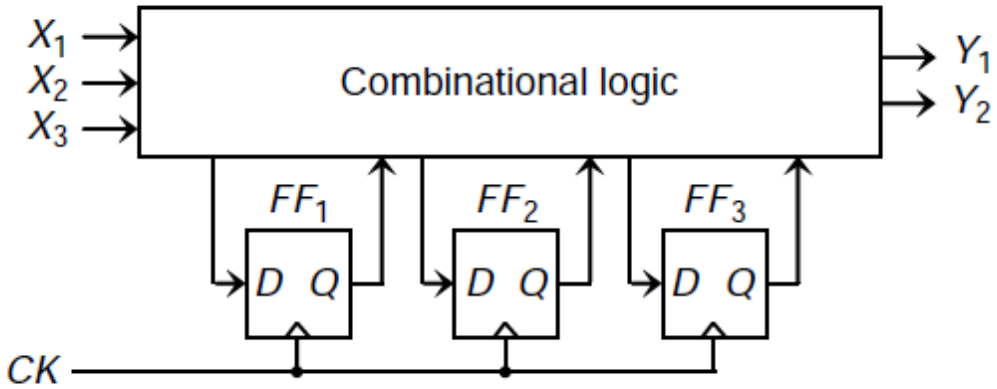

Figure 23: Normal sequential circuit [16]

Figure 23 shows a normal sequential circuit with primary inputs X and primary outputs Y and flip-flop memory elements that feed into the combinational logic. Figure 24 is the equivalent D muxed scan circuit. The same primary inputs and outputs are still there with an addition to two primary inputs, scan in (SI) and select (SE), and one

primary output, scan out (SO); however new inputs and outputs are added to the combinational logic. Pseudo inputs (PPIs) are the outputs of the scan cells that are feed back into the combinational logic while Pseudo outputs (PPOs) are the inputs of the scan cells that are from the combinational logic. Furthermore, each flip-flop was replaced w a D muxed flip-flop. The output and inputs of the cells are still connected to the combinational logic. Also, each scan cell output is connected to the input of the cell after it to form a chain called scan chain while having the first cell SFF_1 input as the SI and the last cell SFF_3 output as the SO. For shift mode the SE must be equal to one, shift mode, thus making the cells a single chain which allow the insertion of any vector from the SI primary input. On the other hand, when the SE is equal to zero, capture mode, it allows the scan cells to capture the outputs from the combinational logic. The PPOs can be captured then by using the shift mode it the scan chain can be outputted through the scan output [16].

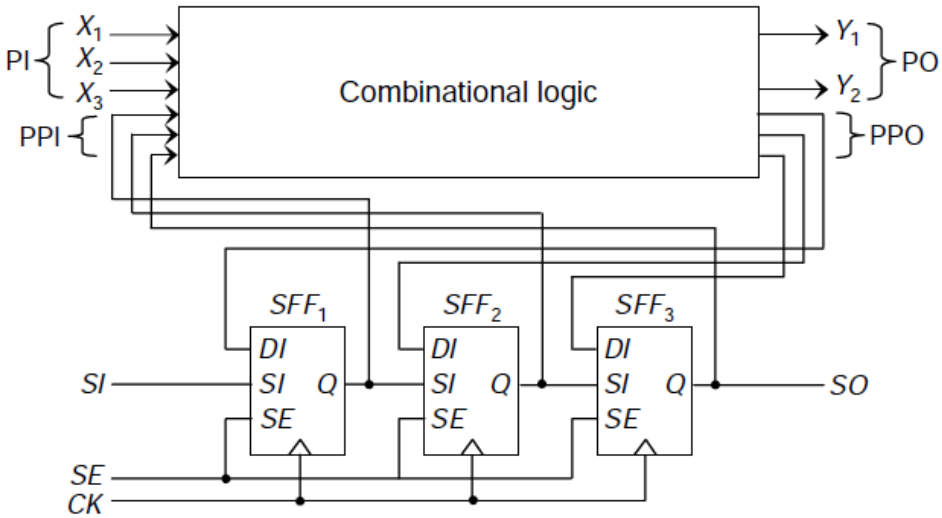

Figure 24: Muxed D scan circuit of Figure 23 sequential circuit [16]

4.2.2 Clocked scan architecture

Like the muxed D architecture every memory element in the clocked scan architecture is replaced with a clocked scan cell which is similar to the D flip-flops. Like the Muxed D cell the scan clock cell have an extra input SI while having the output act as the normal output of the flip-flop and the SO. The main difference between the

muxed D cell a cock scan cell is the lack of SE in the clock scan cell while having another signal, the shift clock (SCK) as shown in Figure 25. The selection process between the DI and SI is done by the input of the data clock DCK and the SCK instead of the SE. Figure 26 shows the operation of the clocked scan cell. When the positive edge of the (DCK) is applied the output of the cell is DI while if the positive edge of the SCK is applied the output will be the SI.

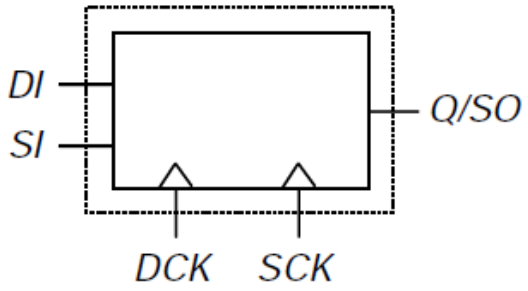

Figure 25: clocked scan cell [16]

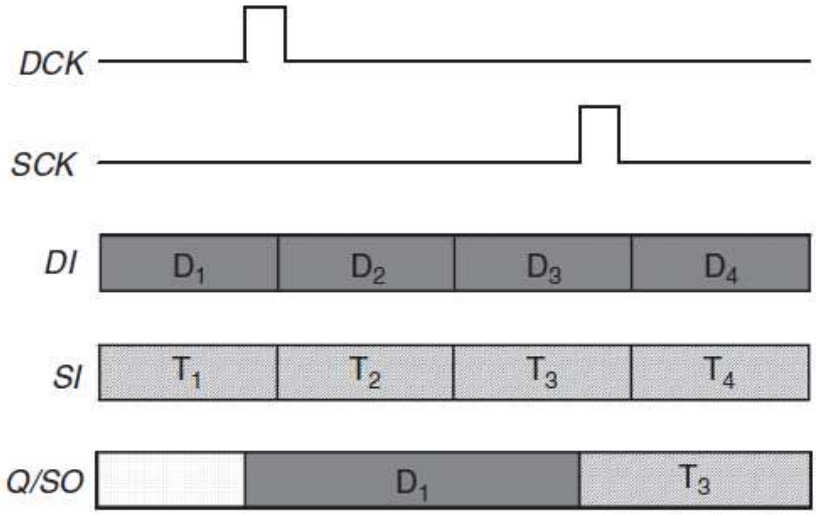

Figure 26: Operation of clocked scan cell [17]

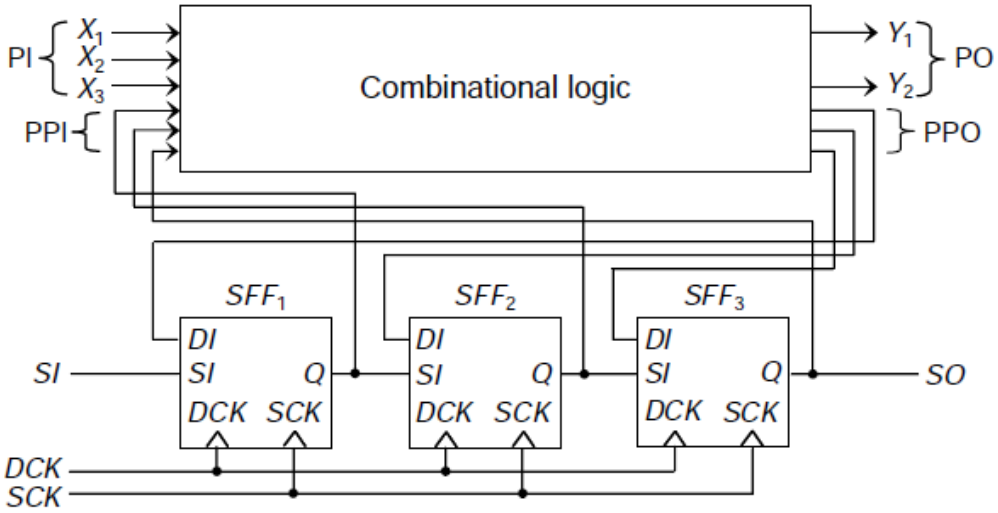

Figure 27: Clocked scan circuit of Figure 23 sequential circuit [16]

Like the muxed D equivalent circuit each flip-flop shown in Figure 23 is replaced with a clocked scan cell as shown in Figure 27. The functionality of the circuit is nearly the same. The only difference is the application of the SCK instead of driving the SE. for the shifting mode the DCK is set to zero while every positive edge of the SCK shifts the input into the chain. While for normal operating the DCK is normal and the SCK is zero [16]. The advantage of the clocked scan over the Muxed D scan is that it has no multiplexer in the path of the data thus decreasing the delay and increasing the performance. However it more complex due to the extra routing of the SCK which needs to have low latency and jitter [17].

4.2.3 Enhanced scan architecture

The enhanced scan architecture is a modification of the Muxed D architecture. Its purpose is to store two bits of data and apply them after each other to the combinational logic. This can be achieved by adding a D latch to the Muxed D cell as shown in Figure 28. This architected is mainly used to test path delay faults which the application of the vectors are time sensitive [16].

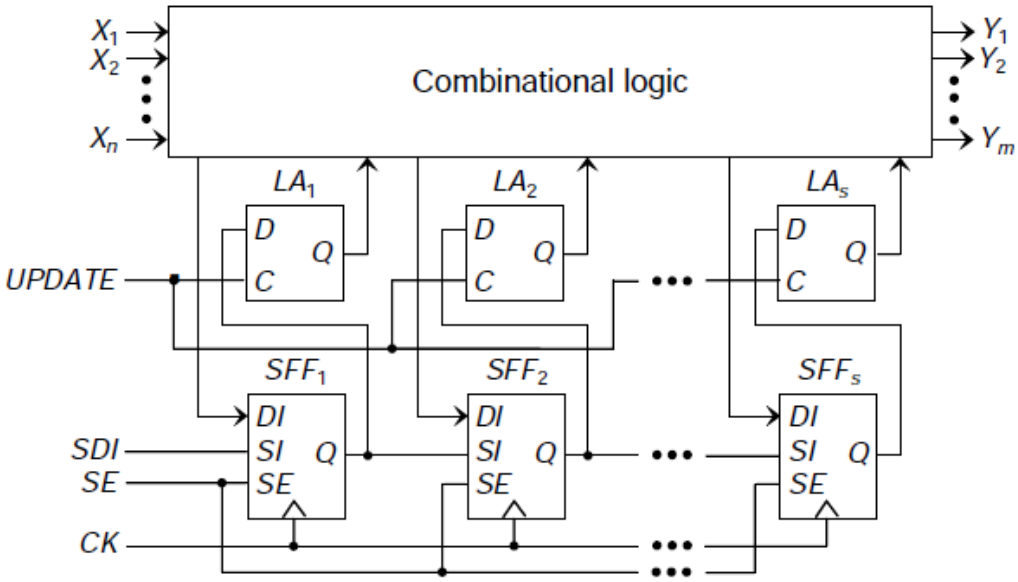

Figure 28: Enhanced scan design [17]

4.3 Logic built-in self-test

Logic built-in self-test (BIST) is used to test digital circuits inside the device itself, either on the chip or on the board, without having to use any external equipment for the test. As shown in Figure 29, BIST consists of four modules, the test pattern generator (TPG), the circuit under test (CUT), the output response analyzer and the logic BIST controller. TPG is provides the CUT with the test patterns. The TPG generates these patterns automatically. The output of the CUT is then analyzed by the ORA. All of these modules are controlled by the BIST as it sets the control signals and the clocks. Linear feedback shift registers (LFSR) are usually used in the TPG to generate the test patters. Pseudo random, exhaustive and pseudo exhaustive testing are commonly used in the TPG. Exhaustive testing is when all possible vectors are applied to the circuit and their output is checked. For an n input circuit the exhaustive test generates 2^n vectors and yields a 100% fault coverage; however circuits that have large number of inputs requires long time to test and that poses a limitation to the exhaustive test. Therefore, pseudo random and pseudo exhaustive test were developed. Pseudo random testing uses a subset of the 2^n and through simulations the coverage is calculated. While the pseudo exhaustive generates 2^w patterns where it depends on a subset of the inputs to maintain the high coverage. ORAs are usually made of multiple

input signature registers (MISR), which consist of the LFSR and an XOR gates. The output of the CUT is connected to a network of XOR gates that is connected to the inputs of the MISR, which is called a linear phase compactor, which decreases the overhead of the ORA hardware [16].

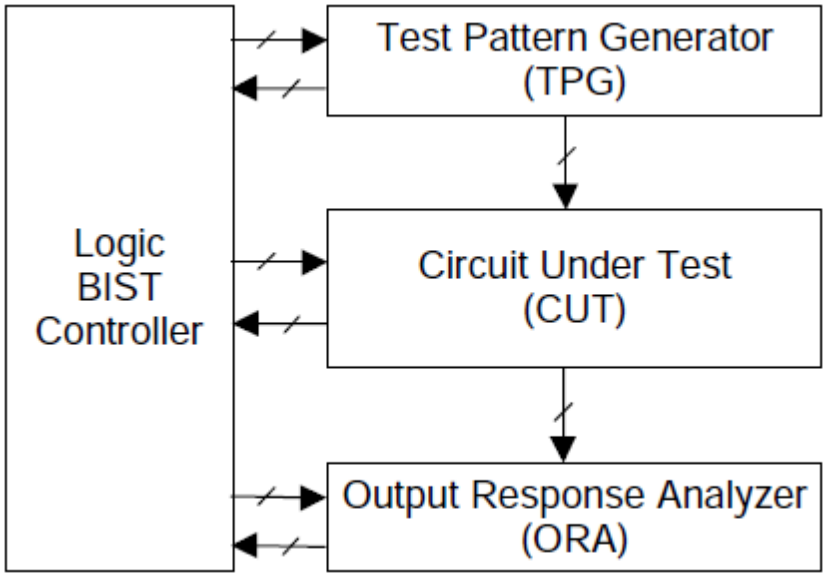

Figure 29: BIST modules [16]

5. Leakage current fault modeling and testing

To test the effect of TID on CMOS leakage current, a fault model for the leakage current must be achieved. MIL-STD-883, method 19, standard urged the importance of using worst case test vectors (WCTVs) to test ASIC devices. However, WCTV have been barely used to test the effects of TID due to the complexity of the fault modeling. To understand the fault model of the leakage current and how to generate WCTV for that model a few concepts must be discussed. The first concept is how to model the leakage current of a gate. Then how to model a leakage current of a block. Then a sequential circuit [3]. After modeling the leakage current come the generation of the WCTVs. These vectors can be generated in many ways. They can be generated by algorithms or exhaustively [4].

5.1 Leakage current Failure

During the off state of the CMOS transistor some current flows from the drain to the source. This current operates in the subthreshold region and is given by the following equation.

$$I_{ds} = I_o \frac{W}{L}\left(1 - e^{\frac{V_{ds}}{v_t}}\right) e^{\left(\frac{V_{gs} - V_{vth} - V'_{off}}{\eta V_t}\right)} \quad (4)$$

V_{th} is the threshold voltage. While I_o and V'_{off} are constants. With v_t as the thermal voltage and Ŋ is the subthreshold swing [19]. The relationship between the leakage current I_{ds} is inversely exponentially proportional to the threshold voltage V_{th}. As mentioned in section 3.1.3 the threshold voltage of the CMOS devices can be affected by the TID. Thus leading to the increase of the leakage current, in orders of magnitude, after the exposure to radiation. The maximum degradation of an NMOS happens when its gate is biased with high voltage during the irradiation phase. While the leakage current happens during the off state of the transistor, when the gate voltage is low [11].

5.2 Leakage current Combinational logic fault modeling

Unlike the stuck at model, to generate a test vector that will result in maximum leakage current two vectors are needed, irradiation and post-radiation. The irradiation vector is applied during the radiation phase while the post-radiation vector is after the device is subjected to radiation. The irradiation vector must insure the maximum degradation of the transistors, while the postirradiation should drive the transistors low so that leakage current can be measured. For example to get the maximum leakage current from a CMOS inverter that was exposed to radiation the NMOS should be biased high in the irradiation phase then biased low in the postirradiation phase. So the test vector should be "10" where the most significant bit represents the input of the CMOS inverter during the irradiation phase and the least Signiant bit represents the input during the postirradiation phase [2].

Fault modeling is simplified version of the circuit to make it easier to generate test vectors. In [2] a model is introduced, the model considers each input of the circuit as two I, irradiation input, and P, postirradiation input. It defines I as $I = [I_1 I_2 \dots I_m]$ while P as $P = [P_1 P_2 \dots P_m]$ where $I_j \in \{0,1\}$ and $P_j \in \{0,1\}$. So for every CUT there are 2^{2m} possible test vectors as each P and I inputs have 2^m possible combinations.

Leakage current fault failure happens when the amount of current that is drawn from the supply,I_{ddq}, exceeds the maximum limit. I_{ddq} is defined as the summation of the leakage currents of the logic gates inside the circuit. To ensure the flow of leakage current from Vdd to ground some conditions must be satisfied. These conditions are as follows:

1- At least one of the inputs must be high voltage during the irradiation phase to ensure maximum degradation of the NMOS transistor/s it's connected to. While having a low voltage in the postirradiation phase for the leakage current to flow. This is be called 1/0 input combination.
2- The pairs of the NMOS and PMOS must have 1/0 inputs that ensures that the V_{dd} and the ground have a path between them.
3- To ensure the leakage current failure the postirradiation, P, vector should drive the output of the logic gate to 1 [1].

So these conditions define the excitation function E. The excitation function is modeled after a binary model because either the gate follows the conditions and therefore results in leakage current or not. For example, the CMOS inverter must have the irradiation input as one and the postirradiation input as zero so its excitation function as follows.

$$E_{inv(I,P)} = (I_1\overline{P_1}) \tag{5}$$

When the excitation function is equal to 1 that means that the vector will produce leakage current due to the radiation [1]. As for the CMOS two input nor gate the excitation function is

$$E_{nor2(I,P)} = (I_1 + I_2)\,\overline{P_1}\ \overline{P_2} \tag{6}$$

Table 1 shows different Irradiation and post radiation inputs that of the two input nor gate. Which may or may not cause the manifestation of the leakage failure [1].

Table 1: Nor excitation function evaluation [1]

I_1	P_1	I_2	P_2	E_{NOR2}
1	0	0	0	1
0	0	1	0	1
1	0	1	0	1
1	0	0	1	0
0	1	0	1	0
1	1	1	1	0
0	0	0	0	0

As Table 1 shows there are 3 possible input combinations that will result in leakage failure for the two input nor however the leakage current for each one may differ. Knowing the leakage current of each input vector is important to find the maximum leakage current and hence the WCTV. In [2] the methodology to calculate the leakage current was introduced. According to [2] the current depends on the excitation of each individual transistor, the placement of the transistors compared to each other and finally their size. As shown in Figure 30 the nor gate's pull down network has two NMOS transistors parallel to each other. Thus it have two leakage current paths. Each transistor can be exited during the irradiation and thus degraded then during the postirradiation if the transistor is off leakage current will path through

it if the output of the gate was driven to high. So, the leakage current equation for the nor gate is a follows:

$$I_L(I,P)_{nor2} = \left(I_1\overline{P_1}\ \ \overline{P_2}\,W_{n1} + I_2\overline{P_1}\ \ \overline{P_2}W_{n2}\right) \qquad (7)$$

The channel widths are noted as W_{n1} and W_{n2} as the leakage current is directly proportional to the width of the transistor [2].

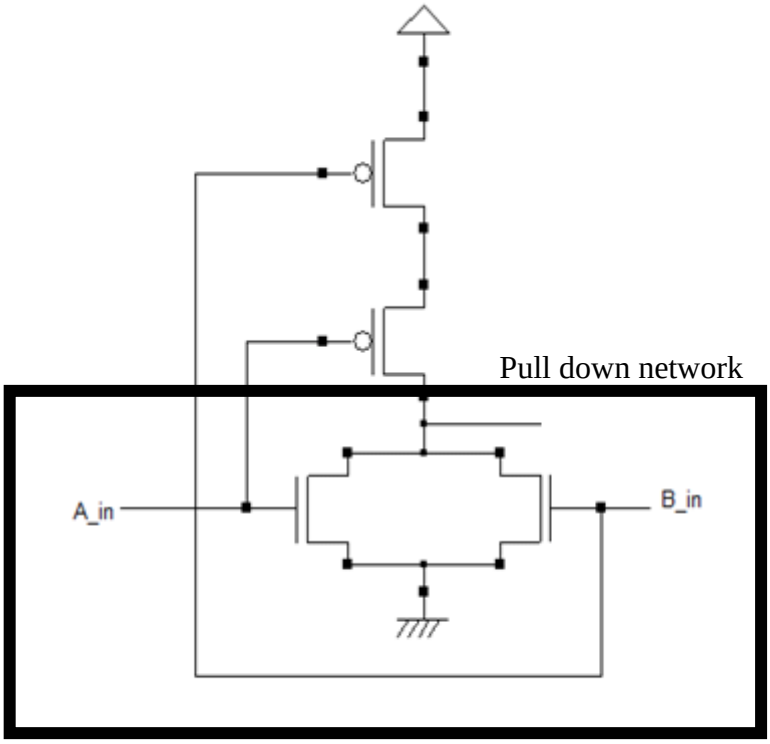

Figure 30: CMOS NOR gate [20]

In [2], the fault model is extended to a standard cell library that is used by synthesis tools for ASIC chip fabrication. The fault model uses Mentor Graphics' ASIC design kit (ADK) 3.1 that supports the following technologies AMI 0.5um and 1.2/1.5um and TSMC 0.35um, 0.25um, and 0.18 um. To generate WCTV for any circuit that uses the ADK the fault model for each cell must be implemented. As shown in Table 2 there are over 90 cells in the ADK.

Table 2: ADK 3.1 Cell Library [2]

Category	Cell
Basic Logic Gates	and02, and03, and03, or02, or03, or04, nand02, nand02_2x, nand03, nand03_2x, nand03_2x, nand04, nand04_2x, nor02, nor02_2x, nor02ii, nor03, nor03_2x, nor04, nor04_2x, xnor2, xnor2_2x, xor2, xor2_2x, mux21, mux21_ni, hadd1, fadd1, buf02, buf04, buf08, buf12, buf16, inv01, inv02, inv04, inv08, inv12, inv16, tri01, trib04, trib08
AND-OR	ao21, ao22, ao221, ao32, ao32, aoi22, aoi221, aoi222, aoi32, aoi321, aoi322, aoi33, aoi332, aoi333, aoi422, aoi43, aoi44,
OR-AND-INV	oai21, oai22, oai221, oai222, oai32, oai321, oai322, oai33, oai332, oai333, oai422, oai43, oai44,
Flip-Flops/Latches	dff, dffr, dffs, dffs_ni, dffsr, dffsr_ni, latch, latchr, latchs, latchs_ni, latchsr, latchsr_ni, sff, sffr, sffr_ni, sffs, sffsr, sffsr_ni,
Pads	PadInC, PadOut, PadBidirHE

[2] Then gives an example of the fault model of an AND-OR gate. The gate that was used is the 2-1 AND–OR-Invert (aoi21) gate which is shown in Figure 31.

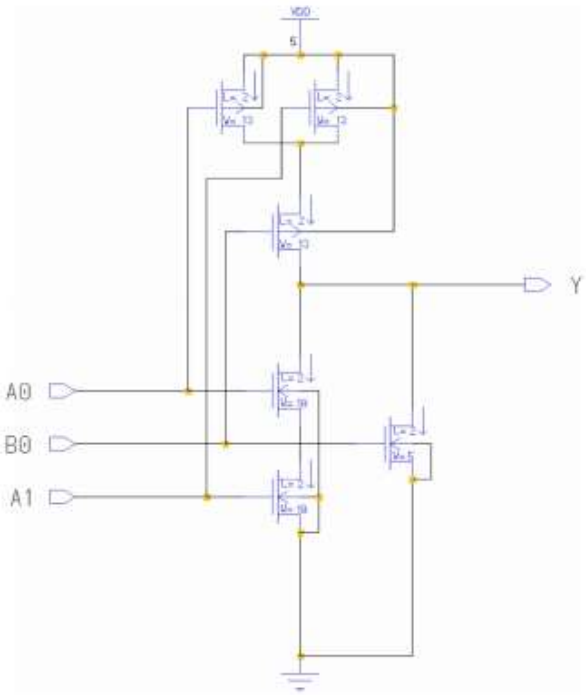

Figure 31: aoi21 gate at the transistor level [2]

There are two paths of leakage current therefore each path should have its own part in the leakage current equation. If the transistors are in series their leakage current

depends on their excitation and their sizes. The leakage current for the gate is as follows:

$$I_L(I,P)_{aoi21} = E_{aoi21}(I,P)[I_{B0}\overline{P}_{B0}(\overline{P}_{A0} + \overline{P}_{A1})W_{nB0} + \frac{1}{\frac{(I_{A0}\overline{P}_{B0})}{W_{nA0}} + \frac{(I_{A1}\overline{P}_{B0})}{W_{nA1}}} \quad (8)$$

Where

$$E_{aoi21}(I,P) = (I_{A0}\,\overline{P}_{A0}P_{A1} + I_{A1}P_{A0}\overline{P}_{A1} + I_{A0}I_{A1}\overline{P}_{A0}\overline{P}_{A1})\mathrm{P}_{B0} + I_{B0}\overline{P}_{B0}(\overline{P}_{A0} + \overline{P}_{A1}) \quad (9)$$

```
*
* Globals.
*
.global GND VDD
*
* Component pathname : $ADK_DEV/parts/aoi21
*
.subckt aoi21  Y A0 A1 B0

        M_I$12 N$8 A1 GND GND n L=2e-06 W=1e-05
        M_I$11 Y A0 N$8 GND n L=2e-06 W=1e-05
        M_I$7 Y B0 N$4 VDD p L=2e-06 W=1.3e-05
        M_I$6 N$4 A1 VDD VDD p L=2e-06 W=1.3e-05
        M_I$5 N$4 A0 VDD VDD p L=2e-06 W=1.3e-05
        M_I$13 Y B0 GND GND n L=2e-06 W=5e-06
.ends aoi21
```

Figure 32:aoi21 SPICE netlist[2]

The Model then was validated by SPICE simulation and the dimension of the transistors were extracted from the SPICE netlist as shown in Figure 32 and then the calculation of the leakage current was expressed in a VHDL function as shown in Figure 33 [2].

```
leakage current aoi21
function IL_aoi21 (IPA0,IPA1,IPB0 : std_logic_vector(1 downto 0))
                                    return real is
variable IL1, IL2, IL: real := 0.0;
variable IP: std_logic_vector (3 downto 0);
begin

   if((IPB0=EC1) and ((IPA0(0)='0') or (IPA1(0)='0'))) then
       IL1 := 5.0;
   end if;

   IP :=IPA0 & IPA1;
   if (IPB0(0) = '0') then
      if ( IP = EC2) then
         IL2 := 5.0;
      elsif ( ((IPA0= EC1) and (IPA1(0) = '1')) or
      ((IPA1= EC1) and (IPA0(0) = '1'))) then
         IL2 := 10.0;
      else
         IL2 := 0.0;
      end if;
   else
       IL2 := 0.0;
   end if;
   IL := IL1 + IL2;
   return IL;
end;
```

Figure 33: aoi21 leakage current VHDL function[2]

5.3 Leakage current sequential logic fault modeling

Unlike combinational logic, sequential logic depends on the inputs of the circuit as well as the previous inputs. The sequential logic stores the information in memory elements like flip-flops. These memory elements depend on the clock as every clock cycle they get updated. Synchronous sequential circuits are widely used in VLSI designs. These circuits can be categorized into two categories, Cyclic and Cyclic free sequential circuits. Each one of these have a different fault model [3].

5.3.1 Cyclic free sequential circuits fault modeling

A Cyclic free sequential circuit doesn't have any feedback loops from the memory elements that are in the design. Cyclic free fault modeling is simpler that the cyclic fault modeling due to the lack of feedback. In [3] a model of cyclic free sequential circuits is introduced. The model removes the memory elements completely and

connects each memory element input to its output as shown in Figure 34 on a D flip-flop.

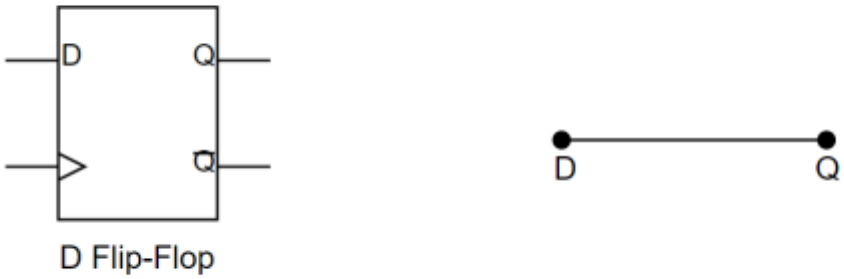

Figure 34: equivalent circuit to D Flip-Flop [3]

This hence turn the sequential circuit to a combinational circuit completely and the WCTV can be generated using the combinational fault modeling mentioned in the previous section. [3] Then used a 5*5 pipelined multiplier as a non-cyclic sequential circuit example.

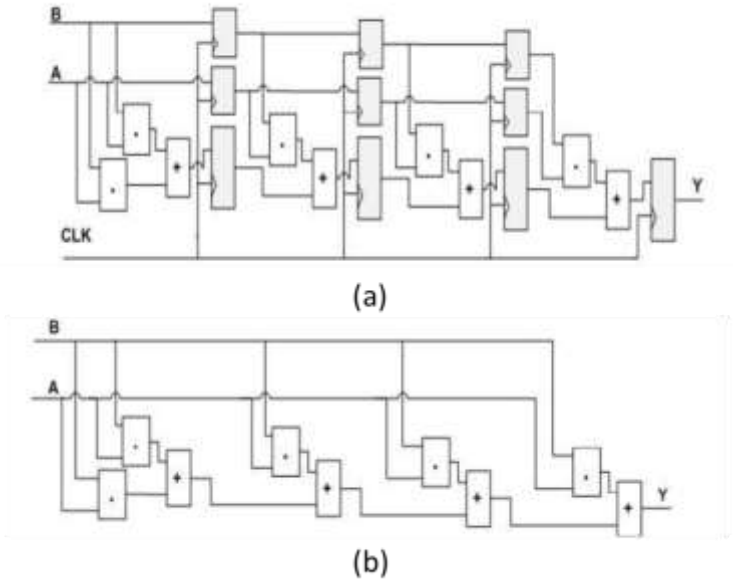

Figure 35: (a) 5*5 pipelined multiplier sequential circuit, (b) 5*5 pipelined multiplier equivalent combinational circuit [3]

Then after the extraction of the equivalent combinational circuit show in Figure 35 the fault model of [2] was used to generate the WCTV for the multiplier while ignoring the effect of the memory elements due to the fact that the leakage current of the memory elements is much lower than normal cells and normally their number are much less than the combinational cells [3].

5.3.2 Cyclic sequential circuits fault modeling

Finite state machine (FSM) circuits are the most widely used cyclic circuits. Similar to the cyclic free sequential circuits an equivalent combinational model is used as shown in Figure 36. The input of the state register is also connected to the output however to generate the WCTV this input is added to the primary inputs of the circuit.

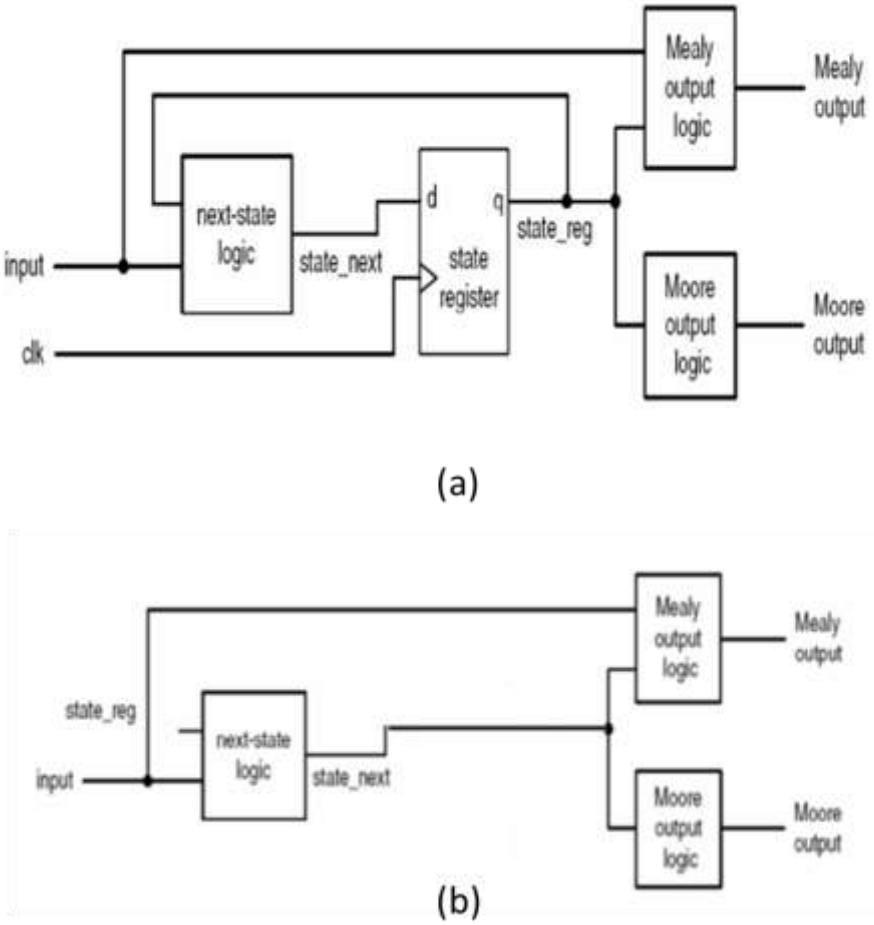

Figure 36: (a) normal FSM, (b) proposed FSM [3]

After the generation of the WCTV, analysis to the sequential circuit is made so the the inner states can be driven from the primary inputs as there is no access to the inner

states of the sequential circuit from the outside. The limitation of the process begins to show when the circuits get large. As the complexity of the circuit increase driving the inner states becomes impossible. Generating the WCTV won't be enough as they can't be applied to test the circuit [3].

In [3] a simple 13 bit bus bridge circuit was used as a proof of concept. The circuit was manufactured and tested to produce the maximum leakage current. Although the sequential circuit was simple its test and analysis complex as shown in both Table 3 and Figure 37Table 1.

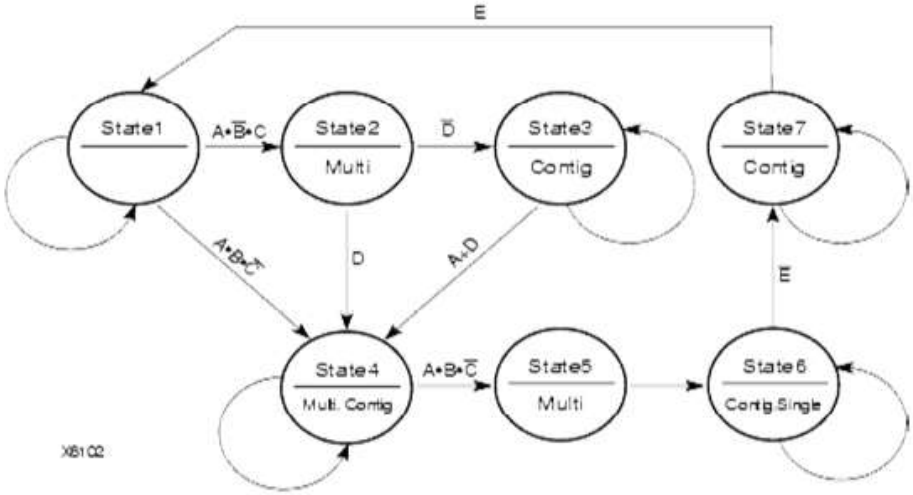

Figure 37: 13 bit bus bridge IC FSM [3]

Table 3: 13 bit bus bridge IC WCTV generation[3]

Irradiation WCTV Sequence								
m	RESET	CE	A	B	C	D	E	next STATE
1	1	0	0	0	0	0	0	STATE 1
2	0	1	1	1	0	0	0	STATE 4
3	0	0	1	0	1	1	0	STATE 4

Postirradiation WCTV Sequence								
m	RESET	CE	A	B	C	D	E	next STATE
1	0	1	1	1	0	0	0	STATE 5
2	0	1	0	0	0	0	0	STATE 6
3	0	1	0	0	0	0	0	STATE 7
4	0	1	0	0	0	0	1	STATE 1
5	0	1	1	0	1	0	0	STATE 2
6	0	0	0	1	0	0	1	STATE 2

5.4 WCTV generation for leakage current failures

To generate WCTV for leakage current failures the CUT must be tested. So to calculate the leakage current two identical CUT instances are instantiated, one for the irradiation and one for the postirrradiation. Then these instances are added to the test-benches to calculate the maximum leakage current per input vector. The test-bench uses the Verilog/VHDL functions that was modeled in [2] to calculate the total leakage current. The vector is divided into two part the irradiation part and postirradiation part. Then the test-bench can generate WCTV using algorithms to calculate the total leakage current and hence find the WCTV for the CUT as shown in Figure 38[2].

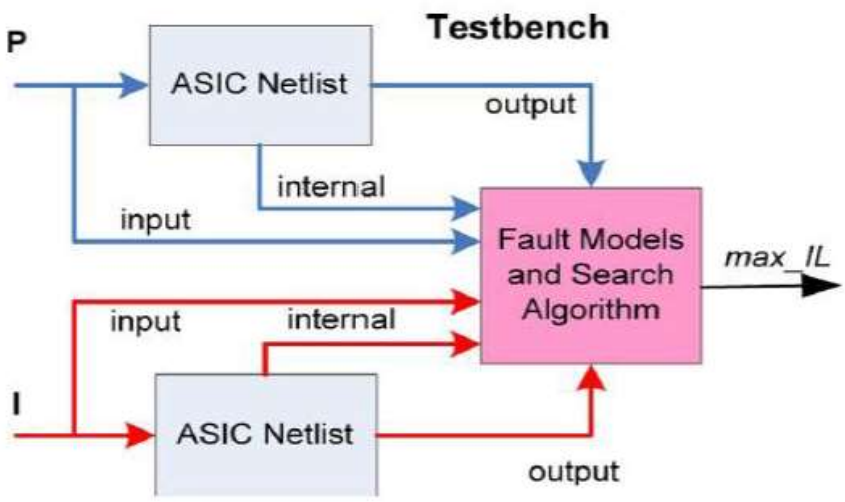

Figure 38: WCTV maximum leakage current test bench setup [2]

[2] used the exhaustive search algorithm to generate the WCTV. The exhaustive search applies all possible combinations to the netlist and calculate the leakage current and after all the combinations are applied the vector that results in the maximum leakage current is identified. However, exhaustive generation shows its limitation as the number of inputs increase. The number of possibilities grows exponentially with the inputs. So it would take a long time to go through all possible combinations for large circuits. For example for a 64x64 multiplier to find the WCTV exhaustively it would take 2^{128} combinations to complete which would take a very long time and considered impossible. So [4] introduced a new methodology to generate the WCTV. The methodology, for leakage current failures, uses a genetic algorithm. The

methodology uses field oxide leakages current fault model that was produced in [2]. The methodology used the synthesized code of the CUT to produce a netlist that was then used in a System Verilog to search for the WCTV using a genetic algorithm. This tool was then converted into a C# code that does the same exact algorithm however it provided a GUI to change the parameters of the genetic algorithm and used as an application instead of a system Verilog code. However to use the C# application the user must edit the code for every design. Also the library of the code didn't have the 90 plus cells of ADK 3.1 so any new cells must be added as well. The genetic algorithm code takes much less time compared to the exhaustive search. For example an 8x8 multiplier circuit took 2 days to generate its WCTV exhaustively while the genetic algorithm took few seconds. Although the genetic algorithm doesn't get the WCTV that results in the maximum leakages current it gets a WCTV that will be get a close number to the maximum leakages current which will also result in leakage current failure [4].

6. Methodology

Although [3] proposes a methodology to generate WCTV for sequential ASIC chips leakage current failures, the methodology has its limits. Due to the complexity of driving the inner states of the sequential circuits, it becomes highly difficult to test them for leakage current failures. Also, DTF has been used for a long time in the electronics industry, however it was never used to test leakage current failures induced by TID effects. In this thesis, a new methodology of generating WCTV is introduced. The methodology combines DTF and fault models proposed in [2] while modifying them due to the insertion of DFT hardware. Then, a verification comparison is done between exhaustive WCTV generation and genetic algorithm WCTV generation introduced in [4]. In the end, the thesis combines [2], [4] and DFT to explore uncharted testing territory.

6.1 DFT sequential circuit models

As mentioned in section 4.2.1, DFT increases the controllability of the circuit and makes it possible to drive the inner states of sequential circuit. Due to the limitation of [3], especially in large cyclic circuits, as driving the inner states needed a lot of complex analysis and even impossible for very large circuits, this methodology was introduced. The methodology uses DFT, which means replacing memory elements with scan cells that increases the controllability of the circuit while avoiding the complex analysis of driving the inner states. The methodology works for the two models for sequential circuits mentioned in [3]: cyclic and cyclic free sequential circuits. While maintaining the same method for both sequential circuits, unlike [3], a modified method is also introduced to cyclic free pipelined sequential circuits. The methodology uses Muxed D sequential circuits, however, any DFT technique can be used.

6.1.1 Cyclic and cyclic free generalized fault model

A fault model should be developed to identify the WCTV. As mentioned before, the fault model of [2] is used to calculate the normalized leakage current of each cell, normalized to the inverter's leakage current, inside the sequential circuit. By using this model with DFT, any sequential circuit can be turned into a combinational circuit. However, the model of the combinational circuit is different due to the insertion of the DFT hardware. Muxed D scans are wildly used in DFT as clocked scan cells are more complex and require additional clock routing. That's why for this methodology Muxed D scan cells are used for the DFT, and hence the model is based on them. Every memory element in the sequential circuit is replaced with a Muxed D scan flip-flop. In [3] flip-flop leakage current was ignored due to the fact that the number of flip-flops is much less than the number of combinational cells, and that the flip-flops have low leakage current compared to the other cells. However, by introducing the Muxed D scan cell, this assumption can't be made, as each Muxed D cell contains a multiplexer inside of it. The leakage current of the multiplex is comparable and even higher than some of the combinational cells, therefore, that's why the proposed model is as shown in Figure 39.

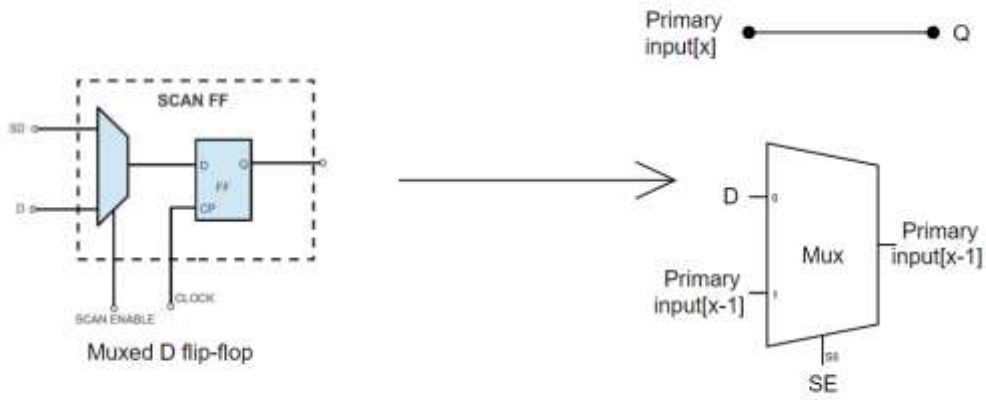

Figure 39: Proposed model for a Muxed D flip-flop

As Figure 39 shows, the Muxed D scan cell is replaced with a multiplexer and its output is connected as a primary input to the sequential circuit. The multiplexer's input is connected to the input of the scan cell, which is the output of the previous cell and the D of the Muxed D scan cell. By using this model, the sequential circuit is converted to a combinational circuit completely, WCTVs tools can generate WCTVs for the circuit,

and at the testing phase these vectors can be applied to the circuit using the shifting mode of the DFT mentioned in section 4.2.

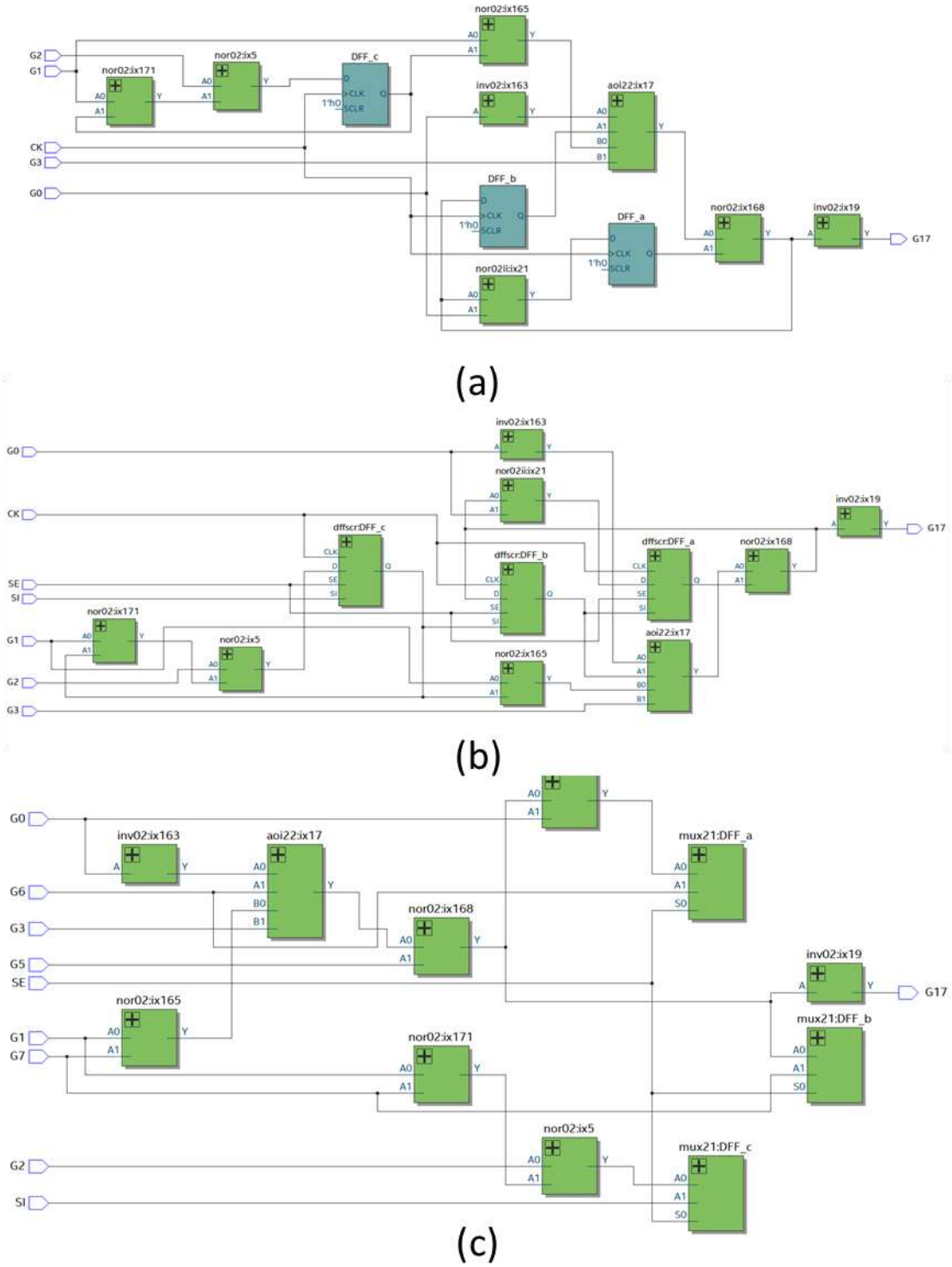

Figure 40: Proposed methodology

Figure 40 explains the methodology further. The CUT is s27 an ISCAS'89 benchmark circuit [21]. As seen in Figure 40(a), the CUT was synthesized by Mentor Graphics'

Leonardo spectrum using ADK 3.1 as mentioned in 5.2. Then, after using Mentor Graphics' DFT advisor, the CUT's 3 flip-flops were replaced with 3 Muxed D scan cells and each output of their outputs was connected to the input (SI) of the next Muxed D flip-flop, as shown in Figure 40(b). Then, by using the proposed methodology to convert the still sequential circuit to a combinational circuit that can be analyzed by the WCTV generation tool mentioned in both [15] and [16], each Muxed D flip-flop was replaced with a multiplexer, and the output of the Muxed D flip-flop is considered a primary input to the modified CUT, as shown in Figure 40(c).

6.1.2 Cyclic free pipelined sequential circuits fault model

Some of the sequential circuits are defined as cyclic free sequential circuits, which means that there is no feedback from a memory element. Some of these circuits are pipelined so that not only there is no feedback, but also they are divided in such a way between flip-flips that ensures the possibility of pure combinational circuits between the flip-flops, as shown in Figure 41.

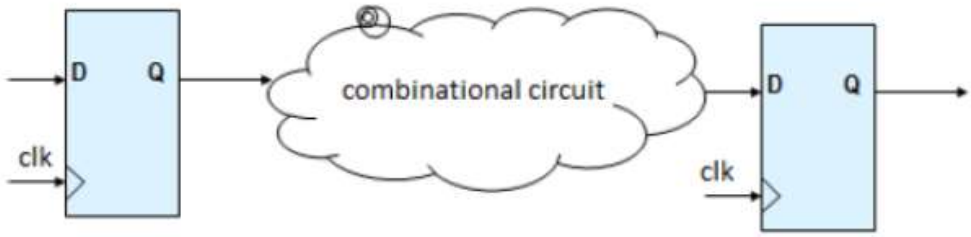

Figure 41: Synchronous sequential circuit example [22]

This feature can be used to simplify modeling of sequential circuits and the WCTV generation. Due to this feature, the combinational circuit after the flip flop has no dependency on the one before it. Using DFT makes these circuits basically independent, thus each combinational circuit can have its own normalized leakage current analysis. As seen in Figure 42, a 5x5 4 stage multiplier can be divided into 4 different combinational circuits, each circuit can have its own fault model, and WCTV can be used when testing the original circuit by using DFT techniques.

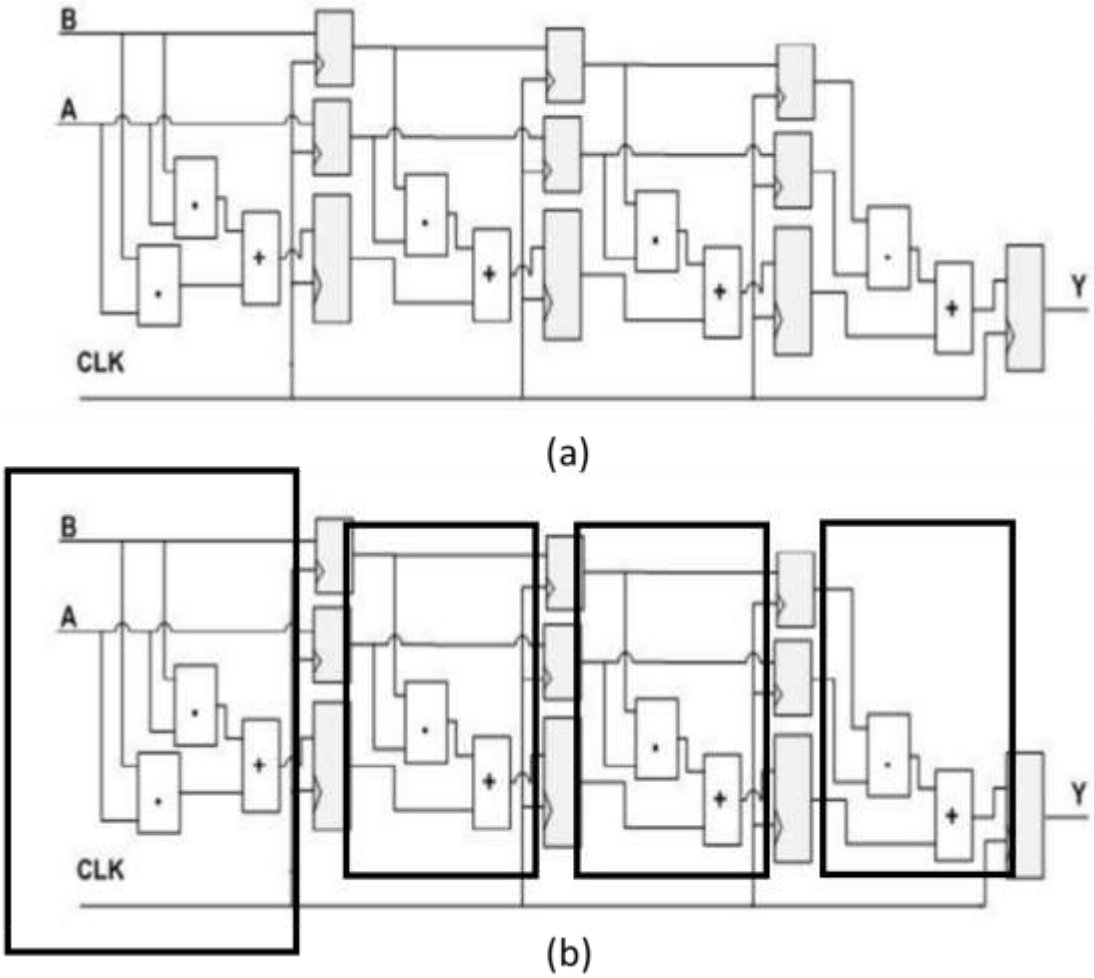

Figure 42: 5*5 4 stage multiplier circuit and its model

Instead of having roughly four times the primary inputs to generate the WCTV, only the input of each stage will be used to generate the WCTV, which will be quicker for exhaustive tests as the number of combinational vectors are 2^{2n} , as mentioned section 5.2. Using an exhaustive search for generating the vectors is more accurate than using other algorithms, like the genetic algorithm. Therefore, in the case of having a cyclic free pipelined sequential circuit using this model, dividing cyclic free pipelined sequential circuits into much smaller independent combinational circuits is more accurate than the normal cyclic model.

6.2 Simulation results

To validate the methodology mentioned in the previous section, 8 designs were used: a 5x5 multiplier, a 13-bit bus bridge, and six ISCAS'89 benchmarks. All designs were synthesized using Mentor Graphics' Leonardo spectrum. Scan cells were added using Mentor Graphics' DFT advisor. Then the modeling, replacing muxed D scan cells with multiplexers and dividing the sequential circuit into stages in the case of cyclic free pipelined sequential circuits fault model, manually. After that for the exhaustive test, the netlist was edited manually to two netlist irradiation and postirradiation and the Verilog code used in [3] was used to find the WCTV exhaustively. In the case of using the C# code of [4], another C# tool was used to convert the Verilog code to a C# code. The code also retuned normalized leakage current functions as shown in Figure 43. Furthermore, two of each netlist were returned for the irradiation and postirradiation. Then the C# code used in [4] was edited manually for the new netlist and then used to generate WCTV using the genetic algorithm. Due to the large number of standard cells in ADK 3.1 not all the cells were modeled in both C# codes and thus the codes were edited to include the new cells as shown in

Table 4. For example standard cell ao21, AND-OR 21, wasn't included in both codes. Figure 44 shows the added code for the Verilog to C# converter. While Figure 45 shows its output. Finally, Figure 46 shows the function that calculates the normalized leakage current for ao21.

```
nor02ii ix15 (.Y (G119), .A0 (G0), .A1 (nx8)) ;
G119[0] = !( G0[0] | !nx8[0]) ;
G119[1] = !( G0[1] | !nx8[1]) ;
IL_nor02ii(G0, nx8 )
```

Figure 43: nor02 example of C# code

Table 4: List of added standard cells

buf02
nor02ii
ao32
ao21
aoi321
aoi221
or03
aoi222
and04
oa21
oai221
oai32
oai43
ao22
mux21_ni

```
case "ao21":
    Y0 = Temp.Substring(Temp.IndexOf(".Y (") + 4, (Temp.IndexOf(")") - (Temp.IndexOf(".Y (") + 4)));
    A0 = Temp.Substring(Temp.IndexOf(".A0 (") + 5, ((Temp.IndexOf(("), .A1")) - (Temp.IndexOf(".A0 (") + 5)));
    A1 = Temp.Substring(Temp.IndexOf(".A1 (") + 5, ((Temp.IndexOf(("), .B0")) - (Temp.IndexOf(".A1 (") + 5)));
    B0 = Temp.Substring(Temp.IndexOf(".B0 (") + 5, ((Temp.IndexOf("))")) - (Temp.IndexOf(".B0 (") + 5)));

    OutputText += Y0 + "[0] = ((" + A0 + "[0] & " + A1 + "[0]) | ( " + B0 + "[0] ) );\r\n";

    ILfunction += "IL_" + nameOfGate.Trim() + "("
        + A0 + ", "
        + A1 + ", "
        + B0 + ") +\r\n";
    break;
```

Figure 44: Example of Verilog to C# added code for the standard cell ao21

```
ao21 ix253 (.Y (G30), .A0 (nx598), .A1 (G29), .B0 (nx248)) ;
G30[0] = ((nx598[0] & G29[0]) | ( nx248[0] ) );
G30[1] = ((nx598[1] & G29[1]) | ( nx248[1] ) );
IL_ao21(nx598, G29, nx248)
```

Figure 45: output of Figure 44 added code

```
  ////-------------------------------------ao21----------------------------------////

double IL_ao21(bool[] IPA0, bool[] IPA1,  bool[] IPB0)
{
    double IL1, IL2, IL3;
    bool[] IP = new bool[2];

    IP[1] = !((IPB0[1]) || ( IPA1[1] & IPA0[1]));
    IP[0] = !((IPB0[0]) || ( IPA1[0] & IPA0[0]));

    bool IPA010 = IPA0[1] & !IPA0[0];
    bool IPA110 = IPA1[1] & !IPA1[0];
    bool IPB10 = IPB0[1] & !IPB0[0];


    if ((IPB10) && ((IPA0[0] == false) || (IPA1[0] == false)))
        IL1 = 5.0;
    else
        IL1 = 0.0;

    if (IPB0[0] == false)
        if (IPA010 && IPA110)
            IL2 = 5.0;
        else if (((IPA010) && (IPA1[0] == true)) ||
        ((IPA110) && (IPA0[0] == true)))
            IL2 = 10.0;
        else
            IL2 = 0.0;

    else
        IL2 = 0.0;

    if (IP[1] == true & IP[0] == false)
        IL3 = 5.0;
    else
        IL3 = 0.0;

    return IL1 + IL2 + IL3;

}
```

Figure 46: Example of the added normalized leakage current function of standard cell ao21

6.2.1 Exhaustive-Genetic algorithm verifications simulations

To verify the methodology simulations using both exhaustive and genetic algorithms were made. These simulations were made on the smallest ISCAS'89 benchmarks, s27 and s298, as the exhaustive search takes a long time with larger cells. The first bench mark was s27, it have 4 primary inputs and 3 internal flip-flops. By using the methodology the inputs become 7. The exhaustive search was made over 14 bits, irradiation and postirradiation. While the same netlist was used for the genetic algorithm. As for the s298 the primary inputs were 3 while having 14 internal flip-flops making the model's inputs 17 bits. Thus the exhaustive search was made on 34 bits which took a very long time to complete compared to the genetic algorithm search

which took a few seconds solidifying the importance using it. Both simulation data shown in Table 5 and Table 6 was conclusive with the results of [4].

Table 5: s27 WCTVs for exhaustive and Genetic algorithm

Test case	Test vector I/P (G7,G6,G5,G3,G2,G1,G0)	Normalized Leakage current
Exhaustive WCTV	1101110/0110101	60
Genetic algorithm WCTV	0100100/0101011	50

Table 6: s298 WCTVs for exhaustive and Genetic algorithm

Test case	Test vector I/P	Normalized Leakage current
Exhaustive WCTV	11111010101010110/00000101010101110	668.666667
Genetic algorithm WCTV	10000011111111000/11110110001110110	526.1667

6.2.2 Genetic algorithm verification for cyclic sequential circuits simulations

The analysis of [3] was used as an example for this simulations in comparison with the new methodology. The limitation for [3] cyclic modelling shows in large sequential as it becomes impossible to drive the inner states of the circuits. The new methodology offers a solution as DFT increases the controllability of the circuits using Muxed D flip-flops. The simulation was made on the ISCAS'89 s27 benchmark and the 13 bit bus bridge used in [3]. A new analysis to drive the inner states for the s27 made while the one formation in [3] was used for the bridge. The genetic WCTV was used in both circuits to be conclusive as exhaustive test for bridge circuit wasn't possible due to its large number of inputs and flip-flops. As shown in both Table 7 and Table 8, the analysis to drive the inner states is very complex. Hence using the new

methodology will make the analysis simpler as no state analysis of the sequential circuits will be made and it only deals with the primary inputs and the flip-flop outputs as shown in Table 9 and Table 10.

Table 7: 13-bit bus bridge WCTV state sequence [3]

Irradiation WCTV Sequence								
m	RESET	CE	A	B	C	D	E	next STATE
1	1	0	0	0	0	0	0	STATE 1
2	0	1	1	1	0	0	0	STATE 4
3	0	0	1	0	1	1	0	STATE 4

Postirradiation WCTV Sequence								
m	RESET	CE	A	B	C	D	E	next STATE
1	0	1	1	1	0	0	0	STATE 5
2	0	1	0	0	0	0	0	STATE 6
3	0	1	0	0	0	0	0	STATE 7
4	0	1	0	0	0	0	1	STATE 1
5	0	1	1	0	1	0	0	STATE 2
6	0	0	0	1	0	0	1	STATE 2

Table 8: s27 WCTV state sequence

Irradiation WCTV sequence							postrradiation WCTV sequence						
m	Reset	G0	G1	G2	G3		m	Reset	G0	G0	G1	G2	G3
1	1	0	0	0	0		1	1	0	0	0	0	0
2	0	0	1	1	1		2	0	0	0	1	1	1
3	0	1	0	1	1		3	0	1	1	0	1	1
4	0	1	1	0	1		4	0	1	0	0	1	0

Table 9: s27 Genetic algorithm WCTV

Test case	Test vector I/P (G7,G6,G5,G3,G2,G1,G0)	Normalized Leakage current
Genetic algorithm WCTV	1101110/0110101	50

Table 10:13-bit bridge Genetic algorithm WCTV

Test case	Test vector I/P	Normalized Leakage current
Genetic algorithm WCTV	1000010101000100101111 0110000000010100011000 1000001111101010110100 00011101001/01110011100	1200

	1010001011001111011001 1000111100000101110011 0100110101001000101111	

6.2.3 Genetic algorithm for larger cyclic sequential circuits simulations

After the verification of the methodology in the previous sections, the limitation of the approach of [3] was explored in 4 ISCAS'89 bench mark circuits. Table 11 shows the number of primary inputs, number of flip-flops and the number of the modified design inputs. As shown the number of primary input after the modeling would make it impossible to get the WCTV exhaustively that's why the genetic algorithm was used as shown in Table 12.

Table 11: ISCAS'89 benchmark circuits' inputs [21]

Design	Primary inputs	Flip-flops (after synthesis)	Number of gates	Modified design primary inputs
S344	9	15	160	24
S349	9	15	161	24
S382	3	21	158	24
S9234	36	145	5597	182

Table 12: Genetic algorithms WCTV for ISCAS'89 Benchmarks

Test case	Test vector I/P	Normalized Leakage current
S344	100100001011101010010000/ 011101010101111101101110	462.5
S349	110001000101001000000100/ 011101010101001000001011	565.5
S382	000100010011010101010110110/ 110010111011110100111111010	609.5

S923 4	1010000000001000011001110 0000100101100101101000111 0100111100100000110110101 0001000100010110011101001 1100010001000001100110110 1011110011010000111111010 1100111110110000101000111 011101/000110111100010111 1101010000111001101000111 1101101110001000011001001 1101111010100110001110110 0111011111100000000010011 0111111110000100100001111 1100000100001111011010011 1100000010101	2107.5

6.2.4 Cyclic free pipelined sequential circuits simulations

To verify the cyclic free pipelined sequential circuits methodology simulations on 5x5 multiplier used in [3] was made. The netlist was segmented into 4 netlists as shown in section Cyclic free pipelined sequential circuits fault model6.1.2. then exhaustively the normalized leakage current was calculated for each segment. If the normal methodology mentioned in section 6.1.1 was used, it would have used 40 bit input and the exhaustive search would have been impossible. Then to results were compared to the model used in [3] as shown in section 5.3.1. to get the WCTV for the maximum normalized leakage current, exhaustive and genetic algorithm simulations were made. As shown in Table 13 the results of segmenting the multiplier were more accurate as they produce WCTVs that result in higher normalized leakage current with the exhaustive as the more accurate one. The genetic algorithm was used as a proof of concept due to the fact that in larger designs the stages can have high number of inputs.

Table 13: Genetic algorithms and exhaustive WCTV for 5x5 4 stage pipelined multiplier circuit

Test case	Test vector I/P	Normalized Leakage current
Stage 1 exhaustively	1010000/0111111	182.5
Stage 1 Genetic algorithm	1001001/0100101	170
Stage 2 exhaustively	11111110110/01010101001	177.5
Stage 2 Genetic algorithm	01010011011/10101110110	172.5
Stage 3 exhaustively	01011001111/10100110010	202.5
Stage 3 Genetic algorithm	00001111100/01100101111	195
Stage 4 exhaustively	11001010111/00110101010	202.5
Stage 4 Genetic algorithm	00001001010/00111100001	187.5
Total normalized leakage current using exhaustive search		765
Total normalized leakage current using genetic algorithm		725
[3] Multiplier model Genetic algorithm	0011100000/1110100110	685

7. Conclusions and future work

7.1 Conclusions

In this thesis a methodology was introduced to identify WCTV for leakage current failures induced by TID effects in large cyclic and cyclic free sequential circuits. This thesis uses a previously developed fault model and a WCTV generation technique while using DFT to improve and solve the limitations, accessing the inner states of large sequential circuits, of current models.

A model for cyclic sequential circuits was introduced. This model introduced after DFT techniques are applied. To access the inner states of sequential circuits every memory element is replaced with a scan cell, Muxed D. The scan cell is then modeled with two input multiplexer and a primary input addition. This model converts any sequential circuit to combinational circuit. Also, a modified model is introduced in the special case of cyclic free pipelined sequential circuit. Then either using a genetic algorithm or exhaustively the WCTV is generated.

Then simulations were made to verify the methodology. The simulations started with the verification of two small designs by generating WCTV using both the exhaustive search and genetic algorithm techniques. Then for cyclic sequential circuits two small designs were used to verify the model by comparison to a previous developed model. Then to explore the limitation of the developed model simulation for 3 medium circuit and one large circuit was made. Finally, simulations on the modified model proofed its importance and higher accuracy against a previous developed model.

7.2 Future work

More DFT techniques, like clocked scan can be used, modeled and compared to the suggested methodology. Furthermore experimental results can be obtained by fabricating a test chip with the suggested methodology. Then validating the methodology by measuring the leakage current after applying the WCTV and exposing it to TID radiation using Cobalt 60 radiation facility. Finally the WCTV generation flow can be facilitated by developing tools and using scripts to edit and partition the netlists.

8. References

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