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THE AMERICAN UNIVERSITY IN CAIRO

SCHOOL OF SCIENCES AND ENGINEERING

Two Dimensional Quantum and Reliability Modelling for Lightly Doped Nanoscale Devices

A thesis submitted in partial fulfillment of the requirements for the Degree of the Master of Science

in

Electronics and Communication Engineering

ECNG Department, School of Sciences and Engineering

By:

Rana Y. ElKashlan

Under the supervision of:

Prof. Yehea Ismail

Assoc. Prof. Hamdy Abd El Hamid

August 2017

Cairo, Egypt

The American University in Cairo

Department of Electronics and Communication Engineering (ECNG), School of Sciences and Engineering (SSE)

Two Dimensional Quantum and Reliability Modelling for Lightly Doped Symmetric Nanoscale Devices

A Thesis Submitted by

Rana Yasser Gomaa Mohamed ElKashlan

In partial fulfillment of the requirements for the degree of
Master of Science in Electronics and Communication Engineering
has been approved by

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Date ____________________

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ABSTRACT

The downscaling of MOSFET devices leads to well-studied short channel effects and more complex quantum mechanical effects. Both quantum and short channel effects not only alter the performance but they also affect the reliability. This continued scaling of the MOS device gate length puts a demand on the reduction of the gate oxide thickness and the substrate doping density. Quantum mechanical effects give rise to the quantization of energy in the conduction band, which consequently creates a larger effective bandgap and brings a displacement of the inversion layer charge out of the Si/SiO_2 interface. Such a displacement of charge is equivalent to an increase in the effective oxide layer thickness, a growth in the threshold voltage, and a decrease in the current level. Therefore, using the classical analysis approach without including the quantum effects may lead to perceptible errors in the prognosis of the performance of modern deep submicron devices.

In this work, compact Verilog-A compatible 2D models including quantum short channel effects and confinement for the potential, threshold voltage, and the carrier charge sheet density for symmetrical lightly doped double-gate MOSFETs are developed. The proposed models are not only applicable to ultra-scaled devices but they have also been derived from analytical 2D Poisson and 1D Schrödinger equations including 2D electrostatics, in order to incorporate quantum mechanical effects. Electron and hole quasi-Fermi potential effects were considered. The models were further enhanced to include negative bias temperature instability (NBTI) in order to assess the reliability of the device. NBTI effects incorporated into the models constitute interface state generation and hole-trapping. The models are continuous and have been verified by comparison with COMSOL and BALMOS numerical simulations for channel lengths down to 7nm; very good agreement within ±5% has been observed for silicon thicknesses ranging from 3nm to 20nm at 1 GHz operation after 10 years.

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List of Abbreviations

1DEG	One Dimensional Electron Gas
2DEG	Two Dimensional Electron Gas
DG	Double-Gate
DIBL	Drain-Induced Barrier Lowering
DOS	Density Of States
EDA	Electronic Design Automation
FD	Fermi-Dirac
GAA	Gate-All-Around
HCI	Hot Carrier Injection
ITRS	International Technology Roadmap for Semiconductors
MOSFET	MOS Field-Effect Transistor
NBTI	Negative Bias Temperature Instability
PD	Partially Depleted
PDE	Partial Differential Equation
SCE	Short Channel Effects
SOI	Silicon On Insulator
SON	Silicon On Nothing

CHAPTER 1

INTRODUCTION

1.1 SEMICONDUCTOR HISTORY BRIEF

Gordon Moore published his renowned paper in1965, in which he anticipated that the quantity of transistors per chip would increase fourfold in at regular intervals [1]. This forecast has subsequently been known as *Moore's law* and been strikingly followed by the semiconductor industry throughout the past four decades as shown in Figure 1.

The initiative taken by semiconductor organizations and the academic community since the early 90's to foresee precisely the future of the industry brought forth the International Technology Roadmap for Semiconductors (ITRS) organization [2].

The ITRS issues a yearly report that portrays the sort of technology, outline devices, hardware and metrology devices that should be produced to keep pace with the exponential advancement of semiconductor devices anticipated by Moore's law. The semiconductor industry's pillar technology is silicon CMOS, and the CMOS building block is the MOS field-effect transistor (MOSFET).

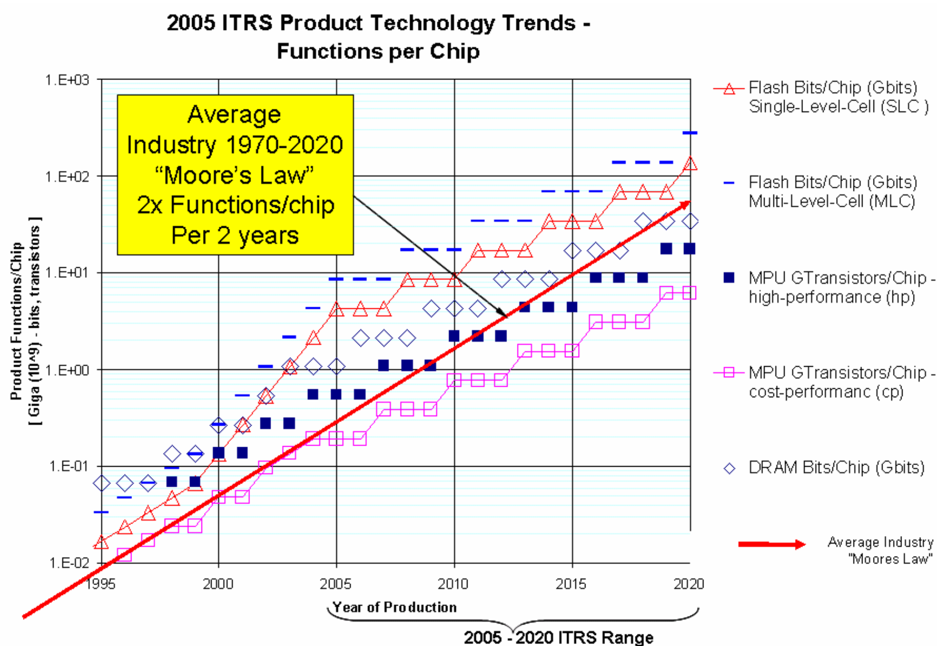

Figure 1.1 Figure 1 ITRS Product Technology Trends: Product Functions/Chip and Industry Average "Moore's Law" Trends. [3]

To keep up with the frantic pace predicted by Moore's law, every three years transistor dimensions were decreased by half. The sub-micron dimension limitation was overcome in the 1980's, and by 2010 manufacturers created transistors with a gate length of 32 nm. Despite the fact that the first integrated circuit transistors were manufactured on "bulk" silicon wafers, by the end of the 1990's it became evident that notable performance enhancement could be achieved by using a new substrate, called *Silicon-On-Insulator*(SOI) with which transistors are made in a thin silicon layer layered on top of a silicon dioxide layer.

SOI improves not only circuit speed, but also power utilization. In the 2000's, real semiconductor organizations, including IBM and AMD, started fabricating chips utilizing SOI substrates on a large industrial scale. SOI devices have a decreased parasitic capacitance and an improved current drive.

1.2 MOSFET TECHNOLOGY OVERVIEW

There are major challenges affecting the achievement of the goals of the semiconductor industry, which are increasing the clock speed, the number of transistors per chip, and the memory storage density, as well as reducing the power dissipation to increase the chip yield.

The ITRS is responsible for highlighting these requirements on a periodical basis. So far, the device dimensions have been consistently scaled as explained in the previous section, until reaching the current 14nm channel length. The nanoscale dimensions of the current technology node cause a decrease in the gate's potential distribution and channel current flow control. This is chiefly a result of the nearness of the source and drain in nanoscale devices. Thus, the electrostatics of devices in the nanoscale regime are affected by unwanted short channel effects (SCE). The most notable short channel effects are [4]:-

- Charge sharing (causes a threshold voltage roll-off)
- Punch-through (causes a degradation in the subthreshold slope)
- Drain-induced barrier lowering (DIBL) (the injection of electrons from source to channel is affected by the closeness of the source and drain

terminals, thus affecting the electron injection barrier between source and channel.)

These short channel effects are the reason behind the modelling and fabrication of multiple gate devices, which are shown in Figure 1.2. These devices include: Double Gate, Triple Gate, and Quadruple Gate MOSFETs. These multi-gate structures have an improved gate control that is much stronger than standard and planar bulk MOSFETs. The robust gate control stems from the increase in the electric field of multi-gate structures, thereby enhancing their electrostatics. Most of the time, the word *double gate* refers to the presence of one gate electrode on two opposite sides of the device. Likewise, the term *triple gate* is used when the gate electrode is folded over three sides of the device. [4]

Moving into the deca-nanometer regime has brought the effects of quantization to the industry's attention, seeing as quantization is inevitable if the device channel thickness has the same order of magnitude as the de Broglie wavelength [5]. This adds to the complication of nanoscale modelling as complex mathematical and physical modelling is required to correctly predict the device behavior. Furthermore, deca-nanometer device fabrication is another added issue, since the doping fluctuates at these dimensions. [6]

Partially Depleted (PD) SOI single gate MOSFETs were used in high temperature applications before becoming the conventional device for microprocessors with high performance. In order to improve the subthreshold slope and current drive, a contact between the body and gate is created which improves the body effect factor. However, this contact causes the device to not operate effectively if the supply voltage is below 1 volt. Fully Depleted SOI MOSFETs already have an improved subthreshold slope, drive current, and body effect factor due to superior coupling between the gate and the channel. Hence, they are mostly used in low voltage and power applications. [7], [8]

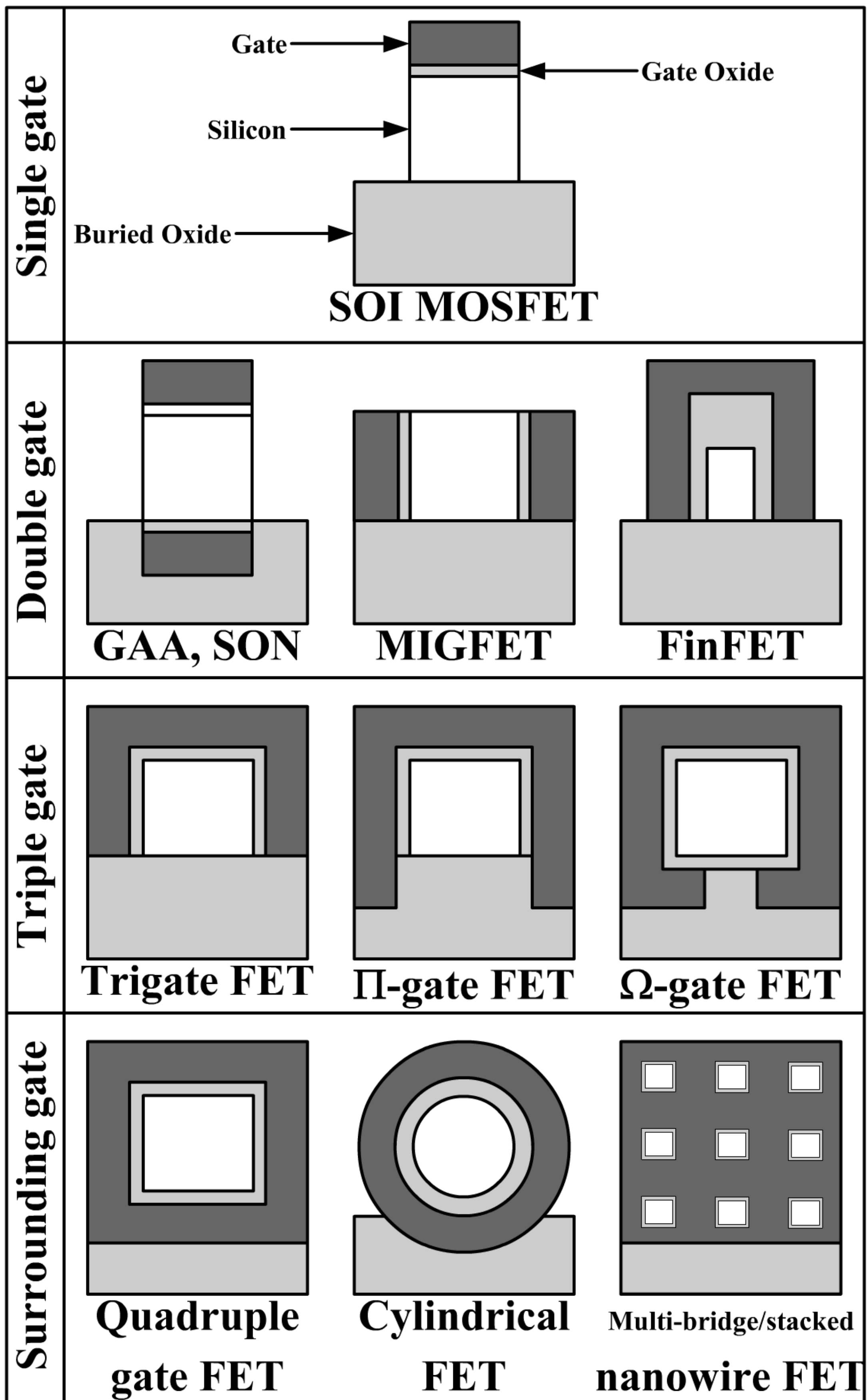

Figure 1.2 Multi-Gate Transistors [4]

Double-gate MOSFETs were first introduced as XMOS transistors in the work published in 1984 [9]. The transistor was named an XMOS transistor because its cross section resembled the Greek letter Xi (Ξ). The research's findings are summarized in the fact that short channel effects can be reduced by placing a Fully Depleted SOI MOSFET between two gate electrodes that are interconnected. Thus, the channel depletion region is better controlled through the reduction of the drain's electric field on the channel. Three years later, a research group published the paper in [10] which highlighted the volume inversion property in DG devices.

Classical device physical modelling predicted confinement at the Si/SiO_2 interface; however, it was later discovered that carriers in multi-gate MOSFETs are confined at the center of the silicon film rather than the Silicon/Oxide interface. In 1990, volume inversion was observed for Gate-All-Around (GAA) structures. The structure of the GAA at that time included a polySi gate electrode surrounding the channel region's entirety. The width of the device was larger than that of the silicon thickness, hence, the device was actually a DG MOSFET; particularly due to the lack of contribution of the side gates to the electrostatic channel control. This is shown in Figures 1.3 and 1.4 [11]

The first double-gate MOSFET to be fabricated was the DELTA MOSFET in 1989 [12]. DELTA stands for "fully **DE**pleted **L**ean channel **T**r**A**nsistor". This transistor was made as a vertical ultra-thin MOSFET with selective field oxide for SOI isolation. This vertical tall thin silicon was called a "fin". The cross section of the DELTA MOSFET is shown in Figure 1.5. It is also interesting to note that the FinFET structure is similar to that of the DELTA device, with the exception of a hard mask on the silicon fin. This hard mask is comprised of a dielectric layer and is used to eliminate parasitics at the top corners. [13] There are other implementations of double-gate MOSFETs; those include [11]:

- FinFET
- SON (Silicon-on-Nothing) MOSFET
- MFXMOS (Multi-Fin XMOS)
- Triangular-wire SOI MOSFET
- Δ-channel SOI MOSFET

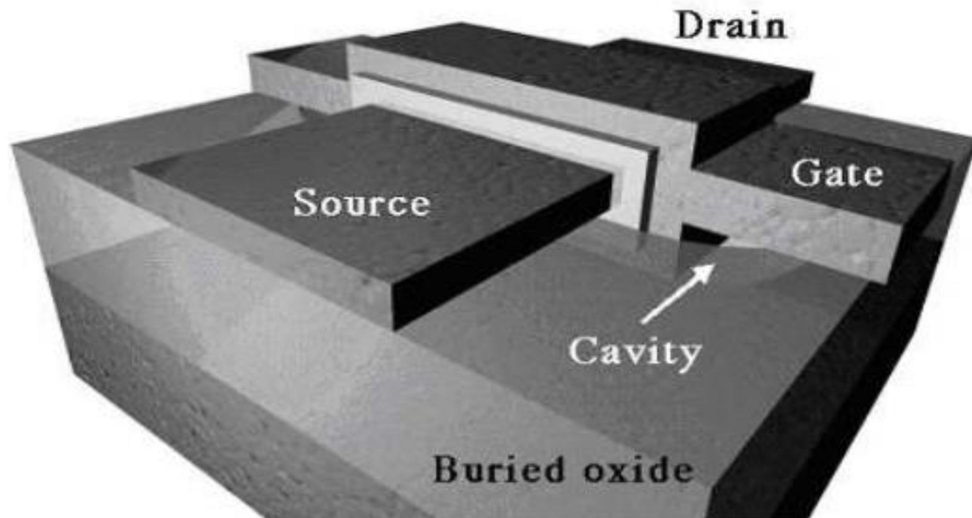

Figure 1.3 Original GAA structure [11]

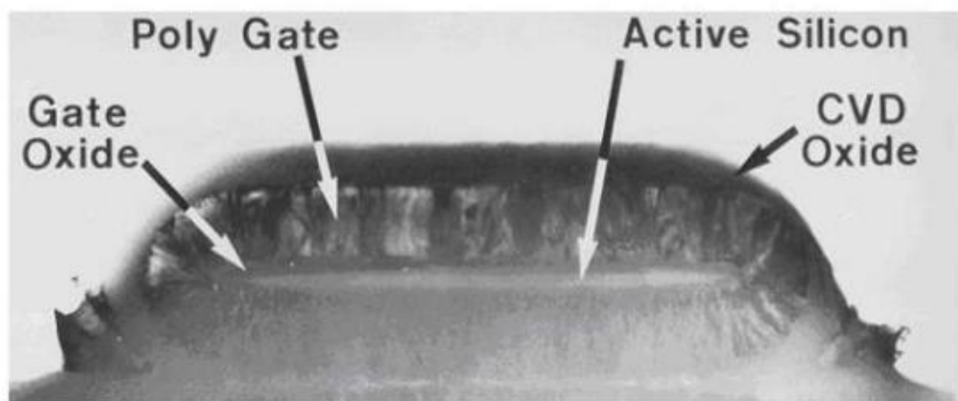

Figure 1.4 TEM Cross Section of the Original GAA device [11]

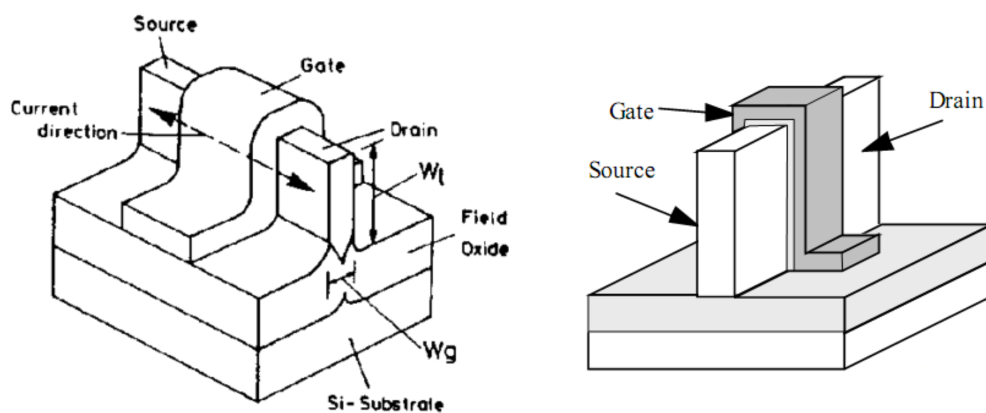

Figure 1. 5 DELTA DG MOSFET [12]

1.3 DEVICE MODELLING FOR CIRCUIT DESIGN

The production cost and time consumed in design and manufacture are one of the major challenges in today's field of circuit design. EDA (Electronic Design Automation) tools are the pillar of cost and time reduction for design, synthesis for masks, and simulation of discrete devices. EDA tools enable the designer to analyze the entirety of a semiconductor chip to guarantee proper functionality. The majority of the environment variables can be controlled through the EDA tools; such as temperature, power supply variations, dopant fluctuation, and statistical variations resulting from line/edge roughness. [14]

There are two major discrete device simulators used extensively by circuit designers; Silvaco's ATLAS, and TCAD Sentaurus. These tools provide 2D and 3D device simulations with the capability of including highly complex physical models and numerical simulation methods. This is carried out through a volume grid based on the dimensionality of the system (2D or 3D) and each grid point is solved through a PDE (Partial Differential Equation) iterative solver. The downside is that if a 3D structure is being simulated, then the simulation time could take one to several days depending on the required result accuracy settings. [14]

This is why these iterative methods are not used in circuit simulators; instead, compact approximate models are used to emulate the device's actual characteristics with enough accuracy. The most commonly used circuit simulators are SPICE and ELDO. There are different models that exist for these tools which take into account different physical effects. These models can be divided into three groups as shown in Figure 1.6.

The first group of model types, *Surface-potential-based models*, solve the surface potential for the input equation at the two terminals of the channel of the device. The charges for the terminals as well as the current, and other characteristics are calculated from the surface potential solution. Examples for these models include: MOS Model 11, PSP and the SP Model as shown in Figure 1.6.

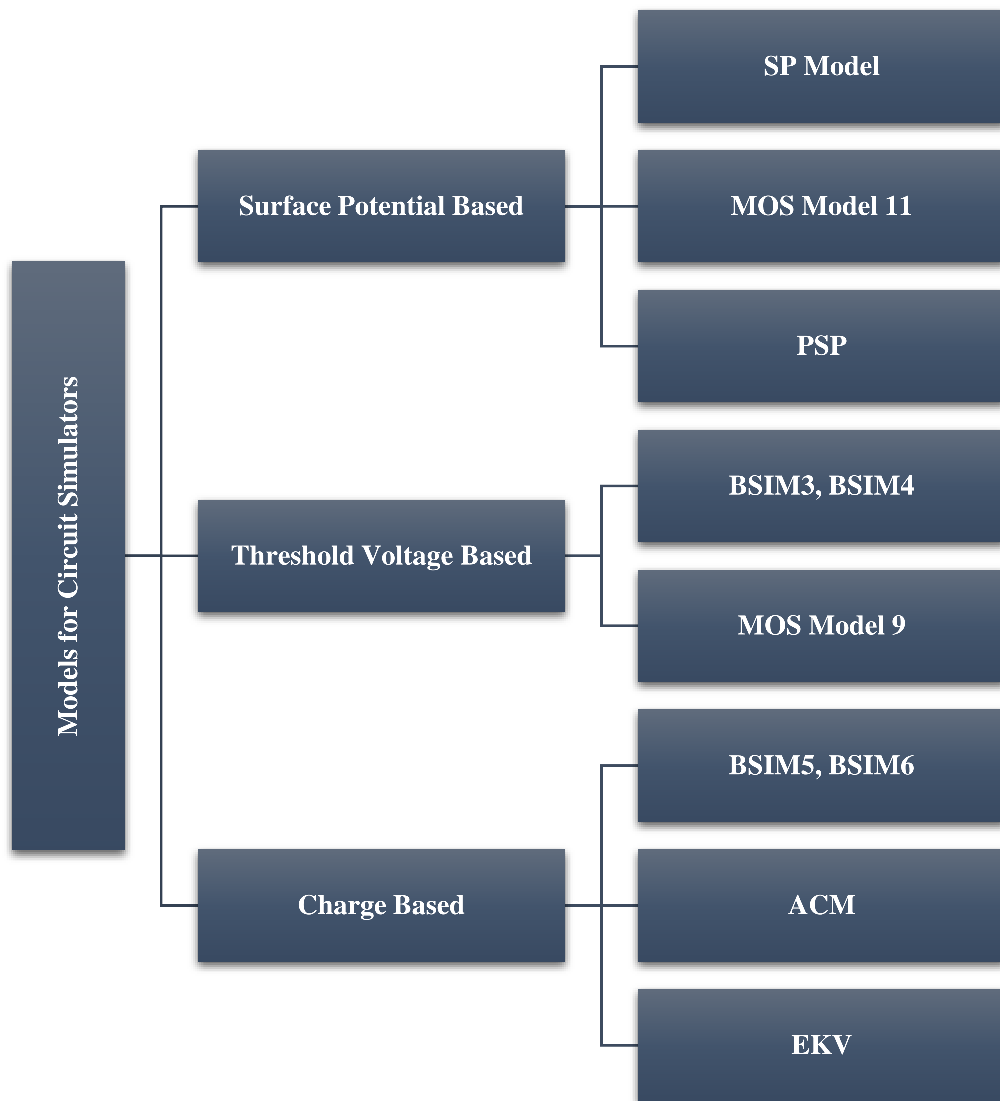

Figure 1.6 Classification of models for Circuit Simulators [15]–[20]

The second group of models for circuit simulators are *Threshold voltage based models*. These models approximate the surface potential as a function of the input gate-source voltage, V_{GS}, in the following manner:

- Constant, if $V_{GS} > V_{TH}$
- Linear, if $V_{GS} < V_{TH}$

The result is divided into separate solutions for each region of operation, and thus, smoothing functions are applied for the regions to be connected. Examples for this group of models are the BSIM3, BSIM 4 and the MOS Model 9.

The third and final group of models are *Charge-based models*. These models calculate the inversion charge density at the two ends of the channel of the device. These charge densities are used in the expression of the output of the model. The capacitances and conductance are derived from these densities as well. As shown in Figure 1.6, some examples are BSIM5, BSIM6, ACM and EKV models.

Compact models suitable for circuit simulators are required to emulate the behavior of the transistors in all regions of operation as accurately as possible. These models are classified into three groups: physics-based, numerical fit, and empirical based models.

Physics-based models encompass the use of solely physics-based formulas to describe device behavior. This gives the advantage of modelling the devices that have been downscaled. Published physics-based models are frequently developed to define the behavior of either single electrical device characteristics (such as threshold voltage and subthreshold slope) or long channel devices.

The second class of models are numerical fit models. These models are mathematical formulas which have no relation to the actual device physics. Simulations are performed and fitted with several fitting parameters in order to obtain a model result that is suitable for device behavior emulation. However, this makes the model's validity unknown outside the simulated data range. Furthermore, these models do not offer any insight into the physical device behavior.

The final class of models are empirical based models, which are a combination of the aforementioned types. They are comprised of less complex physics-based equations in addition to numerical fitting parameters. The advantage is that the models produced are considerably simpler than physics-based models and provide an enhanced performance when compared to numerical fit models. However, the downside lies in the use of fitting parameters, which hinder the model's ability to describe the device behavior if the device physics are modified.

There are certain requirements to be met if a compact model is to be used in a circuit simulator. These requirements are:

- In order to effectively model the electrical behavior of the device, the modelling must be derived with a high enough accuracy so as to cover all regions of transistor operation.
- The models must not only be accurate, but also simple (accuracy/simplicity trade off).
- A single model should be valid for all device dimensions used in the current technology node.
- Convergence problems should be taken into account while modelling the drain current, as they must be continuous in the first order derivatives or higher derivatives depending on the application type.

1.4 LITERATURE REVIEW

Since quantum models are considerably more complex than semi-classical ones, in order to simplify calculations it is convenient to start with a relatively simple classical model that can qualitatively describe the semiconductor and then create a quantum version of it (quantum correction).

The simplest class of semi-classical models of semiconductor devices are drift diffusion models, first introduced by Van Roosbroeck in 1950 [21]. They were obtained by rescaling the Boltzmann transport equation and using the distribution function expansion of Chapman-Enskog.

Given that semi-classical drift-diffusion models have been researched in depth [22], their results are used extensively in the industry. Nonetheless, they are only applicable when the dimensions are within the micrometer range, i.e. when the electrical fields are not rapidly changing. Since there are two types of carriers in semiconductors, bipolar drift diffusion equations were introduced. Rigorous derivation of semi-classical drift-diffusion equations for various cases were done by Poupaud, Ben Abdallah/Tayeb, and Masmoudi/Tayeb over the past 25 years. Solution analysis came

into existence in the 70's and 80's by Mock and Gajewski/Groeger. Numerical solutions were obtained as early as 1964 by Scharfetter/Gummel.

Thus far, a large amount of work has been published regarding the incorporation of quantum effects in devices. The prominent 1993 work by M. Shur [23] incorporated drain induced barrier lowering (DIBL) effects in short channel MOSFETs and explored the subthreshold regime of operation. Nonetheless, countless quantum effects have been exposed in nanoscale devices since this publication. The work published by Li & Yu [24] presented a DG model derived from hydrodynamic transport; however, it is a simulation based model that relies on iterations. While Wagner et al [25] produced a DG model based on diffusive transport, it is also a computational based model. Both [24] and [25] do not provide explicit models for the potential or the threshold voltage. Additionally, the 2D DG threshold voltage roll off model developed by Chen et al [26] did not include DIBL effects. Baccarani and Reggiani [27] developed a DG model accounting for quantum effects including confinement, Fermi statistics, and non-static transport effects; however, the confinement's field dependency is not included.

The research completed in [28], [29] modelled the carrier confinement based on the effective oxide thickness definition and did not introduce a threshold voltage compact model. However, the lowest energy band was considered to account for the threshold voltage, while ignoring the short channel effects. A new analytical model incorporating both symmetric and asymmetric DG in a single structure on SON rather than SOI is proposed in more recent work [30]–[32], through solving 2D Poisson's equation with 1D Schrödinger under the dual material front gate to obtain the potential distribution. However, the fabrication of this structure requires additional masking procedures due to its asymmetric design.

The vast majority of the models in literature neglect high channel doping effects and resort to lightly doped and undoped devices. This is due to the fact that the absence of depletion charges in undoped devices boost the mobility of carriers. Depletion charges generally cause degradation in the drain current as a result of their effect on the electric field. Furthermore, lightly doped devices do not suffer from any dopant fluctuations, thereby avoiding threshold voltage fluctuations. [33], [34]

The work done in [35] by Taur included the mobile charge term in Poisson's equation to present an analytical one dimensional model for undoped DG MOSFETs as well as a capacitance model. The work was further developed in [36] by deriving an analytical drain current model from the current continuity and Poisson's equations solutions in closed form. In [37], a continuous subthreshold model for the long channeled version of the device was proposed.

In [38], a charge-based model that is oriented towards design was presented. The device is an undoped symmetrical DG device. In the paper, the authors linked their methodology to the EKV bulk MOSFET modelling, thereby leading to a distinctive g_m/I_d design technique for DG structures.

The first explicit expressions for the potential distribution as a function of biasing and geometrical dimensions was proposed in the 2010 work in [39]. The compact quantum modelling involved the electrostatic potential and electric charge for thin film symmetric undoped DG MOSGFETs. The validity of the model was confirmed through comparisons with self-consistent Schrodinger-Poisson solvers.

Most of the aforementioned models were validated through comparisons versus numerical data resulting from Silvaco (ATLAS) and Sentaurus (TCAD). The proposed models were well matched; however, it must be noted that most of the models are effective in long channel regions. Thus, they cannot be used for electrostatics prediction in the new nanometer structures. Furthermore, the nanoscale fabrication constraints require the presence of doping in the channel region, thereby influencing the electrostatic performance. The channel doping causes a shift in the threshold voltage as well as a degradation in the carrier mobility and subthreshold slope. This adds to the urgency of short-channel device compact model development which correctly predict the electrostatic behavior.

1.5 RESEARCH MOTIVATION AND THESIS STRUCTURE

The double-gate MOSFET geometry gives the device numerous prominent features that deem it suitable to meet the deca-nanometer roadmap requirements as

opposed to the standard bulk MOSFET [40]. The DG device permits shorter channel lengths, as well as a 60mV/dec subthreshold slope, compared to 80mV/dec for the bulk MOSFET which leads to a higher overdrive voltage for the same off current [41] [27]. One main advantage of DG devices is improved carrier transport, as the device can essentially be undoped. Its dual-gate structure allows for the lowered channel doping which not only controls short channel effects, but also provides a solution to one of the key limitations in device scaling, which is tunneling leakage current. [42][43].

Although the DG MOSFET is more scalable than the standard FET, migrating into the nanometer regime leads to quantum effects in addition to short channel effects. Thus, device models based on classical and semi classical theories are not applicable for devices below 20 nm. Quantum effects, particularly quantum confinement, must be accounted for in order to obtain more precise models. [44] Additionally, DG MOSFETs operating in the deca-nanometer regime face reliability apprehensions as a result of degradations, most notably hot carrier injection (HCI) and negative bias temperature instability effects (NBTI) [45][46]. These two particular degradation mechanisms cause permanent interface traps which are irrecoverable after some time of operation. HCI is less significant in PMOS, because the mean free path and mobility for holes are less than that for electrons[47][48]. NBTI not only causes a decrease in transconductance and channel carrier mobility, but also causes an increase in the off current and in the absolute threshold voltage value [49].

In spite of these contributions, there is still a need for a relatively simple Verilog-A compatible model of the DG device to study its influence on various aspects of circuit performance in order to aid in forthcoming design procedures. In this thesis, a quantum-corrected model based on the quantum-free work of [50] is proposed. The proposed model is based on solving 2D Poisson's equation with 1D Schrödinger as done in [30]–[32]. An explicit compact expression modelling the threshold voltage and inversion charge is proposed including short channel effects, DIBL, and quantum effects including quantum confinement. Furthermore, this thesis presents, for the first time, two dimensional simple compact models incorporating quantum confinement, NBTI and short channel effects (SCE). The device considered in the modelling is a symmetrical lightly doped DG device, while its source and drain are highly doped. A

lightly doped DG provides better carrier transport along with a reduction in scattering [42], [43].

This thesis is divided into five chapters. Chapter 1 is the introduction and comprises a brief background on the semiconductor MOSFET industry, as well as, a review of the current multi gate MOSFET technology. It also includes an in depth literature review covering prominent research involving DG MOSFET modelling, along with an insightful review of the relation between device modelling and circuit design.

Chapters 2 and 3 are the fundamental chapters of the research. Chapter 2 starts by covering the underlying physics behind quantum confinement in semiconductors, particularly MOSFET devices. Types of quantum confinement are explained, as well as a brief mathematical overview of Poisson and Laplace equations which are vital to modelling the potential distribution. The details of the two dimensional modelling of symmetrical lightly doped double-gate MOSFETs are then delved into. The modelling procedure is presented thoroughly taking into consideration short channel effects and quantum confinement. Expressions for the potential distribution, threshold voltage, and the carrier charge sheet density are derived from analytical 2D Poisson and 1D Schrödinger equations including 2D electrostatics while taking into account electron and hole quasi-Fermi potential effects. Finally, the models are validated versus 2D numerical simulations carried out on COMSOL Multiphysics, as well as published BALMOS numerical simulations.

Chapter 3 incorporates NBTI to the model to assess reliability. NBTI modelling work in [51] was used to incorporate effects of interface state generation and hole trapping due to NBTI. The result is compact 2D models for the potential distribution and threshold voltage for undoped symmetrical double-gate p-channel MOSFETs (PMOS), including quantum confinement effects and negative bias temperature instability. The models are then verified for accuracy by comparison with numerical COMSOL simulations.

Finally, Chapter 4 concludes the thesis with a summary of the research and the intended future work.

CHAPTER 2
QUANTUM DEVICES

2.1 QUANTUM CONFINEMENT IN MOSFETS

In highly scaled MOSFETs, the carriers in the inversion layer suffer from quantum confinement which affects not only the threshold voltage but also the gate capacitance. The scaling of semiconductor devices into the deep submicron and deca-nanometer scale entails high doping levels and thin oxides in order to minimize short channel effects. As a result, a sharp potential well is created due to the electric field increase at the Si/SiO_2 interface. This potential well induces carrier quantization energy. In partially depleted (PD) MOSFETs, quantum confinement is in the potential well characterized by the silicon conduction band and the gate/oxide boundary. A quantum well is formed by the Silicon/Oxide conduction band offset and the silicon conduction band bending as shown in Figure 2.1. The carriers are confined in this quantum well, which causes energy level splitting into sub-bands, thereby forming a two dimensional density of states (DOS). Furthermore, the lowest electron energy level does not overlap with the conduction band bottom as illustrated in Figure 2.1. [52], [53]

In a 2D system, the DOS for low energies is less than that in a classical system (3D). Thus, the total number of carriers is less in a 2D system than a 3D system for the same Fermi level. This affects the inversion layer's net sheet charge, which results in the critical issue of a rise in the threshold voltage of the device. Carriers, which are compactly confined in the potential well, occupy the lowest energy levels, while those not as securely confined behave like classical particles. The confinement of the carriers in the well increases as the electric field increases, which results in an increase in the system quantization. The quantum mechanical confinement causes a modification in the distribution of carriers in the channel, seeing as the inversion charge's maximum is pulled away from the interface into the Si film as shown in Figure 2.1. [52], [53]

Quantum carrier confinement in nanoscale DG MOSFETS is manifested as a result of two possible occurrences: electric confinement and structural confinement (Figure 2.2). The first type, electric field induced confinement, results from the presence of a strong interface electric field, while the latter, silicon thickness induced

confinement, is an outcome of the thin silicon film potential well. Quantum mechanically confined carriers in nanoscale thin DG MOSFETs are both structurally and electrically confined, thus quantum mechanical effects on both the drain current and threshold voltage are significant.

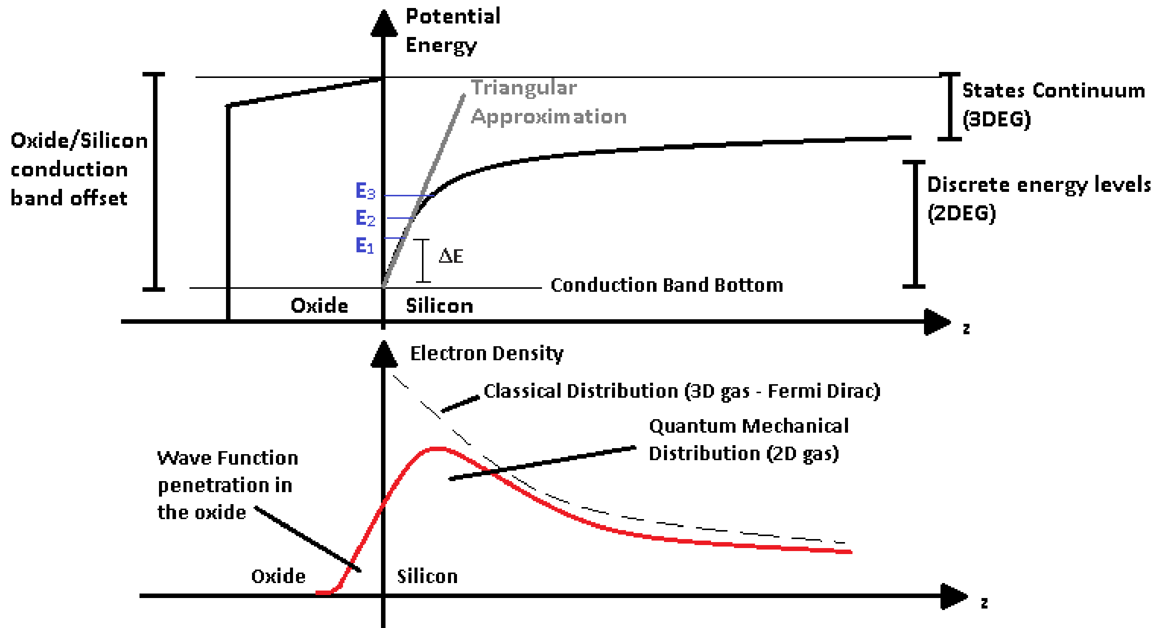

Figure 2.1 Conduction Band Bending of a PD MOSFET in inversion regime showing the different energy levels resulting from the quantization effects of the 2DEG confined in the surface potential well and the corresponding electron distributions in the direction perpendicular to the interface for the classical and quantum-mechanical case.

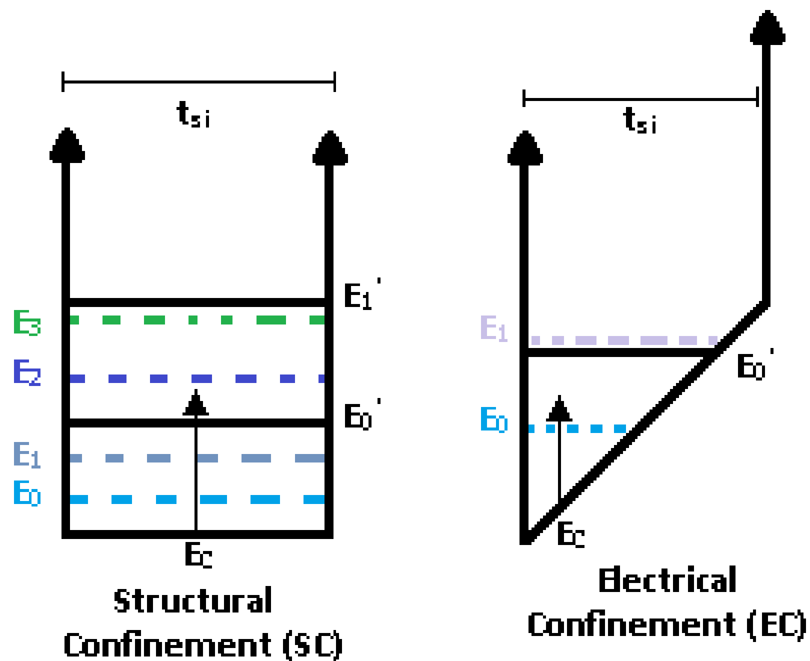

Figure 2.2 DG NMOS vertical cross section energy band diagrams illustrating carrier confinement due to structural confinement and electrical confinement in the silicon film.

2.2 TWO DIMENSIONAL POTENTIAL IN DG MOSFETS

A schematic for a symmetric DG MOSFET and its band diagrams in vertical and horizontal channel cross sections is shown in Figure 2.3, as drawn in the work in [54]. In the diagram, y is the silicon thickness direction, x is the channel length axis, t_{ox} is the oxide thickness, and V_G is the gate bias voltage. The current flows in a direction along the channel length (x-axis) and the quasi-Fermi level, E_{FN}, is assumed constant along the thickness. The quasi-Fermi electron level of the source, E_{FS}, is the reference taken for the energy levels in the diagram. In the vertical cross-section, the potential distribution is presented through a parabolic dependency on the silicon film position. It should be noted that this occurs when the gate bias voltage is the same on both gates and in the strong inversion regime.

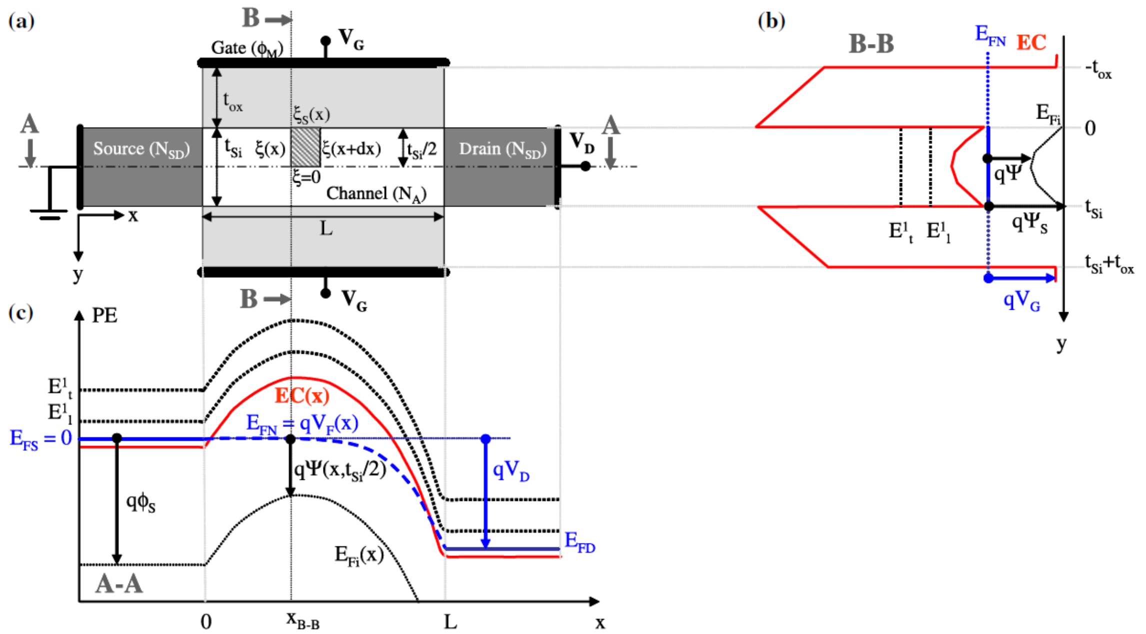

Figure 2.3 (a) Schematic for a symmetric DG MOSFET and its band diagrams in a vertical (b) and horizontal (c) cross section in the channel [54]

In order to model this 2D potential, two vital equations are utilized in physical and electrostatic modelling. These two equations are Poisson and Laplace equations. Poisson's equation is a partial differential equation based on Maxwell. Electrostatics calculations are performed through relating the electrostatic potential to the charge density along a gradient. The electric field for the gradient is related to the charge density through a divergence operation. This is shown in equation (2.1). [55]

$$\nabla.\overrightarrow{E(r)} = \frac{\rho(r)}{\varepsilon} \tag{2.1}$$

where ρ is the charge density, r is the gradient, $\vec{E}$ is the electric field, and ε is the material permittivity.

The electric field of Poisson's equation can then be incorporated as in (2.2)

$$-\nabla.\overrightarrow{E(r)} = \frac{-\rho(r)}{\varepsilon} = \Delta\phi(r) \tag{2.2}$$

where ϕ is the potential and if it is taken as three dimensional, the Laplace operator, Δ can be used as in (2.3). Then the Poisson potential can be expressed as in (2.4).

$$\Delta = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \tag{2.3}$$

$$\Delta\phi(x, y, z) = \frac{-\rho(x,y,z)}{\varepsilon} \tag{2.4}$$

2.3 QUANTUM STATISTICAL ESTIMATION FOR 1D AND 2D CONFINEMENT

One dimensional confinement occurs in devices with a small thicknesses L_z but with a large enough width L_y, and length L_x. For such device, the electron density is calculated by (2.5) and (2.6), which were calculated using Fermi-Dirac statistics. The two density equations describe the conducting electron density in the source and channel respectively.

$$n_s \approx K \frac{mkT}{\pi\hbar^2 L_z} \sum_j ln\left[1 + e^{-Q_j+\eta+\frac{V_s}{V_T}}\right] \tag{2.5}$$

$$n_{ch} \approx K \frac{mkT}{\pi\hbar^2 L_z} \sum_j ln\left[1 + e^{-Q_j+\eta+\frac{\phi_{(y)}}{V_T}}\right] \tag{2.6}$$

$$\eta = \frac{E_F - E_C}{V_T} \tag{2.7}$$

where K describes the influence of doping in the same manner as the valence degeneracy factor, $\hbar$ is the reduced Planck's constant, V_s is the source voltage, k is the Boltzmann constant, T is the temperature in Kelvin, Q_j is the ratio of quantum energy due to confinement along the z axis, $\phi_{(y)}$ is the electrostatic potential, and V_T is the thermal voltage.

The classical analogue for these two density formulas would be that of the potential field being entered by a gas along the ordinate and redistributing its density. In the DG MOSFET, this would be because of the gate potential as explained in Section 2.2.

To account for quantum confinement, a 2nm silicon thickness and a gate voltage up to 0.6V will allow the confinement energy to dominate the exponential in (2.5) and (2.6). This will cause j levels to give a steadily decreasing contribution, thus the logarithm can be approximated, and calculating with the first two levels is sufficient for a first quantum approximation. However, if a device is to be described with all three small dimensions, quantum confinement along the ordinate becomes important as well. Consequently, not only should Poisson's equation be solved simultaneously along the infinite well with potential gradient, but Schrödinger's equation should also be solved along the abscissa. Density equations for this problem are of the form shown in (2.8).

$$n \sim \sum \frac{F_{-1/2}(\theta)}{L_y L_z} \tag{2.8}$$

where F is the Fermi-Dirac (FD) integral.

2.4 POISSON AND SCHRÖDINGER'S EQUATION SOLUTION

Utilizing the well-studied particle in the box problem, with a zero potential inside the box, the wave function solution is zero on the sides of the box and the energy is discrete, starting with zero point level energy. Given that the probability density is the square of the modulus of the wave function, it is expected to have a carrier density of zero near the gate terminal.

In this problem, the potential is not zero and its presence modifies the wave functions. Therefore, both the Schrödinger (2.9) and the Poisson (2.10) equations must be solved simultaneously.

$$2m[E + e\phi]\psi = -\hbar^2\psi'' \tag{2.9}$$

$$\phi'' = \frac{en}{\varepsilon} \tag{2.10}$$

$$n \sim |\psi|^2 \tag{2.11}$$

where the derivatives are in the thickness direction.

Since both imaginary and real components of the wave function ψ satisfy Schrödinger's equation, as well as, the fact that the zero potential energy is purely real, the probability density in (2.11) can be modified as shown in (2.12).

$$n = n_s\psi^2 \tag{2.12}$$

Substituting psi with n in Schrödinger's equation, expressing potential in terms of n, along with its derivative, and taking double derivative leads to:

$$\phi'' = -\frac{\hbar^2}{2me}\left[\frac{(\sqrt{n})''}{\sqrt{n}}\right]'' = -3Q'' \tag{2.13}$$

where Q is Bohm's quantum potential. So Poisson's equation (2.10) could be solved for n instead of phi:

$$-\frac{\hbar^2}{2me}\left[\frac{(\sqrt{n})''}{\sqrt{n}}\right]'' = \frac{en}{\varepsilon} \tag{2.14}$$

$$\left[\frac{(\sqrt{n})''}{\sqrt{n}}\right]'' = \alpha n,\ \alpha = -0.664/nm \tag{2.15}$$

The result is a fourth order nonlinear differential equation. The numerical solution representing the wave functions derived from (2.15) is shown in Figure 2.4. Similar to the zero potential case, the probability density is largest in the center of the device, but has a number of local minima and maxima before it reaches the gate.

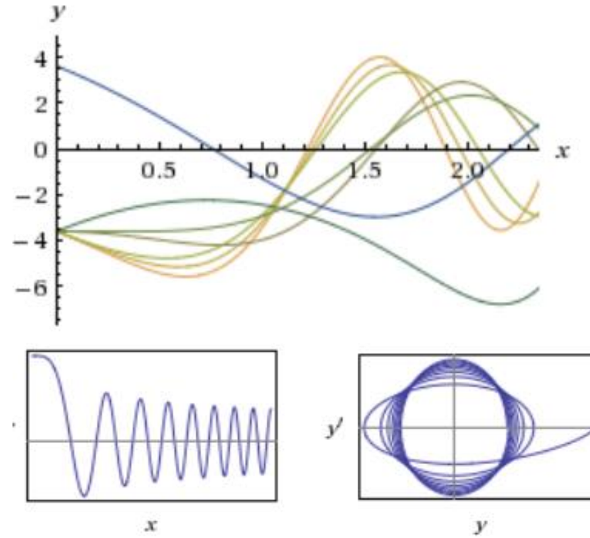

Figure 2.4 Numerical Solution for the Fourth Order Differential Equation in (2.15) where the ordinate represents the density, and abscissa is the Silicon Thickness

In the DG MOSFET, confinement exists in two directions and in one direction the electron moves freely in and out of the device. In the case where the source cross section is the same as the space inside the two gates, the carrier electron wave function does not change when it crosses the source-channel boundary. Schrödinger's equation (2.9) and Laplace's equation (2.16) will be solved.

$$\Delta\phi = 0 \tag{2.16}$$

Laplace's equation will provide the solution for the potential, while combining both equations will result in the wave function and the density. The boundary potentials for the side of the box are equal to the gate, source, and drain potentials, and are zero for the two remaining sides. Laplace's equation in rectangular coordinates for three dimensions has a general solution (2.17) which satisfies the boundary conditions.

$$\emptyset = e^{\pm i\alpha z} e^{\pm i\beta z} e^{\pm x\sqrt{\alpha^2+\beta^2}} \tag{2.17}$$

2.5 POTENTIAL MODEL DERIVATION

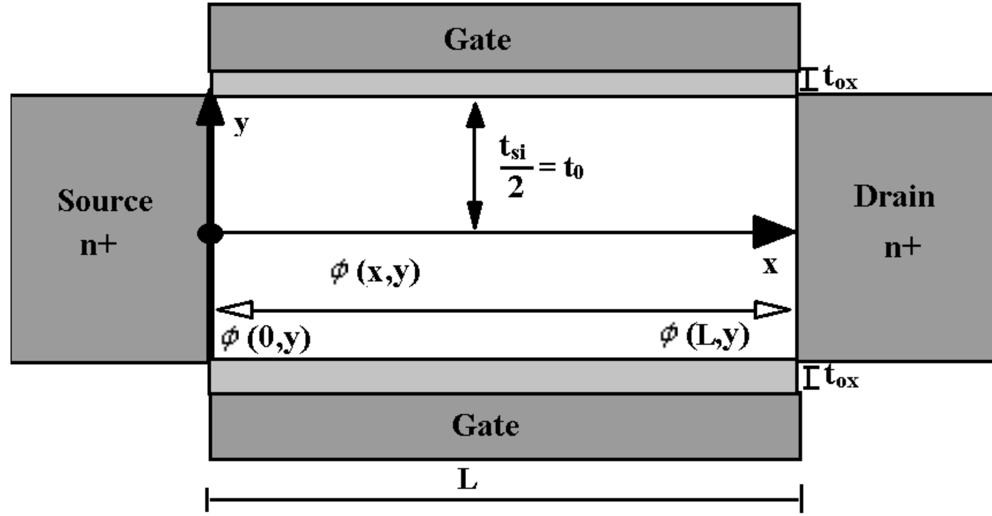

Figure 2.5 Cross section of the DG MOSFET with the used coordinate system

Figure 2.5 shows the DG MOSFET used in the modelling, which is similar to that utilized in [50]. Quantum mechanics provides some simplification to the work done in [50].

For accurate device modelling, the electrostatic body potential distribution for the range of biasing conditions must be modelled. The potential modelling is described based on Poisson's 2D equation:

$$\frac{\partial^2 \varphi}{\partial x^2} + \frac{\partial^2 \varphi}{\partial y^2} = \frac{-\rho\,(x,y)}{\varepsilon} \tag{2.18}$$

where φ is the electrostatic potential, ρ is the space charge density, and ε is the dielectric constant.

In order to solve Poisson's equation, superposition is applied to separate the solution into a 2D Laplace equation for the capacitive coupling of the inner electrodes and the remainder comprises the potential arising from body charges. The boundary conditions are defined by the contacts at the source, drain, gates, and dielectric gaps in the body cross sections. Since the DG MOSFET used is lightly doped, the doping concentration is up to 10^{16} cm^{-3} [56], then their contribution is negligible in the

subthreshold region compared to the electrode capacitive coupling and charge coupling. This is valid even if the electron concentration rises upon connecting the device to a positive voltage, seeing as the quantum confinement energy will cause the density to fall quickly. [57]

As a result, Poisson's equation is simplified to a 2D Laplace equation. The decomposition of potential by superposition is no longer necessary. A single potential depending solely on x and y, can be found. That potential satisfies the same equation as φ_1 in [50], but with slightly different boundary conditions shown in equations (2.19) to (2.22):

$$\varphi_{\left(x,\pm\frac{Ly}{2}\right)} = V_g - \varphi_{ms} \tag{2.19}$$

$$\varphi_{\left(-\frac{Lx}{2},y\right)} = V_s \tag{2.20}$$

$$\varphi_{\left(\frac{Lx}{2}\right)} = V_d \tag{2.21}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_{gs} - \varphi_{ms}\right] = -\varepsilon_{si}\frac{\partial\varphi_{\left(x,\pm\frac{Ly}{2}\right)}}{\partial y} \tag{2.22}$$

where V_g, V_d, V_s, V_{gs} are the gate, drain, source, and gate-source voltages respectively and φ_{ms} is the effective contact potential difference. In the quasi 2D case, the solution for potential is found in (2.23), (2.24), and (2.25).

$$\varphi = \varphi + \tilde{\varphi} \tag{2.23}$$

$$\varphi = \frac{4\left(V_g - V_{bi}\right)}{\pi \cosh\left[\frac{(2k+1)\pi L_y}{2L_x}\right]} \times \sum_k \frac{(-1)^k}{2k+1}\left[\cos\left(\frac{(2k+1)\pi x}{L_x}\right)\right]\left[\cosh\left(\frac{(2k+1)\pi x}{L_x}\right)\right] \tag{2.24}$$

$$\tilde{\varphi} = \left(\left(\sum_{\tilde{k}} \left\{ \frac{2}{\pi \sinh\left[\frac{(2\tilde{k}+1)\pi L_x}{2L_y}\right]} \times \frac{(-1)^{\tilde{k}}}{2\tilde{k}+1} \cos\left(\frac{(2\tilde{k}+1)\pi y}{L_y}\right) \times \left[(V_d + V_s)\left(\tanh\left(\frac{(2\tilde{k}+1)\pi L_y}{2L_x}\right)\right)\left(\cosh\left(\frac{(2\tilde{k}+1)\pi x}{L_x}\right)\right) + (V_d - V_s)\left(\sinh\left(\frac{(2\tilde{k})\pi x}{L_x}\right)\right) \right] \right\} \right) \right) \quad (2.25)$$

The fourth boundary condition was not used; nevertheless, it is valid when the surface charge on the boundary is zero in the quasi-2D case. It should be noted that the necessity of superposition of the two potentials here is from the boundary conditions, not for the elimination of density from one equation. Figure 2.6 depicts the surface potential distribution along the channel for the proposed model compared with the classical model from [50] for a silicon thickness of 5nm. The proposed model was also compared with 2D numerical simulations using COMSOL for further result verification, as shown in Figure 2.7. There is good agreement between the model's results and the numerical simulation. Figure 2.8 shows the proposed model's result along the silicon thickness compared with the BALMOS numerical simulation provided in [40]. The results are well matched within ±5%.

Figure 2.6 Surface potential distribution along the channel for t_{si}=5nm, t_{ox}=1nm, L=20nm,V_{gs}=0.1V, V_{bi}=0.6V N_A=10^{16}cm^{-3} for the proposed model compared with the classical model from [50]

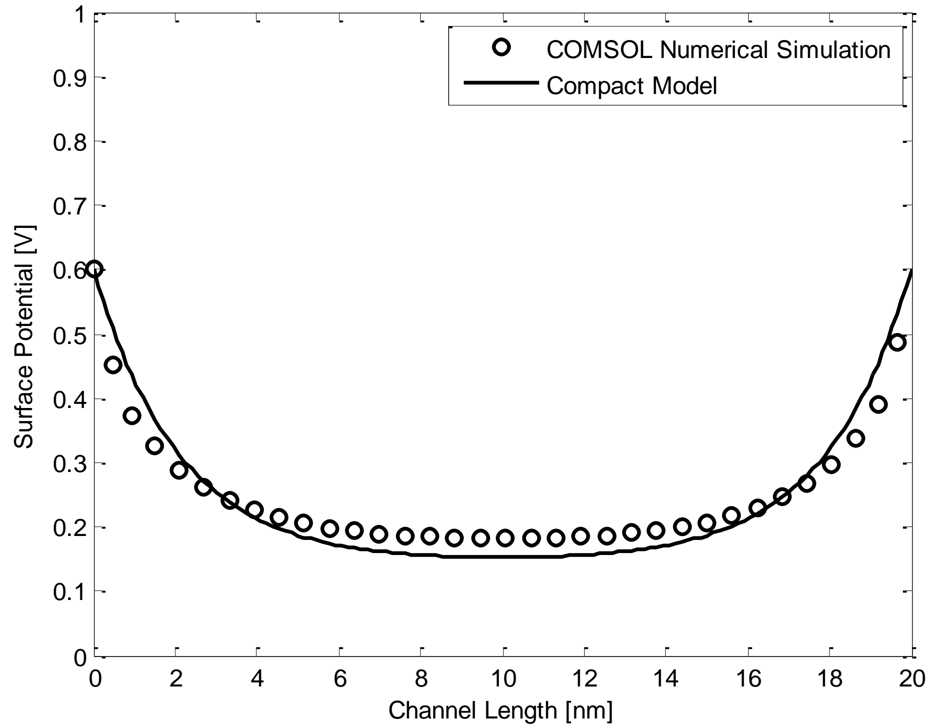

Figure 2.7 Surface potential distribution along the channel for t_{si}=5nm, t_{ox}=1nm, V_{ds}=0V, V_{gs}=0.5V, V_{bi}=0.6V $N_A = 10^{16}$ cm^{-3} for the proposed model compared with numerical simulations using COMSOL.

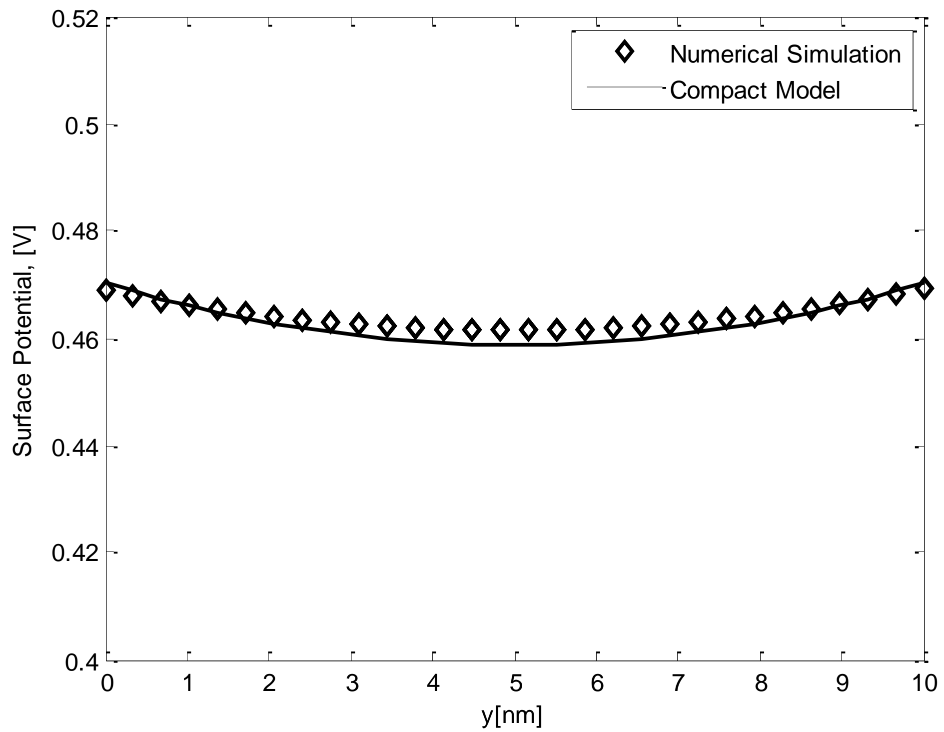

Figure 2.8 Surface Potential along the Silicon Thickness for t_{si}=10nm, N_A=10^{16}cm^{-3} for the proposed potential model compared with the BALMOS numerical simulations in [40]

2.6 THRESHOLD VOLTAGE MODEL AND INVERSION CHARGE

In order to obtain expressions for the inversion charge and subsequently the threshold voltage, the density and wave functions are deduced by simultaneously solving Poisson and Schrodinger's equations. Since the potential energy for the electron in the region between two gates is small compared to its total energy, for nanoscale devices, it can be regarded as a small perturbation. Thus, the quantum perturbation theory [58] holds the answer to electron energy correction. What is of interest here is the correction of the wave function with respect to the case when the potential is zero.

Since this is a nanoscale DG MOSFET, the electrons in the channel form a Two Dimensional Electron Gas (2DEG) as a result of their quantum confinement in one direction. In this model, the particle system considered is confined in two directions and one transport direction in order to further extend its application to GAA structures. This is based on modelling a 1D quantum wire formed between the gates in the same manner as a quantum wire transistor.[59] The system is first solved for one dimensional confinement, then solved for two dimensional confinement in order to be certain that it is valid for both cases. The first correction for the lowest confinement energy sub-band can be solved by:

$$\psi_1^{(1)} = \frac{1}{2L_y}\sum_{m\neq 1}\begin{bmatrix} \frac{\psi_m}{E_1-E_m}\int_{-L_y/2}^{L_y/2} dy \ \times \\ \left[\cos\frac{(2m+1)\pi y}{L_y}\right]\left[\cos\frac{\pi y}{L_y}\right] e^{ik_x x}\varphi \end{bmatrix} \tag{2.26}$$

This formula leads to extensive calculations since the expression for ϕ is large. It appears that not only are all the corrections for the wave function small, because eVg is much smaller than the zero point energy for nanoscale devices, but also that the sum over m is dominated by the first few terms. [29] Furthermore, the sum is alternating. As an example, one of the largest terms of the first correction for the wave function is:

$$\frac{e}{\pi^2 E_1}\frac{V_{ds}}{12\sinh\frac{\pi L_x}{2L_y}} \tag{2.27}$$

the wave function of the electron on the lowest confinement energy level is close to the same for zero potential:

$$\psi = \cos\frac{\pi y}{L_y} \quad (2.28)$$

$$n = \left[\cos\frac{\pi y}{L_y}\right]^2 \quad (2.29)$$

Thus, for nanoscale devices, the carrier density depends almost entirely on the thickness. It is zero near the gate and the boundary condition shown in (2.22) could be applied. Since the Fermi-Dirac distribution for the ideal electron gas is:

$$f = \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \quad (2.30)$$

the number of electrons is equal to:

$$N = 2\sum_n \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \quad (2.31)$$

The sum over n can be replaced by an integral in the phase space. When the domain of integration is much larger than the cell of the phase space, which is given by the uncertainty principle, the cell is taken to be Planck's constant. However, if the phase space domain is much larger than Planck's constant for all three dimensions, this reduces to the expression in (2.32)

$$N = \frac{2}{h^3}\int dx\, dy\, dz\, dp_x dp_y dp_z \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \quad (2.32)$$

the factor "2" represents the number of spin states. By integrating over the spatial coordinates, the volume in (2.33) results.

$$N = \frac{2V}{h^3}\int dp\, d\theta\, d\varphi\, p^2 \sin\theta \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \quad (2.33)$$

Subsequently, an integration over angles results in 4π, which allows for the deduction of (2.34).

$$N = \frac{8\pi V}{h^3} \int dp\, p^2 \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \tag{2.34}$$

Since $p^2 = 2mE,\ dp\, p^2 = m\sqrt{2mE}\, dE$

$$N = \frac{8\pi V}{h^3} \int m\sqrt{2mE}\, dE \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \tag{2.35}$$

by changing the variable from E to $\frac{E}{kT} = \varepsilon$ and for a constant $\frac{E_F}{kT} = \eta$, N will further evolve into the expression shown in (2.36)

$$N = \frac{8\pi V}{h^3} \sqrt{2} [mkT]^{\frac{3}{2}} \int d\varepsilon \sqrt{\varepsilon} \left[1 + e^{\frac{E_n - E_F}{kT}}\right]^{-1} \tag{2.36}$$

$$N = \frac{4V}{\sqrt{\pi}} \left(\frac{2\pi mkT}{h^2}\right)^{\frac{3}{2}} F_{1/2}(\eta) = \frac{4V}{\sqrt{\pi}\lambda_T^3} F_{1/2}(\eta) \tag{2.37}$$

where F is the Fermi-Dirac integral for parameter ½ and lambda is the De Broglie wave length (2.38).

$$\lambda_T^{-2} = \frac{2\pi mkT}{h^2} \tag{2.38}$$

So far, the confinement was only considered for the 2DEG DG MOSFET. As previously explained in the beginning of this section, quantum confinement will be considered in an additional direction in order to extend the application of the model to GAA structures. Thus, if quantum confinement takes place in two dimensions, the sum for that dimension cannot be replaced by an integral, resulting in (2.39).

$$N = \frac{2}{h} \sum_{n_y, n_z} \int dx\, dp_x \left[1 + e^{\frac{E_{(p_x)} + E_{n_y} + E_{n_z} - E_F}{kT}}\right]^{-1} \tag{2.39}$$

$$N = \frac{2L_x}{h} \sum_{n_y,n_z} \int dp_x \left[1 + e^{\frac{E(p_x) + E_{n_y} + E_{n_z} - E_F}{kT}}\right]^{-1} \quad (2.40)$$

Through changing the variable from p_x to $\varepsilon_x = \frac{p_x^2}{2mkT}$ and taking $\eta_{n_y,n_z} = \frac{E_F - E_{n_y} - E_{n_z}}{kT}$, the following expression results:

$$N = \frac{\sqrt{2}L_x}{\sqrt{\pi}\lambda_T} \sum_{n_y,n_z} F_{-1/2}\left(\eta_{n_y,n_z}\right) \quad (2.41)$$

where F is the FD integral for parameter -½ and λ_T is the DeBroglie wave length. For calculating carrier densities, the distributions change somewhat and can be expressed according to Fermi statistics as:

$$F_e = \left[1 + e^{\frac{(E_n - E_C) - (E_F - E_C + q\varphi)}{kT}}\right]^{-1} \quad (2.42)$$

$$F_h = \left[1 + e^{\frac{-(E_n - E_V) - (E_F - E_C - q\varphi)}{kT}}\right]^{-1} \quad (2.43)$$

where φ is the potential, q is the magnitude of the elementary charge, k is the Boltzmann constant, T is the absolute thermodynamic temperature, and E_c, E_v are the boundaries of the conduction and valence bands, respectively. This distribution describes the probability for the electron and hole to be in the conducting and valence bands respectively.

For conducting electrons, the calculations go as follows:

$$N = 2\sum_n \left[1 + e^{\frac{(E_n - E_C) - (E_F - E_C + q\phi)}{kT}}\right]^{-1} \quad (2.44)$$

$$N = \frac{2}{h} \sum_{n_y,n_z} \int dx\, dp_x \left[1 + e^{\frac{(E_x - E_C) - \left(E_F - E_C + q\phi - E_{n_y} - E_{n_z}\right)}{kT}}\right]^{-1} \quad (2.45)$$

$$N = \frac{2\,L_x}{h} \sum_{n_y,n_z} \int dp_x \left[1 + e^{\frac{(E_x - E_c) - \left(E_F - E_c + q\phi - E_{n_y} - E_{n_z}\right)}{kT}}\right]^{-1} \quad (2.46)$$

by applying the approximate parabolic dispersion relation $E_x - E_c = \frac{p_x^2}{2m}$

$$N = \frac{2L_x}{h} \sum_{n_y,n_z} \int \left[d\sqrt{2m(E_x - E_c)}\right] \left[1 + e^{\frac{(E_x - E_c) - \left(E_F - E_c + q\phi - E_{n_y} - E_{n_z}\right)}{kT}}\right]^{-1} \quad (2.47)$$

and the switching variable $\varepsilon = \frac{2m(E_x - E_c)}{kT}$ and $\eta_{n_y,n_z} = E_F - E_c + q\phi - E_{n_y} - E_{n_z}$

$$N = \frac{\sqrt{\frac{2}{\pi}}V}{\lambda_T L_y L_z} \sum_{n_y,n_z} F_{-1/2}\left(\eta_{n_y,n_z}\right) \quad (2.48)$$

thus, the density of conducting electrons is:

$$n = \frac{\sqrt{\frac{2}{\pi}}V}{\lambda_T L_y L_z} \sum_{n_y,n_z} F_{-1/2}\left(\frac{E_F - E_c + q\varphi - E_{n_y} - E_{n_z}}{kT}\right) \quad (2.49)$$

Similarly, for holes:

$$p = \frac{\sqrt{\frac{2}{\pi}}V}{\lambda_T L_y L_z} \sum_{n_y,n_z} F_{-1/2}\left(\frac{E_v - E_F - q\phi + E_{n_y} + E_{n_z}}{kT}\right) \quad (2.50)$$

where the confinement length L_Z and E_{n_z} account for the additional confinement in GAA structures. For silicon to be electro-neutral in the absence of potential it is required that p = n.

If there were no confinement energies, the expression would be reduced to the classical result; since the argument would solely be $\frac{-E_F}{kT}$, and that is much smaller than zero, so the Fermi-Dirac integral transforms into a Maxwellian expression.

The sum over n_y, n_z is problematic because exact E_{n_y}, E_{n_z} levels are unknown. In general, it is known that confinement energies rise as L_y, L_z shrink, so the arguments in the FD integrals for n and p should fall and rise respectively. Electro-neutrality then implies the rise of the band gap, rise of the conducting band, and fall of the valence band energies. Sums over FD integrals can be changed to effective FD integrals:

$$n = \frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y L_z} F_{-1/2}\left(\frac{E_F - E_c + q\phi - \frac{\Delta G}{2}}{kT}\right) = \frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y L_z} F_{-1/2}\left(\frac{-E_F + q\varphi - \frac{\Delta G}{2}}{kT}\right) \tag{2.51}$$

$$p = \frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y L_z} F_{-1/2}\left(\frac{E_v - E_F - q\phi - \frac{\Delta G}{2}}{kT}\right) = \frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y L_z} F_{-1/2}\left(\frac{-E_F - q\phi - \frac{\Delta G}{2}}{kT}\right) \tag{2.52}$$

where ΔG is the deviation of gap energy for quantum wire from the gap energy of bulk material.

The current is then carried by electrons that tunnel through the potential barrier from the source to the drain. The potential that describes the barrier can be found by solving Poisson and Laplace equations for all regions of operation. Since the electron density described by (2.50) falls exponentially for an argument much smaller than -1, the non-degenerate limit is taken as shown in (2.53). For arguments smaller than 3KT in (2.53), the non-degenerate density can be expressed as in (2.54).

$$E_F - E\varphi + \frac{\Delta G}{2} \geq 3kT \tag{2.53}$$

$$n = \frac{\sqrt{2/\pi}}{\lambda_T L_y L_z} e^{\left(\frac{-E_F + q\varphi - \frac{\Delta G}{2}}{kT}\right)} \tag{2.54}$$

Since the volume is small, the mean number of electrons is fewer than unity and is deduced as in (2.55).

$$N \leq \frac{\sqrt{2/\pi L_x}}{\lambda_T} e^{-3} \tag{2.55}$$

For arguments larger than 3kT, the FD integral has a different degenerate limit and the degenerate density is:

$$n = \frac{\sqrt{2/\pi}}{\lambda_T L_y L_z} \frac{2}{\sqrt{\pi}} \sqrt{\frac{-E_F + q\varphi - \frac{\Delta G}{2}}{kT}} \tag{2.56}$$

The barrier potential is then calculated for both degenerate and nondegenerate limits. If this degenerate limit is applied to the whole space, then a Poisson solution that rises very rapidly is implied. To verify this implication, Poisson's equation is then:

$$\varphi_o'' = \frac{2\sqrt{2}q}{\pi\varepsilon\lambda_T L_y L_z} \sqrt{\frac{-E_F + q\varphi - \frac{\Delta G}{2}}{kT}} \sim 250nm^{-2} \sqrt{\frac{-E_F + q\varphi - \frac{\Delta G}{2}}{kT}} \tag{2.57}$$

By changing the variable from φ to $\alpha = \frac{-\frac{E_F}{q} + \phi - \frac{\Delta G}{2q}}{V_T}$, a differential equation results

$$\alpha = 10^4 \frac{nm^{-2}}{V} \sqrt{\alpha} \tag{2.58}$$

The numerical solution for (2.58) is shown in Figure 2.9. From the solution, it is seen that for a small 0.08 nm change in the degenerate layer thickness, the potential rises about $200V_T = 5.2V$. This means that the degenerate layer is very thin even in the nanoscale regime.

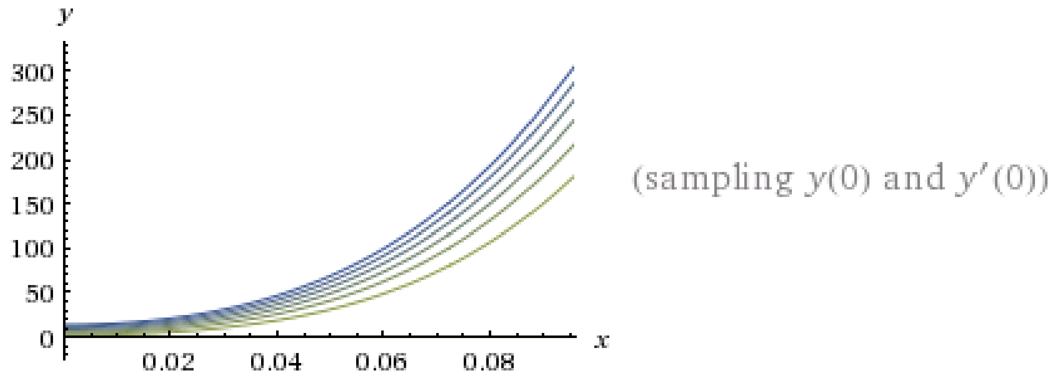

Figure 2.9 Numerical Solution for (2.58). The ordinate represents alpha, while the abscissa is the thickness of the degenerate layer

If the nondegenerate limit in (2.53) is taken between the gates, then a small number of electrons would be present since quantum tunneling is not considered in this model. Hence, the alternate possibility is that when the average density is small enough, Poisson's equation is reduced to Laplace's equation as a result of the reduction of the many electron problem to a one electron problem. Laplace's equation can be used to determine the potential which rises slowly with the thickness of the degenerate layer. If the number of electrons goes beyond unity, the area rapidly shrinks into a layer.

$$\varphi_o'' = 0 \tag{2.59}$$

$$\varphi_o = A\tilde{y} + B = \frac{V_g - \varphi_{ms} - \frac{\Delta G}{2} - E_F}{l_{(x)} + \frac{\varepsilon}{\varepsilon_{ox}} t_{ox}} \tilde{y} + \frac{\Delta G}{2q} + \frac{E_F}{q} \tag{2.60}$$

where $l_{(x)}$ is the thickness of the degenerate is layer dependent on position along the channel and $\tilde{y}$ measures the change in thickness inside the layer. Constants A, B are determined so that alpha is zero on the lower boundary of the layer and on the upper boundary, the condition is same as in [50].

In [60], Figures 2 and 9 show that below threshold voltage and at the subthreshold region, there is a significant difference between lightly doped and highly doped devices not only at the minimum potential values, but also in electron concentrations. This consequently has an effect on the threshold voltage; our model is introduced based on the inversion charge at the minimum potential value. The sheet density of the inversion charge can be expressed as:

$$Q_{inv} = 2 \frac{2\sqrt{2}}{\pi \lambda_T L_y L_z} \int_0^{l_{x_o}} \sqrt{\frac{\varphi_1^{min} + \frac{V_g - \varphi_{ms} - \frac{\Delta G}{2} - E_F}{l_{(x)} + \frac{\varepsilon}{\varepsilon_{ox}} t_{ox}} \tilde{y}}{V_T}} \, d\tilde{y} \tag{2.61}$$

where l_{x_o} is the thickness at the position at which the potential reaches its minimum value. This virtual cathode position can be calculated as in (2.62). φ_1^{min} (2.63) is the minimum potential at x_o.

$$x_o = \frac{L}{2} - \frac{t_o}{\lambda} \ln \sqrt{\frac{C_o}{C_1}} \tag{2.62}$$

$$\varphi_1^{min} = e^{-\frac{L\lambda}{2t_o}} 2\sqrt{C_0 C_1} \cos \lambda \frac{y}{t_o} \tag{2.63}$$

where C0, C1 are shown in Appendix A. The integral is then substituted with $l_{(xo)} \tilde{y}^{eff}$

$$Q_{inv} = 2 \frac{2\sqrt{2}l}{\pi \lambda_T L_y L_z} \sqrt{\frac{\varphi_1^{min} + \frac{V_g - V_{ms} - \frac{\Delta G}{2q} - \frac{E_F}{q}}{l + \frac{\varepsilon}{\varepsilon_{ox}} t_{ox}} \tilde{y}^{eff}}{V_T}} d\tilde{y} \tag{2.64}$$

For the classical and quantum approaches, there are different connections between the sheet inversion charge and potential. The expression in [50] is shown in (2.65) and (2.66) shows the proposed expression incorporating quantum effects.

$$V_T \ln \frac{Q_{inv}}{2 t_o n_i} = \varphi_{\left(x_o, \frac{t_o}{2}\right)} \tag{2.65}$$

$$V_T \left[\frac{Q_{inv} \pi \lambda_T L_y L_z}{4\sqrt{2}l}\right]^2 = \varphi_{\left(x_o, \frac{t_o}{2}\right)} \tag{2.66}$$

φ_1^{min} is taken at V_g=V_{TH} seeing as C_0, C_1 are parameters that depend on the gate voltage through the dependence of φ_1 on the gate voltage through the surface potential φ_{S0}. $\tilde{y}^{eff}$ is taken to be at l/2. φ_1^{min} is the same as in [50] except for a change in φ_{S0} as shown in (2.67). The inversion sheet charge at the threshold is taken to be 3×10^{10}cm^{-2}.

$$\varphi_{S0} = \frac{V_g - \varphi_{ms} - \frac{\Delta G}{2} - E_F}{1 + \frac{4 t_{ox} \varepsilon}{t_o \varepsilon_{ox}} t_{ox}} \tilde{y}^{eff} + \frac{\Delta G}{2q} + \frac{E_F}{q} \tag{2.67}$$

The FD integral has a very good approximation, with an error smaller than 0.5%.

$$F_{-1/2}(\eta) = \frac{e^{-\eta} - \xi'}{[e^{-\eta} - \xi]^2} \tag{2.68}$$

where:

$$\xi = 3\sqrt{\frac{\pi}{2}}\left[\eta + 2.13 + (|\eta - 2.13|^{2.4} + 9.6)^{5/12}\right]^{-3/2} \tag{2.69}$$

After some calculation, it can be deduced that:

$$F_{-1/2}(0) \approx 1 \tag{2.70}$$

So for $\eta = \varphi - \frac{E_F}{q} - \frac{\Delta G}{2q} \geq 0$ there would be more than unity electrons present, which is not in agreement with the threshold sheet charge taken. Hence, it can be taken that η is negative, and because the channel length is at least four times larger than the DeBroglie thermal length, we can go to the nondegenerate limit to calculate the threshold voltage. The threshold inversion charge can then be expressed as in (2.71).

$$Q_{inv} = 2\,\frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y L_z}\int dy\, e^{\left(\frac{\phi - \frac{\Delta G}{2} - E_F}{V_T}\right)} = \frac{\sqrt{\frac{2}{\pi}}}{\lambda_T L_y}\, e^{\left(\frac{V_{TH} - \phi_{ms} + \phi_1^{min}\big|_{y=\frac{t_O}{2}} - \frac{\Delta G}{2q} - E_F}{V_T}\right)} \tag{2.71}$$

By reusing φ_1^{min} in (2.63), the derived quantum corrected threshold voltage for [14] can be formulated as in (2.72) for the DG MOSFET with 2DEG confinement;

$$V_{TH} = V_T \ln\left(\frac{\mathrm{Q_{inv}}\lambda_T L_y}{2\sqrt{\frac{2}{\pi}}}\right) + \varphi_{ms} - \left(e^{-\frac{L\lambda}{2t_o}} 2\sqrt{C_0 C_1}\cos\lambda\frac{y}{t_o}\right) + \frac{\Delta G}{2q} + E_F \tag{2.72}$$

where

$$C_0C_1 = \begin{pmatrix} S_2^2[V_{TH} - \varphi_{ms}]^2 \\ -[V_{TH} - \varphi_{ms}][V_{bi} + V_{ds}]\left[1 - e^{-\frac{L\lambda}{t_o}}\right] \\ +S_1^2\left[(V_{bi} + V_{ds})\left(1 - e^{-\frac{L\lambda_Q}{t_o}}\right)^2 V_{bi} - V_{ds}^2 e^{-\frac{L\lambda}{t_o}}\right] \end{pmatrix} \tag{2.73}$$

where S_1 and S_2 depend on the device dimensions and are shown in Appendix A. The solution can be found by solving a quadratic equation in the threshold voltage. If L>>t in (2.72), the influence of the third term can be neglected, and the only significant correction is that resulting from the gap change. It is reasonable to conclude that the nondegenerate limit describes the subthreshold regime, while the saturation regime is the degenerate limit.

The numerical BALMOS simulations provided in [40], [61] were utilized for the validation of the threshold voltage results. Figure 2.10 shows the plot for proposed threshold voltage model for silicon thicknesses from 3 to 25 nm, with L = 20 nm, t_{ox}=1nm, and V_{DS}=0.15V. Good agreement within ±3% is observed with the numerical simulation.

Figure 2.11 shows the threshold voltage for V_{DS} values of 0.1, 0.5 and 1V to account for DIBL for channel lengths ranging from 10 to 50 nm. The model correctly shows a decrease in the threshold voltage not only as channel length decreases, but also as the drain source voltage increases. Figure 2.12 shows the threshold voltage roll off for channel lengths ranging from 7 – 100 nm for 5, 10, and 15 nm thicknesses and a 1nm oxide thickness. No fitting parameters have been used in any of the simulations.

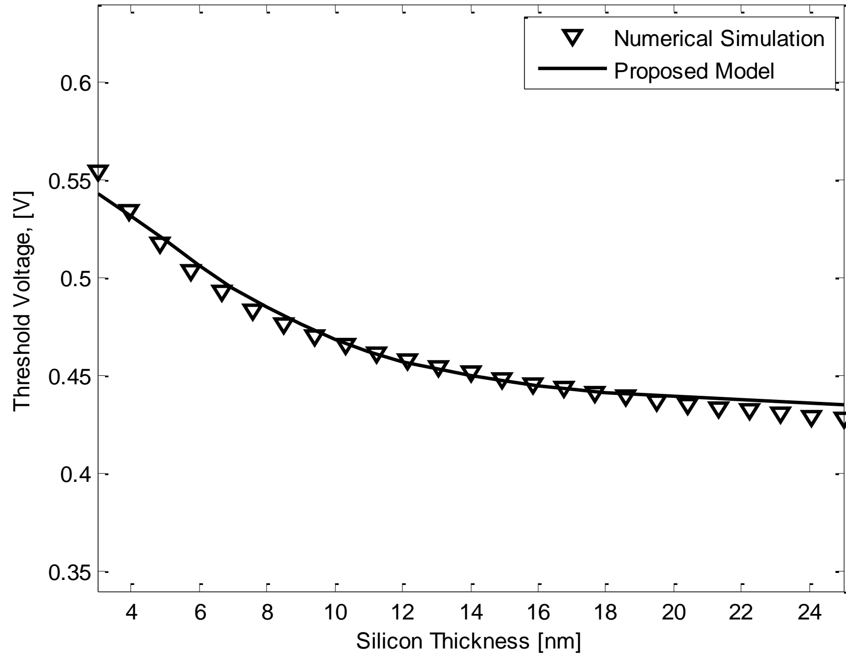

Figure 2.10 Threshold Voltage Vs tsi ranging from 3 to 25 nm for the proposed model in (35) in comparison with the BALMOS numerical simulation presented in [61]

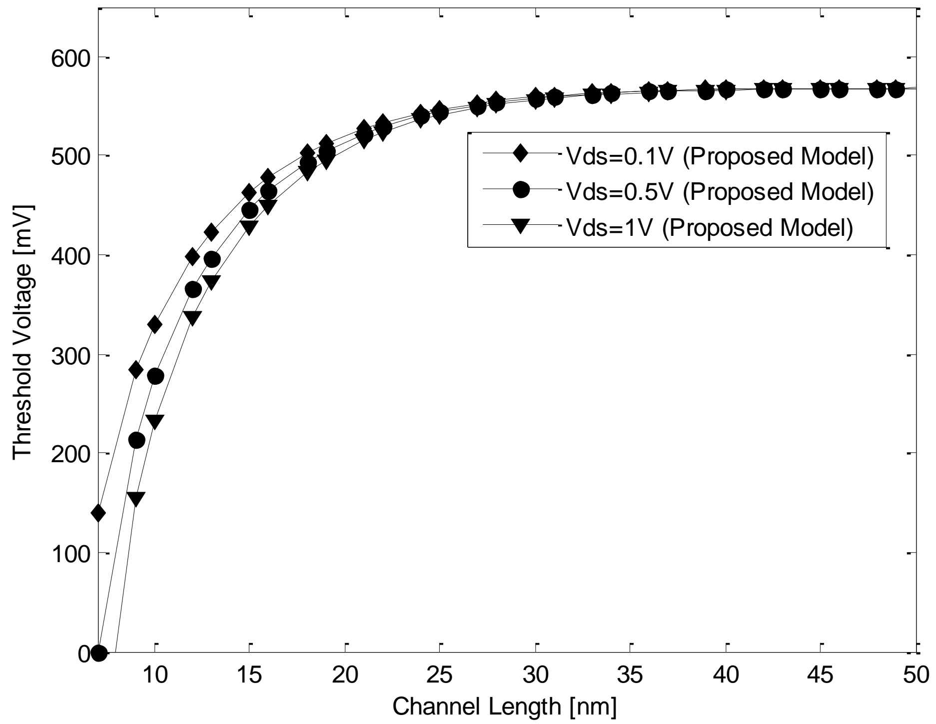

Figure 2.11 Threshold Voltage for L ranging from 10-50 nm for various Drain-Source voltages for the proposed model in (35) at tsi=5nm.

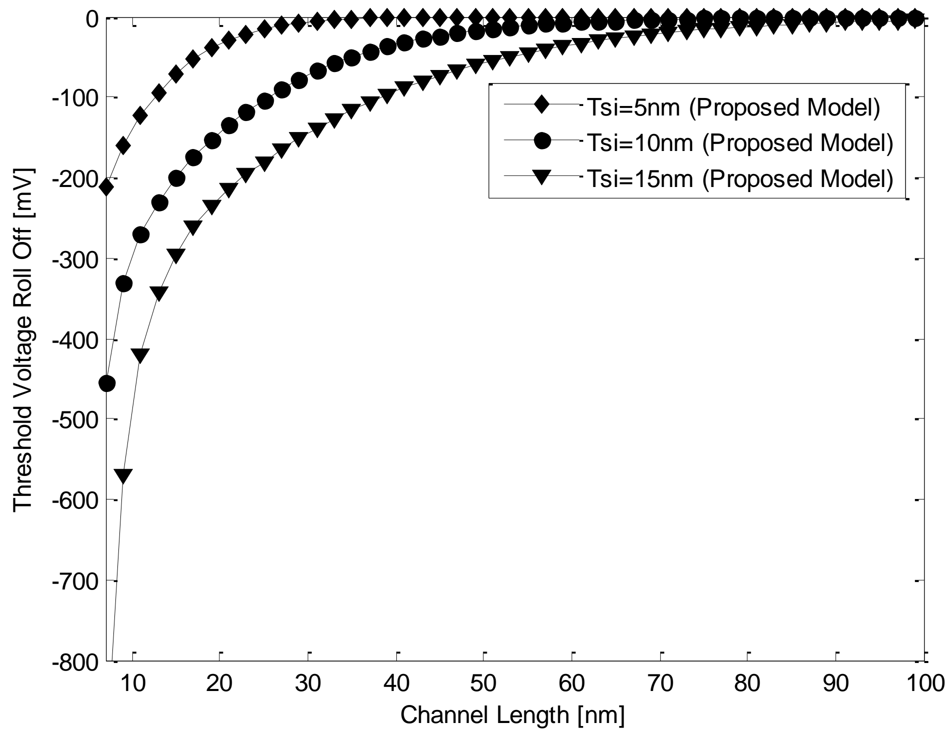

Figure 2.12 Threshold Voltage Roll-Off for L ranging from 7-100 nm at various t_{si} for the proposed model in (35).

CHAPTER 3

RELIABILITY MODELLING

3.1 INTRODUCTION

DG MOSFETS operating in the deca-nanometer regime face reliability apprehensions as a result of degradations; most notably Hot Carrier Injection (HCI), as well as negative bias temperature instability effects [45][46]. These two particular degradation mechanisms arise from the permanent interface traps which are irrecoverable after some time of operation. NBTI not only causes a decrease in transconductance and channel carrier mobility, but it also causes an increase in the off current and in the absolute threshold voltage value. [49]

Numerous varying work has been published in the area of device modelling including nanoscale scaling effects. The 2011 work in [62] modelled the quantum mechanical effects of NBTI degradation, however, quantum effects and quantum confinement were not studied. The two dimensional models provided in [26] did not incorporate the effects of DIBL nor degradation. The two-stage model in [46] remarkably captures all aspects of NBTI effects; nevertheless, quantum confinement was not discussed. The recently published quantum modelling work in [37][63] focuses on accurate physics-based modelling of ballistic devices without the inclusion of reliability.

In order to fully model the deca-nanometer performance of DG structures, it is crucial to model the effects of quantum confinement in addition to degradation effects on the electrostatics of the device. This work represents, for the first time, two dimensional simple compact models incorporating quantum confinement, NBTI, as well as, short channel effects (SCE).

3.2 POTENTIAL MODEL DERIVATION

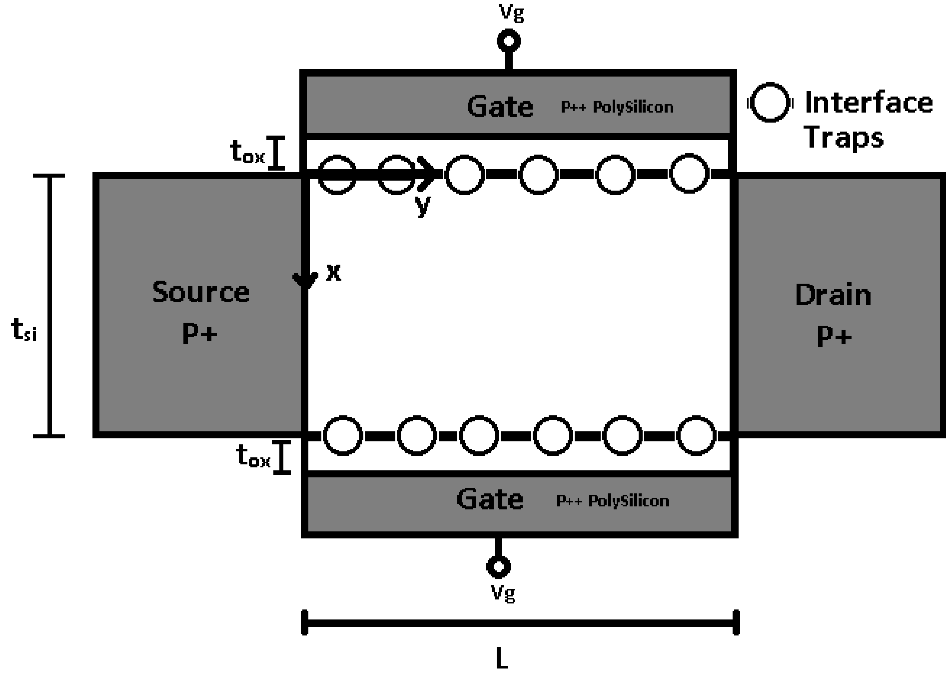

Figure 3.1 Cross section of the DG PMOSFET with the used coordinate system assuming a homogenous distribution of interface traps

A cross section of the DG MOSFET used is depicted in Figure 3.1. The potential model in [51] was derived based on the solution of a 2D Poisson equation. Utilizing the potential model previously derived in [51], the expression can be rewritten in a compact form as shown in (3.1)

$$\boldsymbol{\varphi_{NBTI,SC}} = \boldsymbol{F} \times \boldsymbol{\varphi_{sc}} + \boldsymbol{E} \tag{3.1}$$

where $\varphi_{NBTI,SC}$ is the potential when the SCEs and NBTI effect are considered and φ_{sc} is the potential when SCEs are only considered, and

$$F = \frac{5040L\lambda_1^6+840L^3\lambda_1^4+42L^5\lambda_1^2+L^7}{5040L\lambda_1^6+840L^3\lambda_1^4+42L^5\lambda_1^2+L^7+5040LS+840L^3g+42L^5\lambda\prime} \tag{3.2}$$

$$\lambda_1 = \sqrt{\frac{\epsilon_{si}t_{si}t_{ox}+\epsilon_{ox}(t_{si}x-x^2)}{2\epsilon_{ox}}} \tag{3.3}$$

$$\lambda' = \frac{-\alpha\epsilon_{si}t_{ox}}{\epsilon_{ox}+\alpha\epsilon_{si}t_{ox}}\lambda_1^2 + \frac{\alpha\epsilon_{si}t_{ox}(t_{si}x-x^2)}{2\epsilon_{ox}+2\alpha\epsilon_{si}t_{ox}} \tag{3.4}$$

$$\boldsymbol{S = 3\,\lambda_1^4\lambda' + 3\,\lambda_1^2\lambda'^2 + \lambda'^3} \tag{3.5}$$

$$\boldsymbol{g = 2\lambda_1^2\lambda' + \lambda'^2} \tag{3.6}$$

where L is the channel length, $\in_{si}$ is the silicon permittivity, t_{si} is the channel thickness, t_{ox} is the gate oxide thickness, $V_g' = V_g - V_{fb}$, V_{fb} is the flat band voltage, A,B,C are constants, and α and β are NBTI parameters discussed in [51]

$$E = \frac{1}{5040L\lambda_1^6 + 840L^3\lambda_1^4 + 42L^5\lambda_1^2 + L^7 + 5040LS + 840L^3g + 42L^5\lambda'} \times \begin{bmatrix} \boldsymbol{V_d\left(5040yS + 840y^3g + 42y^5\lambda'\right) +} \\ \boldsymbol{V_{bi}\left(5040LS + 840((L-y)^3 + y^3)g + 42y^5\lambda'\right)} \\ \boldsymbol{-Vg'g(840(L-y)^3 - L^3 + y^3) +} \\ \boldsymbol{42\left((L-y)^5 - L^5 + y^5\right)\left(\lambda' + \lambda_1^2\right)} \\ \boldsymbol{-A'(840(L-y)^3 - L^3 + y^3)\left(g + \lambda_1^4\right)} \end{bmatrix} \tag{3.7}$$

and

$$\mathbf{A'} = \frac{\boldsymbol{-\alpha\in_{si}t_{ox}Vg' - \beta\in_{si}t_{ox}}}{\boldsymbol{(\in_{ox} + \alpha\in_{si}t_{ox})}} \tag{3.8}$$

Given that the model derived in Chapter 2 incorporates SCEs, φ_{sc} can be replaced with the potential model including both quantum effects and SCEs. Thus, the potential for quantum confinement effects and NBTI together can be expressed as in (3.9).

$$\boldsymbol{\varphi_{NBTI,QE} = F \times \varphi_{QE} + E} \tag{3.9}$$

where $\varphi_{NBTI,QE}$ is the potential of the combined effect of NBTI and quantum confinement effects and φ_{QE} is the compact quantum confinement potential model derived in the previous chapter.

The combined expression in (3.9) is used in plotting the surface potential along the channel as shown in Figure 3.2 and Figure 3.3 at a channel length of 10 nm, a built-in voltage, V_{bi} of -0.6V and a drain voltage, V_d, of 0V and -0.5V respectively. The figure also shows the potential distribution for each effect separately. At an oxide thickness of 1nm and L=10nm, the NBTI effect is significant, furthermore, a silicon thickness of 5nm allows quantum confinement to be prominent as well. Therefore, the results represented for the combined model show the effect of both quantum confinement and NBTI on the distribution of the surface potential.

In order to validate these results, numerical simulations were carried out using COMSOL to predict the surface potential under both effects at a channel length of 20 nm and a 5 nm silicon thickness. The COMSOL simulation was performed by solving two Partial Differential Equations (PDEs). The 2D Poisson and 1D Schrodinger equations were solved self consistently in multi-physics mode.

Figure 3.4 shows the proposed model compared with the numerical results. Very good agreement within ±3% is observed, thereby verifying the model for channel lengths down to 20 nm. Furthermore, not only is it matching within ±3% achieved at a zero volt drain voltage, but it is also within ±6% at a drain voltage of -0.5V.

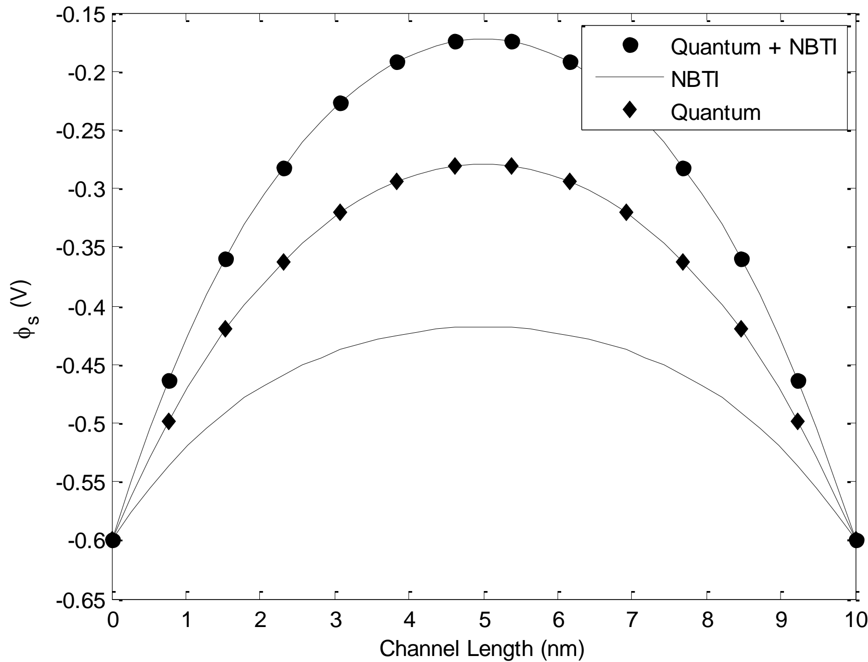

Figure 3.2 Potential Distribution along the channel for the combined effect of Quantum and NBTI effects and for Quantum and NBTI separately for L=10nm, Tsi=5nm, Tox=1nm, Vds=0V, Vbi=-0.6V, after 10 years of operation

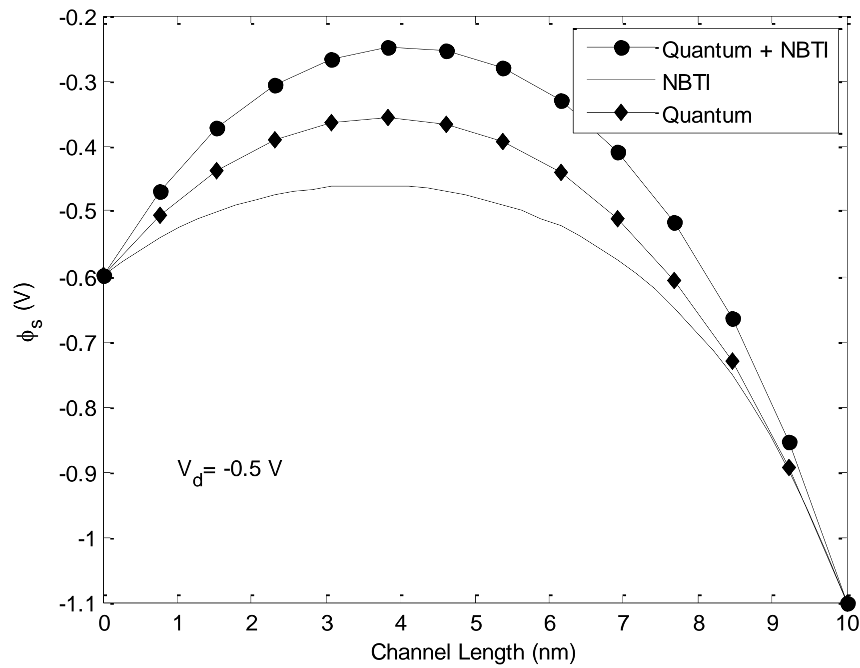

Figure 3.3 Potential Distribution along the channel for the combined effect of Quantum and NBTI effects and for Quantum and NBTI separately for L=10nm, Tsi=5nm, Tox=1nm, Vds=-0.5V, Vbi=-0.6V, after 10 years of operation

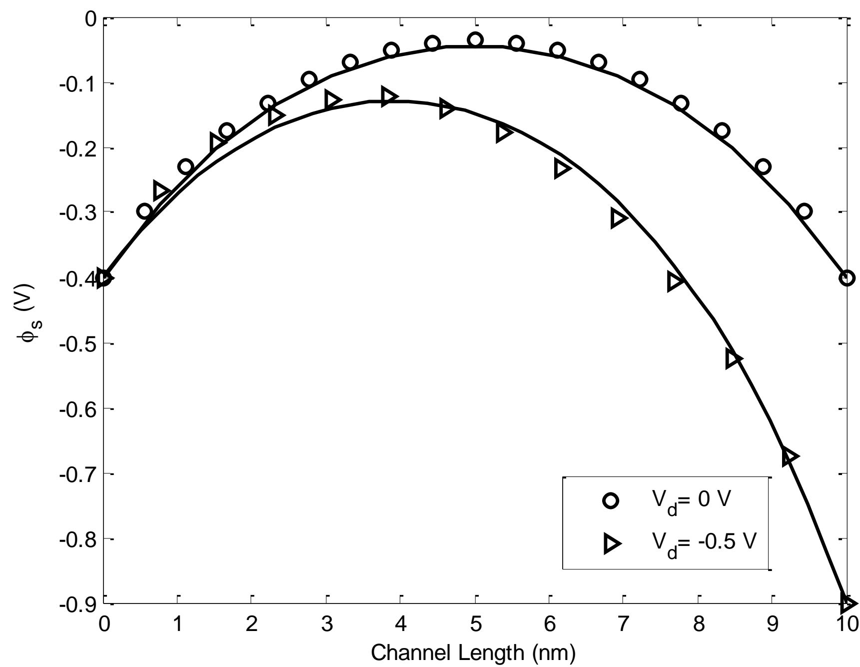

Figure 3.4 Potential Distribution along the channel for the model compared with the numerical COMSOL simulation for L=10nm, Tsi=5nm, Tox=1nm, Vbi=-0.4V, after 10 years of operation

3.3 THRESHOLD VOLTAGE DERIVATION

The threshold voltage expression in [51] can be separated in a compact form as shown in (3.10)

$$V_{th_{NBTI,SC}} = (1-\xi)(\mathrm{V_{fb}}+\mathrm{m}) + \xi . V_{th_SC} + d \tag{3.10}$$

where V_{th_NBTI} is the threshold voltage including NBTI and SCEs effects, V_{th_SC} is the threshold voltage including SCEs only, and also ξ, m, d are NBTI factors.

$$m = \frac{1}{\mathrm{c}}\left(a'(V_{bi}+V_d) + b'V_{bi}\right) \tag{3.11}$$

$$\mathrm{c} = 1-\mathrm{a}-\mathrm{b},\ a = \frac{\sinh\left(\frac{y_{min}}{\lambda_1}\right)}{\sinh\left(\frac{L}{\lambda_1}\right)}, b = \frac{\sinh\left(\frac{L-y_{min}}{\lambda_1}\right)}{\sinh\left(\frac{L}{\lambda_1}\right)} \tag{3.12}$$

$$d = -\frac{\beta' \epsilon_{si} tox}{(\epsilon_{ox}-\beta'' \epsilon_{si} tox)} - \frac{a'(V_{bi}+V_d)+b'V_{bi}}{\mathrm{c}} \tag{3.13}$$

$$\mathrm{a}' = \frac{\sinh\left(\frac{\mathrm{y_{min}}}{\lambda_{\mathrm{NBTI}}}\right)}{\sinh\left(\frac{\mathrm{L}}{\lambda_{\mathrm{NBTI}}}\right)} - \frac{\sinh\left(\frac{\mathrm{y_{min}}}{\lambda_1}\right)}{\sinh\left(\frac{\mathrm{L}}{\lambda_1}\right)}, \mathrm{b}' = \frac{\sinh\left(\frac{\mathrm{L-y_{min}}}{\lambda_{\mathrm{NBTI}}}\right)}{\sinh\left(\frac{\mathrm{L}}{\lambda_{\mathrm{NBTI}}}\right)} - \frac{\sinh\left(\frac{\mathrm{L-y_{min}}}{\lambda_1}\right)}{\sinh\left(\frac{\mathrm{L}}{\lambda_1}\right)} \tag{3.14}$$

$$\mathrm{r} = \frac{\epsilon_{\mathrm{ox}} - \beta'' \epsilon \mathrm{si\ tox}}{(\epsilon_{\mathrm{ox}} + \alpha \epsilon_{\mathrm{si}} \mathrm{tox})} \tag{3.15}$$

$$\xi = \frac{1}{\mathrm{r}}\left(1 + \frac{\mathrm{a}'+\mathrm{b}'}{\mathrm{c}}\right) \tag{3.16}$$

$$\lambda_{\mathrm{NBTI}} = \sqrt{\frac{\epsilon_{\mathrm{si}} t_{\mathrm{si}} t_{\mathrm{ox}} + (\epsilon_{\mathrm{ox}} + \alpha \epsilon_{\mathrm{si}} t_{\mathrm{ox}})(t_{\mathrm{si}} x - x^2)}{2\epsilon_{\mathrm{ox}} + 2\alpha \epsilon_{\mathrm{si}} t_{\mathrm{ox}}}} \tag{3.17}$$

$$\lambda_1 = \sqrt{\frac{\epsilon_{\mathrm{si}} t_{\mathrm{si}} t_{\mathrm{ox}} + \epsilon_{\mathrm{ox}}(t_{\mathrm{si}} x - x^2)}{2\epsilon_{\mathrm{ox}}}} \tag{3.18}$$

Where α and β'' is parameter for NBTI defined in [51] and y_{min} is defined as shown in (3.19)

$$y_{\min} = \lambda_1 \tanh^{-1}\left(\frac{\sinh\left(\frac{L}{\lambda_1}\right) - f(V_d)}{\cosh\left(\frac{L}{\lambda_1}\right)}\right) \tag{3.19}$$

$$\text{And } f(V_D) = \frac{V_{bi} + V_d - V_{g'}}{V_{bi} - V_{g'}} \tag{3.20}$$

A compact threshold voltage model for the combined effect of both NBTI and quantum effects can be estimated based on (3.10)

$$V_{th_{NBTI,QC}} = (1 - \xi)(\mathrm{V_{fb}} + \mathrm{m}) + \xi . V_{th_QC} + d \tag{3.21}$$

where $V_{th_{NBTI,QC}}$ is the threshold voltage for the combined effect of NBTI and quantum confinement effects and V_{th_QC} is the threshold voltage including quantum confinement effects as derived in Chapter 2 and is rewritten as in (3.22) to account for the co-ordinate system difference. Q_{inv} is taken to be $3\times10^{10}\mathrm{cm}^{-2}$.

$$\mathrm{V_{TH_QC}} = \left(\begin{array}{c} \mathrm{V_T} \ln\left(\dfrac{\mathrm{Q_{inv}}\lambda_\mathrm{T} \mathrm{t_{si}}}{2\sqrt{\frac{2}{\pi}}}\right) + \mathrm{V_{fb}} \\ -\left(\mathrm{e}^{-\frac{\mathrm{L}\lambda_\mathrm{Q}}{2\mathrm{t_o}}} 2\sqrt{\mathrm{C_0 C_1}} \cos\lambda_\mathrm{Q}\dfrac{\mathrm{x}}{\mathrm{t_o}} + \dfrac{\Delta\mathrm{G}}{2\mathrm{q}} + \mathrm{E_F}\right) \end{array}\right) \tag{3.22}$$

where

$$\mathrm{C_0 C_1} = \left(\begin{array}{c} \mathrm{S_2^2}\left[\mathrm{V_{TH_{QC}}} - \mathrm{V_{fb}}\right]^2 - \left[\mathrm{V_{TH_{QC}}} - \mathrm{V_{fb}}\right][\mathrm{V_{bi}} + \mathrm{V_{ds}}] \\ +\mathrm{S_1^2}\left[(\mathrm{V_{bi}} + \mathrm{V_{ds}})\left(1 - \mathrm{e}^{-\frac{\mathrm{L}\lambda_\mathrm{Q}}{\mathrm{t_o}}}\right)^2 \mathrm{V_{bi}} - \mathrm{V_{ds}^2}\mathrm{e}^{-\frac{\mathrm{L}\lambda_\mathrm{Q}}{\mathrm{t_o}}}\right] \end{array}\right) \tag{3.23}$$

$$2\lambda_\mathrm{Q} \tan(\lambda_\mathrm{Q}) = \mathrm{C_r} \tag{3.24}$$

$$\mathrm{C_r} = \frac{\varepsilon_\mathrm{ox} \mathrm{t_o}}{\varepsilon_\mathrm{si} \mathrm{t_{si}}} \tag{3.25}$$

where S_1 and S_2 are as defined in Appendix A. V_T is the thermal voltage, V_{ds} is the drain source voltage, E_F is the energy of Fermi level, $t_o = \frac{t_{si}}{2}$, ΔG is the deviation of gap energy for quantum wire from the gap energy of bulk material, q is the magnitude of the elementary charge, and λ_T is the De Broglie wavelength.

Variations in the channel length affect current transport models (I_{ON} and I_{OFF}), while changes in the silicon thickness define the quantum confinement. Hence, even in very long channel devices, if the silicon thickness is below 10nm quantum confinement will be significant. [64] This is evident in the threshold voltage plot at t_{si}=5nm and t_{ox}= 1nm in Figure 3.5, as the V_{TH} value in the long channel range ($V_{th_{long}}$) varies significantly between the quantum free NBTI model, and the proposed model. Figure 3.6 corroborates this as t_{si} is taken at 18nm, thereby eliminating the effect of quantum confinement. As shown, the long channel V_{TH} value converges towards the same value for all three models. The proposed model correctly models the behavior of the device as it exhibits both phenomena.

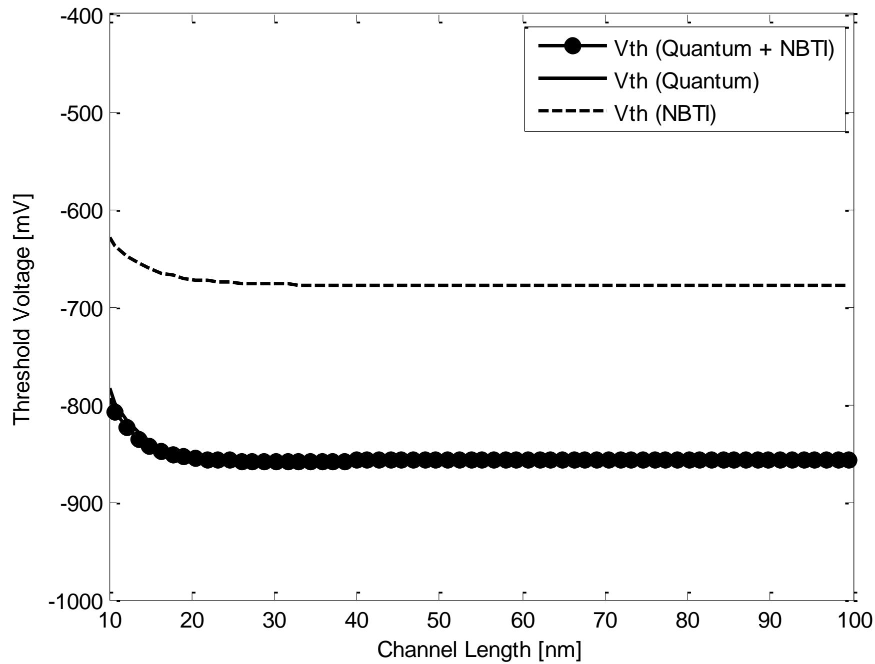

Figure 3.5 Threshold Voltage for NBTI, Quantum and the proposed model effect at Tsi = 5nm, Vds=0V, Tox=1nm after 10 years of operation

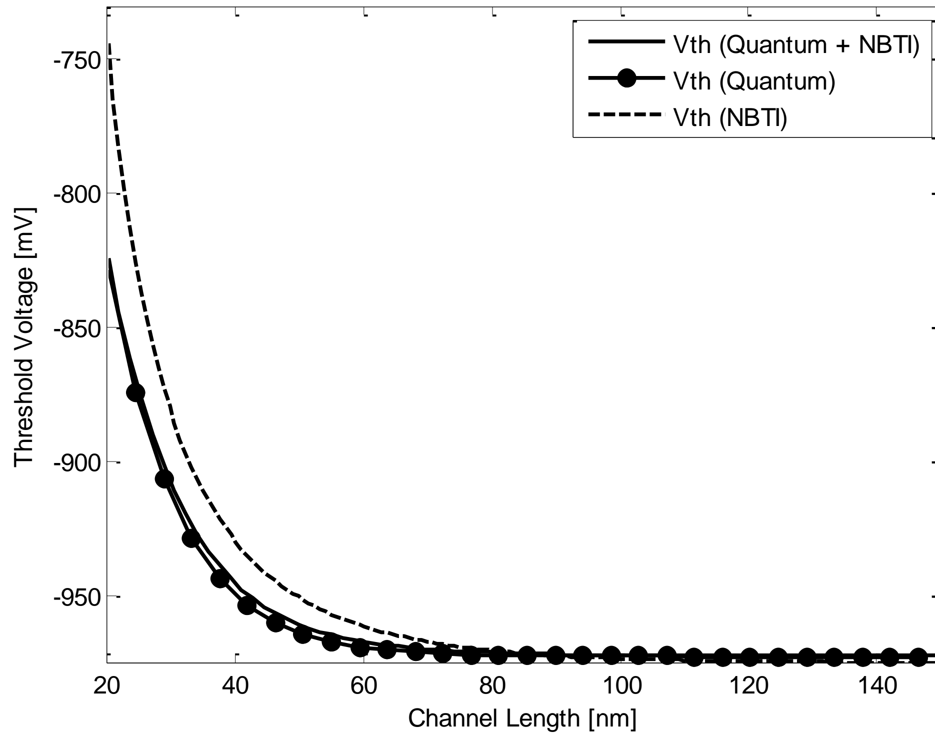

Figure 3.6 Threshold Voltage for NBTI, Quantum and the proposed model at Tsi = 18nm, Vds=0V, Tox=1.5nm after 10 years of operation

Since it is evident that quantum confinement has a higher effect on the threshold voltage, the plot in Figure 3.7 shows the combined threshold voltage model compared with the quantum model for a channel length range of 8 to 25nm. The graph is plotted at different V_d values to represent the influence of DIBL. The NBTI effect in the combined model is significant at a channel length below 16nm, and is more substantial at higher drain voltages which agrees with the findings in [65]. Figure 3.8 depicts the comparison between the proposed threshold voltage model in (3.22) and the COMSOL simulation which shows that any approximations in the model do not affect its accuracy.

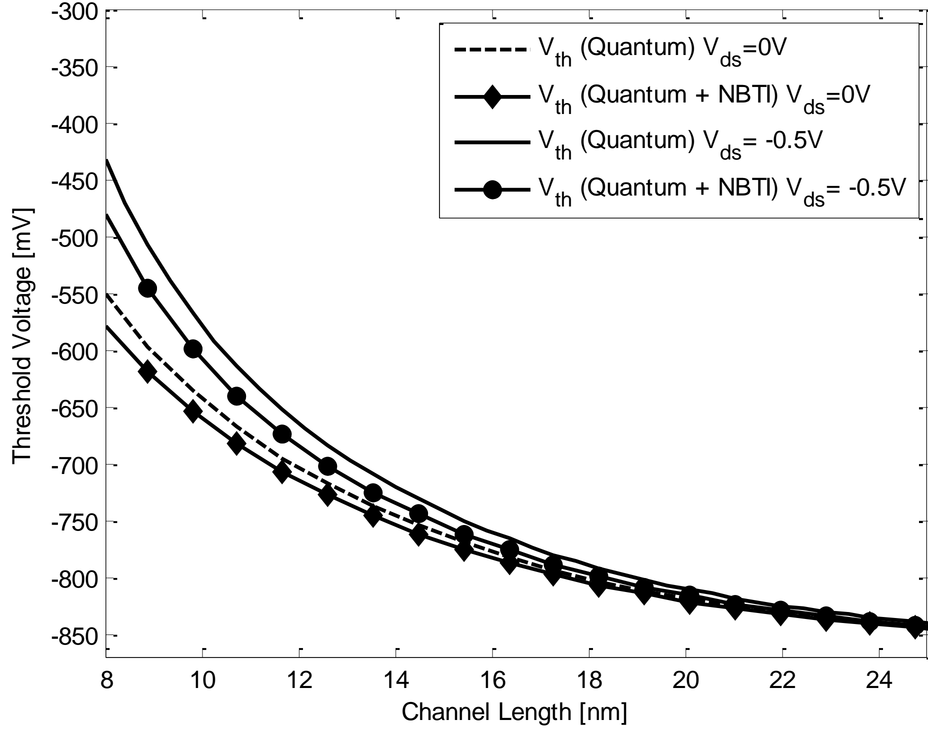

Figure 3.7 Threshold Voltage for combined model compared with Quantum Threshold Voltage at Vds=0V and -0.5V, Tsi = 5nm, Tox=1nm, for L ranging from 8 – 25nm after 10 years of operation

The threshold roll-off voltage and drain-induced barrier lowering (DIBL) are respectively shown in Figures 3.9 and 3.10, where the threshold voltage roll off is calculated according to:

$$V_{th-roll-off} = V_{th_{long}} - V_{th} \tag{3.26}$$

And the DIBL is calculated as shown in (3.27)

$$DIBL = \frac{V_{th}(V_{d(low)}) - V_{th}(V_{d(high)})}{V_{d(high)} - V_{d(low)}} \tag{3.27}$$

where $V_{d(high)}$=-0.5V and $V_{d(low)}$=0V.

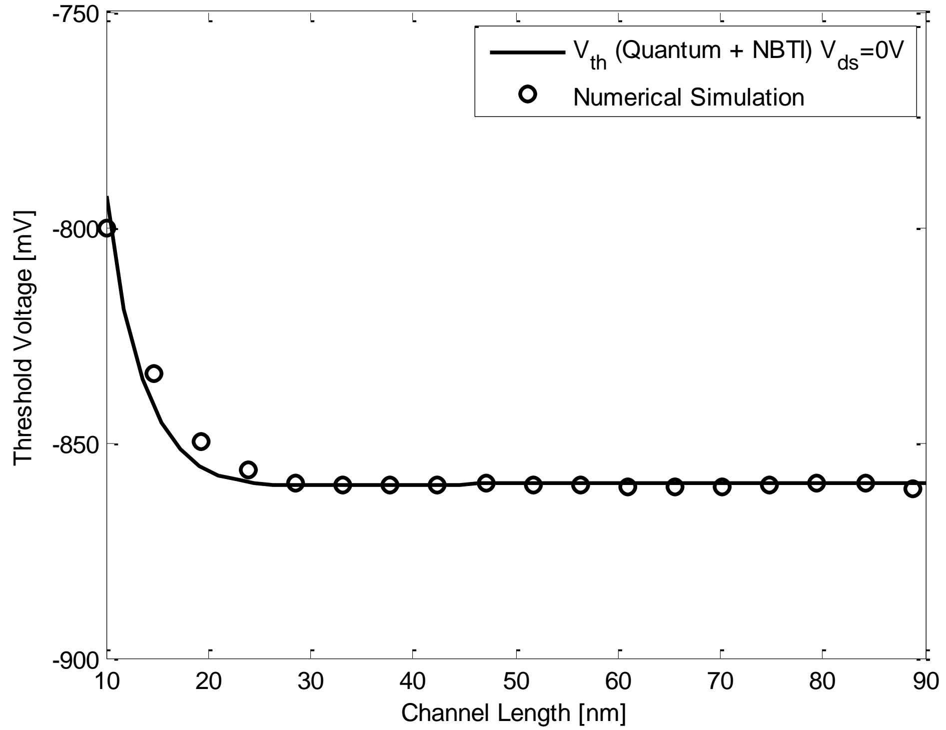

Figure 3.8 Threshold Voltage for the proposed model verified against the numerical simulation at Tsi = 5nm, Vds=0V, Tox=1nm after 10 years of operation

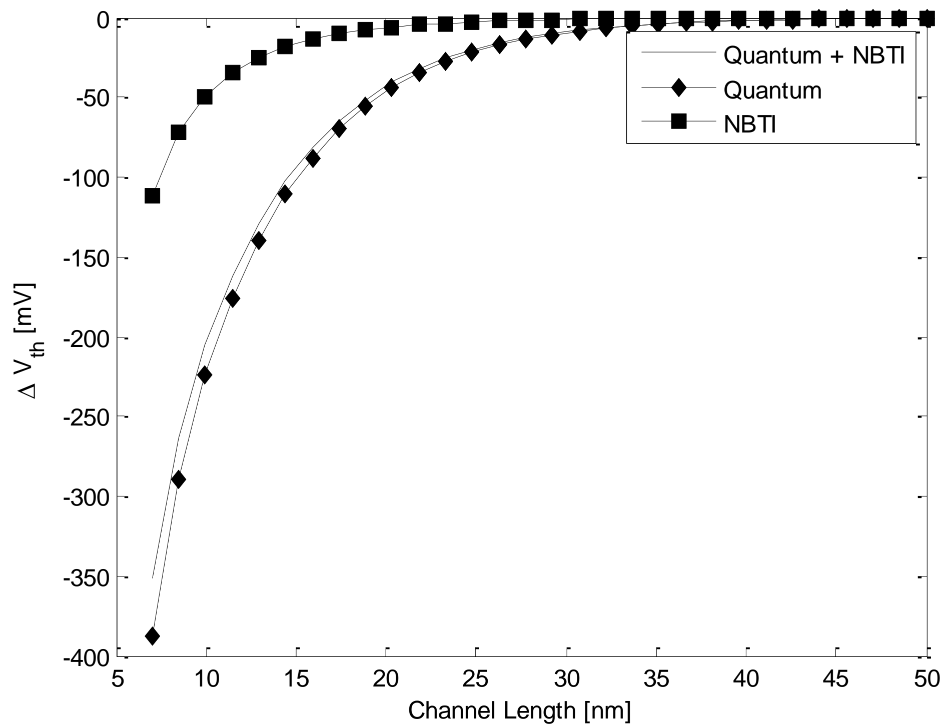

Figure 3.9 Threshold voltage roll-off for combined effect of Quantum and NBTI effects and for Quantum and NBTI separately at Tsi = 5nm, Tox=1nm, for L ranging from 7 – 50nm.

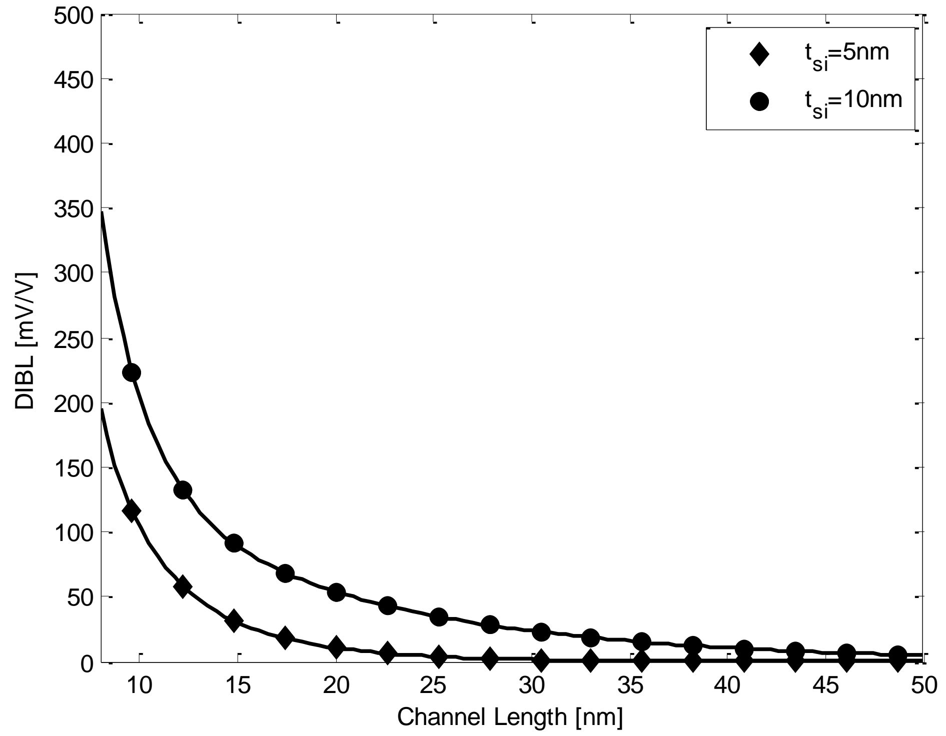

Figure 3.10 DIBL for the combined effect of Quantum and NBTI effects at t_{si}=5 nm and t_{si}=10 nm, for L ranging from 8 – 50nm.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

4.1 CONCLUSION

This thesis has presented simple 2D compact analytical quantum correction continuous models for potential, threshold voltage, and inversion charge in a symmetrical lightly doped DG MOSFET including quantum confinement for the potential, threshold voltage, and the carrier charge sheet density by solving 2D Poisson and Schrödinger’s equation along the silicon film thickness. The electron and hole quasi-Fermi potentials were taken into account.

The models were also extended to include the combined effects of quantum confinement and NBTI on the 2D electrostatics of an undoped symmetrical DG MOSFET. The model results have shown that the effects of quantum confinement are more significant when compared to the effects of NBTI studied after 10 years of operation at a 1GHz frequency. Nonetheless, NBTI has a noteworthy impact on the threshold voltage, which is more extensive at higher drain voltages, at channel lengths below 16nm. All proposed models are Verilog-A compatible and have been verified against numerical simulations.

The quantum corrected potential and threshold voltage models were verified versus BALMOS and COMSOL numerical simulation. Agreement has been observed within ±5% with numerical simulations for silicon thicknesses ranging from 3 to 20 nm. The compact combined models provided for the potential distribution and the threshold voltage have been verified against COMSOL numerical simulations with very good matching within ±3-6% for channel lengths down to 7nm as well.

4.2 FUTURE WORK

Future extensions intended for this work include:

- Modelling carrier transport through an analytical current model to compute the gain and transconductance. This would allow the model to be suitable for SPICE Simulators.

- Validation for GAA structures and narrow channel ballistic devices
- Reliability modelling for other nanoscale devices; such as FinFET and SPIN devices.
- Reliability modelling for new materials, such as III-V materials.

There are certain factors and phenomena that can be added to the models to increase their accuracy. The proposed models avoided these effects in order to maintain the simplicity of the model. Effects avoided include:

- Inter sub-band scattering modelling
- Solving a 3D Poisson equation instead of solving a 2D Poisson equation to model the surface potential. This would validate the overall potential profile with a higher precision.
- Solving a 2D Schrodinger equation instead of a 1D Schrodinger equation would offer a more accurate representation of the charge profile.

LIST OF PUBLICATIONS

Journal:

1. R. Y. Elkashlan, H. Abd, E. Hamid, and Y. I. Ismail, “Two-Dimensional models for quantum effects on short channel electrostatics of lightly doped symmetric double-gate MOSFETs,” *IET Circuits, Devices Syst.*, Accepted, 2017.

2. R. ElKashlan, O. Samy, H. ElHamid, and Y. Ismail, “Unified quantum and reliability analytical threshold voltage model for nanoscale double gate MOSFETs,” *Electron. Lett.*, Submitted, 2017

APPENDIX A

PARAMETER EQUATIONS FROM [50]

PARAMETER	EQUATION
λ	$2\lambda \tan(\lambda) = C_r \quad (A.1)$
C_r	$\dfrac{\varepsilon_{ox} t_o}{\varepsilon_{si} t_{si}} \quad (A.2)$
S_1	$\dfrac{4\sin(\lambda)}{[2\lambda + \sin(\lambda)].\left[1 - e^{-2\frac{L\lambda}{t_o}}\right]} \quad (A.3)$
S_2	$\dfrac{4\lambda\cos\left(\frac{\lambda}{2}\right)\left(1 - e^{-\frac{L\lambda}{t_o}}\right)}{[2\lambda + \sin(\lambda)].\left[1 - e^{-2\frac{L\lambda}{t_o}}\right]} \quad (A.4)$
C_0	$S_1 * \left[V_{DS} + V_{bi}\left(1 - e^{-\frac{L\lambda}{t_o}}\right)\right] - S_2 * \varphi_{so} \quad (A.5)$
C_1	$S_1 * \left[V_{bi}\left(1 - e^{-\frac{L\lambda}{t_o}}\right) - V_{DS}\left(e^{-\frac{L\lambda}{t_o}}\right)\right] - S_2 * \varphi_{so} \quad (A.6)$

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