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# A novel control mechanism for hybrid 5-level DC-DC converter for higher switching frequency and lower voltage ripple

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# A NOVEL CONTROL MECHANISM FOR HYBRID 5-LEVEL DC-DC CONVERTER FOR HIGHER SWITCHING FREQUENCY AND LOWER VOLTAGE RIPPLE

by

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## ABSTRACT

The introduction and development of hybrid DC-DC converters present a valuable opportunity in on-chip power management, as they combine the advantages of buck and switched-capacitor converters while alleviating shortcomings such as conversion efficiency and sizing requirements. In this paper, a new control methodology is presented for the recently developed 5-level hybrid DC-DC converter, which utilizes the Virtex 5 LX50T FPGA to drive the converter. This control method allows for a higher switching frequency of 1MHz and an improved conversion efficiency while also allowing for dynamic voltage control based on the desired output voltage. Simulations as well as a test circuit are used to illustrate the proper control functionality, with tabulated results that showcase the efficiency advantage over prior control methods as well as the buck and 3-level hybrid converters.

## ACKNOWLEDGEMENTS

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# Chapter 1

# INTRODUCTION

## 1.1 Motivation

The topic of DC-DC converters has garnered a lot of attention and demand during recent years, as the need for them has become ever so pronounced, with developments and advancements growing to be a highlight in literature. This need has largely been caused by the current tendency in consumer electronics, which happen to require increasingly lower voltage supplies [1]. The decrease can be attributed to trending miniaturization, or what is otherwise known as Moore's Law, happening alongside an increase in performance and functionality, as seen in portable electronics and high-end computers.

The law, essentially an observation made and published by Gordon Moore in 1965, stated that the number of components in an integrated circuit was to increase at a rate of twice per year [2]. This figure was then revised to be a doubling every two years/18 months, and was proven to be accurate enough to become a guideline for designers and manufacturers, allowing them to set future targets for research and development. However, as smaller components found their way onto chips, and with the power draw for such transistors remaining largely the same, the chip power density was observed to be gradually rising at an alarming rate [3]. Such rise in power density leads to an inevitable increase in operating temperatures, which would have a catastrophic effect on chip integrity. Thus, a need arose for ways to reduce power consumption while maintaining the current trends in sizing and efficiency, driving efforts in research and design.

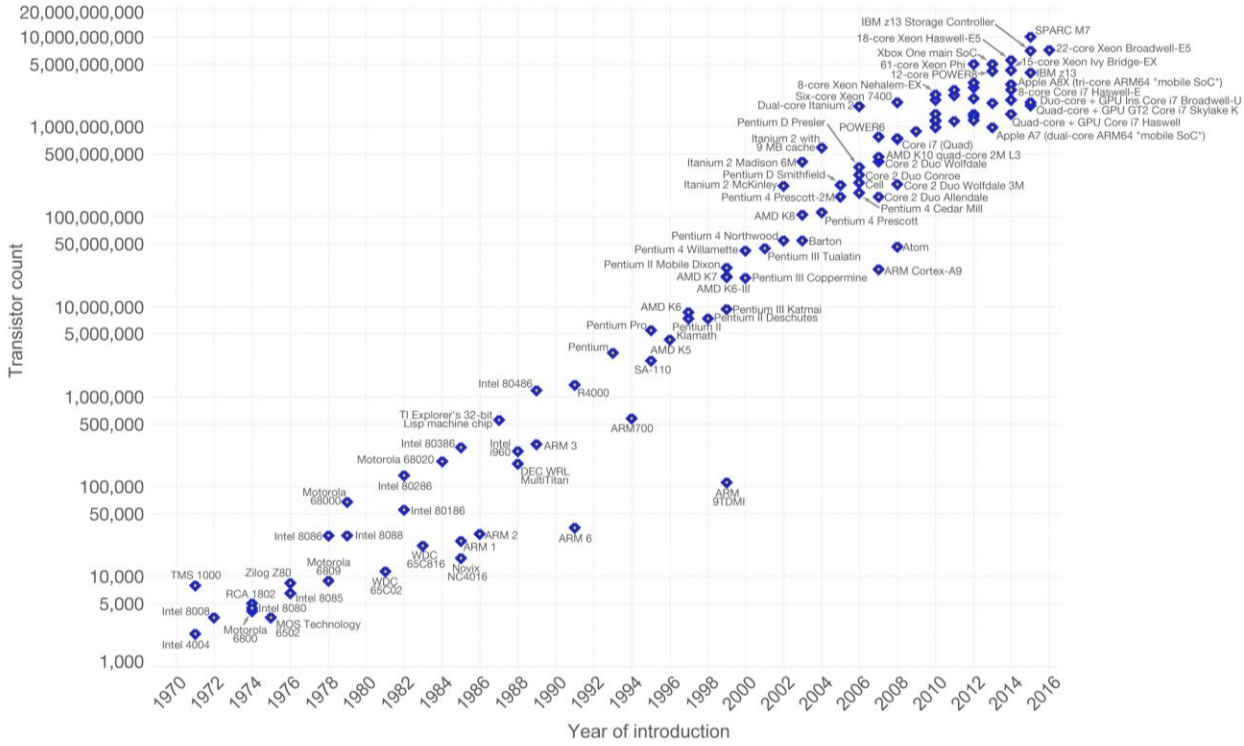


Figure 1: Moore's Law visualized: number of transistors vs. year of introduction, with inset graph illustrating the original prediction [39].

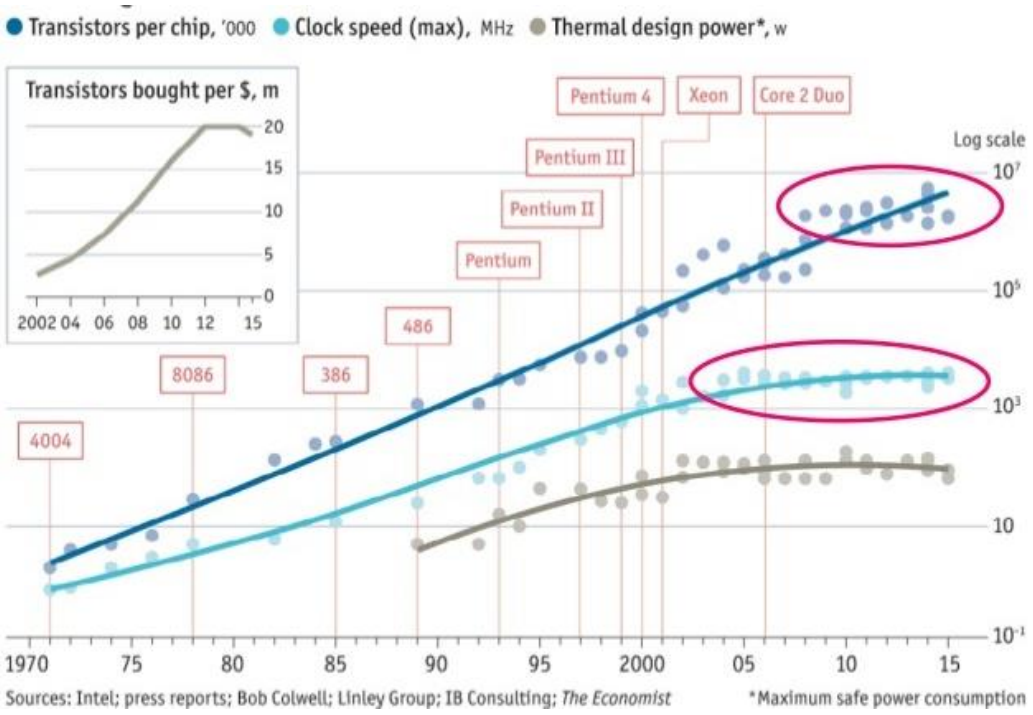


Figure 2: Clock speeds and thermal design power alongside microprocessor development [40].

The most common and effective way to counteract increasing power density was observed to be reducing the supply voltage for the chip, as any decrease in the voltage would equate to a quadratic decrease in the dynamic power consumed. The reduction in supply voltages is a trend that has been observed and predicted through the International Technology Roadmap for Semiconductors (ITRS) report, a publication that is generally regarded as a reference guide for upcoming trends in research and manufacturing. Looking at the 2013 ITRS roadmap, supply voltages were predicted to fall from 0.86V in 2013 to 0.64V in 2028 [5]. The trend continued and became even more aggressive in later reports, as the 2015 ITRS report indicates, with values ranging from 0.8V in 2015 to 0.4V in 2030 [6]. Such predictions clearly indicate that the miniaturization and lowering of supply voltages trend is here to stay.

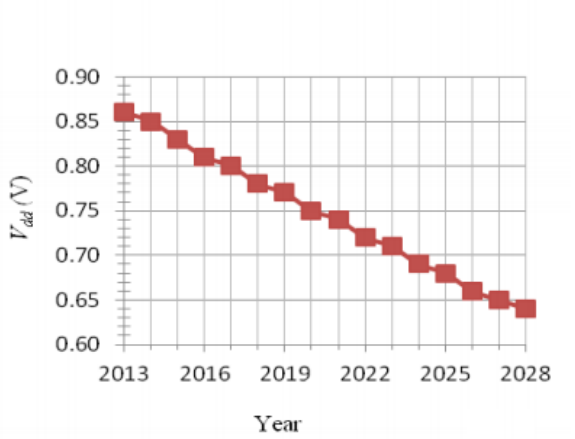


Figure 3: Supply voltage trends expected by the 2013 ITRS report [5].

**Electrical Properties of Transistors**

| YEAR OF PRODUCTION | 2015 | 2017 | 2019 | 2021 | 2024 | 2027 | 2030 |
|---|---|---|---|---|---|---|---|
| Logic device technology naming | P70M56 | P48M36 | P42M24 | P32M20 | P24M12G1 | P24M12G2 | P24M12G3 |
| Logic industry "Node Range" Labeling (nm) | "16/14" | "11/10" | "8/7" | "6/5" | "4/3" | "3/2.5" | "2/1.5" |
| Logic device structure options | FinFET FDSOI | FinFET FDSOI | FinFET LGAA | FinFET LGAA VGAA | VGAA, M3D | VGAA, M3D | VGAA, M3D |
| DEVICE ELECTRICAL SPECS | | | | | | | |
| Power Supply Voltage - Vdd (V) | 0.80 | 0.75 | 0.70 | 0.65 | 0.55 | 0.45 | 0.40 |
| Subthreshold slope - [mV/dec] | 75 | 70 | 68 | 65 | 40 | 25 | 25 |

Figure 4: Transistor properties, including supply voltage predictions, made in the 2015 ITRS roadmap [6].

## 1.2 Challenges and the Need for DC-DC Converters

However, the downside to that is the delay which is negatively impacted by reducing the supply voltage. Thus, in most portable designs, the solution that consumes the least power yet maintains verity and computational throughput is to run the circuit at the lowest possible supply voltage, and then aim to make up for the inevitable decrease in performance by optimizing the design architecture or the logical structure of the circuit itself [7]. Such optimizations all have the expectation that the supply voltage is a controllable variable that the designer can set to be as low

as possible, whereas the truth of the situation is that in portable devices, the voltage is supplied by a single battery that has only one voltage level to provide. Hence, the need arose for DC-DC converters to be able to convert the one battery supply level to the level expected by the designer for efficient, correct behavior. Among such optimizations is clustered voltage scaling, where a higher supply voltage is provided to the timing critical segments of the chip, whereas a lower one is used for the parts not on the critical path [8].

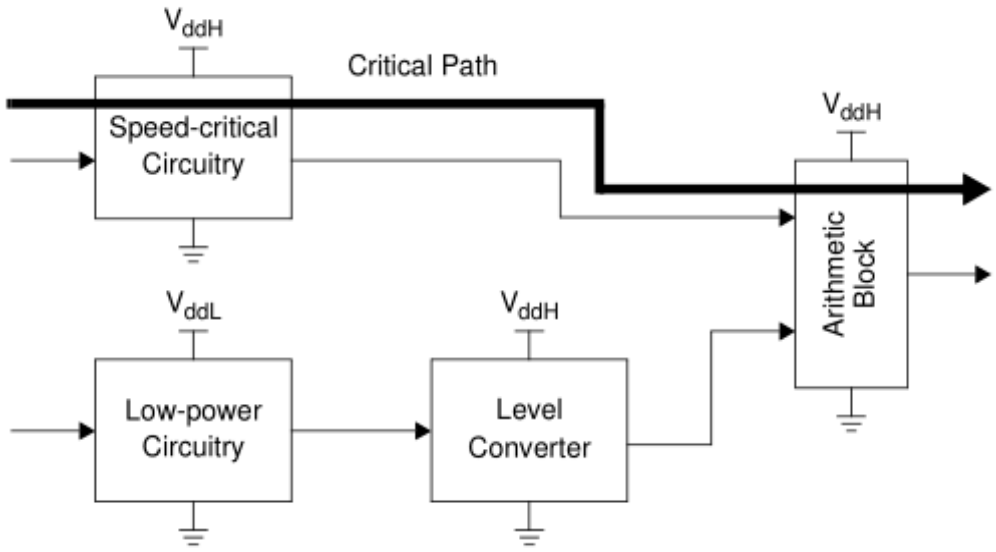


Figure 5: Clustered voltage scaling [26].

This allows for an optimization where power consumption is reduced without hugely impacting performance, and can be expanded on through providing more than two supply voltages for different parts of the chip with different supply voltage needs. However, this expansion is limited by the effect of the power consumed through the addition of multiple DC-DC converters, which would eventually counter-act the savings in power consumption made through using them. Using DC-DC converters for voltage scaling also opens up opportunities for optimization using architectural techniques, such as parallelism and pipelining, which allow

for a reduction in clock frequencies and thus a reduction in switching losses and power consumption up to 30% [7].

For general purpose processors, whose need for consistent fast execution renders performance-degrading optimization efforts less than ideal, voltage scaling via tracking DC-DC converters offers a different means of optimization. Dynamic Voltage Scaling (DVS) [9], allow the processor to take advantage of the low throughput requirements of many of the operations it performs. In such cases, the processor often finishes such operations much earlier than is needed, and thus involve an amount of energy wasted [10]. DVS aims to counter that by dynamically scaling both voltage and clock speed so as to meet the real-time requirements of the user, as illustrated in figure 6 [26]. This allows a reduction in power consumed that can theoretically reach an order of magnitude more than existing power management techniques. However, for this technique to be useful, the processor must spend most of its operating time carrying out low throughput processes, as these are the ones for which the voltage and clock are scaled downwards [11][13].

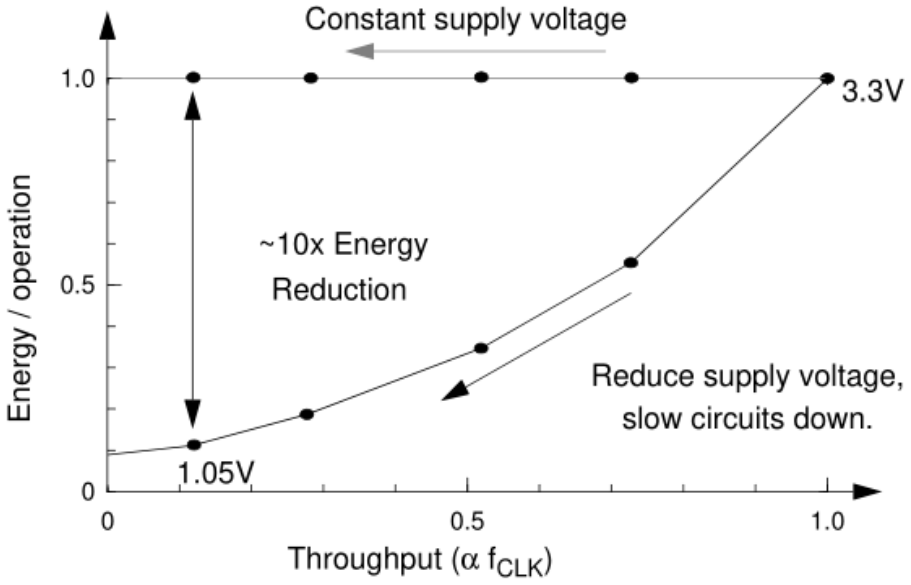


Figure 6: DVS scaling process [26].

Beyond the power savings allowed by DC-DC converters, they can also act as regulators, allowing for an extension of battery run-time, when inserted between the battery source and the load [26]. This applies to cases where the operating voltage is far below that of the battery, as the battery's discharge behavior is not flat, which leads to power consumption beyond the minimum operating one. However, by inserting the converter and using it to supply the low voltage required by the load from the battery source, the circuit will consume the minimum operating voltage which extends the battery run-time by up to 50% [26].

It is thus abundantly clear that DC-DC converters are of great importance within the current circuit design climate, as they enable further miniaturization efforts and provide great savings in energy consumption. They can be made to satisfy various design needs, be it low voltage/high current devices such as advanced micro-processors, or low voltage/low current load devices, as in ASICS implemented onto mobile chips [1]. Such advantages have fueled massive efforts in

the research and development of various types of DC-DC converters, each of which possessing their own advantages and disadvantages. The main characteristics upon which such converters are judged are efficiency, area, cost and noise [12]. First off, the converter must possess a high conversion efficiency, such that the energy losses during the conversion process are minimized as much as possible. This is necessary so that the converter losses do not negate the savings made through supply voltage reduction. Furthermore, such efficiency should be maintained not only at one load level, but over a range of loads reflecting the system's varying states of operation. An equally important metric is that of sizing and area considerations, especially seeing as DC-DC converters are largely utilized in portable applications, where area and power density is at a premium. The smaller a converter is, the easier it is to integrate on a chip alongside other components, making it a more attractive choice. Converters are also judged based on their cost and noise generation, as both factor into the viability of a converter for the chip being designed; a wireless communication application cannot abide a highly noisy converter, whereas a commonplace consumer item would require a converter of low cost.

## 1.3 Related Work

This work depends in great part on the efforts of Ismail and Amgad, patented in [38], where the development of multi-level multi-state voltage regulators was carried out. These regulators or hybrid converters as they're sometimes called, as will be explored in detail in chapter 4, differ from prior efforts in switching voltage converter designs, which often fell into one of two categories: switched-capacitor or buck. On the other hand, multistate regulators present a different way of carrying out voltage conversion, through the reliance on both switched-capacitor

and buck converters, in different stages and providing several levels of output voltage values. The attractiveness of this method with regards to the benefits it provides in terms of efficiency and converter sizing has led to plentiful research efforts adopting it to investigate possible implementation methods, as well as simulated and physical results. Among those, the ones referred to in this work are [20] and [32], which adopted the work through the design of a 3-level converter as well as simulating the design and examining the improvement in performance. While 3-level converters definitely provided better results than prior counterparts, further enhancement continued to be sought by researchers. To that effect, it is the efforts carried out in [31] that represent the guiding path for this work, as it explores the design and simulation of a 5-level multistate regulator. This was then followed by [33], which implemented the design using off-chip components in order to verify the design and gain insights regarding its performance and challenges. This work follows closely behind, as it explores the aspect of controlling the multi-state converter designed in [31] and implemented in [33], using field-programmable gate array instead of a microcontroller, so as to achieve better accuracy and faster conversion frequencies. Thus, a lot of the aforementioned papers is reiterated within this work for clarity and structure.

## 1.4 Organization of the Thesis

In designing DC-DC converters, as with almost all design problems, tradeoffs have to take place as designers decide which characteristics are deemed more important for the problem at hand. The three main types of DC-DC converters all excel at particular aspects, such as the higher efficiency of the buck converter and the smaller size of the switched capacitor one, but it happens at the cost of other factors, being the sizing and performance respectively. As will be discussed in this thesis, the buck converter offers a great chance at optimization, as it is more

possible to reduce its form factor and make it more integrable than it is for a switched capacitor one to greatly improve its efficiency.

Therefore this thesis focuses on the implementation and testing of a possible optimization of a buck converter, through the introduction of a hybrid topology. In order to tackle this task, a thorough analysis of the existing types of converters takes place in chapter 2, as well as the losses they exhibit and possible optimization efforts in chapter 3. Afterwards, in chapter 4, the hybrid topologies are presented and analyzed, whereas chapter 5 discusses the proposed FPGA-driven control methodology, presenting and explaining the results in full. Finally, in chapter 6, conclusions of the current research effort and future research possiblities are outlined.

# Chapter 2

## TYPES OF DC-DC CONVERTERS

### 2.1 Linear Regulators

DC-DC converters generally fall into one of two categories; linear regulators and switching converters (which are then classified into switched capacitor converters and buck converters). Linear regulators are usually viewed as the simplest type of DC-DC converter, as they are in essence a voltage divider circuit. As seen in figure 7, a linear regulator consists of a pass device (such as a transistor) fed by the input voltage, and generating the required output voltage [26]. These converters contain very little in the way of reactive components, such as capacitors or inductors, and occupy very little space in comparison to other types.

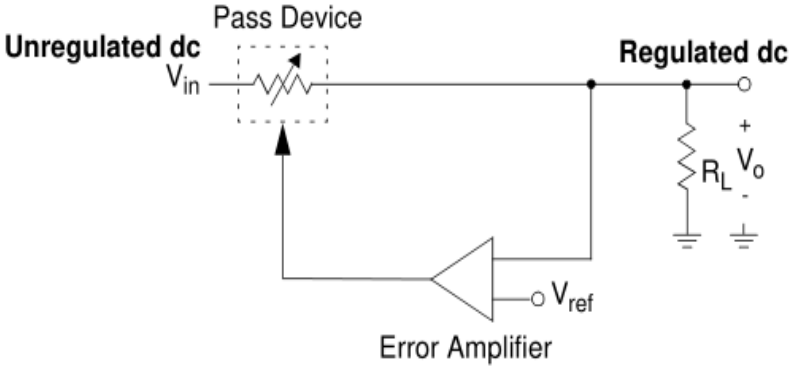


Figure 7: Linear regulator structure [26]

However, the simplicity of the linear regulator does not come without its drawbacks, which manifest in the form of functionality and efficiency limitations. Due to the structure of the regulator, it can only be used in cases where the output required voltage is lower than that of the

input voltage. Furthermore, the efficiency cannot be higher than $\frac{Vout}{Vin}$, which means that the converter is only capable of achieving high efficiency when the output voltage is very close to the input one [20]. The linear regulator efficiency relies on two main parameters; the quiescent current – which determines the power consumption in the converter's unloaded state – and the dropout voltage, defined as the minimum difference between input and output voltages needed to maintain regulation. Linear regulators are often called Low Dropout Regulators (LDR), as the dropout voltage needs to be very low to achieve the necessary efficiency. Due to the aforementioned characteristics, LDRs present an attractive solution to a smaller, simpler applications requiring an output voltage very close to the input one.

## 2.2 Switching Converters

Beyond linear regulators, the most common and versatile class of converters is switching converters, where the main conceit is to rely on a reactive element, such as a capacitor or an inductor to store the charge and then transfer it to the output. Such converters usually operate in phases, controlled by active switching elements, during which charge storage and release takes place. When compared to linear regulators, these converters are seen to be much more capable, as they can be used to provide a voltage that is lower than the input, higher than it, or even in a different polarity [14]. This versatility makes them suitable for a variety of applications and designs. Switching converters also exhibit higher efficiencies than their linear brethren, though it comes at the cost of area usage and structural complexity [15].

The two main types of switching converters are buck converters and switched capacitor (SC) converters. While both topologies rely on the usage of switches and phases, the difference lies in the component being used for charge storage and transfer. In a buck converter, an inductor is

usually the component in use, whereas SC devices utilize capacitive elements for charge storage and transfer. These two types possess their own advantages and shortcomings when it comes to efficiency, area considerations and design complexity, which makes each of them better suited for different types of applications. A more thorough analysis of the operation of each follows below.

### 2.2.1 Switched Capacitor

Switched Capacitor (SC) converters consist mainly of switches and capacitors, which are arranged in a certain manner – called a topology - to achieve a particular conversion ratio [18]. SC converter topologies correspond to several gain configurations, which define the conversion ratio based on what is required. Such gain configurations can be greater than, less than, or equal to one. A single SC converter can become a multi-ratio converter, by accessing different topologies based on which switches are clocked within the device [21]. The operation of the SC converter can be described as a sequence of phases controlled by the clock, where each phase denotes a certain number of switches being turned on or off. In the first phase, the connection of switches allows certain capacitors to be charged by the input voltage. In the following phase, the switch connection is changed, allowing the charged capacitors to release the stored charge, leading to an output voltage that is a certain fraction of the input [22]. The capacitors within the SC converter are either flying capacitors, which change their common-mode voltage with respect to ground, or bypass capacitors which are fixed with respect to ground. In figure 8, the capacitors C4 and C5 are flying ones, whereas C2, C3 and C1 are bypass.

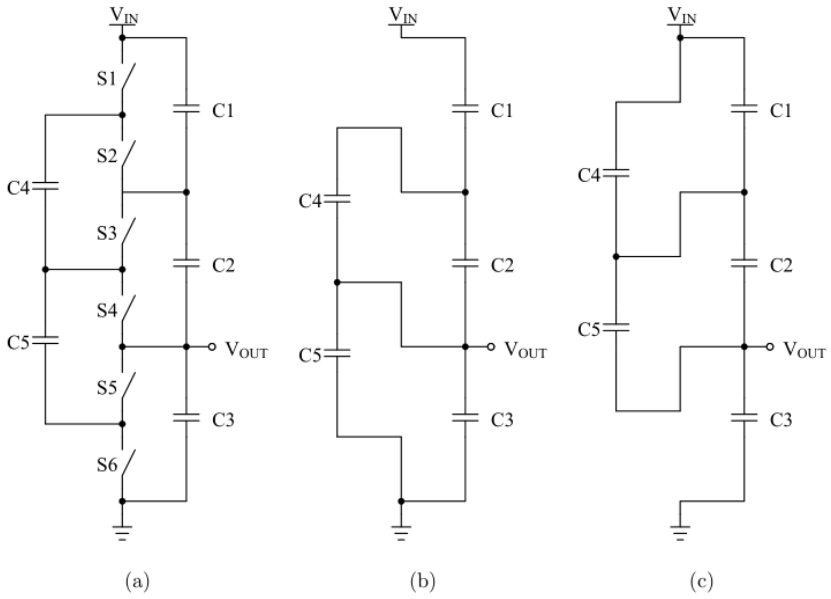


Figure 8: Switched capacitor converter, (b) shows phase 1 of operation, (c) shows phase 2 [21].

In this converter example, the conversion ratio is three to one, providing an output voltage that is one third of the input, as well as three times the charge. Beyond that, a SC converter can also contain several copies of the same topology, which are accessed in parallel via equally-spaced clocking techniques. This process is called interleaving, and it allows the converter to increase output ripple frequency and decrease ripple magnitude, helping to improve the output signal and general converter stability. SC converters, consisting mainly of capacitors and switches, usually occupy a very small area and aren't very costly, which makes them attractive for smaller applications such as wireless sensors and energy harvesters. However, the efficiency remains somewhat similar to that of a LDR, except for the fact that the output voltage is a multiple of the input voltage, which gives this equation for the efficiency $\frac{Vout}{M\,Vin}$, where Vout is the output voltage and M is the multiplier applied through the conversion ratio [23]. So the efficiency drops immensely the farther the output voltage falls from ($M*V_{in}$). Thus, as load is

applied at the output, and the voltage drops away from the ideal unloaded voltage, the efficiency of the converter drops [24].

### 2.2.2 Buck Converter

In the buck converter, the reactive element utilized to store the charge and release it between phases is the inductor. The functionality of a buck converter can be summarized as follows; the input voltage is chopped by utilizing a switch which generates a square waveform of variable duty cycle, having the average voltage desired at the output. This switching process takes place in two phases; in phase one the power switch (usually a MOSFET) connects the input voltage source to the inductor, whereas in the second phase, the inductor is connected to the ground via a diode (often called a catch or freewheeling diode) or another MOSFET. The choice of power-off switching element relies on the trade-off between design simplicity and higher efficiency [25]. The square waveform Vx is then fed into a low pass filter consisting of an inductor and a capacitor, which leaves the DC component of the signal and filters out the AC component. The structure of a buck converter is illustrated in figure 9.

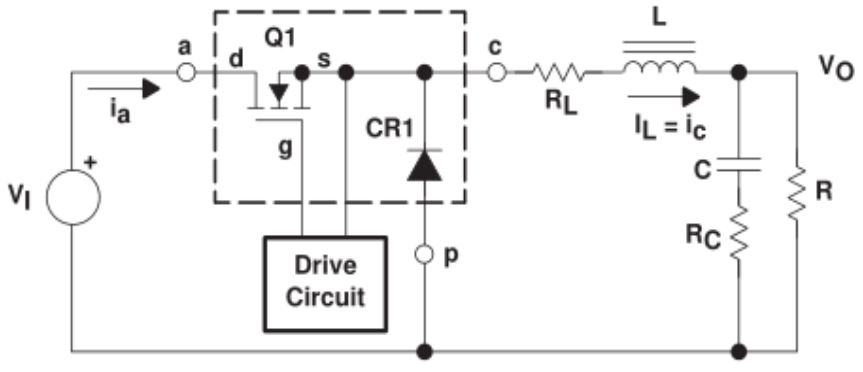


Figure 9: Buck converter structure [25].

The output voltage in this case is the product of the input voltage and the duty cycle D of Vx. The control in this topology is applied through comparing the output voltage to the reference voltage, and then using the error to pulse width modulate the duty cycle of the switch, increasing or decreasing it as necessary [26]. Buck converters can generally operate in two modes, called continuous conduction (CCM) and discontinuous conduction (DCM). These modes rely on the output load current, where the converter operates in CCM as the output load current remains fixed, and switches to DCM whenever the current falls to below critical levels [25]. These two modes have widely varying implications with regards to the voltage conversion relationship; for the CCM, the relationship is a function of the input voltage and the duty cycle (Vout = Vin * D). Whereas in DCM, the converter operates in three phases rather than two, complicating the conversion relationship, which becomes a function of input voltage, duty cycle, power stage inductance, switching frequency and load resistance. The buck converter's efficiency can theoretically reach 100%, but physical implementations of it are typically capable of reaching 75-90% efficiency, which is much higher than that of the switched capacitor converter[26]. However, the area constraints presented by the form factor of the inductor have often made it difficult to integrate on chip, and thus have kept it out of the running for many portable applications. Thus optimization goals focus on reducing the form factor to enable it to be integrated on chip, and thus make use of the higher efficiency it provides.

# Chapter 3

## SOURCES OF LOSS IN DC-DC CONVERTERS

In order to better optimize the efficiency of existing DC-DC converters, an understanding of the sources of loss within these devices is necessary, so as to work towards reducing or negating them. There are certain sources that are shared between buck and switched capacitor converters, however there are others which are unique to each, based on their topology and the choice of components.

### 3.1 Switched Capacitor Loss Sources

#### 3.1.1 Conduction losses

These losses reflect the power that is lost in the switches as the flying capacitors are charged. The loss can be determined through equation 1.

$$P_{cond} = M_{sw} \frac{I_{out}^2}{N_{phase}} \frac{R_{on}}{W_{sw}} \text{ [27]} \qquad (1)$$

Where $M_{sw}$ is a constant relying on the topology, $I_{out}$ is the output current delivered by the converter, $R_{on}$ is the switch resistance per unit width and $W_{sw}$ is the switch width. This switch width is directly proportional to the switching frequency as well as the total amount of flying capacitance, as given by equation 2

$$W_{sw} = \sigma \gamma f_{sw} \frac{C_{sw}}{N_{phase}} \text{ [27]} \qquad (2)$$

Such conduction losses can be reduced by changing the switch size, particularly in multi-topology converters, through turning on a number of parallel switches to achieve the size required. Furthermore, decreasing the frequency decreases the width, and thus increases the conduction losses and reduces efficiency [19].

### 3.1.2 Parasitic losses

Such losses refer to the parasitic bottom plate capacitances exhibited by the flying capacitors within the design, which are charged during every switching cycle as well[17]. The power lost can be given by equation 3.

$$P_{para} = M_p f_{sw} C_{sw} V_{dd}^2 [27] \qquad (3)$$

where $M_p$ is a constant that relies on the topology being used, $f_{sw}$ is the switching frequency and $C_{sw}$ is the total flying capacitance. Such losses are largely reliant on the type of capacitor technology used in the converter, and thus it is often recommended to use deep trench capacitors, as they exhibit less parasitics than CMOS ones [27].

### 3.1.3 Gate-drive losses

These losses correspond to the energy expended in charging the gate capacitances for the charge-transfer switches within the converter during every switching cycle. As seen in conduction losses, increasing the switch width helps reduce the conduction losses, but it also makes the drive losses substantial enough to figure into the SC loss model. Such losses can be given by equation 4.

$$E_{sw} = nC_{ox} W L V_{BAT}^2 [24] \qquad (4)$$

where $E_{sw}$ is the energy expended is switching the gate capacitances, n is the number of switches used and $C_{ox}$ is the gate capacitance per unit area, whereas W and L are the width and length of the switches in use and $V_{BAT}$ is the battery voltage. Reducing the gate-drive losses can be done in several ways, such as relying on a single transistor rather than a transmission gate comprising both NMOS and PMOS [24], which reduces the total gate capacitance. Also, reliance on frequency scaling techniques help reduce the switch width as the load power decreases, and thus also reduce gate losses.

### 3.1.4 Load power losses

Such losses manifest mainly due to voltage ripples in the converter, which can be given by the equation [27], reflecting the effect of the switching frequency and flying capacitance on ripples in the system. Load losses also include voltage droop, which takes place the farther the voltage source is from the utilization point.

### 3.1.5 Control circuitry losses

Control losses are of concern during the provision of ultra-low load power. These energy losses can be categorized into a dynamic switching part and a static leakage part, as seen in the equation 5.

$$E_{CONT} = K_c V_{BAT}^2 + I_{leak} V_{BAT} T_{sw} \text{ [24]} \qquad (5)$$

$K_c$ is the capacitance switched in the control circuitry every charging cycle, whereas $I_{leak}$ is the sub-threshold leakage current and $T_{sw}$ is the switching period of the charge cycle. Generally, conduction losses in the SC converter increase as the difference between the output voltage and the no load voltage increases, whereas the other forms of losses decrease. This leads to an

optimization point, where there is an optimum value for this difference that allows for the highest efficiency.

### 3.1.6 Switching limits

Another means of examining steady-state SC converter performance is through examining the output impedence, which is a function of the frequency and has two asymptotic limits [28]. One limit exhibits the behavior where resistive paths are the major portion of the impedence, and the other is where charge transference across idealized capacitors is the dominating factor. These limits allow for a different evaluation of the efficiency as a function of the load of the SC converter, and combining them equates to the total output impedence of the device.

#### 3.1.6.1 Slow switching limit (SSL) impedence

The SSL impedence is calculated with the assumption that switches and conductive interconnects are ideal, and currents between input/output sources and capacitors are impulse charge transfers. This limit is inversely proportional to the switching frequency and the size of the capacitors[16].

#### 3.1.6.2 Fast switching limit (FSL) impedence

The FSL impedence however, is calculated through assuming that the resistances associated with switches, capacitors and interconnects are no longer ideal, but actually dominate the impedence. Capacitors are treated as fixed voltage sources, and current flows in independent, constant manner [28]. In FSL, the capacitors never reach equilibrium due to the high values of other impedences, and the losses are largely modeled by the conduction losses in resistive elements in the device.

## 3.2 Buck converter Loss Sources

The buck converter, while containing a lower number of capacitors and switches and thus bound to experience less losses related to those components, does still experience energy losses due to many sources. The switching transistors, called high-side and low-side MOSFET devices, experience conduction and switching losses, similar to the switches in SC converters. In high-side MOSFET, both sources of loss are present. Conduction losses are, as seen in equation 6 [29].

$$P_{cond} = I_{out}^2 R_{dsON} \frac{V_{out}}{V_{in}} \qquad (6)$$

Where $R_{dsON}$ which is the MOSFET drain to source resistance in the ON state, whereas switching losses rely on the gate charge of the MOSFET. These two factors change inversely, as lower R coincides with high gate charge and vice versa. A choice thus arises to optimize the selection of MOSFET based on the duty cycle and switching frequency [29]. Low duty cycle, high frequency applications suffer from high switching losses, so MOSFETs with low gate charge are preferred, whereas high duty cycles suffer from high conduction losses, needing lower resistance. Low side MOSFETs on the other hand, experience very low switching losses due to the conduction of the body diode during dead time [29] and thus conduction losses are the major contributor. Furthermore, the usage of the inductor introduces more losses, as seen in equation 7 [30].

$$P_{loss(inductor)} = P_{core} + P_{dcr} + P_{acr} \qquad (7)$$

Where $P_{core}$ is the inductor core loss, $P_{dcr}$ are losses are caused by the DC resistance of the inductor windings, as well as the hysteresis within the magnetic material and $P_{acr}$ are AC

resistance losses. Such losses can be reduced through the reduction of switching frequency as well as the usage of an inductor with a larger diameter wire [29]. Additional losses also exist, such as those due to the equivalent series resistance (ESR) of the input and output capacitors, as well as PCB trace copper losses and reverse recovery losses in the body diode. However, such losses are small enough that working on reducing them does not provide a particularly high return on investment.

Another method of representing buck converter performance and efficiency is the examination of inductor current ripples [31]. The ripples end up being directly responsible for increasing the RMS value for current flow through parasitic resistances and thus higher conduction losses. Furthermore, they affect the output voltage quality, causing ripples to be introduced. The value of the peak to peak current ripple has been calculated as seen in equation 8.

$$\Delta i_{L,p-p} = \frac{\Delta V D(1-D)}{L F_{sw}} \quad (8)$$

The equation indicates that it is affected by ΔV, the voltage difference between the two levels being switched, the inductor size L and the switching frequency f. Therefore, in order to reduce the current ripples, the switching frequency and the inductor size need to be increased. However, there is a limit imposed upon each of those, particularly for on-chip applications which represent a growing segment in electronics. Inductors cannot be too big, or they risk not being integrable. Thus, the only remaining factor to be optimized for lower current ripples is ΔV, through lowering it at the inductor input. This provided the drive for the development of a hybrid kind of converter, where the usage of switched capacitors can allow for a smaller voltage difference

between the two switched levels at the inductor, and thus improving the efficiency while allowing the converter to be integrated on-chip.

# Chapter 4

## DESIGNING HYBRID DC-DC CONVERTERS

### 4.1 Three-level Hybrid Converter

The prior analysis of switched capacitor and buck converters clearly outlines that an opportunity exists to overcome the shortcomings of both devices while making use of their advantages through hybridization. SC converters are small and easy to integrate on chip, but suffer from lacking efficiency and many sources of loss. Buck converters are more efficient and experience much lower parasitic losses, but include an inductor which, for high efficiency values, has to be large enough to negate losses. By combining both designs, it is possible to obtain a buck converter with a high conversion efficiency that is also possible to integrate on-chip.

#### 4.1.1 Design

Several hybrid DC-DC converter designs have been suggested in literature. A particularly well-developed one, and the basis for the 5-level converter discussed in this report, is the 3-level hybrid off-chip converter presented by [32] for envelope tracking. As seen in figure 10, the design of the hybrid converter brings in elements of both switched-capacitors and buck converters.

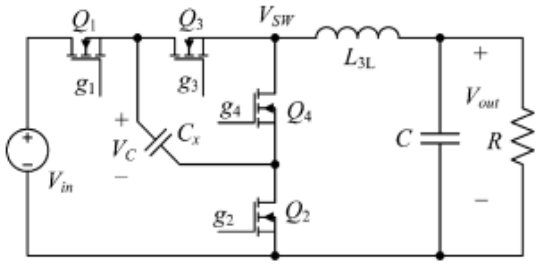


Figure 10: Three-level buck converter [32].

The first stage of the converter consists of four switches, arranged in two pairs with a flying capacitor inserted between them. The switches operate at a duty cycle D, and are phase-shifted by 180 degrees [32]. This allows the voltage at the inductor input to have one of three values; 0, Vin, and Vin/2. The second stage of the converter consists of the inductor and the capacitor forming the low pass filter that essentially takes in the DC component of the square wave provided by the switches. The buck converter thus is either switching between Vin and Vin/2, or Vin/2 and 0. Furthermore, the phase shift of the switching process essentially doubles the switching frequency [32]. The combination of the lowered voltage swing and the doubling of the switching frequency opens up a variety of avenues for improving the converter characteristics, such as reducing the inductor current ripple and output voltage ripple, or maintaining the ripple while reducing the inductor size, as well as increasing the open-loop bandwidth. For example, maintaining the same frequency and current ripples, the 3-level converter needs a quarter of the inductance and half the capacitance of the normal buck converter [32]. A simulated sample of the output voltage ripple in the 3-level converter vs the buck converter can be seen in figure 11.

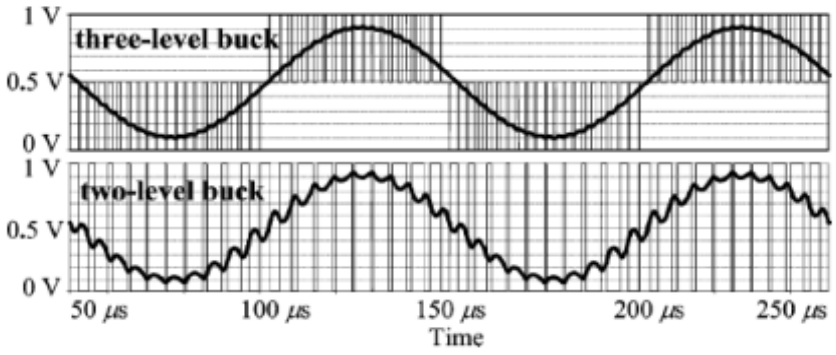


Figure 11: Output voltage ripples in 3-level converter and buck converter [32].

In terms of conduction losses, the 3-level converter exhibits much higher (up to 4 times) losses than a 2-phase buck converter, when inductor current ripples are small [32]. However, in cases where the ripples are large, as in low output load application, such conduction losses are equal or lower than their 2-level counterpart.

### 4.1.2 Analysis

Further work in analyzing 3-level converter operation was carried out in [20], where switching frequencies and number of conversion phases are optimized to improve efficiency. Generally, high switching frequencies cause a rise in switching losses, but reduce resistive losses due to current ripple. When utilizing a duty cycle close to 50%, inductor current ripples are observed to be low, and thus the switching frequency is also kept low to reduce switching losses. However, as the duty cycle moves away from the 50% mark, ripples increase and thus the frequency is increased to suppress its losses, but at the cost of higher switching losses [20]. Furthermore, the process of phase interleaving through the usage of more than one copy of the topology as mentioned before, allows for the creation of multi-phase converters, which help

divide current flow and reduce voltage ripple. However, the larger number of phases causes an increase in resistive losses, and so an optimized selection of phase number takes place based on the application. When the duty cycle is near 50%, the low inductor current ripple allows the converter to use all its phases, whereas the number is reduced the further the duty cycle is from 50%. Increasing the number of phases also allows a portion of the flying capacitor to be idle, which reduces the bottom plate parasitic capacitance. The simulated efficiency of the 3-level converter when compared to the buck converter can be observed in figure 12, clearly indicating the performance boost achieved through the hybrid design.

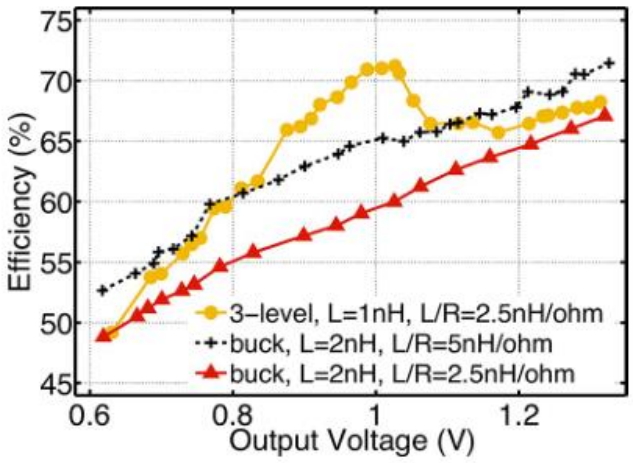


Figure 12: Conversion efficiency of 3-level converter vs. Buck converter for various inductor qualities [20].

### 4.1.3 Control

Control of hybrid converters is also an important task in converter design, seeing as the control stage helps regulate the voltage and achieve the desired output and quality. Such control strategies borrow from previously developed efforts for both SC and buck converters, as the design typically includes both. Those include techniques such as soft switching and pulse

frequency modulation for buck converters, as well as switch size modulation and digital capacitance modulation for switched capacitor converters [33].

### 4.1.4 Dead Time

An important part of converter control is the management of dead time, which is the period between the turning on/off of a pulse-width modulated (PWM) signal and the corresponding turning off/on of a different signal. Too short a period, and a short circuit is created between the supply and ground, creating massive spikes. Too long a period, and body-diode conduction and reverse recovery take place leading to lower efficiency values [34]. This behavior can be seen in figure 13, where signal behavior in short, long and optimum dead time values is portrayed [34].

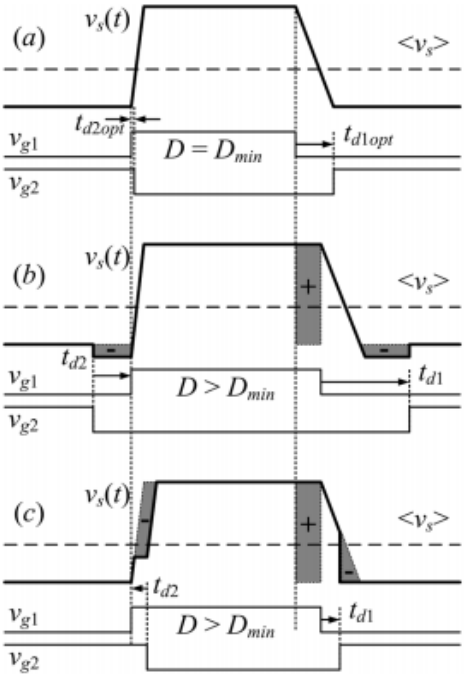


Figure 13: Representation of signal behavior in optimum, short and long dead times [34].

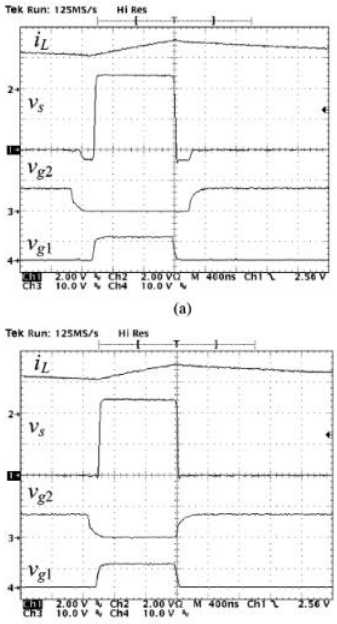


Figure 14: Dipping in signals due to long dead times [34].

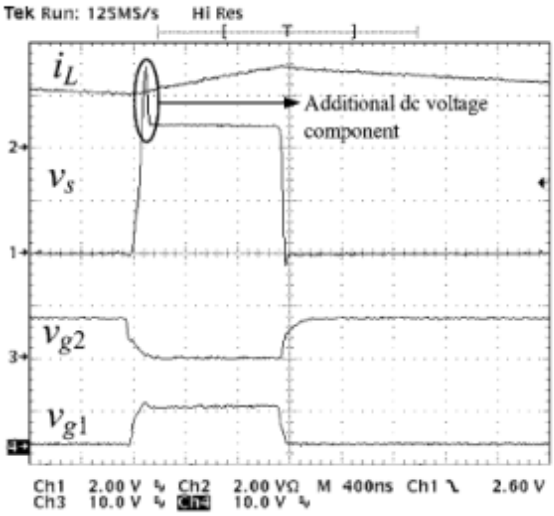


Figure 15: Observed voltage spiking due to short dead time [34].

A dead-time control mechanism was developed in [34] which relies on minimizing duty cycle commands to assign the optimum dead-time, leading to an improvement of efficiency from 87% before optimization to 92% after optimization [34]. Hence, it is made clear that optimizing dead

time is necessary to avoid damaging current spikes, as well as enhance the overall efficiency in the converter.

A viable method to improve upon the existing 3-level converter is through borrowing the switched capacitor technique of introducing of several topologies to allow for more conversion levels. Different from interleaving, in this case a number of switched capacitor topologies are integrated into the same design, then depending on which conversion level is required, the appropriate flying capacitors are switched while the others are kept off. Introducing this technique into hybrid converters has a clear benefit, as it increases the number of voltage levels at the inductor input, and thus allows for more outputs while keeping the voltage difference low. This is the concept upon which the 5-level hybrid converter under analysis is based.

## 4.2 5-level Hybrid Converter

### 4.2.1 Design

The 3-level hybrid converter, while capable of high conversion efficiencies, does continue to suffer from limitations due to the inductor sizing that make it difficult to integrate at a size that guarantees high efficiency. Hence, a need arose to reduce the inductor size further without sacrificing performance or conversion efficiency. The 5-level hybrid converter attempts to answer that need.

As seen in figure 16, the converter design, as in the 3-level one, combines aspects of switched capacitor and buck converter designs. The SC converter stage consists of eight switches and two flying capacitors, which are utilized to switch between the different topologies to provide the necessary conversion ratios. The second stage contains the buck converter elements, represented

by the inductor and capacitor forming the low pass filter that passes the DC component of the voltage signal presented at the inductor input Vx, while removing the AC component of the signal [31].

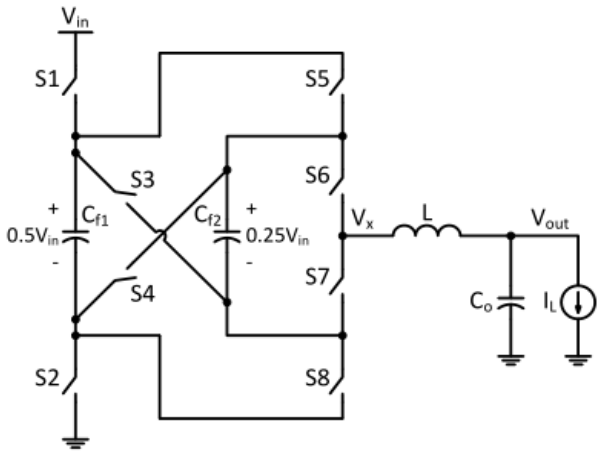


Figure 16: 5-level hybrid converter [31].

Looking at the switched capacitor stage of the converter, it can be surmised through the usage of KVL equations that the two flying capacitors are balanced at half and quarter the input voltage respectively (0.5Vin and 0.25Vin). Based on that, the SC stage is capable of providing 5 voltage levels at the inductor input, depending on which switches are turned on and whether the flying capacitors are charging or discharging, as seen in table 1.

Table 1: Configuration of switches for each voltage level [31].

| Voltage Level | Turned-on Switches | $C_{f1}$ | $C_{f2}$ |
|---|---|---|---|
| $V_{in}$ | S1 & S5 & S6 | - | - |
| $0.75V_{in}$ | S1 & S5 & S7 | - | ↑ |
| | S1 & S6 & S8 | ↑ | ↓ |
| | S2 & S3 & S6 | ↓ | ↓ |
| $0.5V_{in}$ | S1 & S7 & S8 | ↑ | - |
| | S2 & S5 & S6 | ↓ | - |
| $0.25V_{in}$ | S1 & S4 & S7 | ↑ | ↑ |
| | S2 & S6 & S8 | - | ↓ |
| | S2 & S5 & S7 | ↓ | ↑ |
| 0 | S2 & S7 & S8 | - | - |

The 5-level converter is thus always switching between two of these levels at the inductor input, allowing for an output voltage that lies between those two levels. This structure thus allows for a lower voltage swing than either the buck or 3-level converter, as in the buck the swing is always the full difference between Vin and 0, and in the 3-level it's always Vin/2. The 5-level however allows for a maximum swing of 0.25Vin, offering 5 voltage levels of 0, 0.25Vin, 0.5Vin, 0.75Vin and Vin [31]. For the common voltage inputs of 3V and 5V, this translates to 0/0.75V/1.5V/2.25V/3V and 0/1.25V/2.5V/3.75V/5V respectively.

This allows for an efficiency enhancement on both the SC converter side and the buck converter side. For the SC converter stage, as is established in [24], the efficiency relies on the difference between the output voltage in its loaded and unloaded states as seen in equation 9.

$$\boldsymbol{\eta_{lin} = \left(1 - \frac{\Delta V}{V_{NL}}\right)} \qquad (9)$$

Where $V_{NL}$ is the output voltage at no load and $\Delta V$ is the difference between loaded and unloaded voltages. Thus the efficiency is maximized the closer the loaded voltage is to the

unloaded one, making the presence of several unloaded voltages necessary in cases where the needed output voltage could have a wide range of values [24]. Hence in this case, the 5 levels at hand provide ample opportunity to minimize the difference between loaded and unloaded output voltages. On the buck converter side, based on equation (8) introduced earlier, the reduced voltage swing at the inductor input helps reduce the current ripple and thus improves the efficiency.

The 5-level hybrid converter thus provides four operating regions as compared to the 2 presented by the 3-level one. The regions are [0-0.25Vin], [0.25Vin – 0.5Vin], [0.5Vin-0.75Vin] and [0.75Vin-Vin]. For each of these regions, the inductor receives a square wave that is switching between the two limits of each region, and then generates an average value that is based on the percentage of the switching period occupied by each level. In other words, the 'coarse tuning' of the voltage is done through the selection of an operating region, whereas the 'fine' tuning is done by adjusting the duty cycle value of the converter [31]. This allows for a great deal of freedom and versatility, as it enables the user to pick the region most useful for their application as well as an accurate no-load output voltage that satisfies the user need. The no-load voltage at the output of the inductor can be given by equation 10, where D is the duty cycle value and $V_{levelx}$ refers to the voltage at each limit of the operating region.

$$\boldsymbol{V_{out\ (no-load)} = (D) * V_{level\ 1} + (1 - D) * V_{level\ 2}} \qquad (10)$$

### 4.2.2 Control

The 5-level hybrid converter also utilizes the concept of interleaving in order to improve the switching frequency and enhance the efficiency of the converter. As seen in table 1, there is more than one switching configuration for each required voltage level. For each configuration, the flying capacitors are either charging, discharging or idle. However, in order balance the flying capacitors at their expected values, the total charging time of each capacitor should equal the discharging time [31] An example of that can be seen in the 0.25Vin case, where the configurations allow for the first flying capacitor to equally charge and discharge, whereas the second one charges twice as often as discharging. As this would cause an imbalance in capacitor charge and would break converter functionality. Therefore, the second configuration (S2/S6/S8) would need to be repeated so that the charge and discharge phases are equivalent. This can be expanded to include the other operating regions as well, where for each region a 'switching cycle' exists [31]. Each switching cycle includes 4 switching periods, which can then be broken down into eight time slots. The even time slots are assigned to one voltage level whereas the odd slots are assigned to the other, with the duration of even and odd slots given by the equation 11 and 12, where D is the duty cycle and $T_{sw}$ is the duration of a single switching period.

$$T_1 = T_3 = T_5 = T_7 = D\,T_{sw} \qquad (11)$$

$$T_2 = T_4 = T_6 = T_8 = (1 - D)\,T_{sw} \qquad (12)$$

The switching configurations can be seen in table 2 and the structure of a switching cycle can be seen in figure 17. This operational structure guarantees correct converter behavior and is the target for the converter control system.

Table 2: Switching configuration for the first operation region to obtain equivalent charging and discharging periods [31].

| Time Slot | First operation region | | | | Second operation region | | | | Third operation region | | | | Fourth operation region | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $0.75V_{in} \leq V_{out} < V_{in}$ | | | | $0.5V_{in} \leq V_{out} < 0.75V_{in}$ | | | | $0.25V_{in} \leq V_{out} < 0.5V_{in}$ | | | | $0 \leq V_{out} < 0.25V_{in}$ | | | |
| | $V_x$ | ON Switches | $C_{f1}$ | $C_{f2}$ | $V_x$ | ON Switches | $C_{f1}$ | $C_{f2}$ | $V_x$ | ON Switches | $C_{f1}$ | $C_{f2}$ | $V_x$ | ON Switches | $C_{f1}$ | $C_{f2}$ |
| T1 | $V_{in}$ | S1 S5 S6 | - | - | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ | $\frac{1}{2}V_{in}$ | S1 S7 S8 | ↑ | - | $\frac{1}{4}V_{in}$ | S2 S5 S7 | ↓ | ↑ |
| T2 | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ | $\frac{1}{2}V_{in}$ | S2 S5 S6 | ↓ | - | $\frac{1}{4}V_{in}$ | S2 S5 S7 | ↓ | ↑ | 0 | S2 S7 S8 | - | - |
| T3 | $V_{in}$ | S1 S5 S6 | - | - | $\frac{3}{4}V_{in}$ | S1 S6 S8 | ↑ | ↓ | $\frac{1}{2}V_{in}$ | S1 S7 S8 | ↑ | - | $\frac{1}{4}V_{in}$ | S2 S6 S8 | - | ↓ |
| T4 | $\frac{3}{4}V_{in}$ | S1 S8 S6 | ↑ | ↓ | $\frac{1}{2}V_{in}$ | S2 S5 S6 | ↓ | - | $\frac{1}{4}V_{in}$ | S2 S6 S8 | - | ↓ | 0 | S2 S7 S8 | - | - |
| T5 | $V_{in}$ | S1 S5 S6 | - | - | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ | $\frac{1}{2}V_{in}$ | S2 S5 S6 | ↓ | - | $\frac{1}{4}V_{in}$ | S1 S4 S7 | ↑ | ↑ |
| T6 | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ | $\frac{1}{2}V_{in}$ | S1 S7 S8 | ↑ | - | $\frac{1}{4}V_{in}$ | S1 S4 S7 | ↑ | ↑ | 0 | S2 S7 S8 | - | - |
| T7 | $V_{in}$ | S1 S5 S6 | - | - | $\frac{3}{4}V_{in}$ | S2 S3 S6 | ↓ | ↓ | $\frac{1}{2}V_{in}$ | S2 S5 S6 | ↓ | - | $\frac{1}{4}V_{in}$ | S2 S6 S8 | - | ↓ |
| T8 | $\frac{3}{4}V_{in}$ | S2 S3 S6 | ↓ | ↓ | $\frac{1}{2}V_{in}$ | S1 S7 S8 | ↑ | - | $\frac{1}{4}V_{in}$ | S2 S6 S8 | - | ↓ | 0 | S2 S7 S8 | - | - |

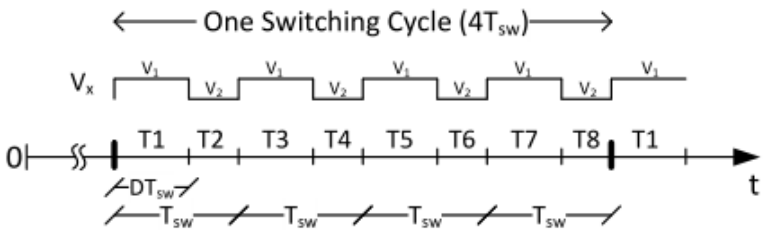


Figure 17: Structure of a switching cycle in a 5-level converter [31].

### 4.2.3 Converter Losses

When examining the design of the 5-level converter, it is important to analyze the possible sources of loss in the circuit. As seen in equation 8, reducing the voltage to a quarter of its size allows for adjustments in the inductor size, given the same current ripples and the same switching frequency [31]. In this case, the inductor can be 4 times smaller than a 3-level one and

16 times smaller than a buck one, which makes it a much more attractive target for integration. This reduction in size also allows for reducing the conduction losses associated with the parasitic resistance of the inductor [31]. The addition of switches and flying capacitors in the SC converter stage of the device also adds a sizeable amount of losses associated with switching and parasitic capacitance, however the aforementioned loss reduction helps mitigate the new losses, leading to an overall improvement in efficiency. Switching losses are also reduced in the hybrid converter due to its unique control strategy, as the structure allows the fewest number of switches to be working as the converter moves from one stage to another. For example, looking at Table 2, in the first operation region, it is clear that one or two switches at most change states from one time period to another. Furthermore, other losses are also negated through the hybrid converter structure, such as charge sharing – an inherent issue in switched capacitor converters – which is avoided through the presence of the inductor between the flying capacitors and the output capacitor [31].

## 4.3 Implementation and Simulations

In order to validate the 5-level converter design, simulations were carried out where the 5-level converter was implemented in TSMC 65 nm technology. Utilizing an input voltage of 1.1V, output voltages of 0.3V to 1.1V were obtained. The efficiency of the converter was then plotted as a function of the output voltage, which can be seen in figure 18, it can be noted that the efficiency peaks at 0.75Vin and 0.5Vin, which are the points where the ripple current approaches zero and the conduction losses are made minimal [31]. The comparison between the efficiencies of the 5-level, 3-level and buck converters can also be seen, where the three converters are given the same switching frequency of 350 MHz as well as the same inductor size of 0.5nH. It is then observed that all three converters approach the same high values of efficiency when the output

voltage is near the input 1.1V, which can largely be attributed to the small size of the inductor and the reduced ESR. However, the efficiency of the buck and 3-level converters start to decline once the output voltage moves away from the input one, as the components cannot make up for the size of the inductor. It is seen that while the 3-level converter generally remains higher than the buck, the 5-level is consistently higher than both, met only by the 3-level at the 0.5Vin point, which is the point where current ripples approach zero as mentioned earlier [31].

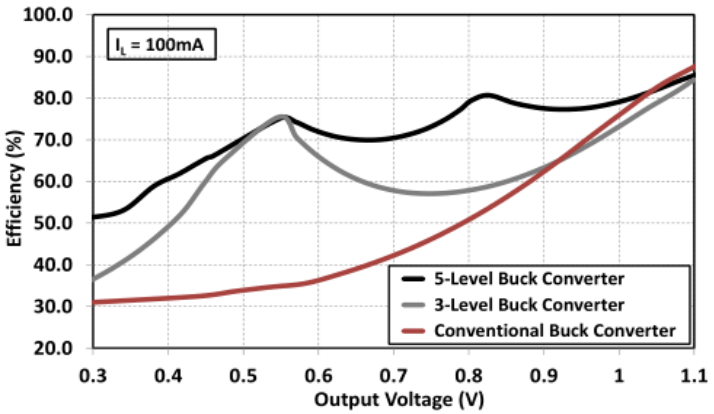


Figure 18: Simulated efficiency vs. output voltage for 5-level, 3-level and buck converter for the same inductor size and switching frequency [31].

### 4.3.1 Physical Implementation

Having verified the functionality of the 5-level converter through simulations, efforts then were directed towards the verification of the functionality through physical implementation, utilizing a PCB and selecting the proper components that allow for the most accurate and functionally efficient model of the converter. Beyond the already established control mechanisms inherent to the converter design, such as the topology control to obtain the necessary output voltage and the duty cycle modulation for fine output control, the initially utilized means to control the converter was an ATMega microcontroller [33]. This was selected due to the efficiency and simplicity of the controller, allowing for a small size package. Using the microcontroller's 8-bit output ports, control signals were piped to the switches according to the previously outlined switching structure in table 2. The signals are also piped with an appropriate amount of dead time between them to avoid current spikes or converter breakdown. MOSFET drivers were inserted between the microcontroller and the switches in order to make sure that any decay in the microcontroller output voltage does not impede proper functionality. The MOSFET drivers allow the switches to completely turn on and off at the appropriate time slots, which provides better accuracy.

Components were then selected for the implementation of the converter. With regards to switches, it was surmised that the usage of one type of switch would allow for a simpler implementation, as it avoids timing challenges introduced by the differing gate capacitances of PMOS and NMOS switches. Hence, NMOS were selected for their simplicity and availability, while focusing on optimizing the selection size between on-resistance and gate capacitance. The utilized switches have on-resistance of 5mΩ and a gate capacitance of 2000pF [33] With regards

to capacitors, the selection differed for flying and output capacitors due to the different needs for those components. In case of the flying capacitor, one was needed which allows for a low series resistance, while also allowing for high temperature ratings to avoid breakdown under stress. For this purpose, ceramic X7R capacitors were chosen for the PCB implementation. For the output capacitor however, the need is largely for a high capacitance to decrease noise and current ripple, as well as high accuracy for measurements. The selection in this case would be a tantalum capacitor with a capacitance of 100uF [33]. Low-side MOSFET drivers were also selected, due to their versatility over a large range of output voltages, as well as their simplicity and lack of need for extra components. Selection of the inductor also took place after careful consideration, due to its vital position within the converter architecture. Seeing as one of the main goals of the hybrid converter design is the minimization of the inductor size to make the converter better suited for on-chip implementation, the selected inductor ought to be of a smaller size. Thus, a coil wound inductor with minimal ESR and low quality factor was selected, to best simulate the needs of an on-chip hybrid converter [33].

Implementation of the design then went through several iterations, as components were swapped in and out to overcome issues such as high parasitic and series resistances, and the layout was changed to reduce track resistance and improve efficiency [33]. The table below indicates the components used for every attempt, as well as the issues faced by the designer.

Table 3: Implementation iterations for 5-level converter

| Implementation Components | Outcome |
|---|---|
| PCB 1: Electrolytic capacitors, IRF 510 NMOS switches, 2.2uH air core inductor | High parasitic resistances, high inductor ESR, no drivers leading to signal inaccuracies |
| PCB 2: Ceramic capacitors, SI3460 NMOS switches, 2.2uHcoil-wound inductor, LTC4440 MOSFET drivers | Switch drivers required additional components, imperfect layout leading to high parasitics |
| PCB 3: Ceramic capacitors, SI7236DP NMOS switches, 2.2 uH shielded coil-wound inductor, LTC4440 MOSFET drivers | Smaller switches allowed for lower ESR and footprint, imperfect layout and high parasitics |
| PCB 4: Ceramic capacitors, SI7236DP NMOS switches, 50  coil-wound inductor, LM5111 MOSFET drivers | Smaller MOSFET drivers used with smaller footprint and no need for peripheral components, high switching losses led to usage of larger inductor. |
| PCB 5: Ceramic capacitors, STL100N1VH5 NMOS switches, 50 uH coil-wound inductor, LM5111 MOSFET drivers | Larger but more efficienct NMOS switches utilized, tighter layout leading to lower losses and higher efficiency. |

### 4.3.2 Results of Implementation

As seen in table 3, the fifth attempt provided the best results, with optimum switch selection and high-efficiency layout. Through reducing switching and conduction losses, the highest efficiency was achieved. Figure 19 displays the efficiency vs. output voltage of the 5-level converter at different loads, indicating an efficiency of above 90% closer to the input voltage, and 80% up to 0.5 Vin. When the 5-level converter performance at 32 ohm load resistance is contrasted against the buck and 3-level converter using the same switching frequency and inductor size, figure 20 is obtained, which indicates that the performance of the 5-level converter lies close to the 3-level and buck when the output voltage is closer to the input. However, throughout the output range, the 5-level outperforms its peers with a difference in efficiency of around 5-10%, until they all realign near the lower end of the output voltage where all converters exhibit very low conversion efficiency, as ripple currents rise causing a corresponding increase in losses. The implementation thus succeeds in validating the 5-level converter design as well as its expected efficiency advantage.

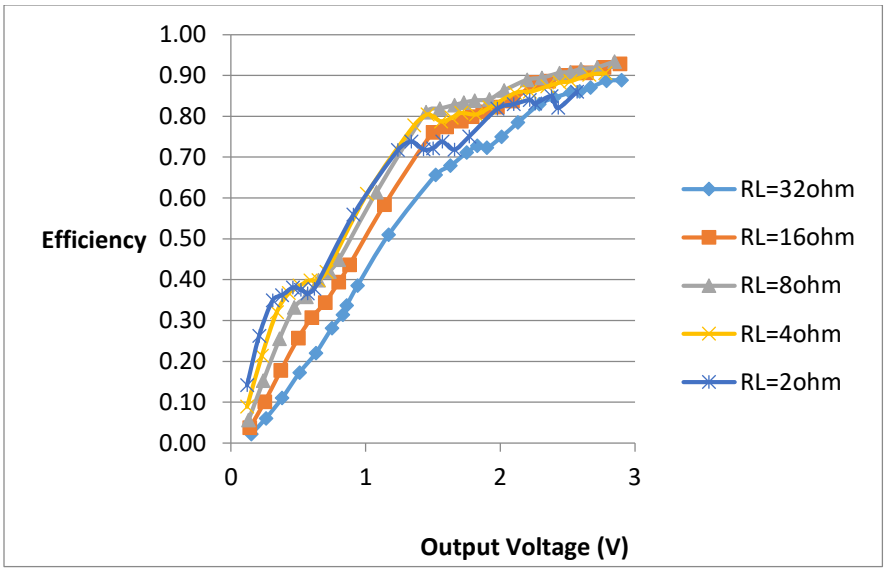


Figure 19: Efficiency vs. output voltage of 5-level converter at different load resistances [33].

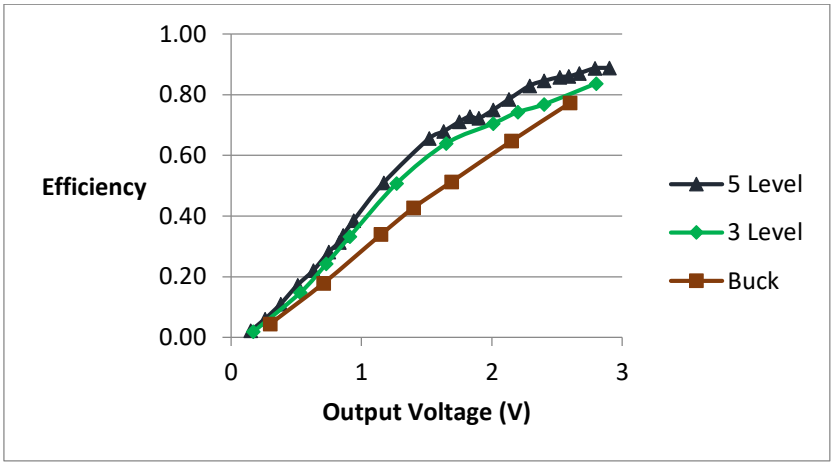


Figure 20: Efficiency of the 5-level vs. 3-level and Buck converters at 32 ohm load [33].

However, there exists an ample chance for improvement upon the current implementation of the hybrid design, such as in the control methodology utilized. For example, instead of the utilization of a microcontroller to provide the switching signals needed by the converter, using a field-programmable gate array (FPGA) for converter control is attractive, due to its added versatility, accuracy and stability at higher frequencies. This is thus investigated.

# Chapter 5

## FPGA DRIVEN CONTROL

### 5.1 Driving Reason and Selection

During the design and implementation of circuits, the question of what to utilize for control often arises. Both microcontrollers and FPGAs prove to be attractive solutions, but the choice mainly depends on the application in question and what factors are in need of accurate control. Microcontrollers are often used in smaller designs and systems, where the designer's need is to implement a simple application without large needs for memory or speed. Microcontrollers are also easier to program, as they often utilize common programming languages such as C/C++, where the instructions are simply executed in sequence and require a great deal of complexity in order to achieve parallel behavior. FPGAs on the other hand are often utilized in designs where there's a need to process a large amount of data in a speedy, timely manner such as in video and image processing software. FPGAs are also structurally different than microcontrollers, as they are essentially an array of raw logic gates, which can be programmed to fit the user's need, making them somewhat more complex but also versatile in the functions they carry out. In terms of programming, FPGAs utilize the hardware descriptive language (HDL), which is a means of describing the structure of the circuit being implemented via coding. Unlike microcontrollers, the instructions to the FPGA are not executed in sequence, but are processed to model the circuit in the form of finite state machines that are operating in parallel [34]. This is the main source of complexity within FPGAs, as it is executed concurrently and requires effort to carry out sequential operation, which makes programming FPGAs a difficult task for traditionally thinking programmers. FPGAs are also capable of supporting multiple logic interfaces with varying

voltages and drive strengths, and are even able to generate multiple clock signals in parallel, while maintaining the correct duty cycle and phase. This timing accuracy makes the FPGA particularly attractive for the hybrid converter design in question, as the converter requires accurate control signals with sufficient dead time, to guarantee that the switches turn on and off at the expected time intervals and with the correct duty cycle requirements, so as to obtain the correct outputs. Furthermore, the capability of the FPGA to boost the switching frequency also allows for a reduction in ripple currents as mentioned in equation 8 which helps improve the efficiency of the hybrid converter.

The FPGA utilized for the control of the converter in this case was the Xilinx Virtex 5 LX50T, implemented as part of the Digilent Genesys circuit board. The Genesys board is a versatile development platform which is based on the Virtex 5 FPGA while also including a number of peripheral components possibly needed by the developer, such as Ethernet, HDMI video and DDR2 memory arrays as well as a robust collection of Input/Output (I/O) interfacing methods, such as switches, LEDs and buttons. The main part of the board however, is the Virtex 5 LX50T FPGA chip, which is optimized for high performance logic operations [35]. The FPGA offers 7,200 logic slices as well as 48 DSP slices and 12 digital clock managers. It also is able to run at 500+ MHz clock speeds, offering a significant improvement over its microcontroller counterparts. The logic blocks of the FPGA contain elements such as function generators, storage elements, arithmetic logic gates and multiplexers, with internal fast interconnects that enable the FPGA to route signals quickly. The structure of the board can be seen in figure 21 which outlines the main components and peripherals included on board. Utilizing the iMPACT USB port to connect it to the PC, the Xilinx ISE Design Suite was utilized to write the VHDL code necessary to control the converter.

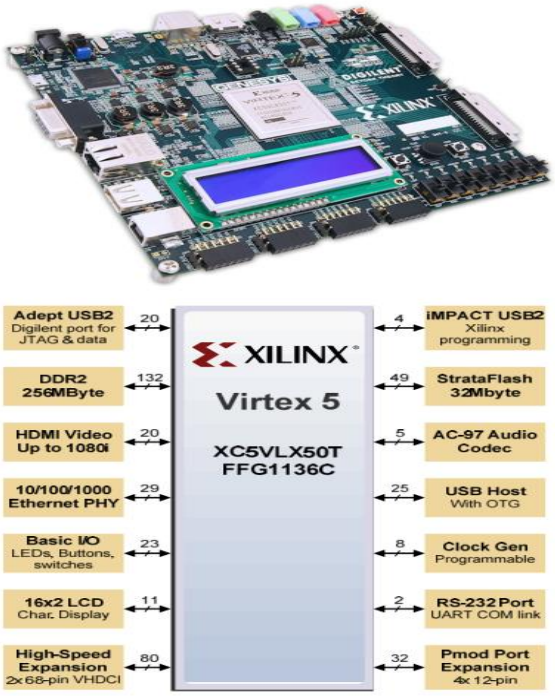


Figure 21: Digilent Genesys Structure [36].

## 5.2 Writing the VHDL Code

In order to understand the structure of the VHDL code, it is necessary to examine how the 5-level converter control takes place. As mentioned before, the converter relies on a switching cycle, which consists of 4 switching periods. Each switching period in turn has 2 time slots, leading to the presence of 8 time slots within each cycle. During each of these timeslots, certain switches are turned on or off in order to allow the flying capacitors to charge or discharge, while being careful to allow equal time for charge and discharge of each capacitor for correct operation. The odd slots of the cycle are assigned to the switch values for one voltage level, whereas the even are assigned to switches of the other. For example, in the first region, odd slots are for the 0V level, and even slots are for the 0.75Vin level [31]. With that in mind, it is clear that the converter initially decides which operating region it is in, then transmits the switch

control signals in the manner outlined in the switching schedule table. This informs the structure of the VHDL code.

### 5.2.1 Entity

A VHDL program starts by defining an entity, which can be seen as a black box that indicates the inputs to and outputs from the program.

Listing 1: Entity.

```
entity another is
port(
        clk,rst: in std_logic;
        z: out std_logic_vector (7 downto 0);
        dutyc: in std_logic_vector (9 downto 0);
        opreg: in std_logic_vector (1 downto 0));
end another;
```

Here the entity defined as ‘another’ indicates that the program relies on clock and reset inputs (clk, rst) as well as inputs indicating the required duty cycle (dutyc) and operating region (opreg) demanded by the user of the converter. The duty cycle is mapped as a 10 bit logic vector to allow for a wide range of operation for testing, whereas the operating region is a 2 bit vector, as we essentially have four operating regions. The output is mapped to an 8 bit vector, supplying the control signals to the 8 switches within the converter at each time slot.

### 5.2.2 Architecture

Listing 2: Architecture.

```
architecture behavior of another is

        signal z1_now, z1_next : std_logic_vector(7 downto 0) ;

signal dutyc: std_logic_vector(9 downto 0) ;

signal duty_now: std_logic_vector(9 downto 0) ;

        signal opreg: std_logic_vector (1 downto 0)  ;

signal te_now, te_next: std_logic_vector (2 downto 0) ;

signal temporal: std_logic;

signal counter: integer range 0 to 124999 := 0 ;
```

The architecture definition in VHDL outlines the internal structure of the control system, showing the connections leading through from input to output. In listing 2, the signals z1_now and z1_next relate to the output signal. Duty_c and duty_now are signals that relate to the duty cycle control, whereas the opreg is associated with the operating region. Te_now and te_next are both logic vectors that control the time slot definition within the code structure, each of which being a 3-bit vector as there exists 8 time slots to each switching period. Finally, the signals temporal and counter relate to the internal progression of the code, as will be outlined below.

### 5.2.3 Clock Process

Listing 3: Clock Process.

```
process (rst, clk)
        begin
if (rst = '1') then
        temporal <= '0';
        counter <= 0 ;
      elsif rising_edge(clk) then
        if (counter = 100) then
          temporal <= NOT(temporal);
          counter <= 0 ;
        else
          counter <= counter + 1;
        end if;
      end if;
end process;
```

The processes in VHDL represent functions or state machines, where each describes a functionality implemented by the code. Listing 3 is the clock generation process, which relies on the previously defined inputs clk and rst, expressed in the entity above. Enabling the rst input

resets the entire control scheme, whereas the clk input is utilized to create an internal, slower clock through the code. Here, the rising edge of the clock increases the counter value by one, until reaching the desired value of 5000, at which point the temporal variable is inverted. This in essence creates a clock (temporal) which is 1/5000 the speed of the fixed input clock signal. Alternatively, one of the digital clock generators in the FPGA could have been utilized to obtain the required clock speed, however this proved to be an easier and more flexible manner of creating the clock.

### 5.2.4 Duty Cycle Process

Listing 4: Duty Cucle Process.

```
process (temporal, rst)
    begin
        if (rst='1') then
                duty_now <= "0000000000";
        elsif rising_edge(temporal) then
                duty_now <= duty_now + "1";
        end if;
end process;
```

Listing 4 is a brief process within the VHDL code structure which aims at creating the duty cycle behavior within the converter. Aside from utilizing the rst signal to reset the behavior, the temporal clock signal created in the previous code segment is used here to increment the

duty_now signal. The usage of the signal itself will be outlined in the following segment, but it essentially is used to maintain the switches on/off status for the required duration of the duty cycle, to guarantee the correct voltage output.

### 5.2.5 General Control Process

Listing 5: General Control Process

```
process (rst, temporal, opreg, duty_now, dutyc, te_now, te_next, z1_now, z1_next)
    begin
    if (rst='1') then
        z1_now <= "00000000";
        te_now <= "000";
    elsif rising_edge(temporal) then
        z1_now <= z1_next;
        te_now <= te_next;
    end if;
```

The main process controlling the hybrid converter starts with the definition of events processing that takes place at each clock cycle. The signals z1_now and te_now indicate the switches status and time slot at the present point in time, whereas z1_next and te_next indicate the following values to be shifted in once the new clock edge is sensed. Thus the sequencing of the switches statuses is established.

### 5.2.6 Operation Cases

Listing 6: Operation cases

```
case opreg is
        when "00" =>
                case te_now is
                        when "000" =>
                                if (duty_now = dutyc) then
                                        te_next <= "001";
                                        z1_next <= "01010001";
                                        else
                                        te_next <= "000";
                                        z1_next <= "00110001";
                                        end if;
                        when "001" =>
                                if (duty_now = "0000000000") then
                                        te_next <= "010";
                                        z1_next <= "00110001";
                                        else
                                        te_next <= "001";
```

```
                z1_next <= "01010001";
                end if;
            when "010" =>
                if (duty_now = dutyc) then
                    te_next <= "011";
                    z1_next <= "10100001";
                else
                    te_next <= "010";
                    z1_next <= "00110001";
                end if;
```

Listing 6 expresses how the code approaches the switch statuses from table 2, where for each operating region, the 8 switches are either turned on or off during every time slot. In order to implement that, the code goes through a case statement, one for each operating region. The one described above is for the '00' case, which is the first operating region switching between 0V and 0.75Vin. The switch states for this region are outlined in table 4, which determines the values used in the case statement. An internal case statement is carried out within every operating region case, representing each time slot during the larger switching period. Within each time slot, the code checks for the current value of the duty cycle. As seen in equations 11 and 12, the odd time slots correspond to duty cycle value D whereas the even slots correspond to the (1-D) value. Thus, for the odd slots, the code checks the current duty cycle value as it gets incremented every clock cycle, and whether it matches the expected value that was input by the

user. As the value remains below the expected, the FPGA outputs the switch states allocated to that time slot, creating the D part of the duty cycle. Once the expected value is reached, the code moves on to the following slot, where the switch state of the slot is output until the duty cycle reaches its maximum value, at which point the duty cycle is reset and the code moves on to the following time slot. This behavior recreates the switching period developed in [31], enabling the converter to function accurately and correctly.

Table 4: Switching states from first operation region [31].

| Time Slot | First operation region | | | |
|---|---|---|---|---|
| | $0.75V_{in} \leq V_{out} < V_{in}$ | | | |
| | $V_x$ | ON Switches | $C_{f1}$ | $C_{f2}$ |
| T1 | $V_{in}$ | S1 S5 S6 | - | - |
| T2 | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ |
| T3 | $V_{in}$ | S1 S5 S6 | - | - |
| T4 | $\frac{3}{4}V_{in}$ | S1 S8 S6 | ↑ | ↓ |
| T5 | $V_{in}$ | S1 S5 S6 | - | - |
| T6 | $\frac{3}{4}V_{in}$ | S1 S5 S7 | - | ↑ |
| T7 | $V_{in}$ | S1 S5 S6 | - | - |
| T8 | $\frac{3}{4}V_{in}$ | S2 S3 S6 | ↓ | ↓ |

## 5.3 Moving from Inputs to Dynamic Operation

While the current control method for the hybrid converter seems adequate, the issue of having to provide a particular duty cycle and operating region for it to function does not model normal usage. Thus efforts were carried out to add a more dynamic control method to the existing code,

where the simple provision of a required voltage allows the converter to pick the operating region and duty cycle necessary to obtain that voltage.

Listing 7: Dynamic operation

```
process (vref)
        begin
                if (vref > "00000000") then
                        if (vref <= "01000000") then
                                opreg <= "00";
                                duty_full <= vref *
std_logic_vector(conv_unsigned(16,8));
                                duty_rec <= duty_full(9 downto 0);
                        elsif (vref <= "10000000") then
                                opreg <= "01";
                                duty_full <= (vref-"01000000")*
std_logic_vector(conv_unsigned(16,8));
                                duty_rec <= duty_full(9 downto 0);
                        elsif (vref <= "11000000") then
                                opreg <= "10";
                                duty_full <=(vref-"10000000")*
std_logic_vector(conv_unsigned(16,8));
                                duty_rec <= duty_full(9 downto 0);
```

```
                else
                        opreg <= "11";
                        duty_full<=(vref - "11000000")*
std_logic_vector(conv_unsigned(16,8));
                        duty_rec <= duty_full(9 downto 0);
                end if;
        else
                        opreg <= "00";
                        duty_full <= "0000000000000000";
                        duty_rec <= "0000000000";
        end if;
end process;
```

Listing 7 added to the control code relies on the provision of an analog-to-digital converted (ADC) voltage value, which is supplied as an input to the FPGA instead of supplying the operating region and the duty cycle. The process examines the digital value of the voltage vref, and compares it to the quarter, half and three-quarters equivalent of the digital voltage value, represented here as an 8-bit logic vector. For each of the four cases, the process then assigns the relevant operating region, which guides the sequence of switch states. It also assigns the appropriate duty cycle, through remapping the voltage level in each region such that the upper limit of the region is viewed as the full 10-bit duty cycle value. The required duty cycle is then calculated as the fraction of vref to the full voltage range. As an example, in the first operating

region, the two 8-bit limits of the voltage range are 0 and 64. In order to calculate the duty cycle for a vref between 0 and 64, the upper limit (64) is viewed as the 100% duty cycle value (1024), and thus duty cycle(vref) is equivalent to vref * 1024/64, or rather vref multiplied by 16, as seen in the code snippet above. This process is then repeated for the three remaining operating regions. There exists a marginal amount of accuracy degradation in this process however, due to the mapping of a 10-bit value to an 8-bit one obtained through the ADC. However, this can be easily overcome through the usage of an ADC that possesses a higher bit resolution, enabling the converter to have a one-to-one value mapping and thus higher accuracy. After defining the operation region and the expected duty cycle, the control code operation resumes as before.

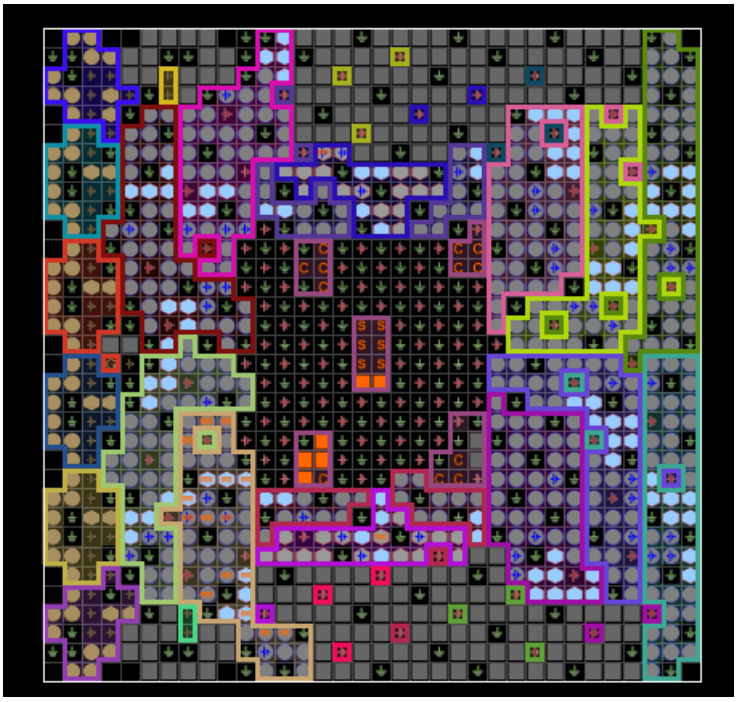

Figure 22: Pin plan for the FPGA, illustrating the logic slices and placement of I/O ports.

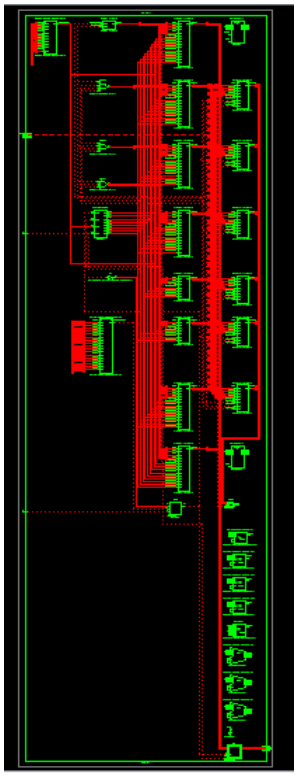

Figure 23: Register Transfer Level (RTL) schematic of the FPGA control code.

## 5.4 Simulations and physical implementation

In order to validate the correctness of the control code, simulations were run through the native Xilinx ISE simulator, utilizing different values for the expected voltage vref and then observing the behavior of the control code.

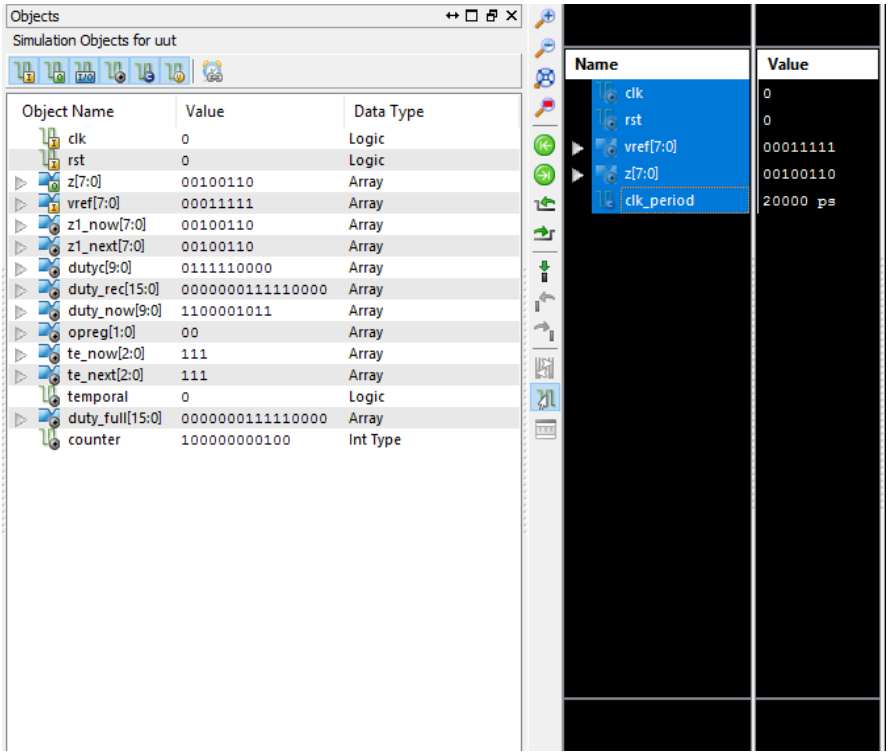


Figure 24: Simulating an output in the first operating region

In the figure above, it can be seen that for the requested voltage vref= 00011111, the converter decides that the necessary operating region is the first one (hence setting opreg to 00) and the duty cycle is seen in duty_full, duty_rec. The converter then starts going through the switch states for each time slot, as seen in the simulation snapshot, with the current timeslot being the sixth one (te_now = 101) and the switch states represented in z1_now. These signals would then be fed to the converter, enabling it to generate the required voltage level. Similar simulations for the other operating regions can also be seen in the following figures.

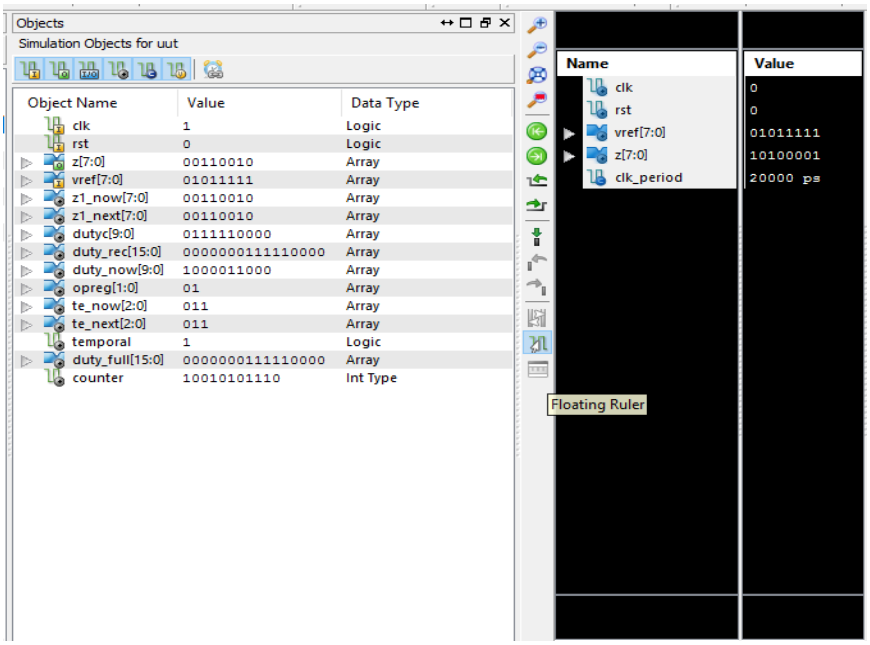


Figure 25: Simulating an output in the second operating region

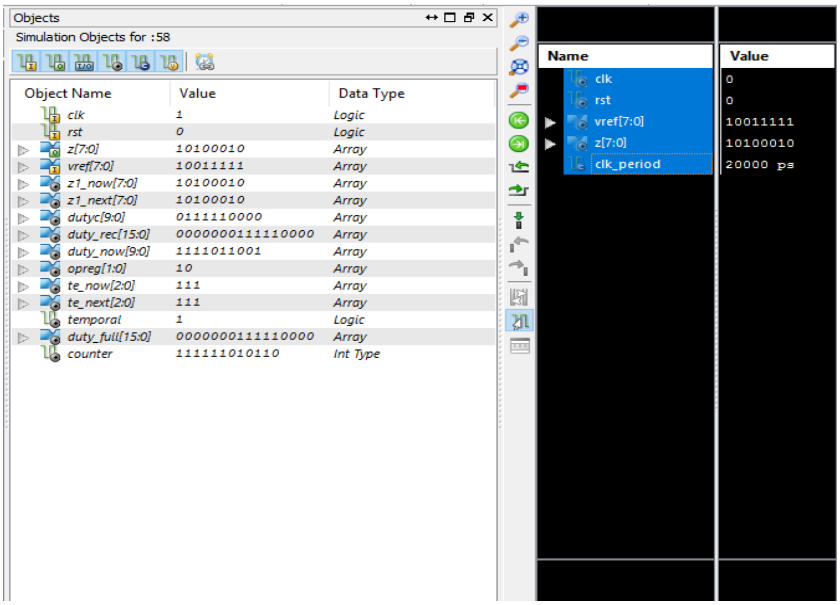


Figure 26: Simulating an output in the third operating region

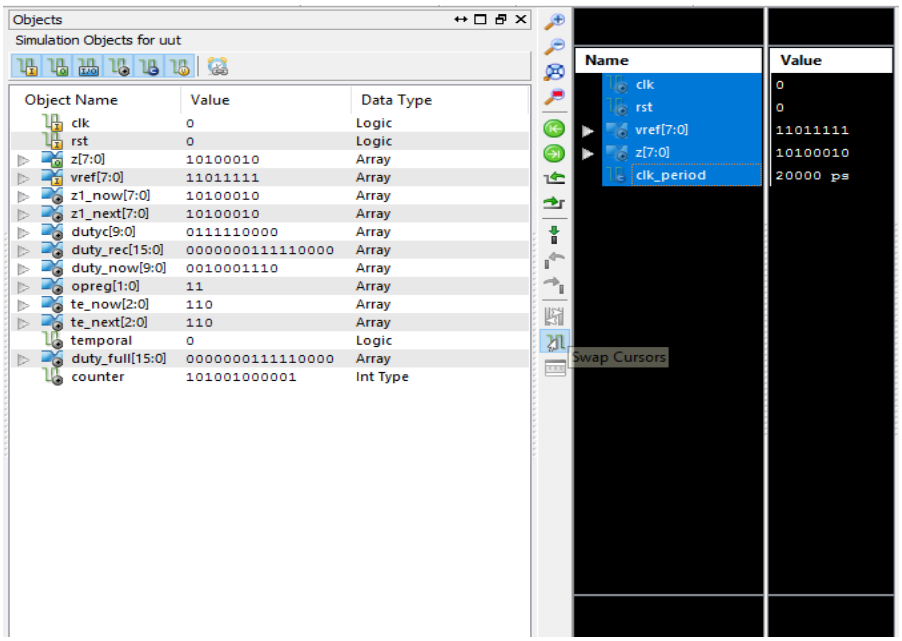


Figure 27: Simulating an output in the fourth operation region

As can be seen in the prior simulation snapshots, the duty cycle and operation region are selected successfully based on the required voltage, then the switch states are cycled through and fed into the converter, generating the required voltage at the output.

### 5.4.1 Physical Implementation and Results

After confirming that the simulated operation of the control code is functioning correctly, work was then done to physically test the code and examine the output. This implementation was carried out in two phases, the first relying on the first version of the code, where the operation region and the duty cycle are fed in manually, whereas the second one utilized an input voltage value and then observed the generated output.

In the first phase of the physical implementation, the previously developed PCB containing the converter circuit was connected to the FPGA, with the FPGA outputs feeding into the switch inputs of the converter, while an input of 3V is provided to the converter, and the outputs are then observed for each of the operating regions.

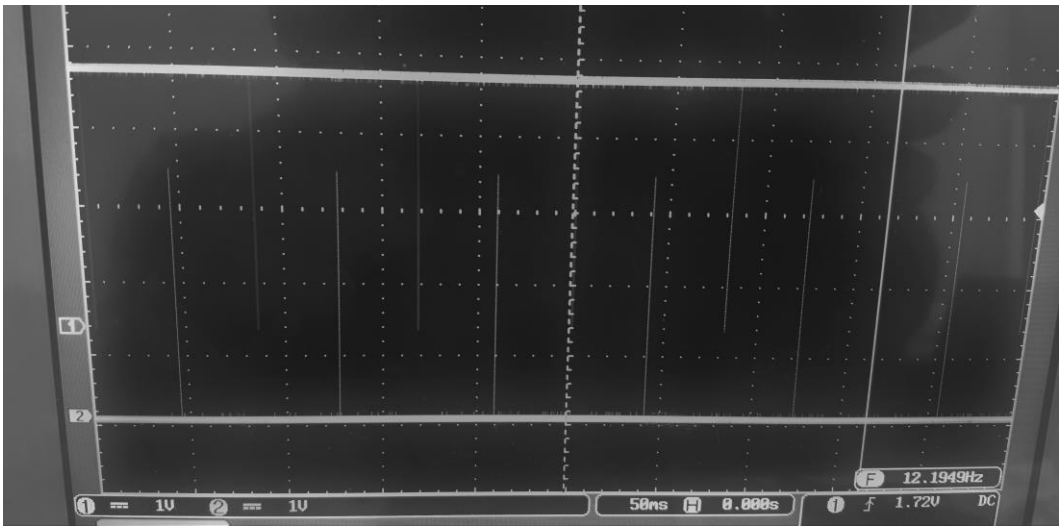


Figure 28: Control bits by the FPGA

Initially, the control code generated by the FPGA was examined to make sure that the signals provided do not overlap. As can be seen in figure 28, the bits for two of the channels feeding the converter have zero overlap, with ample dead time provided between the signals. This guarantees that there would be no current spikes during the converter operation, protecting it against hardware failure and ensuring robustness of output.

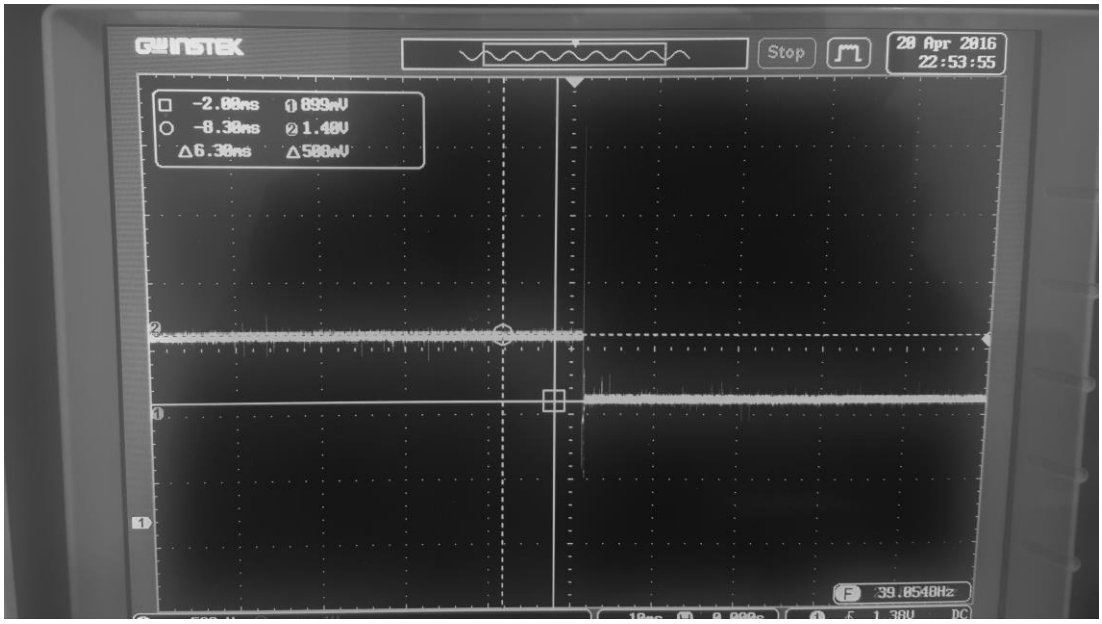


Figure 29: Vx switching between 0.25Vin and 0.5Vin

In order to observe correct operation, the voltage at the input of the inductor Vx is examined to see if the inductor is indeed switching between the correct values. As can be seen here, in the second operating region, the inductor switching between 899mv and 1.48V, which are the 0.25Vin and 0.5Vin values for a 3V input signal. This validates that the converter is being controlled correctly, giving the right voltage switching values.


Figure 30: Output voltage at 0.25Vin

Afterwards, the voltage generated at the output of the converter is examined in each region, with the duty cycle set to 100% so as to see the maximum value in each region and ascertain correct functionality. In figure 30, the output voltage is approximately 600mV which is representative of the 0.25Vin region. The outputs for the 0.5Vin, 0.75Vin and Vin can also be seen in the figures below.

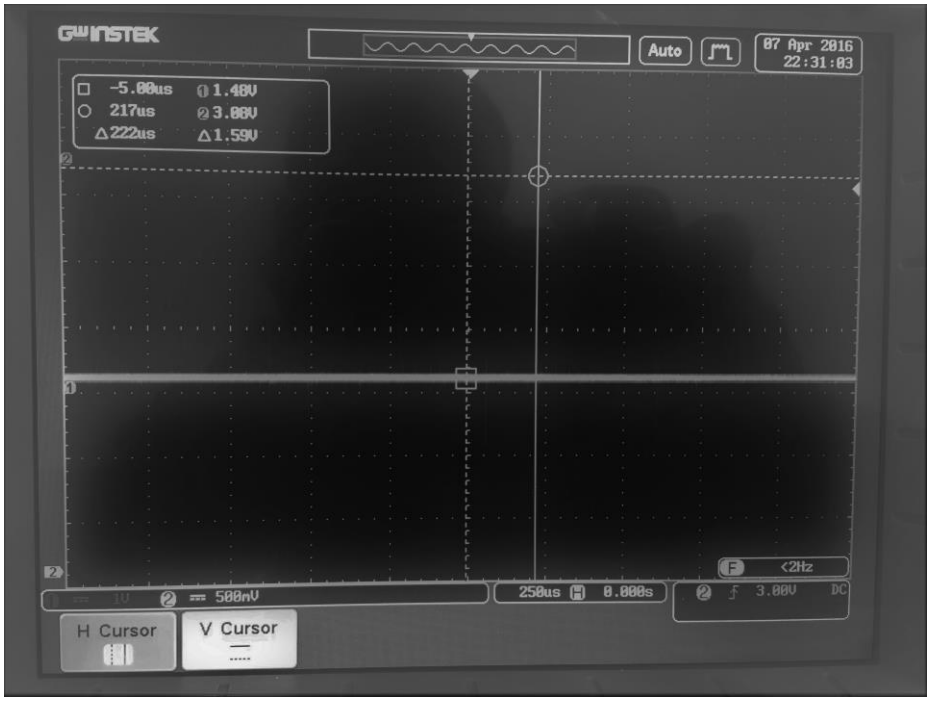


Figure 31: Output voltage at 0.5Vin


Figure 32: Output voltage at 0.75Vin


Figure 33:Output voltage at Vin

In order to examine the effect of duty cycle variation on the output voltage, the 0.75Vin voltage level was examined at 10% duty cycle, 80% duty cycle and 100% duty cycle. As seen in figures 34 to 36, the value of the output voltage ranges from 1.55V at the 10% range to 2.32 at the 100% range, which indicates that the duty cycle control functions correctly within the operating region.

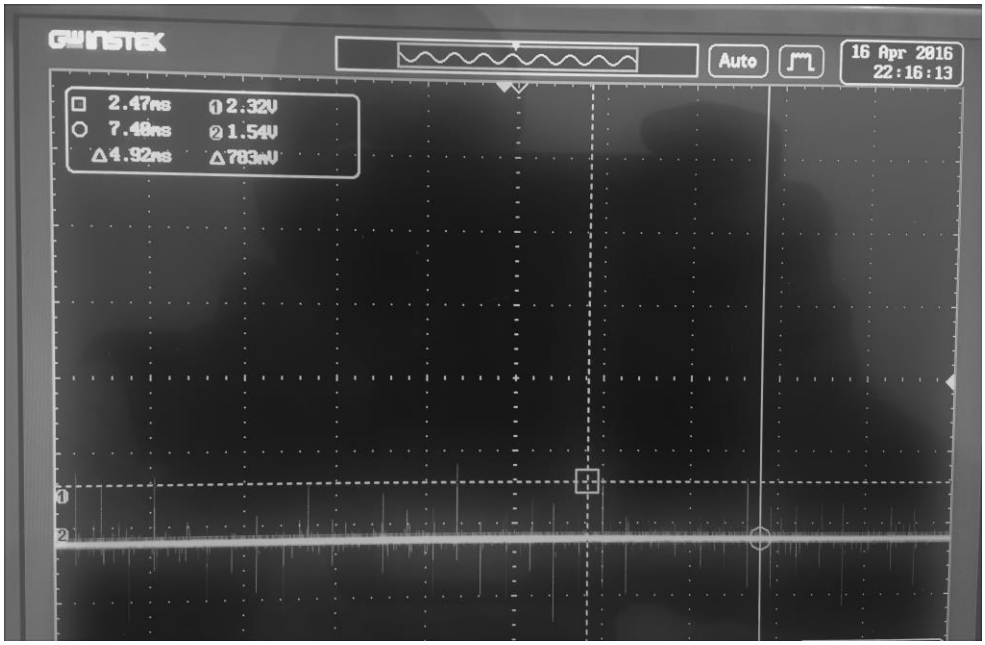


Figure 34: 10% duty cycle for 0.75Vin

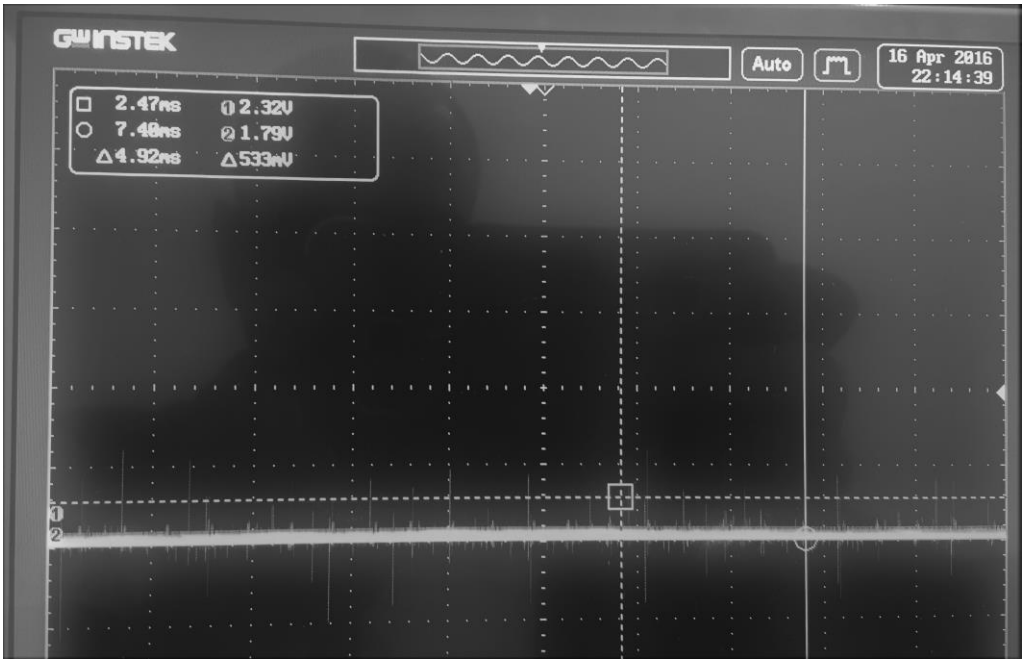


Figure 35: 80% duty cycle for 0.75Vin

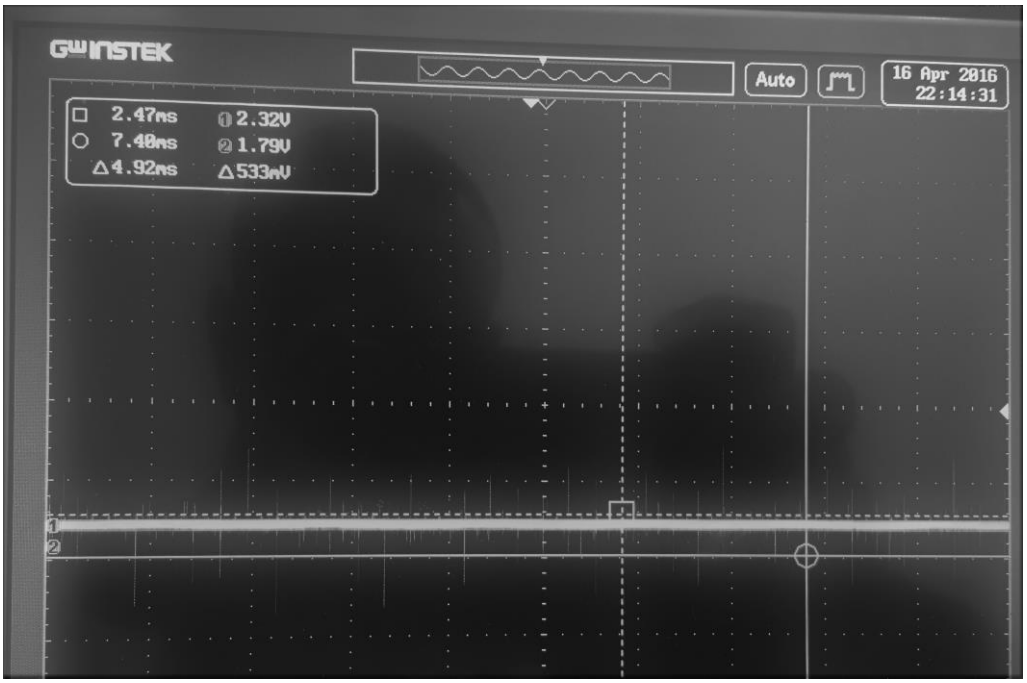


Figure 36: 100% duty cycle for 0.75Vin

However, it was noted that at the switching frequency of around 2MHz, the capacitors weren't given ample time to discharge completely, which was leading to certain spiking in the output voltage level. In order to obtain a cleaner signal with smaller, less disruptive spikes, the switching frequency was reduced to 1MHz, which still exceeds the microcontroller achieved frequency.

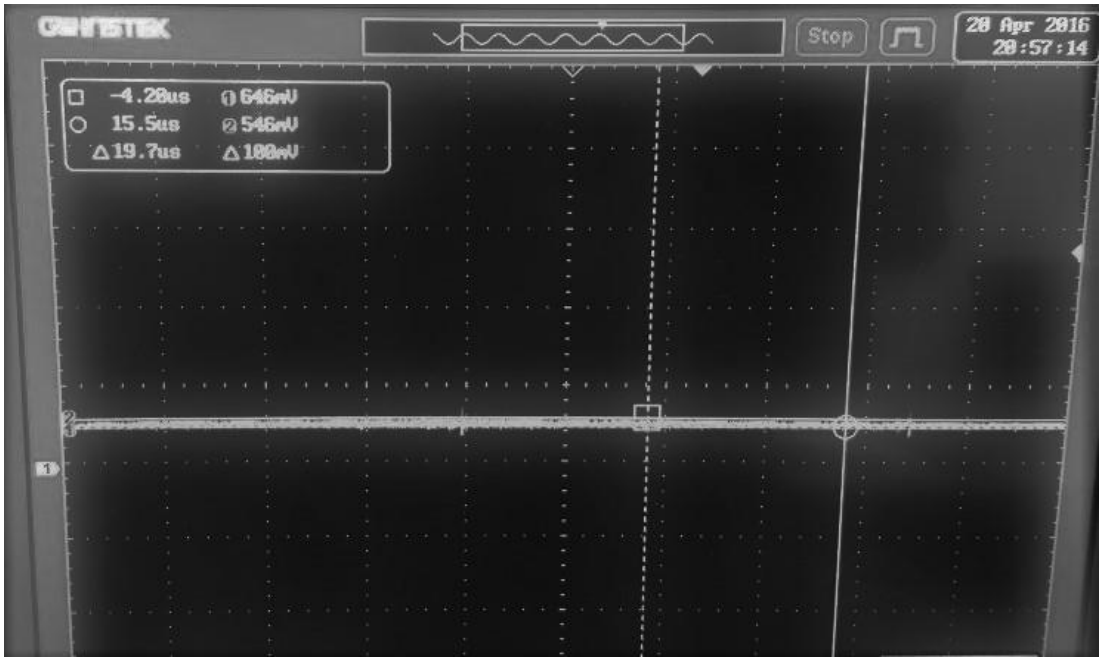


Figure 37: Quarter voltage output at 1MHz

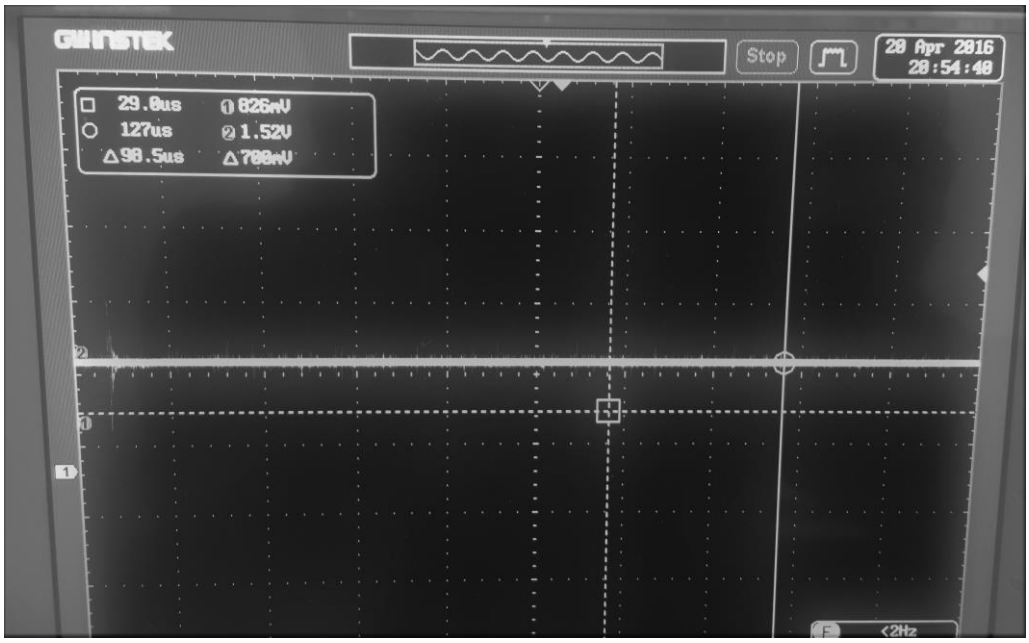


Figure 38: Half voltage output at 1 MHz


Figure 39: Three quarters voltage output at 1Mhz

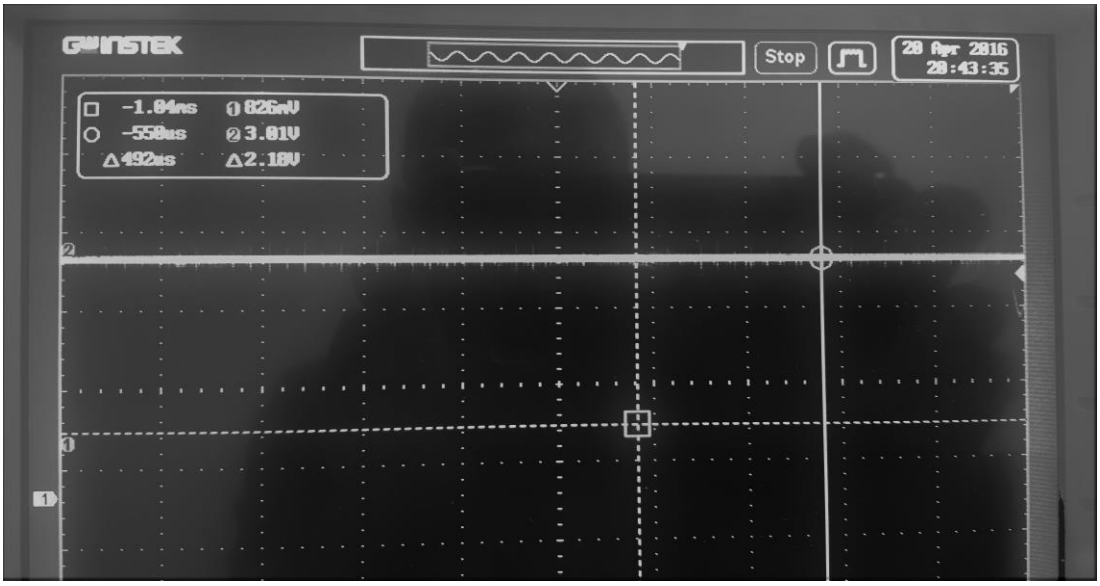


Figure 40: Full voltage output at 1MHz

After validating the converter control code and outputs at different operating regions and multiple duty cycle values, the implementation was expanded to utilize the dynamic voltage

control as well to control the output voltage provided by the converter. In order to do so, an ADC was developed on an ATmega chip which takes in the analog voltage provided at its input and then generates a continuous 10-bit logic vector representation of the analog value. This is the provided as the input to the FPGA, with the rest of the connectivity staying the same as in the first phase of implementation. As seen in figure 41, the generated output is measured to match the input, which in this case was the 3.3 Vin.

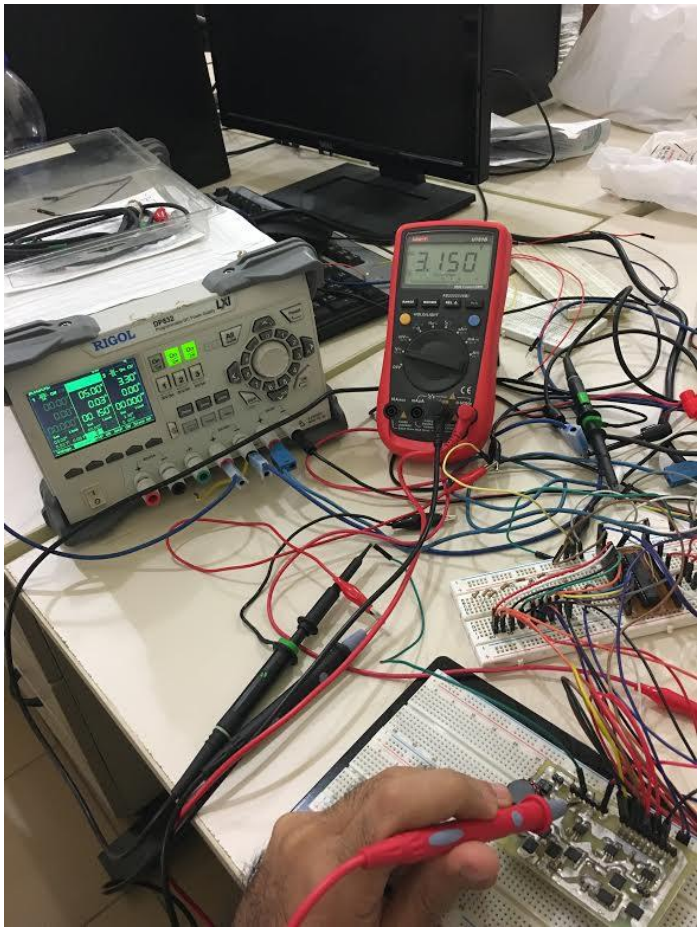


Figure 41: Measuring the voltage at the converter output vs the required voltage delivered to the ADC.

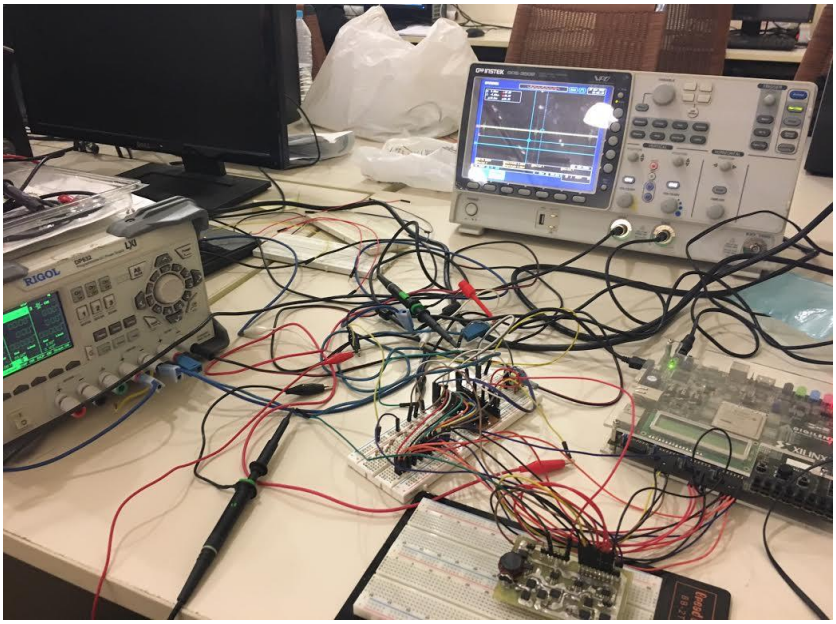


Figure 42: Full work station including ADC on the left, FPGA on the right and converter at the bottom

Utilizing the aforementioned structure, it is possible to examine the efficiency of the hybrid converter at various loads, through the usage of different load resistances at the converter output. It can be seen from figure 43 that the efficiency is higher the lower the resistive load, however even for an R= 32 ohms, the efficiency remains high for much of the voltage range and only decreases below 50% for low values of the output voltage.

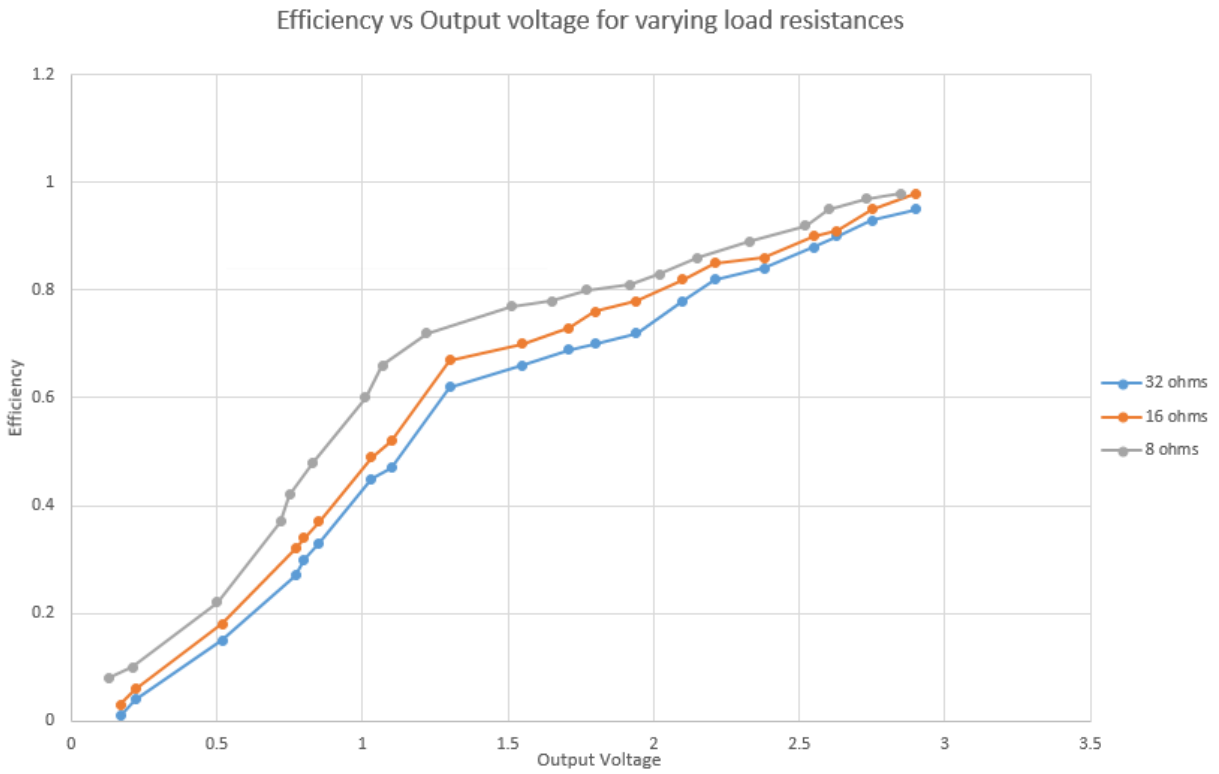


Figure 43: Efficiency vs Output voltage at load resistance = 32, 16 and 8 Ohms

Utilizing previously obtained values for efficiency at output voltage = 2.5V for both the 3-level and buck converter, and contrasting them against that of the FPGA controlled 5-level converter, it can be observed that the 5-level converter maintains an efficiency advantage over the load current range, though the advantage becomes less pronounced at higher load currents, where converters usually exhibit similar behavior.

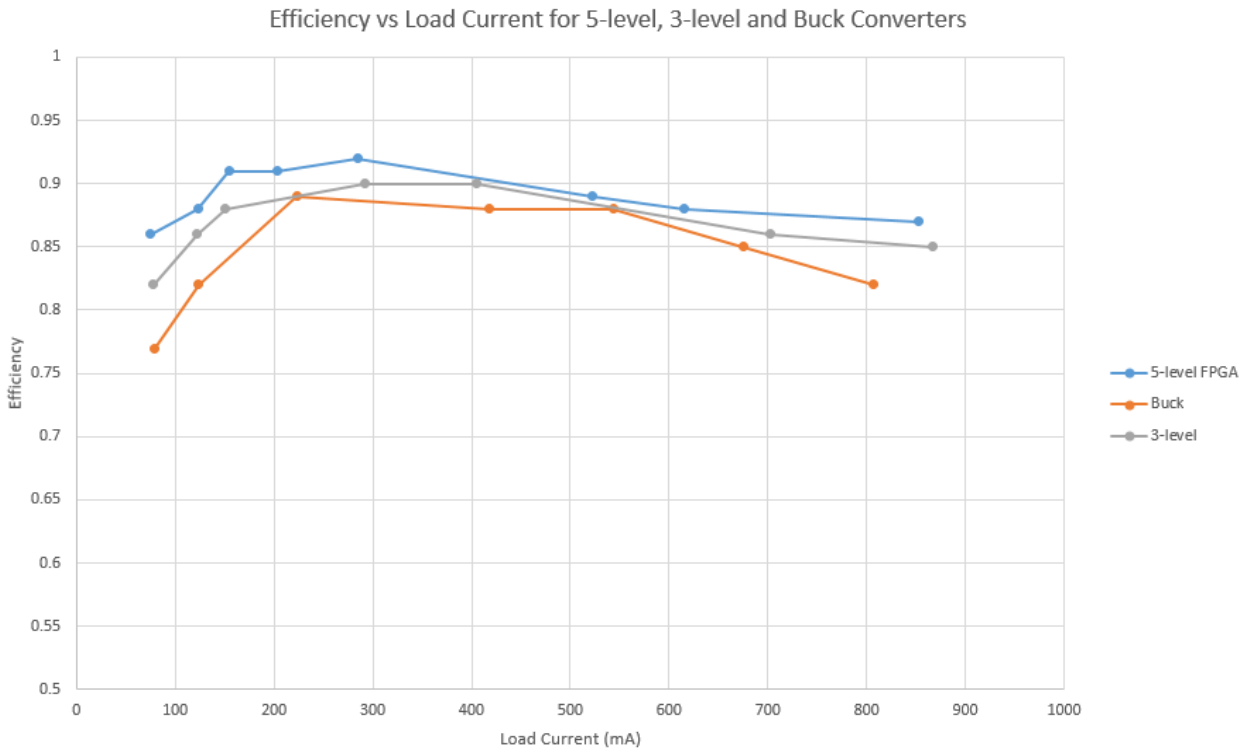


Figure 44: Calculated efficiency vs load currents at output voltage = 2.5 V for an input voltage of 3V

Finally, utilizing the efficiency figures of the microcontroller-controlled 5-level, the 3-level and the buck converter evaluated at load resistances of 32 ohm, the FPGA-controlled 5-level was compared to the aforementioned values. As can be seen in the figure 45, the FPGA-controlled one matches its microcontroller sibling or exceeds it for much of the output voltage range, especially closer to the upper limits of the voltage, where the improvement in efficiency can be as high as 5%. This is partially caused by the improvement in switching frequency which allows for lower current ripples, as well as the higher accuracy in controlling the converter switches. Both 5-levels also display better performance than the 3-level and buck converters, owing to the smaller current ripples for the same inductor size (50uH) utilized.

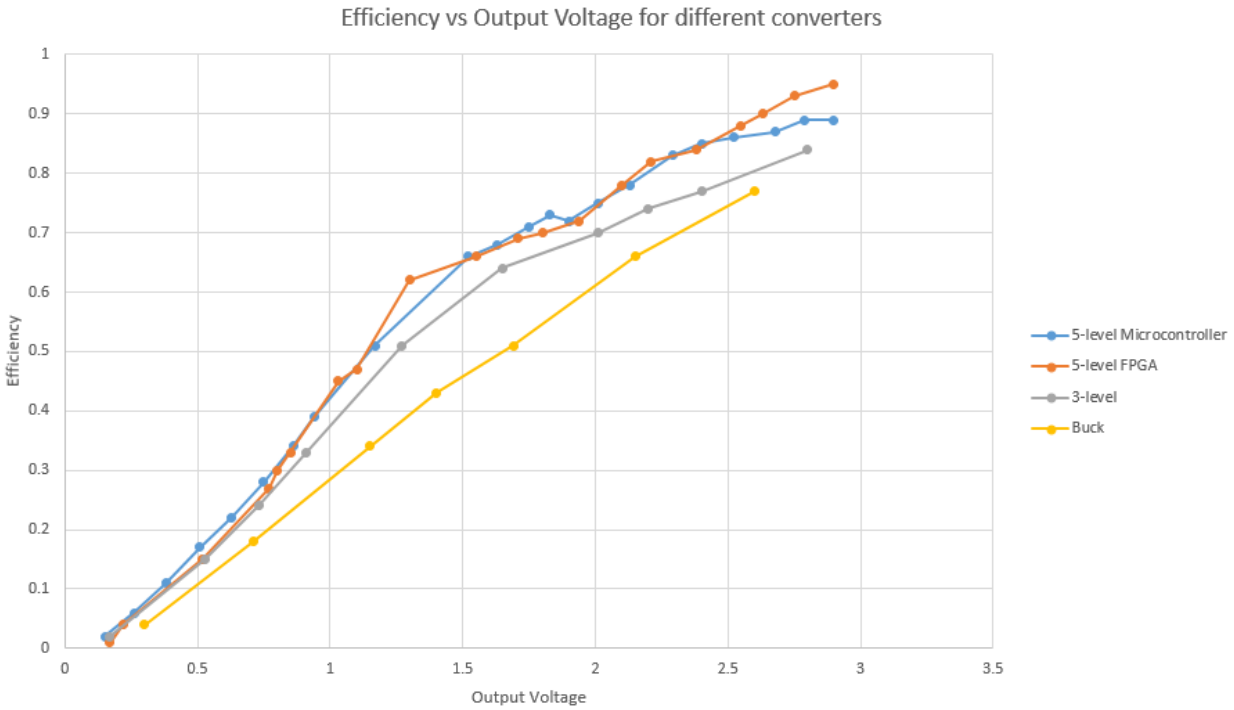


Figure 45: Efficiency vs Output voltage for the two 5-level converters, the 3-level hybrid converter and the buck converter, at load resistance of 32 ohms

# Chapter 6

## CONCLUSIONS AND FUTURE WORK

### 6.1 Conclusions

A new control methodology was utilized for the proposed and implemented 5-level hybrid converter, relying on an FPGA instead of a microcontroller to provide the necessary switching signals. This control methodology was simulated to guarantee the veracity of the developed code, and then implemented physically through programming a Virtex 5 FPGA and using it to control the converter. Furthermore, dynamic voltage control was added to the control scheme, with the code automatically choosing the duty cycle and operating region necessary to obtain the output voltage demanded by the used. This was also simulated and tested using the Virtex 5 FPGA. Obtained results confirmed that the FPGA control allowed for higher switching frequency and a reduction of the current ripples, enabling it to match or outperform the microcontroller-controlled hybrid converter, while consistently improving the efficiency in comparison to the buck and 3-level converter at the same inductor size and quality factor.

### 6.2 Future work

Future efforts in implementing the hybrid converter should explore different means of control, to be used in conjunction with or to replace the topology control and duty cycle modulation utilized in the 5-level design. Two of the most prominent and promising methods of control in DC-DC converters are pulse frequency modulation (PFM) and digital capacitance modulation (DCM). PFM relies on changing the switching frequency of the converter to maintain regulation within the converter, whereas DCM varies the capacitance taking part in the charge transfer [37].

PFM has already been implemented in [24] through the usage of a dynamic comparator and an automatic frequency block to adjust the switching frequency based on the needed output voltage. However, in wireless systems, existing alongside critical RF blocks makes PFM difficult to handle over a wide frequency range. DCM, on the other hand, relies on a fixed frequency, opting to instead vary the amount of flying capacitance based on the output voltage required. This is often done through dividing the used capacitance into banks of varying sizes and switching between them depending on what is required, which allows the designer to accurately predict switching losses and optimize accordingly to obtain the highest possible efficiency.

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