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RF MEMS reference oscillators platform for wireless communications

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RF MEMS Reference Oscillators Platform for Wireless Communications

A Thesis Submitted to

Electronics and Communications Engineering Department

in partial fulfillment of the requirements for

the degree of Master of Science

By Ali Essam Ali Kourani

Under the supervision of:

Prof. Yehea Ismail

Prof. Emad Hegazi

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The American University in Cairo

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Thesis Committee Supervisor _____
Affiliation _____

Thesis Committee Reader_____
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Dept. Chair /Director Date Dean Date

DEDICATION

To my beloved family, my dearest friend Ihsan, and the man who introduced me to Sufism Mr. Abdel-Aal

To every soldier sacrificed his life for a better Egypt

ACKNOWLEDGMENT

Praise be to Allah, Lord of the Worlds

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Also I have to thank my precious family, my father, and my mother for their endless prayers. God bless them and keep them safe.

In The Name of Allah, The Most Beneficent, The Most Merciful

ABSTRACT

OF THE THESIS OF

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A complete platform for RF MEMS reference oscillator is built to replace bulky quartz from mobile devices, thus reducing size and cost. The design targets LTE transceivers. A low phase noise 76.8 MHz reference oscillator is designed using material temperature compensated AlN-on-silicon resonator. The thesis proposes a system combining piezoelectric resonator with low loading CMOS cross coupled series resonance oscillator to reach state-of-the-art LTE phase noise specifications. The designed resonator is a two port fundamental width extensional mode resonator. The resonator characterized by high unloaded quality factor in vacuum is designed with low temperature coefficient of frequency (TCF) using SiO_2 as compensation material which enhances the TCF from -3000 ppm to 105 ppm across temperature ranges of -40˚C to 85˚C. By using a series resonant CMOS oscillator, phase noise of -123 dBc/Hz at 1 kHz, and -162 dBc/Hz at 1MHz offset is achieved. The oscillator's integrated RMS jitter is 106 fs (10 kHz–20 MHz), consuming 850 µA, with startup time is 250µs, achieving a Figure-of-merit (FOM) of 216 dB.

Electronic frequency compensation is presented to further enhance the frequency stability of the oscillator. Initial frequency offset of $\pm$8000 ppm and temperature drift errors are combined and further addressed electronically. A simple digital compensation circuitry generates a compensation word as an input to 21 bit MASH 1-1-1 sigma delta modulator incorporated in RF LTE fractional N-PLL for frequency compensation. Temperature is sensed using low power BJT band-gap front end circuitry with 12 bit temperature to digital converter characterized by a resolution of 0.075˚C. The smart temperature sensor consumes only 4.6 µA. 700 MHz band LTE signal proved to have the stringent phase noise and frequency resolution specifications among all LTE bands. For this band, the achieved jitter value is 1.29 ps and the output frequency stability is $\pm$0.5 ppm over temperature ranges from -40˚C to 85˚C. The system is built on 32nm CMOS technology using 1.8V IO devices.

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List of Abbreviations

3G	Third Generation
ADC	Analog to Digital Converter
AlN	Aluminum Nitride
AM	Amplitude Modulation
BAW	Bulk Acoustic wave
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor.
CP	Charge Pump
EDGE	Enhanced Data for GSM Evolution
EVM	Error Vector Magnitude
FBAR	Film Bulk Acoustic Resonator
FDC	Frequency to Digital Converter
FDD	Frequency Division Multiplexing
FOM	Figure of Merit
FPGA	Field programmable Gate Array
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile
HF	High Frequency
IC	Integrated Circuits
IOT	Internet of things
LFE	Lateral Field Excitement
LPF	Low Pass Filter
LTE	Long Term Evolution
LUT	Look Up Table
MEMS	Micro-Electro-Mechanical Systems
NEMS	Nano-Electro-Mechanical systems
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
PML	Perfectly Matched Layer
ppm	Part per million
PZT	Lead Zicronate Titanate
Q- factor	Quality factor
QPSK	Quadrature Phase Shift Keying
SAR	Successive Approximation Register
SAW	Surface Acoustic wave
SDM	Sigma Delta Modulator
SI	Stored Integer

SNR	Signal to Noise Ratio
SSB	Single side Band
TCF	Temperature coefficient of Frequency
TCMO	Temperature Compensated MEMS Oscillators
TCXO	Temperature Compensated Crystal Oscillators
TDC	Temperature to Digital Converter
TDD	Time Division Multiplexing
TED	Thermoelastic Damping
TFE	Thickness field Excitement
TIA	Trans-impedance Amplifier
TSV	Through silicon Via
UMTS	Universal Mobile Telecommunication System
UTRAN	Universal Terrestrial Radio Access Network
VCO	Voltage Control Oscillator
VLSI	Very Large System Integration
WCDMA	Wide Band Code Division Multiple Access
WI-FI	Wireless Fidelity
XO	Crystal Oscillator
ZnO	Zinc Oxide

1.Introduction

This chapter begins with an overview on MEMS market and applications, it further discuses the motivation behind the research. Design specifications are presented briefly, and at the end comparisons between electrical and mechanical resonators, quartz and MEMS resonators are highlighted.

1.1.MEMS Market Overview

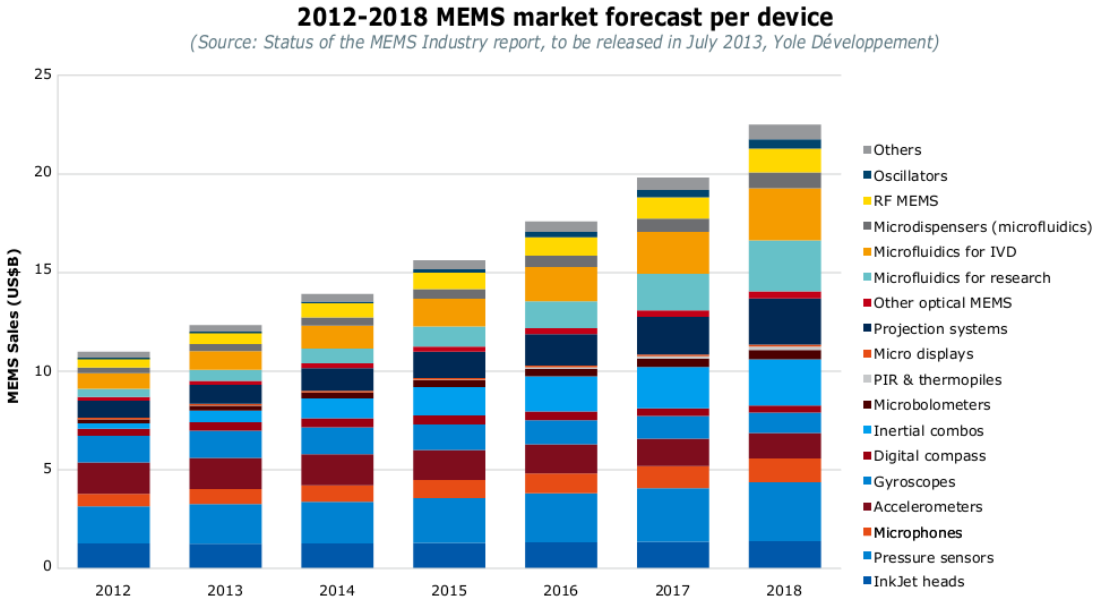

Figure 1-1: MEMS industry forecast [1]

Diverse MEMS products are produced to satisfy all consumer needs in many different applications from telecom to automobile industry, and medical applications. Every electronic device is now capable of interfering with the surroundings using billions of sensors to ease our fast paced life. These devices are no longer luxury, but they become

one of the basic needs for any consumer. Automobile industry is searching for more and more safety procedures thus pressure sensors for tires and accelerometers were developed. Small microphones and speakers made of MEMS can be implanted inside our bodies for hearing-aid medical applications. Compasses and gyroscopes are necessary for navigation. Smart phones nowadays include all these devices for better attachment of the consumer to the surrounding nature. Figure 1-1 shows MEMS market forecast focusing on the emerged devices while Figure 1-2 shows the forecast focusing on the applications.

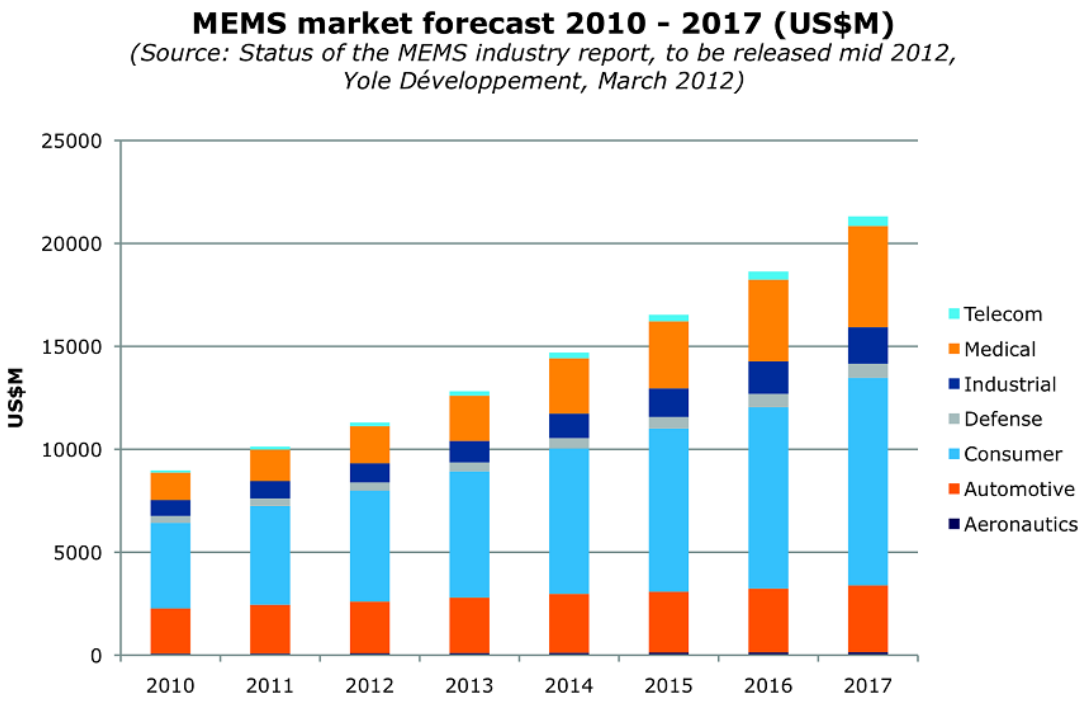

Figure 1-2: MEMS market forecast per application [2]

1.2.Motivation: The Wireless Market

Timing systems are found in most electronic parts due to its importance, where it relate time to any other electronic measurement like jitter, noise, and frequency resolution of a certain system. So it relates an analog nature kind signal to other parameters in electronic world. It can be deduced that these timing systems measure time

or frequency and should be in a very high accurate environment for sake of quality of electronic parts. Unfortunately those electronic devices are made of materials like silicon, germanium which have high temperature dependence. Thus it's not about timing only, but about other nature dependence which is temperature. To make it clearer, consider an example of wrist watch. The watch has to give the real time to the consumer very accurately and should not deviate from such accuracy over years, how that watch senses the real time, and how it's very accurate in order of part per million deviations over many years are the main needs for timing systems which have many figures of merits like frequency resolution, aging, noise. This will be dealt heavily through the thesis.

Reference oscillators are the heart beat of modern communication systems. For decades the quartz crystal has been used for precise frequency control in cellular applications which this thesis targets as an application [3, 4]. Researchers try to answer the question of the applicability of replacing bulky quartz with smaller MEMS resonators. MEMS resonators had successfully replaced quartz in low-end consumer electronic devices like cameras, PCs, TVs, and FPGAs. However the cellular market is still under research due to the stringent phase noise, frequency and temperature stability specifications needed to be achieved by the MEMS reference oscillator; so the question is rather wireless than timing, and rather cellular than IOT wireless applications.

Lately cell phones have become smart, they include mini computers inside that allow browsing the internet, playing games, watching videos, TV, taking photos and videos with very high quality cameras. So a smart phone nowadays include all the trendy, sophisticated features needed by the consumer, whether business man, student, kid. Miniaturization is a high priority in today's smart phones. A single handset has to satisfy the requirements of multiple wireless standards. To name a few, WI-FI, GPS, Bluetooth, GSM and 3G data service are now a base requirement. Each of which needs a reference oscillator and many bulky RF filters. It is increasingly difficult to continue with this large number of off-chip components from form factor and cost perspectives. One of the main bulky components in any electronic system is the quartz crystal resonators, their reluctance to get smaller due to fragility and ruggedness issues drag researcher's attention

to replace it with smaller MEMS resonators. The thesis tries to build a new platform for MEMS based reference oscillators targeting LTE specifications, such replacement will decrease the cost, and the form factor. Solutions are proposed to address few challenges to enhance MEMS resonators temperature and frequency stability and to be comparable to superior Quartz stability performance.

1.3. Cell Phone Standards

The term "3GPP specification" [5] covers all GSM (including GPRS and EDGE), WCDMA and LTE (including LTE-Advanced) specifications. The following terms are also used to describe networks using 3G specifications: UTRAN, UMTS (in Europe) and FOMA (in Japan). Add to this, smart phone serves now GPS and WIFI technologies. These standards have created a burden on all mobile phone companies to satisfy their specifications. The more standards, the more features, the more willing to attract consumers and the more profit, and of course the bigger the challenge for design.

1.4. Reference Oscillators Performance Metrics

1.4.1. Frequency stability

In the increasingly popular field of wireless communications, available frequency spectrum is becoming very limited. Regulatory agencies have imposed tight restrictions on the bandwidth and frequency stability [4]. These requirements vary throughout the spectrum in accordance with the intended applications. Factors affecting the frequency stability of an oscillator include variations in voltage, time, and temperature.

Specifications for frequency stability are expressed as the amount of the divergence from the nominal operating frequency, usually in terms of a percentage or in parts per million (ppm).

AM radio stations must have a carrier frequency accurate within 10Hz of its assigned frequency. SSB radio systems used in the HF range (2-30 MHz) must be within 50 Hz of channel frequency for acceptable voice quality, and within 10 Hz for best results. An ordinary quartz watch must have an oscillator accurate to better than a few parts per million. One part per million will result in an error of slightly less than one half second a day, which would be about three minutes a year. This might not sound like much, but an error of 10 ppm would result in an error of about a half an hour per year. [4]

1.4.2. Non-deterministic frequency stability: Phase noise

The frequency spectrum of an oscillator should ideally contain only a single frequency. In reality, the frequency of any oscillator shows short-term frequency fluctuation and hence a broadening of the frequency spectrum. Phase Noise, often given the symbol $\mathcal{L}(f_m)$. It is the ratio of the power in 1Hz bandwidth, a frequency f_m away from the carrier, to the power in the carrier itself. To convert it to dBc/Hz, we use $10\ log_{10}\mathcal{L}(f_m)$.

Oscillator phase noise originates from flicker noise, white noise and other non-deterministic noise sources that are present in the oscillator loop [3]; Noise of the oscillator's wave front can be decomposed into amplitude noise which can be easily filtered out in the oscillator loop and phase noise that cannot be filtered out, making phase noise an important performance indicator for any oscillator. An important FOM in this context is the Q of the resonator that filters out the noise. High Q-factors results in narrow band filtering of the oscillator noise and are critical for low phase noise output. Mechanical resonators exhibit very high Q-factors up to several million, while LC-based filters show a Q-factor of about 10 and R–C or gm–C filters show a Q of less than 1 [3]. For digital systems, the oscillator noise is specified in terms of jitter. Jitter is the integration of an application-specific frequency band of the phase noise spectrum. Leeson [6] was the first to describe the effect of the oscillator's active and passive components

on the phase noise, based on a linear time-invariant model. Leeson phase noise can be given in the Equation 1.1.

$$\mathcal{L}(f_m) = \left(\frac{kTF}{2P_o}\right)\left(\frac{1}{4{Q_{loaded}}^2}\left(\frac{f_s}{f_m}\right)^2 + 1\right) \tag{1.1}$$

Where F represents the noise figure of the amplifier, k is Boltzmann's constant, T the absolute temperature, $f_m$is the offset frequency from the carrier frequencyf_s, $Q_{loaded}$is the loaded quality factor of the resonator and $P_o$is the carrier frequency power.

As shown in Equation 1.1, Leeson model only explains the $1/f^2$ roll-off and does not explain the additional $1/f^3$ roll-off that is observed in practical oscillators. An improvement over the cyclo-stationary Leeson's model is the cyclo-instationary Lee–Hajimiri model [7, 8]; where noise injection's time variant aspects into the oscillator loop are considered. Although the general form of Equation 1.1 is maintained in the Lee–Hajimiri model, an additional term is added describing the $1/f^3$ roll-off. The $1/f^3$ term is due to the up-conversion of flicker noise as shown in Equation 1.2, where f_c is the flicker corner.

$$\mathcal{L}(f_m) = \left(\frac{kTF}{2P_o}\right)\left(1 + \frac{f_c}{f_m}\right)\left(\frac{1}{4{Q_{loaded}}^2}\left(\frac{f_s}{f_m}\right)^2 + 1\right) \tag{1.2}$$

Both models are linear; they assume that the resonator impedance is independent on the magnitude of the signal that is transmitted through it. However, loop gain has to be nonlinear in order to have finite oscillation amplitude after oscillation start-up. Nonlinearities in both resonator and oscillator usually lead to flicker up-conversion.

1.4.3. Frequency continuity

Intrinsic Eigen modes and mechanical stresses result in multiple spurious modes that approach and in many cases cross the fundamental frequency resulting in static popping

or activity dips [9], both of which impact performance. Quartz manufacturers add manufacturing cost by attempting to pre-stress and pre-screen for devices with activity dips or static popping. However in reality, after reflowing quartz during assembly, spurious modes that caused activity dips or static popping can move. Contour mode MEMS resonators geometries are finely defined and controlled using photolithographic techniques unlike quartz that uses thickness shear mode as fundamental mode [4]. Poor temperature stability can lead to activity dips which result in dropped packets, loss of GPS lock, and cellular signal errors. Spur control and different resonance modes will be discussed in the chapter 2.

1.4.4. Power dissipation

Consumers always set restrictions on power consumption. However, a certain amount of power is required to generate sufficient gain in the oscillator loop in order to sustain the oscillation. Moreover, the signal power should be large enough to have a large SNR and hence low phase noise. Power consumption increases with the resonance frequency.

Other metrics include resonance frequency, startup time, aging, cost, and ruggedness.

1.5. Resonators

A resonator is simply a system that has selective response (sharp peaking action) at a specific frequency. Such behavior is called resonance and the frequencies at which they occur are called resonant frequencies. This behavior may vary from one resonance frequency to another depending on many parameters such as, the principle of operation, geometry, material properties and the type of the resonator itself.

1.5.1. Electrical and Mechanical Resonators

Resonator can have different shapes, domains and features [3]. For Example, mechanical, electric, electromagnetic, acoustic, optical and even molecular resonators are available nowadays. Thus the domain can differ however the same principle abide. To make it clearer, mechanical resonators have the resonance property at resonant frequencies by applying a mechanical force, and produce a mechanical movement in sort of vibrations which are related to certain frequency and speed. On the other hand, electrical resonators depend on the applying voltage or current to have that selective property; moreover, optical ones are excited with light. So the excitement itself differs which is termed as "transduction system" but the results are the same. Figure 1-3 shows the different characteristics of both mechanical and electrical resonators. Electromechanical resonators are another type of resonators, in which actuation and sensing are done in the electrical domain while resonance occurs in the mechanical domain thus combining both the electrical and mechanical resonators in one device. These instruments can be the famous quartz crystal resonators, SAW resonators, BAW and ceramic resonators; which have been widely used with a long history in a wide range of applications from wrist watches to communication systems. The extremely accurate frequency resolution fashion of these parts have guaranteed the design of ultra low-noise oscillators for the high quality and accurate frequency references necessary for wireless communication circuits as well as for almost any synchronous digital circuits such as microcontrollers and processors. Add to that, specific technology helped greatly in designing the high quality filters in the radio front-end [10], which can be found in billions of cell phones worldwide.

After reviewing the advantages of these parts, the disadvantages are questionable. It is mainly one drawback, these micromechanical resonators are not easily integrated on chip with the conventional IC using the well standard CMOS processes, because of using different materials rather than silicon. Silicon is now leading the CMOS cheep manufacturing process. Thus the incompatibility of the new resonator's materials and the technology involved with manufacturing conventional resonators differs from the main stream of VLSI.

In most cases, resonators finally need to be interfaced with ICs, and due to its incompatibility, the connections have to be made off-chip on same package [3]. These external connections are very far from ideal, resulting in many parasitic from the bond wire inductance and the bond pads large capacitances. This will deeply vary the circuit performance, from the operating frequency and resolution. The big deal about integrating resonators in ICs is crucial for cost and size of the die. This will become critical in hand held applications like cell phones, laptops and GPS systems.

Resonator technology	Accuracy df/f_0 (ppm)	Noise FoM_2	Size L x W x H (mm)	System integration
mechanical	<10	~130	>1.6x1.2x0.35	•Bulky hermetic package •Non-CMOS compatible
electrical	>100	~90	<0.5x0.5X0	•Standard plastic package •CMOS design

Figure 1-3: Mechanical and electrical resonators [3]

1.5.2. Quartz versus MEMS resonators

AT-cut quartz oscillators were traditionally used as a high precision frequency source. Figure 1-4 shows the orientations and cuts used in industry. AT-cut is the best for MHz resonance frequency and least TCF [4]. First order temperature compensated quartz resonators, result in roughly 10 ppm of frequency shift over the temperature range from -40˚C to 85˚C. Hermetic packaged high Q quartz insures low close-in phase noise. The tens of ohms range of motional arm resistance made quartz the de facto choice for low power frequency references. Recent papers studied GHz MEMS frequency references [11-13]. Such high frequencies are not reachable using today's fragile thickness shear mode quartz due to resilience and ruggedness issues.

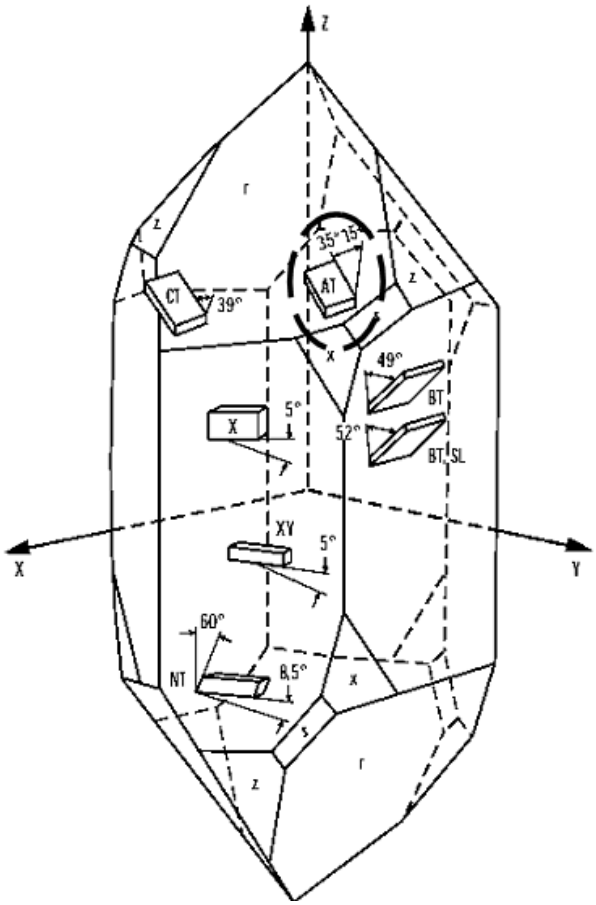

Figure 1-4: Quartz orientation and cuts

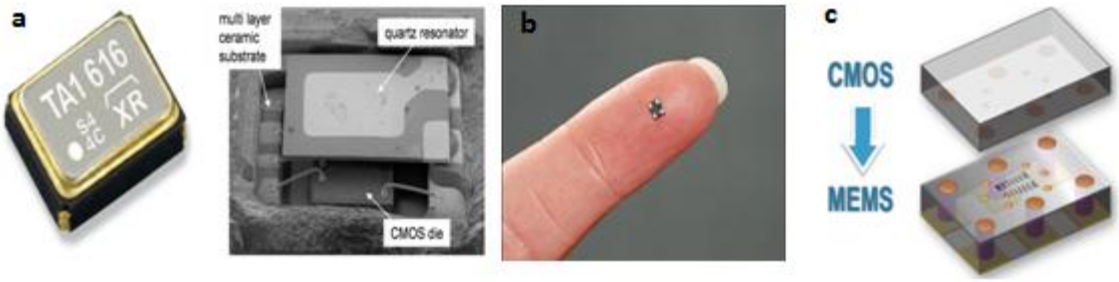

Figure 1-5: (a) bulky crystal resonator in hermetic package [3]. (b) MEMS resonator. (c) TSV used in MEMS-CMOS dies packaging.

The need for decreasing the cost and the form factor is what drive the MEMS market in many applications especially the cell phones, and tablets market in addition to biomedical implantable devices. Processing on large substrate size (8 inches or above), reducing the resonator size as well as the ability to perform zero-level or wafer-level packaging to

yield vacuum-sealed devices are key for lower cost target; this is the only reason for replacing quartz with silicon. With sub-mm dies, above one million units are obtained with a single wafer lot, calling for large volume applications.

Table 1-1: Quartz and MEMS comparison

P.O.C	Quartz resonators	MEMS resonators
Transduction	Piezoelectric	• Piezoelectric • Electrostatic • Others
Resonance mode	Shear thickness	Many modes: • contour mode • thickness extensional • flexural • shear
Cost	High	Low
Size	Large	Small
Temperature stability	Better due to the low TCF AT-cut orientation	Worse
Q	Very high	Depends on transduction type but generally less than Quartz
Package	Off chip - Hermitic sealed in vacuum	Can be on CMOS die, or in SIP solutions
Resonance frequency	• Maximum 40 MHz for fundamental mode • 200 MHz (inverted- Mesa resonators) but very expensive	Can reach GHz fundamental resonance frequencies

Figure 1-5 compares crystal to MEMS sizes; Table 1-1 summarizes the comparison between MEMS and crystal resonators. While Figure 1-6 shows how MEMS were further developed to NEMS for sake of miniaturization and cost reduction and to target new markets like THz and photonics area. It should be mentioned that power consumption is directly proportional to the resonator's thickness.

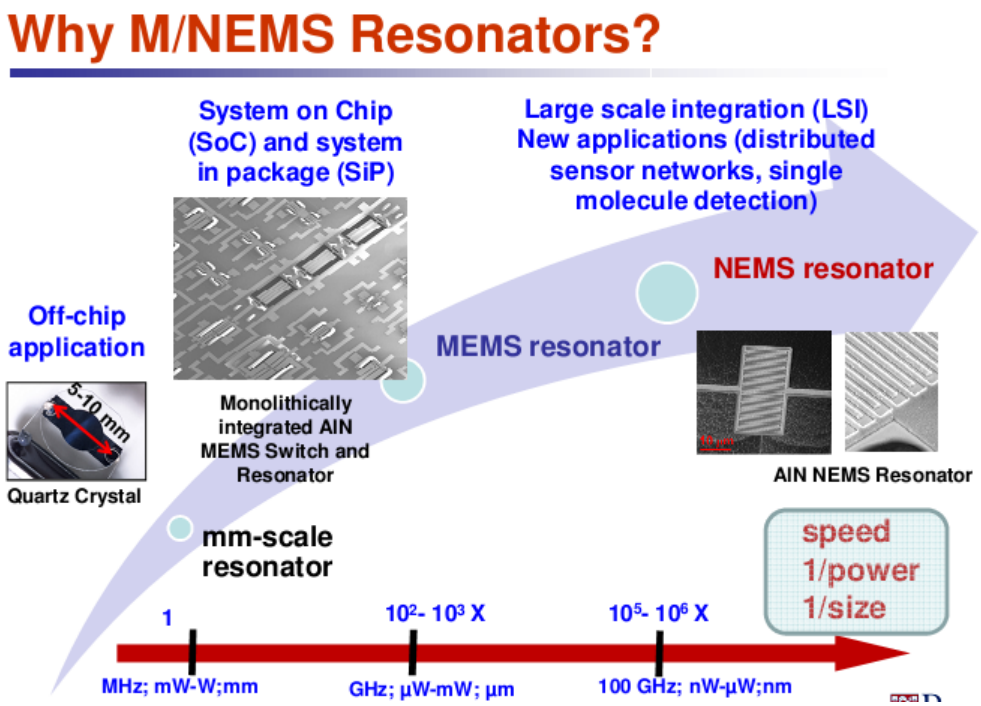

Figure 1-6: speed, power and size as MEMS advances to NEMS [14]

1.6.Problem Statement

MEMS resonator's center frequency is determined by its physical characteristics, settled by materials, design and the fabrication processing. In order to reach < 1ppm level of initial accuracy, laser trimming is used. Trimming add to fabrication complexity and cost; making it highly desirable to find an alternative for achieving high reference accuracy that doesn't require complex trimming. Initial frequency offset due to process variation is estimated around ±8000 ppm and the native MEMS resonator's TCF is around -31 ppm/˚C which results in more than 4000 ppm deviation across the industrial temperature range (-40˚C to 85˚C) [3, 15]. These errors affect the needed frequency resolution from the reference oscillators. Unfortunately, the maximum allowable temperature variation is 0.02 to 1 ppm/˚C for LTE applications. Figure 1-7 compares the TCF of different resonators in the industry. This deviation is unacceptable for cellular applications; Thus temperature compensation becomes of great importance for MEMS reference oscillators.

Material compensation sandwiches a material of a positive TCF, such as Silicon dioxide (SiO_2) in the resonator's stack to mitigate the negative TCF at the resonant frequency. This method is simple to adopt and has the advantage of minimal power consumption; however zero TCF resonators require very thick layers of the silicon dioxide that adversely affects the quality factor of the resonator and thus worsen the close-in phase noise specification. On the contrary, Electronic compensation has the minimal impact on Q, yet needs a large frequency tuning range of 1000 ppm which is beyond the reach of most analog electronic frequency tuning techniques; making analog compensation techniques power hungry. Digital compensation is favorable in this case to save power and for sake of better frequency resolution. State-of-the-resonators use a combination of material and electronic compensation [3]. To sum it up, this work simply answers the question "can we make cellular ICs crystal free?" by replacing the conventional bulky XO with TCMO. Figure 1-8 presents a spider chart for TCXO's and TCMO's performance per design metric, far away lines from center means better performance.

1.7. Thesis Organization

The following chapters will address the complete timing system for LTE reference oscillators. Chapter two deals with MEMS modeling, introduces the main terminology associated with the resonators, and presents the material temperature compensation. Chapter three deals with the active oscillator part. Figures like FOM, phase noise, and power consumption will be revised again. Chapter four introduces the system and the circiut level implementation of the smart temperature sensor. Chapter five is concerned with the temperature compensation system and LTE frequency synthesizer.

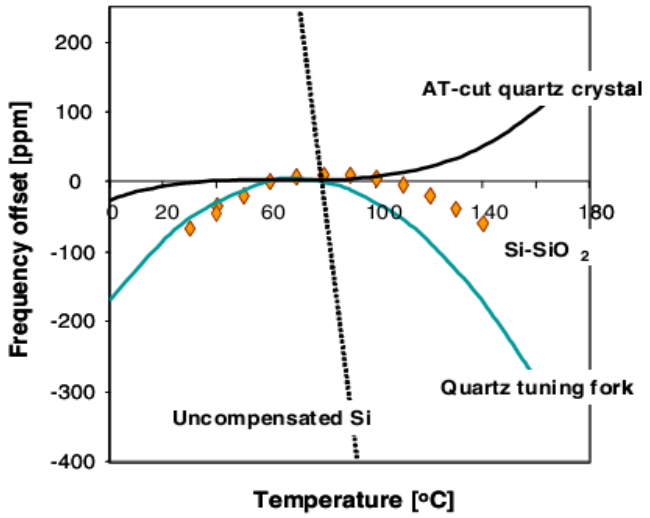

Figure 1-7: TCF of different materials [3]

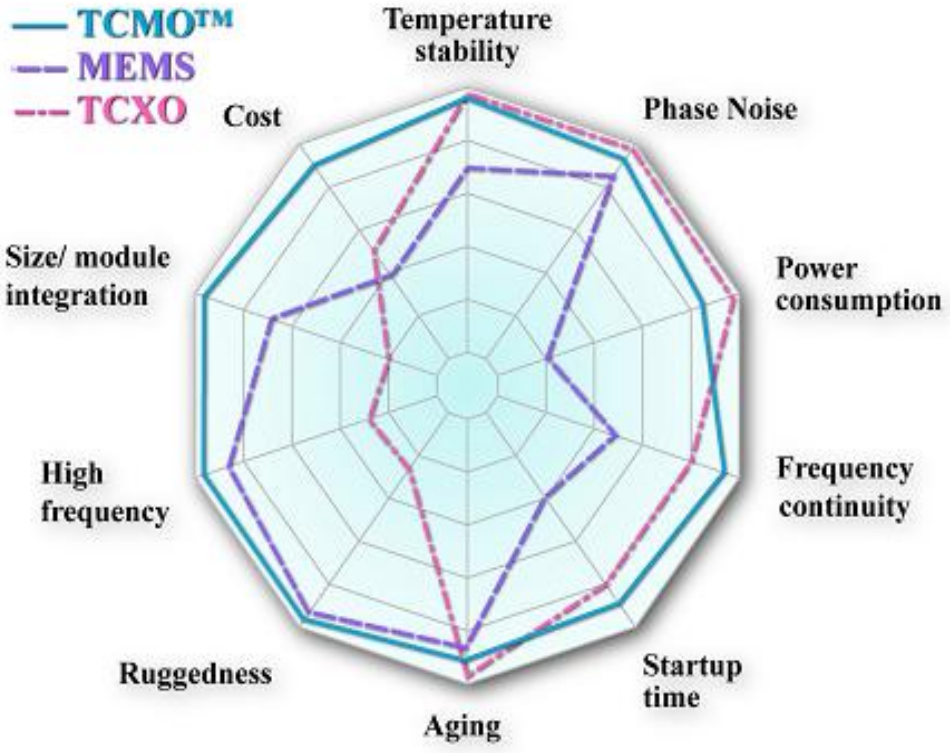

Figure 1-8: Design metrics and for TCXO and TCMO [15]

2.MEMS Resonators

In this chapter the design of MEMS resonators is presented in detail, concepts from energy transduction and the physics behind resonance is presented. A detailed mechanical design approach is introduced taking into account the resonator's damping. A fruitful study of damping and Q- factor is presented for accurate modeling. Material temperature compensation is presented in this chapter to enhance the frequency stability of the resonator. Different concepts from resonance modes, series and parallel resonance, and material choice are highlighted throughout the coming pages. Finally performance optimization study is conducted to account for effects of various parameters on resonator's performance.

2.1.Transduction

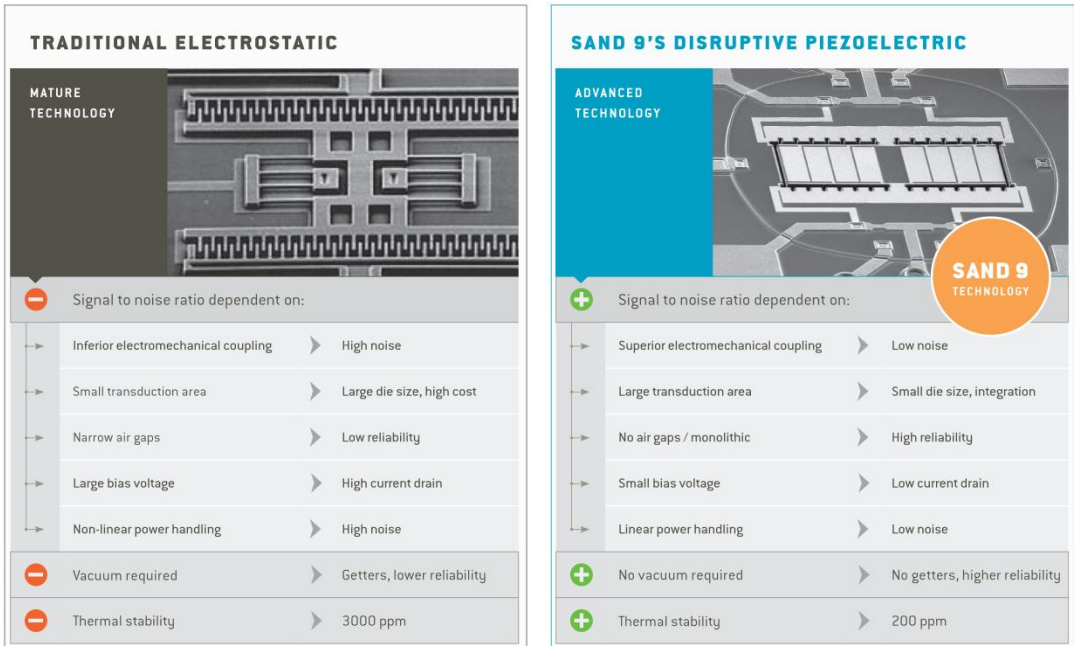

Figure 2-1 : electrostatic versus piezoelectric transductions [16]

Transduction is sort of conversion. Transducers convert one form of energy into another. It can be from kinetic to electric energy like in dynamo or from electric to thermal energy as in heater coils. Micromechanical resonators sense voltages and currents (electrical energy) and convert them to vibrations (mechanical energy) of amplitude resembling the electrical voltage and velocity resembling the electrical current

There are many types of transduction mechanisms, varying from piezoelectricity, to electrostatic, thermal and resistive. The most famous are the first two, due to their high accuracy in sensing. However they totally differ in applications and the resonator's material differs.

Piezoelectricity [17] is the ability of some materials to generate an electric charge in response to an applied mechanical stress. It is an anisotropic property that depends on direction of forces. It is a reversible process, which can be of direct effect involving charge separation due to stress applied as shown in Equation 2.1; and can be of reverse effect involving stress and strain generation when electric field is applied as given in Equation 2.2. To build a timing device, the reverse aspect is used. When the voltage is removed, the crystal relaxes and returns to original size. The two equations are listed below

$$D=e^{T}E+dT \tag{2.1}$$

$$S=s^{E}T+dE \tag{2.2}$$

D is the displacement electric field, e is the permittivity, E is the electric field, S is strain, s is compliance, d is the piezoelectric coefficient and T is stress. In these materials, there is a linear relation between D and strain/stress.

High Q conventional frequency capacitive resonators were reported in the past [18-22]. However, they exhibit high loss which is modeled by a large motional resistance in the range of kilo ohms, high DC polarization voltages for VHF and UHF ranges, and inferior mechanical coupling which results in high output phase noise floor [18,19]. Ultra-thin electrode-to-resonator gap spacing is required for a motional resistance of 1 kΩ [23]; this sets additional restrictions on the fabrication process and the oscillator's power

consumption. On the other hand, piezoelectric *AlN*-on-silicon resonators [23-27] offer a compromised solution for LTE applications, due to *AlN*'s high acoustic velocity (~10,000 m/s), small motional resistance, and its CMOS compatibility. A comparison between both transductions is summarized in Figure 2-1. Generally piezoelectric resonators can be fabricated easily using low temperature processes [23]. Albeit MEMS resonators have inferior unloaded Q compared to quartz crystal counterparts; their circuit loaded Q is not as inferior.

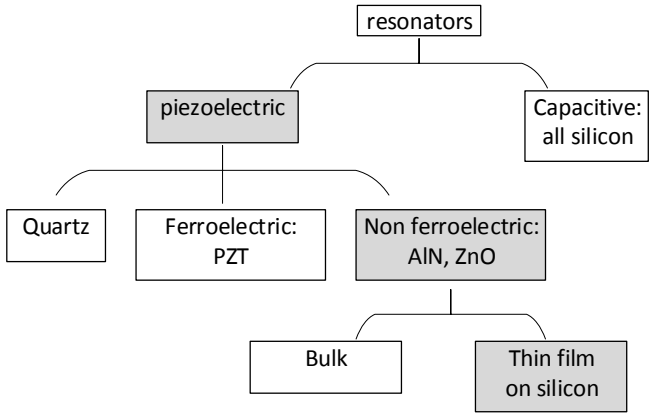

Figure 2-2: MEMS resonator classifications

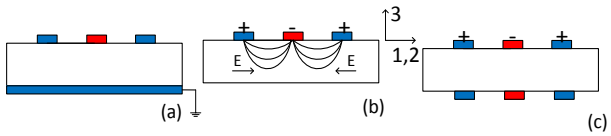

Figure 2-3: (a) Unpatterned bottom electrode thickness field excited (TFE) resonator (b) Lateral field excited (LFE) resonator (b) patterned bottom electrode TFE resonator

Figure 2-2 classifies the different resonators according to their transduction mechanism and materials. Thin film piezoelectric materials are characterized by their polar axes as shown in Figure 2-3, where 3 is the out-plane index, 1 and 2 are the in-plane indices which are equivalent in polycrystalline films ($d_{31}$and d_{32} are the same). However quartz has no polar axis, making it only useful in single crystalline form leading to its incompatibility with CMOS integration [17].

According to the above, d_{33} as an example translates the piezoelectric response in the out-of-plane direction or thickness vibration in the film. In MEMS technology, most of thin piezoelectric films are made of polycrystalline materials such as *AlN*, and *ZnO* where the piezoelectric effect is averaged over all the grains.

Ferroelectricity is a property of certain materials that have a spontaneous electric polarization which can be reversed by applying external electric field. Non-ferroelectric polar materials like *AlN* and *ZnO* do not allow reorientation of the polar axis, thus alignment of the polar directions is a concern through material growth process. In ferroelectric materials like *PZT*, polar axis can be reoriented using electric field leading to higher piezoelectric response than their counterparts; however they show incompatibility for microelectronic integration [17].
The difference between bulk [28] and thin film materials [23-27] shown in Figure 2-2 classification is that thin film materials are used in composite structures, where the elastic properties are often dominated by the thicker substrate. In composite structures, most of the acoustic energy is stored in a low acoustic loss material like silicon, thus boosting the resonator's Q which is essential for oscillator's low phase noise [24].

SAW resonators and thin FBARs are examples of piezoelectric resonators. Typical SAW devices are bulky and incompatible with microelectronic integration in contrast to FBARs that can be integrated with on-chip electronics [23]. FBARs showed Q up to 2000 at GHz frequencies, they utilize thickness vibration mode, where center frequencies can be moderately controlled by selective deposition of metal films. However, obtaining higher Q and multiple dispersed frequency standards on single substrate is challenging using these devices because of the different resonator thicknesses needed for different frequencies generated on single substrate.

Figure 2-3 shows two ways of exciting the resonator with AC voltage. The first way is the TFE using a bottom electrode leading to more confined energy inside the device, this device is characterized by higher coupling coefficient η and lower parasitic components when compared to LFE resonator, where the bottom electrode is removed; as a result, the

electric field has a laterally distributed component which is different from TFE ones whose electrical field is mainly in the thickness direction [12]. Device in Figure 2-3c needs a very accurate manufacturing process, and mask fabrication due to the presence of the patterned lower electrode which complicates the device. As a result, the designed resonators in this thesis are in the configuration shown in Figure 2-3a.

2.2.Damping Study

The most prevailing energy loss mechanisms controlling the resonator's Q can be summarized to Thermo-elastic damping Q_{TED}, anchor losses Q_{anc}, air damping Q_{air}, and intrinsic material losses Q_{MAT} [29]; where the total Q is given in Equation 2.3. In this work, all resonators are designed in vacuum, so air damping is minimized.

$$\frac{1}{Q_{total}} = \frac{1}{QTED} + \frac{1}{Qanc} + \frac{1}{Q_{air}} + \frac{1}{Q_{material}} \tag{2.3}$$

Internal damping studies from material damping (phonon-phonon) and thermoelasticity (TED) are crucial for accurate resonator modeling [30-38]. Strain in solids leads to phonon movement from hot compressed parts to cold tensile parts, however to get the resonator in vibration, energy must be provided leading to non equilibrium state with excess of energy, and thus entropy generation is a must to reach equilibrium back. If entropy increases due to irreversibility of phonon relaxation, the loss is known as Akhieser phonon-phonon (AKE); while if the generation is due to heat conduction, it is TED loss [24].

AKE phonon-phonon damping is the prevailing loss mechanism for MHz range resonators and the main limiter for the intrinsic Q [31]. At 76.8 MHz, the wavelength is larger than the mean free path of phonons ($\omega\tau \ll 1$). AKE dissipation factor (α_{AKE}) stated in Equation 2.4 is calculated for both *AlN* coupling loss [33, 34], and Si structural loss [30], [32], and are shown in Figures 2-4, and 2-5 respectively. It can be noted that for both materials, the damping decreases with the temperature. The constants in equations 2.4 and 2.5 are taken from [32, 33].

$$\alpha_{AKE} = \frac{C_v\, T\gamma^2\tau}{2\rho V^3(1+(\omega\tau)^2)}\,\omega^2 \tag{2.4}$$

$$Q_{AKE} = \frac{\pi\,\omega}{\alpha_{AKE}\,V} \tag{2.5}$$

where C_v is the volumetric heat capacity, T is temperature, ρ is the density, τ is the phonon relaxation constant, ω is the angular frequency, γ is the Grüneisen parameter, and V is the acoustic velocity.

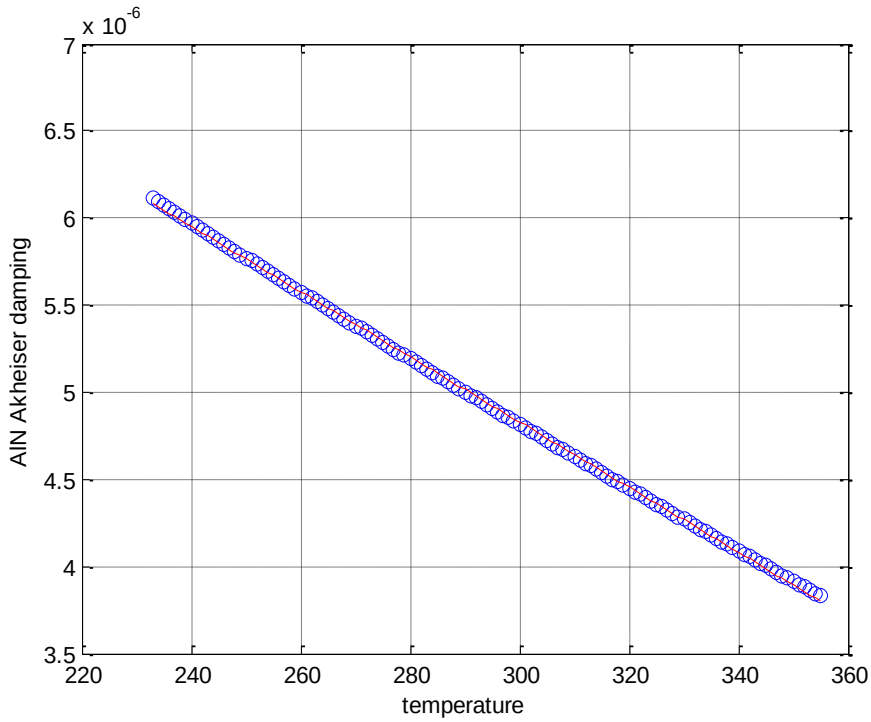

Figure 2-4: AlN coupling loss

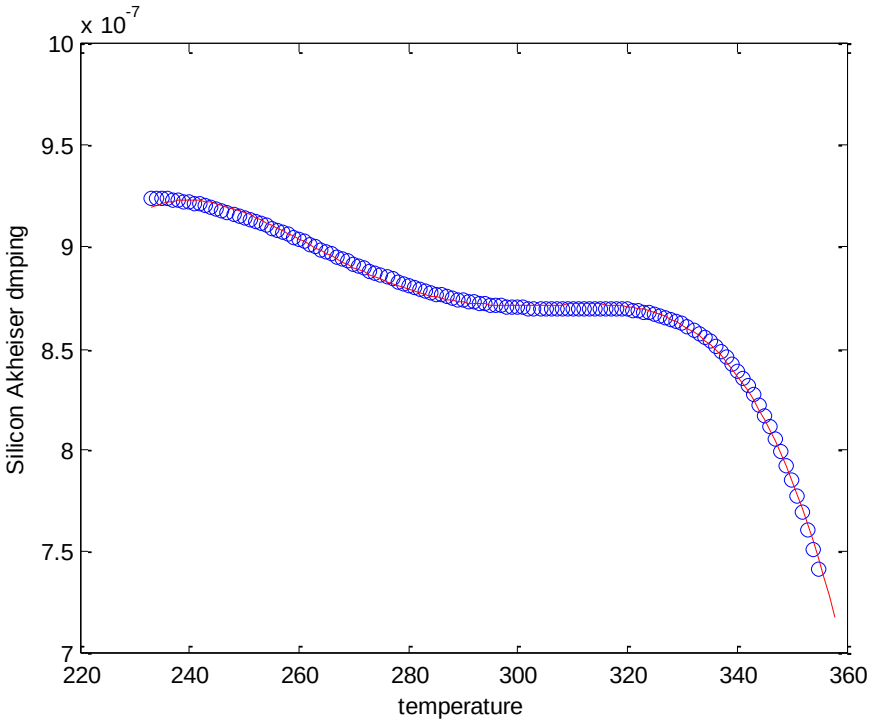

Figure 2-5: Silicon structural loss factor

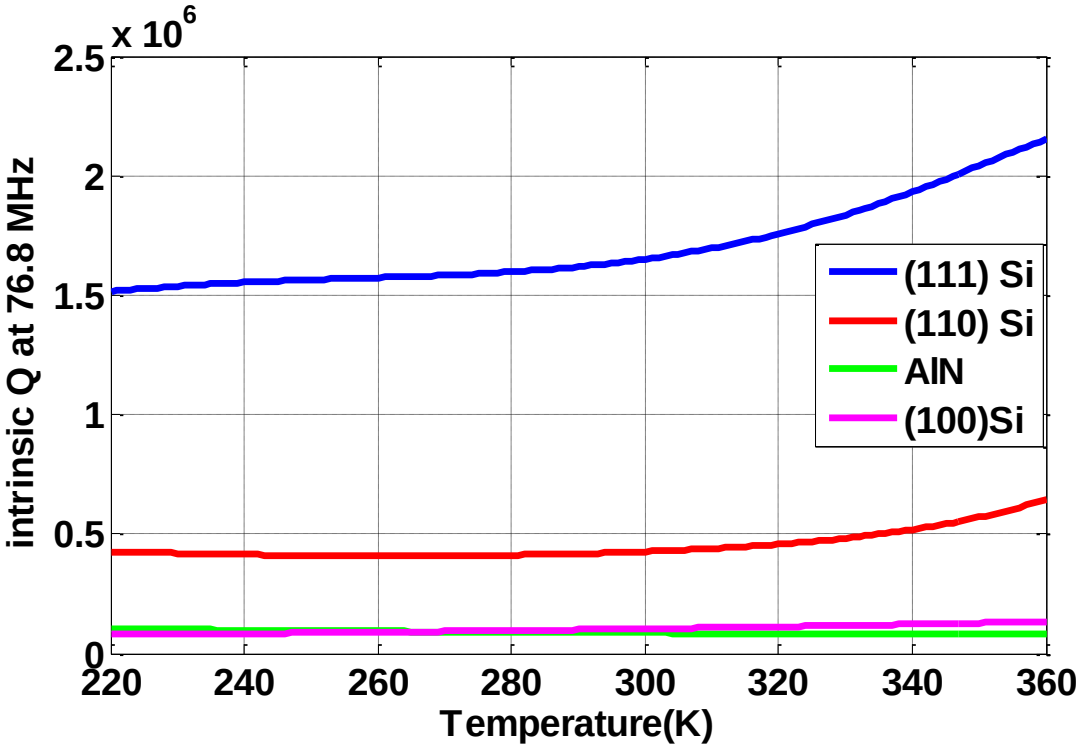

Figure 2-6: Intrinsic Q at 76.8 MHz as result of AKE damping

For SiO_2 the structural loss factor α_{AKE} is assumed to be of 0.0002, while Al electrodes structure loss factor is 0.00057. Q_{AKE} is stated in Equation 2.5, and is shown for different materials in Figure 2-6.

On the other hand, TED [36, 37] is induced through dissipative thermal currents as a result of mechanical strains. These strains in extensional mode resonators are small due to the very small in-plane displacement. Therefore, TED is not the main Q limiter [29]. This loss depends on the mechanical vibration frequency, mode and the thermal relaxation time constant of the structure, and it is notable when the thermal time constant is of the same order as the vibration period [36].

Support losses (anchor losses) [13],[29],[39-43] are modeled using perfectly matched layer (PML), (bluish part in Figure 2-7) which is a virtual layer that absorbs all the energy passing through it from tether to substrate, preventing the waves from returning back to the device, and thus allow loosing energy to surroundings [13]. Devices should be anchored at the minimum displacement points in order not to affect the motion [11]; more tethers can be added between the electrode fingers for further spur reduction.

Quarter wave tethers are used in our study. Optimum tether is of length=$\lambda/4$ =35 μm. A study shown in Fig.2-8 is made by changing the lengths and widths of the tether to prove the validation of our selection. Thinner tether shows better spur suppression and lower R_m value when compared to the wider one. Wide tethers allow more energy escape to the substrate. Results for $\boldsymbol{\lambda}$/8 in Fig.2-8b show closer spurs to the target frequency when compared to $\boldsymbol{\lambda}$/16 and $\boldsymbol{\lambda}$/4 tethers. $\boldsymbol{\lambda}$/4 tethers (Fig.2-8c) provide the best spur suppression and the lowest R_m value with width of 10 μm.

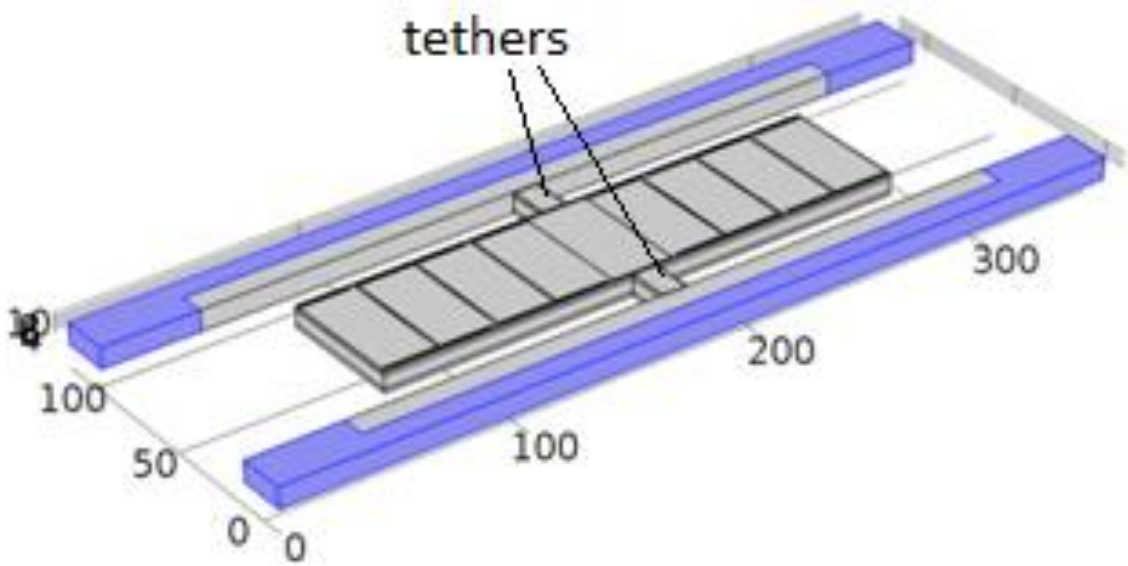

Figure 2-7: 3D view of piezoelectric on silicon bulk acoustic MEMS resonator

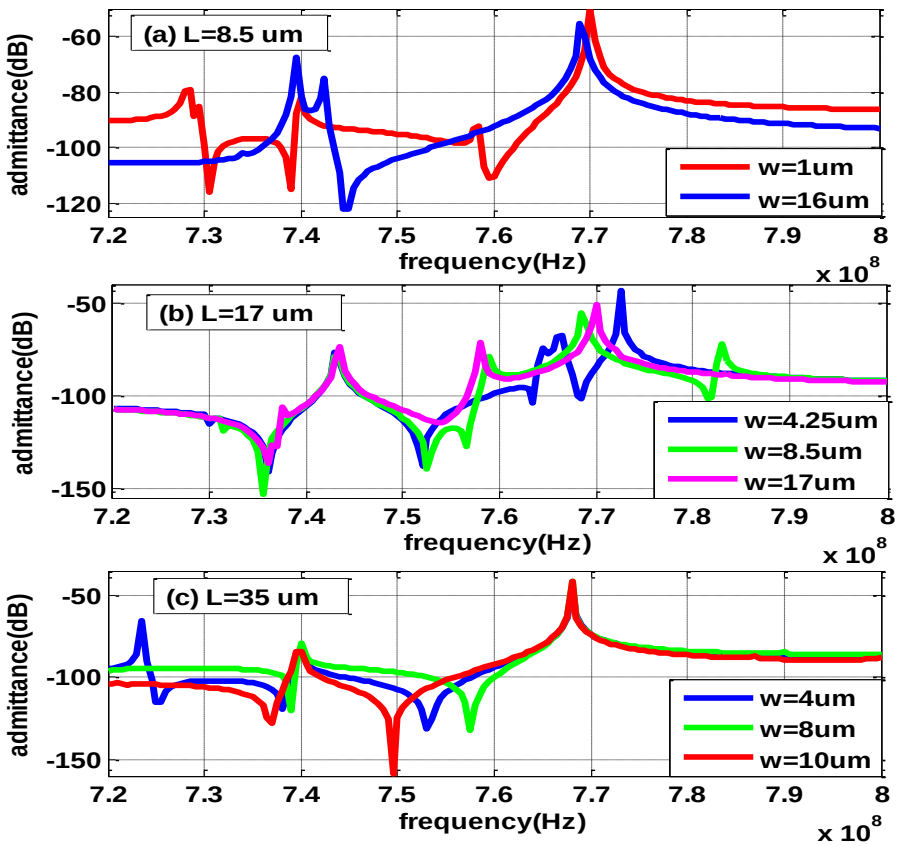

Figure 2-8: Effect of tether lengths and widths on admittance. (a) length of $\lambda/16$, (b) length of $\lambda/8$, (c) length of $\lambda/4$.

2.3.Material Temperature Compensation

Temperature stability [44-53] is crucial in wireless communications. Poor temperature stability can lead to activity dips which result in dropped packets, loss of GPS lock, and cellular signal errors. Activity dips [9] happen when the unwanted modes with large TCF are close to the main mode; these spurious modes may interfere and couple with the main mode; thus the design and control of spurious modes in the proximity of resonance is important and it is mainly controlled by the design of tethers (anchors). For a shear mode Quartz resonator, the resonant frequency f_r is given by,

$$f_r = \frac{1}{2d}\sqrt{\frac{c}{\rho}} \tag{2.6}$$

where d is the Quartz thickness, c is the stiffness constant of is excited mode, and ρ is the density. By differentiating (2.6) with respect to temperature T we get the temperature coefficient of frequency TCF

$$TCF = \frac{1}{f}\frac{\partial f}{\partial T} = -\frac{1}{d}\frac{\partial d}{\partial T} - \frac{1}{2\rho}\frac{\partial \rho}{\partial T} + \frac{1}{2c}\frac{\partial c}{\partial T} \tag{2.7}$$

The first term represents the temperature variation of resonator thickness which is known as the linear coefficient of expansion α. This term depends on the direction and orientation of the material and it is usually positive, hence a rise in temperature will increase the thickness and as a result decrease the frequency. The second term shows the temperature variation with the material density, an increase in temperature results in decrease of density as the dimensions increase while the mass does not. This decrease in density increases the frequency so the first two terms tend to cancel one another. The last term represents the changes in frequency as result of changes in the stiffness constant with temperature. The fractional change in c values is called T_c (parts/˚C); usually increase in temperature makes the material less stiffer giving negative T_c values. Fortunately AT-cut shear mode Quartz's unique property of having a positive temperature dependence of one stiffness coefficient Tc_{66} makes it superior to any other

MEMS material. For silicon resonators, all *Tc* coefficients are negative unlike Quartz and in the order of -60e-6/K to -100e-6/K giving TCF of -28ppm/K to -31 ppm/K.

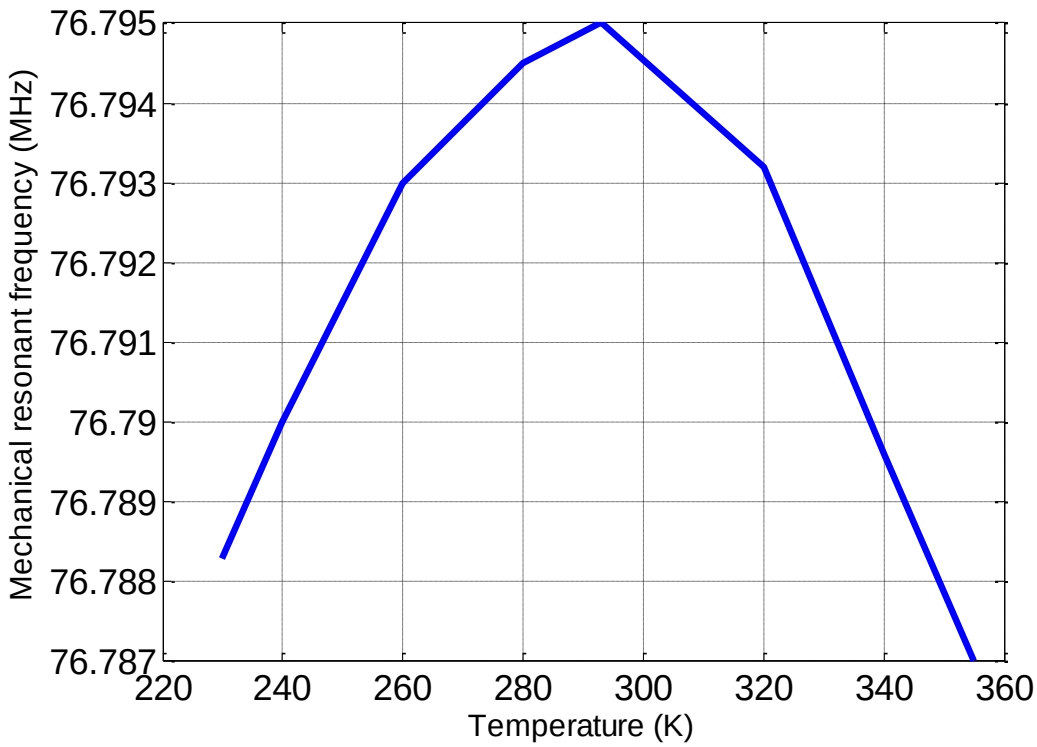

Figure 2-9: Mechanical resonant frequency across temperature after compensation

To reach zero TCF resonators as-per Equation 2.7 across the industrial temperature range, the oscillator or the resonator is required to have a tuning range of 3875 ppm. Resonator's tuning deteriorates the oscillator's performance [54]. Analog tuning of the oscillator increases power consumption and impacts phase noise negatively. Moreover; obtaining a large tuning range is beyond the reach of most electronic frequency tuning techniques [54]. However, passive compensation makes it easier to achieve LTE reference oscillator's temperature stability specifications using simpler electronic compensation circuitry, although this compensation negatively affects the resonator's Q, and increases the resonator's motional resistance, it is used in this work to achieve a low power, simple, and low loading oscillator. A positive TCF material (SiO_2) either in layers [44-48] or in

trenches [49] compensates for the negative TCF of silicon and *AlN*. [50, 51] show that heavy n-doping of Si can enhance temperature stability. [52, 53] use micro ovens for temperature compensation. Our device reaches +0.825 ppm/℃ TCF instead of -30 ppm/℃ for the uncompensated resonator as shown in Figure 2-10 using SiO_2 as compensation material.

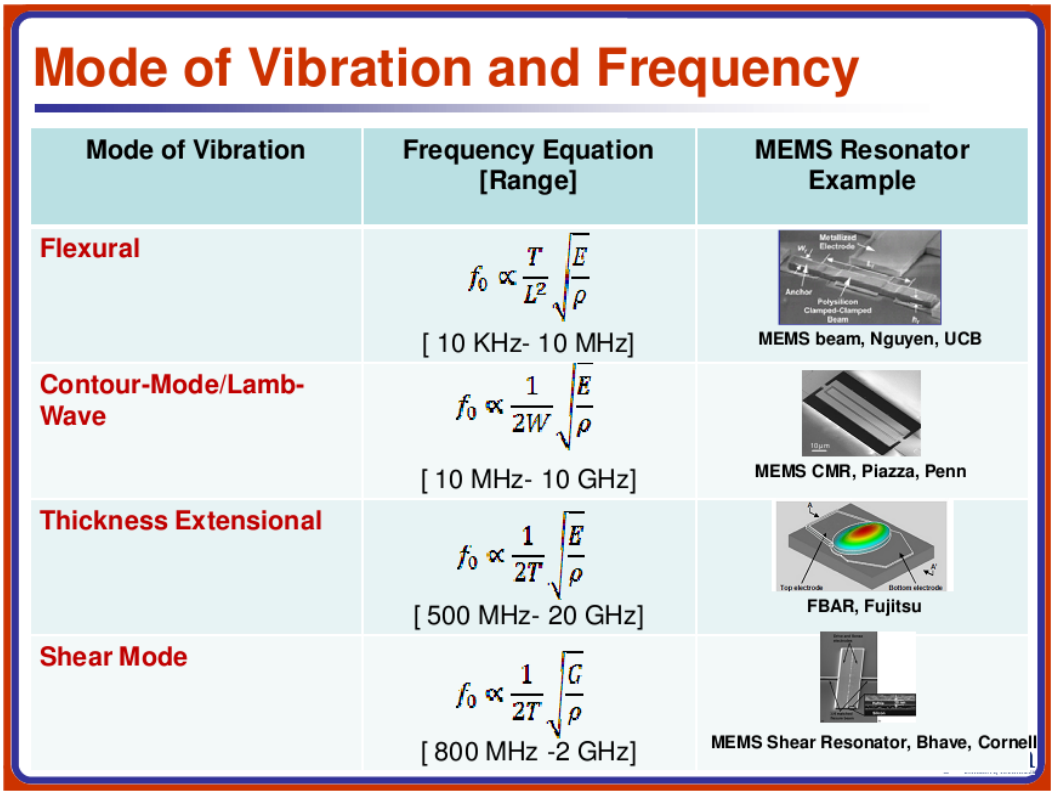

Figure 2-10: vibration modes [14]

2.4.Frequency Setting and Resonance Modes (Mechanical Design)

Figure 2-11 shows the different vibration modes for MEMS resonators. As shown, the vibration mode depends on the resonator dimensions (in-plane and thickness) thus setting the resonance frequency. Quality factor and the coupling factor greatly depend on the targeted mode. Our work targets a 76.8 MHz width extensional mode (contour mode) resonator. Contour mode showed the lowest motional resistance for our targeted resonance frequency. Finite element simulation showed that this mode is the least affected by anchor losses at the targeted frequency.

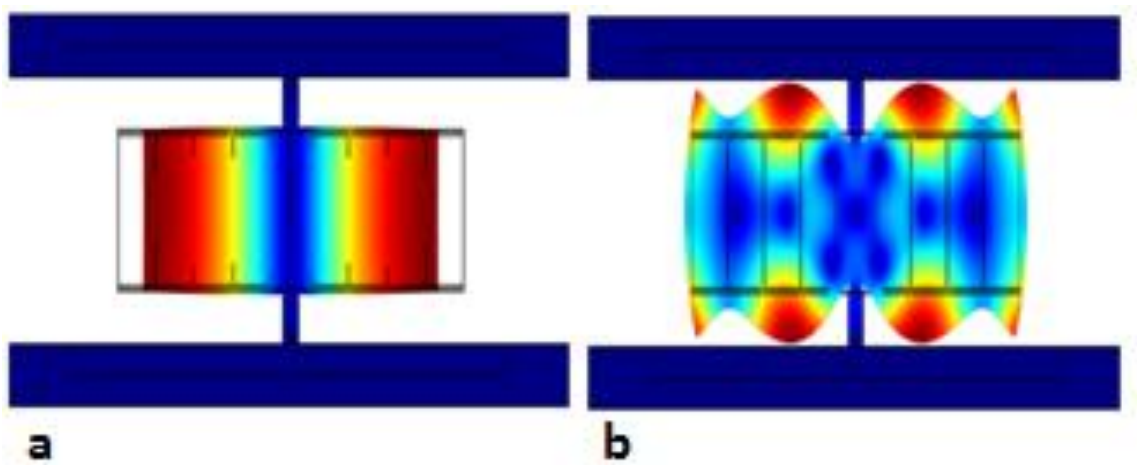

Figure 2-11: Length Extensional mode (a), and Width extensional mode (b)

AC voltage is applied across the thin *AlN* film, this induces in-plane vibrations through the piezoelectric d_{31} coefficient, exciting the resonator either in length or width extensional modes as shown in Figure 2-12, depending on the direction of vibration and the targeted frequency [29].This resulting vibration is converted back to electrical signal on the output of the electrode [55]. Width extensional mode resonators vibrate primarily across its width, while length extensional mode resonators vibrate across its length; as a result, different performance matrix is achieved from resonance frequency, Q, and motional resistance when targeting either of the two modes.

Multi *AlN* bulk extensional-mode resonators can be used on a single substrate [56, 57]

since the resonant frequency is mainly set by in-plane dimensions which are defined nowadays by lithography accuracy, unlike thickness mode FBARs where thickness of the resonator is the main frequency settler. Width extensional mode resonant frequency can be approximated:

$$f_o = \frac{1}{2W}\sqrt{\frac{E_{eff}}{\rho_{eff}}} \tag{2.8}$$

Where w is the resonator width, E_{eff} and ρ_{eff} are the effective Young's modulus and effective density of the composite structure, respectively.

The length and thickness have a 2nd order effect on the resonant frequency setting; yet can be used for Q optimization and tuning the resonator's TCF, respectively.

Modes can be flexures, shears, and in-plane. Only few are detected electrically depending on the Q and the electromechanical coupling η of certain mode [29]. The controllability and observability of a mode is important to be considered. A high Q mode can be designed but the electrodes configuration may not be able to excite it; such mode is not controllable and it may be ignored. On the other hand, a high Q mode that can be driven, but cannot be detected by the sense electrode is not observable and is irrelevant as well. Long devices are subject to more flexures, which degrade Q.

A proper aspect ratio of 4 between the length and the width should be maintained to minimize spurious oscillation as reported experimentally in [29]. This improves the selectivity of the resonator and simplifies the oscillator circuit since no mode suppression circuitry is needed [13].

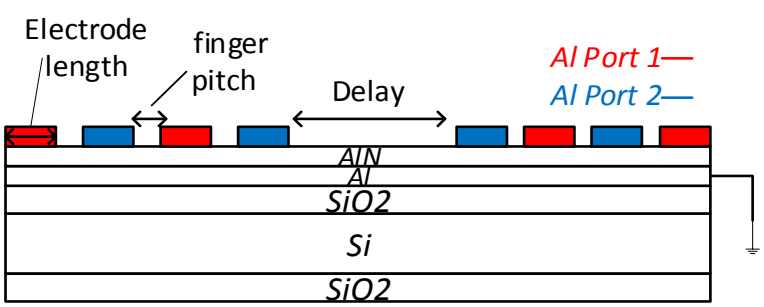

Figure 2-12: cross section of resonator

For two port extensional mode resonators, η and $M_{eq}$are given by

$$\eta = E_{eff} d_{31} L \tag{2.9}$$

$$M_{eq} = \rho_{eff} \frac{WLT}{2} \tag{2.10}$$

Where, L, T are the length, and thickness of resonator respectively. Figure 2-13 shows a cross section of the resonator, showing the resonator material stack, and electrode patterning.

Table 2-1 : Geometric dimensions of 76.8 MHz resenator.

IDT electrodes = 8	Variable Si layer thickness
Variable Device width	Finger pitch = 1 μm
Variable Electrode length	Delay = Electrode length/2
AlN layer thickness = 0.1 μm	
Variable Top = Bottom SiO_2 thickness	
Top = Bottom Al electrode thickness = 0.1 μm	

Mason's model [58-60] is used for theoretical calculations of the composite resonator's resonance frequency using dimensions given in Table 2-1. The model treats different layers of the composite resonator as 1D transmission lines with different phase shifts and acoustic velocities (Figure 2-14). The model estimates the target resonance frequency, observable and controllable modes with good accuracy thus saves a lot of simulation time over finite element simulator. However it is not reliable for Q calculation since it only takes into account the material losses.

[58] Shows a way to model thin film thickness extensional mode BAW resonators using 4 layers device (*Al-AlN-Al-*SiO_2). The Equations 2.11 to 2.26 were adapted to model 6 layer devices to include the temperature compensation layers and to model the width extensional mode rather than thickness extensional mode.

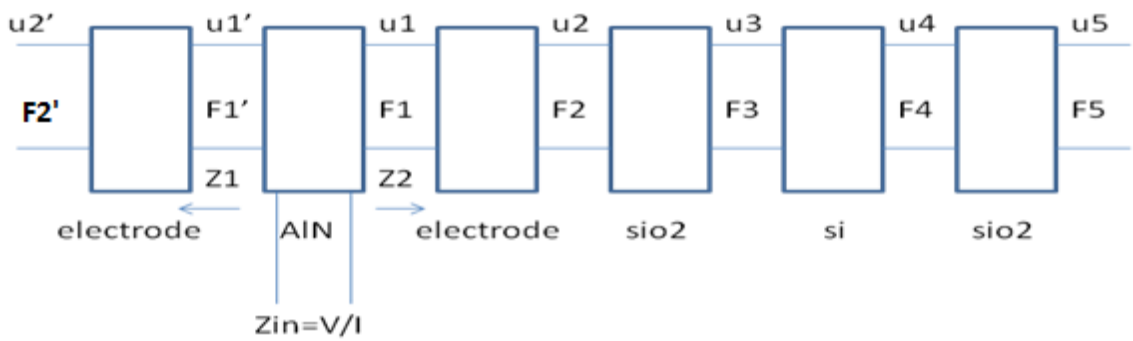

Figure 2-13: Mason model for composite resonators

The following equations deals with the film plates as transmission lines with certain wave velocity v (v_{e1}, v_{e2}, v_{SiO2}, v_{Si}, v_{AlN}), phase shift γ ($\gamma_{e1}, \gamma_{e2}, \gamma_{SiO2}, \gamma_{Si}, \gamma_{AlN}$), the impedance of different layers Z ($Z_{e1}, Z_{e2}, Z_{SiO2}, Z_{Si}, Z_{AlN}$), force F, displacement velocity U, Young's modulus E ($E_{e1}, E_{e2}, E_{SiO2}, E_{Si}, E_{AlN}$), density ρ ($\rho_{e1}, \rho_{e2}, \rho_{SiO2}, \rho_{Si}, \rho_{AlN}$), the resonance angular frequency ω, thickness of different layers t ($t_{e1}, t_{e2}, t_{SiO2}, t_{Si}, t_{AlN}$), width W, length L, and the effective electromechanical coupling factor η.

$$v = \sqrt{\frac{E}{\rho}} \rightarrow \left[v_{e1} = \sqrt{\frac{E_{e1}}{\rho_{e1}}}, v_{e2} = \sqrt{\frac{E_{e2}}{\rho_{e2}}}, v_{SiO2} = \sqrt{\frac{E_{SiO2}}{\rho_{SiO2}}}, v_{Si} = \sqrt{\frac{E_{Si}}{\rho_{Si}}}, v_{AlN} = \sqrt{\frac{E_{AlN}}{\rho_{AlN}}} \right] \quad (2.11)$$

$$\gamma = \frac{\omega \cdot t}{v} \rightarrow \left[\gamma_{e1} = \frac{\omega \cdot t_{e1}}{v_{e1}}, \gamma_{e2} = \frac{\omega \cdot t_{e2}}{v_{e2}}, \gamma_{SiO2} = \frac{\omega \cdot t_{SiO2}}{v_{SiO2}}, \gamma_{Si} = \frac{\omega \cdot t_{Si}}{v_{Si}}, \gamma_{AlN} = \frac{\omega \cdot t_{AlN}}{v_{AlN}} \right] \quad (2.12)$$

$$\begin{bmatrix} F1' \\ U1' \end{bmatrix} = \begin{bmatrix} \cos(\gamma_{e1}) & jZ_{e1}\sin(\gamma_{e1}) \\ \frac{j\sin(\gamma_{e1})}{Z_{e1}} & \cos(\gamma_{e1}) \end{bmatrix} \begin{bmatrix} F2' \\ U2' \end{bmatrix} \quad (2.13)$$

$$F2' = 0 \quad (2.14)$$

$$\begin{bmatrix} F1 \\ U1 \end{bmatrix} = \begin{bmatrix} \cos(\gamma_{e2}) & jZ_{e2}\sin(\gamma_{e2}) \\ \frac{j\sin(\gamma_{e2})}{Z_{e2}} & \cos(\gamma_{e2}) \end{bmatrix} \begin{bmatrix} F2 \\ U2 \end{bmatrix} \quad (2.15)$$

$$\begin{bmatrix} F2 \\ U2 \end{bmatrix} = \begin{bmatrix} \cos(\gamma_{SiO2}) & jZ_{SiO2}\sin(\gamma_{SiO2}) \\ \frac{j\sin(\gamma_{SiO2})}{Z_{SiO2}} & \cos(\gamma_{SiO2}) \end{bmatrix} \begin{bmatrix} F3 \\ U3 \end{bmatrix} \quad (2.16)$$

$$\begin{bmatrix} F3 \\ U3 \end{bmatrix} = \begin{bmatrix} \cos(\gamma_{Si}) & jZ_{Si}\sin(\gamma_{Si}) \\ \frac{j\sin(\gamma_{Si})}{Z_{Si}} & \cos(\gamma_{Si}) \end{bmatrix} \begin{bmatrix} F4 \\ U4 \end{bmatrix} \tag{2.17}$$

$$\begin{bmatrix} F4 \\ U4 \end{bmatrix} = \begin{bmatrix} \cos(\gamma_{SiO2}) & jZ_{SiO2}\sin(\gamma_{SiO2}) \\ \frac{j\sin(\gamma_{SiO2})}{Z_{SiO2}} & \cos(\gamma_{SiO2}) \end{bmatrix} \begin{bmatrix} F5 \\ U5 \end{bmatrix} \tag{2.18}$$

$$F5 = 0 \tag{2.19}$$

$$Z1 = \frac{F1'}{U1'} = jZ_{e1}\tan(\gamma_{e1}) \tag{2.20}$$

$$Z2 = \frac{F1}{U1} \tag{2.21}$$

$$z1' = \frac{Z1}{Zo} \quad (normalized\ impedance) \tag{2.22}$$

$$z2' = \frac{Z2}{Z0} \quad (normalized\ impedance) \tag{2.23}$$

$$Zo = W * L * V_{AlN} * \ \rho_{AlN} \tag{2.24}$$

$$Co = no.of\ electrode\ fingers * e_o * e_{33} * W\ of\ finger * \frac{L\ of\ finger}{t_{AlN}} \tag{2.25}$$

$$Zin = \frac{V}{I} = \frac{1}{j\omega Co}\left[1 - \frac{\eta^2}{\gamma_{AlN}} \frac{(z1'+z2')\sin(\gamma_{AlN}) + j2(1-\cos(\gamma_{AlN}))}{(z1'+z2')\cos(\gamma_{AlN}) + j(1+z1'z2')\sin(\gamma_{AlN})}\right] \tag{2.26}$$

The study starts with the mathematical Mason's model to determine the in-plane dimensions (length and width) for the width extensional mode resonator; hence controlling the resonant frequencies. Figure 2-15 shows the resonator's impedance using Mason's numerical model. After having a reasonable approximation of the targeted resonant frequency, the device is built on a finite element simulator for further investigation of Q, temperature stability, and spurs control. Several resonators are designed throughout the thesis, all having a fixed 76.8 MHz resonant frequency, but with different Q, TCF, and motional resistance specifications, these specifications are investigated by varying some parameters as in-plane dimensions, Si and SiO_2

thicknesses. As shown in Table 2-1, some parameters are fixed and others are varied throughout the thesis to investigate their effect on performance.

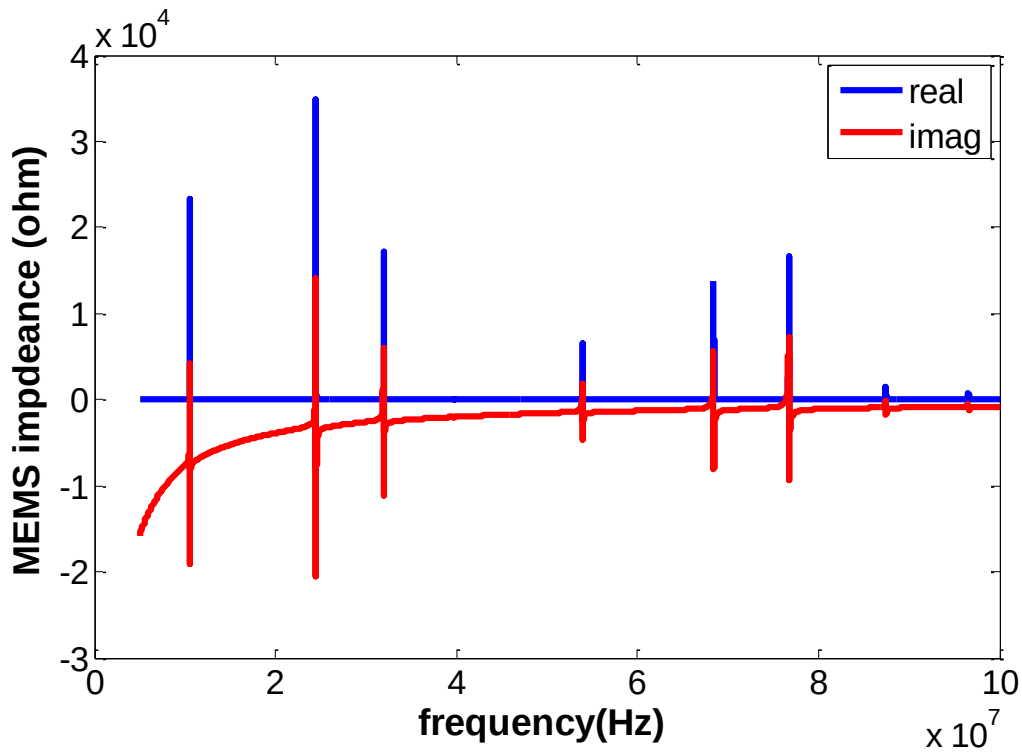

Figure 2-14: Mason's model for the 6 layers composite resonator (using MATLAB) Si thickness=5µm, SiO_2 thickness=1.66µm, width=52 µm, electrode length=23.3 µm.

2.5.Electrical Equivalent Circuit

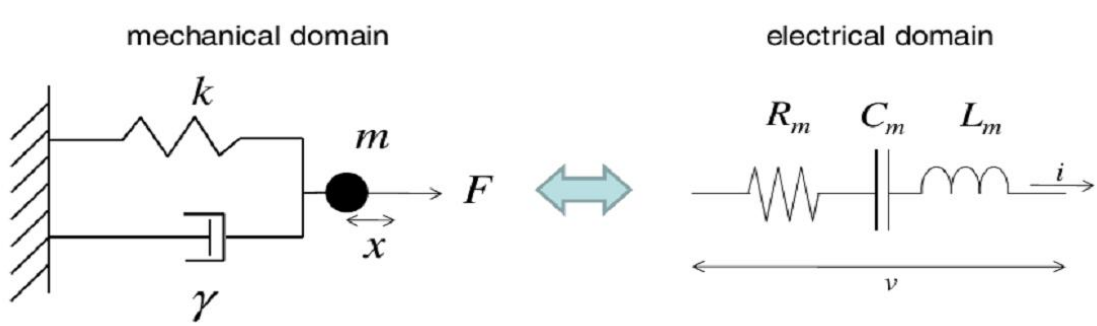

Figure 2-15: Mechanical to electrical domain conversion [3]

Figure 2-16 shows the mechanical model and the electrical one. The mechanical model consists of spring with stiffness constant (K) which has electrical equivalent of motional arm capacitance (C_m), this component resembles the stiffness of the resonator and it mainly determines the quality factor. The other mechanical component is the damping dashpot which is a resistor (R_m) in the electrical domain and it represents the material losses of the resonator, this component is the main one to determine the power and gain requirement of oscillator to satisfy Barkhausen criteria. The last component is the mass which is ideally an inductor in the electrical domain, it represents the stored magnetic energy in the resonator, and it resembles the inertia. General equations guiding any resonator design are listed below

$$m\ddot{x}+\beta\dot{x}+kx=F \tag{2.27}$$

$$\dot{x} = \frac{i}{\eta} \tag{2.28}$$

$$F=\eta v \tag{2.29}$$

$$L_m \frac{\partial i}{\partial t}+R_m i+\frac{1}{C_m}\int i\partial t = v \tag{2.30}$$

$$L_m = \frac{m}{\eta^2} \tag{2.31}$$

$$C_m = \frac{\eta^2}{k} \tag{2.32}$$

$$R_m = \frac{\gamma}{\eta^2} \tag{2.33}$$

$$Y=j\omega C_f+\frac{1}{j\omega L_m+{}^{1}/_{\omega C_m+R_m}} \tag{2.34}$$

Where F is force, *x* is displacement, β is the dashpot resistance, *m* is mass, *k* is the spring stiffness constant, η is the coupling factor, and *v* is the ac voltage drop.

The force F and the displacement *x* can be expressed as ac voltage drop *v* over the two resonator terminals and an ac current *i* going through the resonator respectively by means of the electro-mechanical coupling factor η.

The unloaded Q of the resonator $Q_{unloaded}$ is defined as the ratio of energy stored, E_{stored} in the resonator divided by the energy dissipated caused by mechanical damping during one period of resonance, $E_{dissipated}$ [3]. This translates into

$$Q_{unloaded} = 2\pi \frac{E_{stored}}{E_{dissipated}} = \frac{\sqrt{km}}{\beta} = \frac{1}{R_m}\sqrt{\frac{L_m}{C_m}} \tag{2.35}$$

Two port resonators can be modeled by series $R_m L_m C_m$ with shunt feed-through capacitance C_f that represents the path between the input and output node [11], [61]. Parasitic capacitance *Cp* is caused by the overlap of top and bottom electrodes in addition to pad capacitance.

Butterworth Van Dyke (BVD) model components can be calculated for width extensional mode resonators specifically as-per Equations 2.36-2.39 and as shown in Figure 2-17.

$$C_m = \frac{\eta^2}{(2\pi f_o)^2 M_{eq}} \tag{2.36}$$

$$L_m = \frac{M_{eq}}{\eta^2} \tag{2.37}$$

$$C_p = \in \frac{WL}{T} \tag{2.38}$$

$$R_m = \frac{2\pi f_o M_{eq}}{Q\,\eta^2} = \frac{\pi\,\rho^{0.5}\,T}{Q\,E_{eff}{}^{1.5}\,d_{31}{}^2\,L} \tag{2.39}$$

Figure 2-18 shows the impedance of the resonator extracted from finite element simulations with nearest spur branches (controllable and observable) to fundamental frequency. The least frequency mode shown is the length extensional mode having a resonance frequency of 18.12 MHz, and a motional resistance of 1375Ω which is not suitable for cellular application. This mode will not be excited by a low power oscillator that is designed to have small gain to excite low losses width extensional resonance mode only.

Table 2-2 gives the components values of MEMS electrical equivalent circuit, while Figure 2-19 shows the whole admittance profile including non controllable and non observable modes.

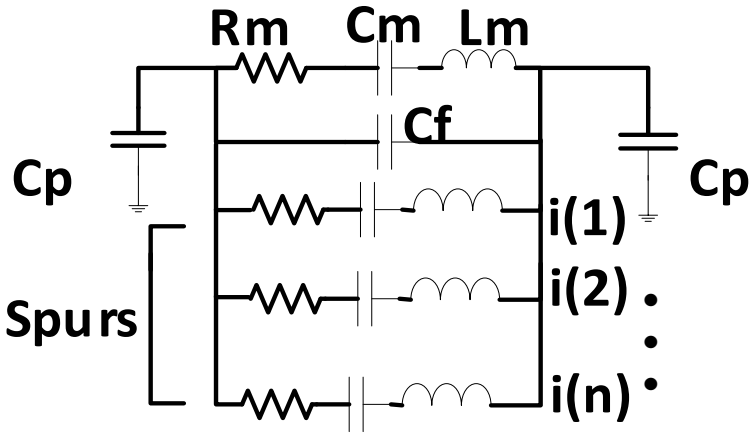

Figure 2-16 : BVD 2 port MEMS resonator model with the nearest different spurs extracted from COMSOL

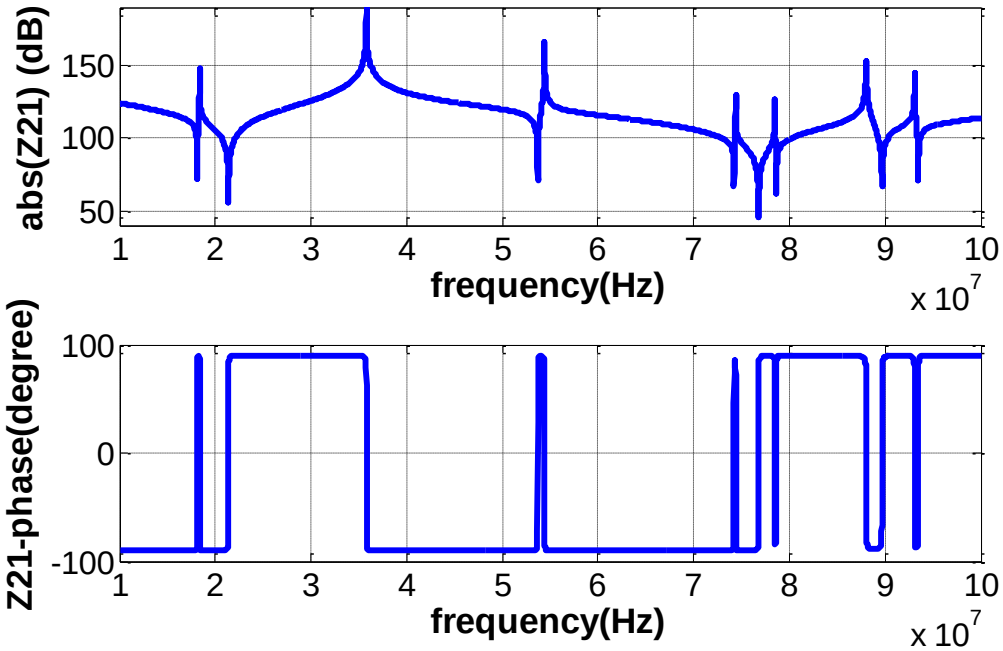

Figure 2-17: Resonator impedance extracted with different spurs. Si thickness =5µm, SiO_2thickness=1.66µm, width=52µm, electrode length =23.3 µm.

Table 2-2 : electrical equivalent circuit component values Si thickness =5µm, SiO_2thickness=1.66µm, width=52µm, electrode length =23.3 µm.

	C_m (fF)	L_m(H)	R_m
Fundamental C_p =3.9pF	**1.573928017**	**2.729234342E-3**	**125**
1st spur	0.606642	0.1272212	1375
2nd spur	5.058633	0.0109453	424
3rd spur	0.091648	0.0958838	3050
4th spur	0.130994	0.0351141	1520
5th spur	0.147573	0.0277482	1280
6th spur	0.199296	0.0158019	2150
7th spur	0.052364	0.0553629	3500
8th spur	0.052701	0.0437703	7000
9th spur	0.016138	0.1318067	8500
10th spur	0.007590	0.2051358	16000
11th spur	0.011463	0.0885883	9000
12th spur	0.082541	0.0185423	1720

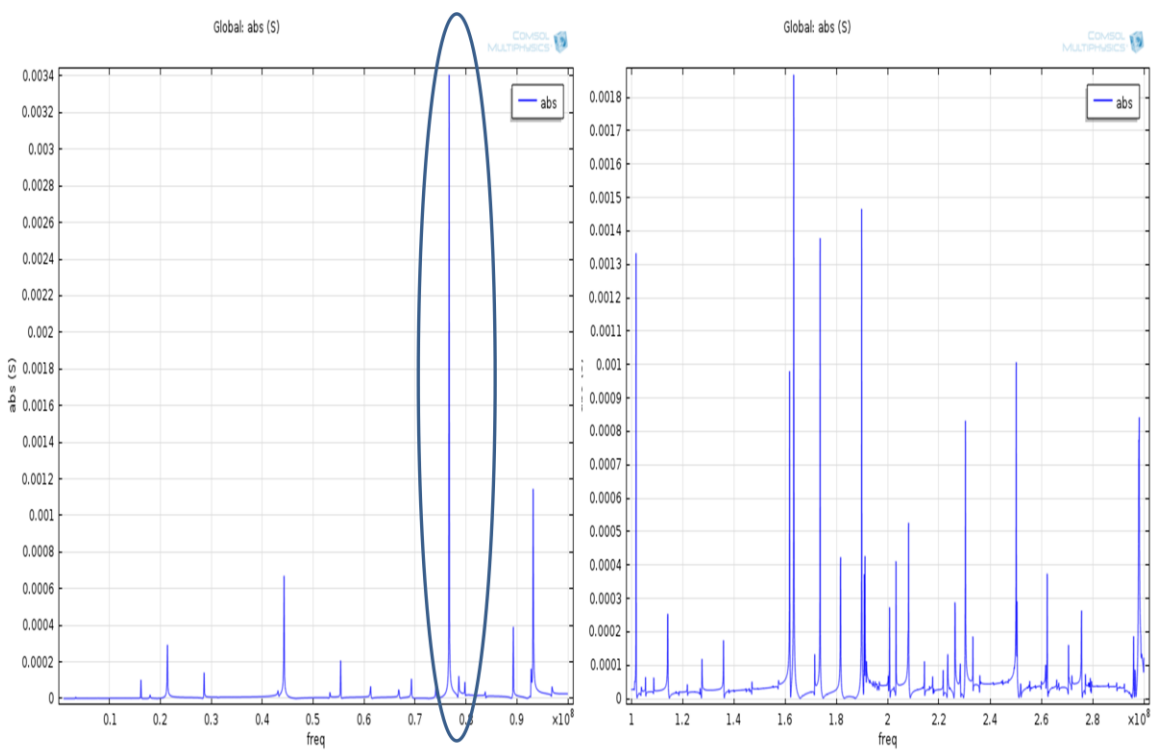

Figure 2-18: absolute input resonator's admittance versus frequency (all modes either observable , controllable or not, activity dips are found with some modes)

A fundamental difference between a two port resonator and a single port resonator is that the electrode to resonator capacitance C_p , in the electrical equivalent circuit model is no longer connecting the input to the output, but shunted to ground. The removal of such big capacitance from the input to output feed-through path is advantageous for the series resonant oscillator used in this work. This is because it better isolates the input from the output, allowing the majority of the current through the device to be filtered by its high Q band-pass transfer function [19]. However a very small capacitance is still present in the feed-through path C_f as due to top interdigitated electrodes [11], this femto-farad range value capacitor does not affect the resonator performance.

2.6.Series and Parallel Resonance

Resonance can be series or parallel, this means that a single resonator has minimum number of two resonant frequencies; one is due to the motional arm of a high quality factor and is called series resonant frequency f_s. The parallel resonant frequency f_p is due to the feedback through capacitance which typically has a lower quality factor.

Figure 2-20 shows the two resonant frequencies. Crystal resonators are bulky and of large electrodes capacitance (>10pF) making it more easier to resonate using a parallel resonant oscillator topology like pierce oscillators unlike MEMS counterparts that are characterized by small to ground capacitances making it ideal for series resonant oscillators as will be shown in chapter 3. For pierce crystal oscillators, the oscillation frequency is found between f_s and f_p in the inductive region that's why oscillation frequency is always greater than the mechanical resonant frequency. This is due to the large parasitic associated with crystal resonators as mentioned above. For inductive series resonant oscillators, the frequency of oscillation is usually lower than the mechanical resonant frequency as in our case.

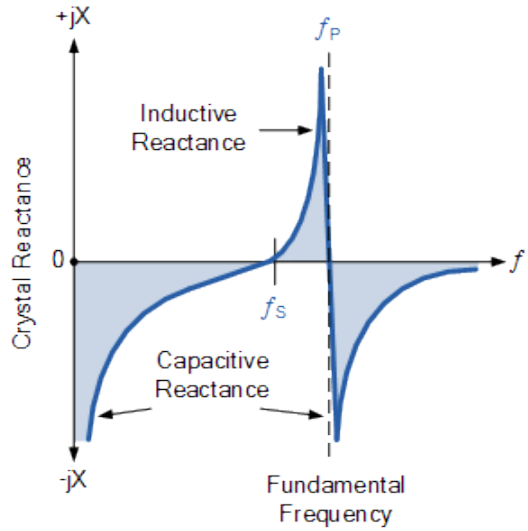

Figure 2-19: series and parallel resonance

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{2.40}$$

$$f_p = \frac{1}{2\pi\sqrt{L_m \frac{C_m C_{//}}{C_m + C_{//}}}} \tag{2.41}$$

$$p = \frac{f - f_s}{f_s} \tag{2.42}$$

$$Z_m = R_m + \frac{2jp}{\omega C_m} \tag{2.43}$$

Series and parallel resonance have only to do with the operating point of the oscillator. For very small frequency pulling factor p (p < $C_m/4C_{//}$), the operating point is close to f_s and in this case, we clearly have a series resonance oscillator. For a fairly large p (p > $C_m/4C_{//}$), the operating point is close to f_p. We will call this a parallel resonance oscillator [4]

2.7. Resonator Material Choice

Resonator's material stack is chosen to maximize $f{\cdot}Q$ product of the resonator to reach the intrinsic values reported in [30]. *AlN* has lower d_{31} coefficient (-1.8 pC/N) when compared to ZnO (-4.7 pC/N) [23], limiting the resonator's η. However, it is chosen as a piezoelectric material for its CMOS compatibility, and its higher acoustic velocity.

Table 2-3 shows the superior performance of (111) Si resonator over its counterparts in terms of motional resistance and Q. Low Rm value is critical for low oscillator's power consumption needed for wireless handsets. High Q resonators are needed for low close in-phase noise performance and it may help also to save oscillator's power consumption. (110) Si resonator showed the best temperature stability but almost double (111) Si resonator's motional resistance value. In this work, (111) single crystal Si is chosen to be one of the materials in the composite resonator structure.

Aluminum is chosen for top and bottom electrodes to benefit from its low mass loading on *AlN* (1.2 times smaller density than *AlN*) [29]. Bottom ground plate enhances η because of strong electric field induced between the 2 metal layers, the ground plate reduces the input/output feed- through capacitance c_f and hence obtain near zero-phase resonance [23]. The high electromechanical coupling of the piezoelectric transduction combined with the low acoustic loss of the single crystal silicon substrates (*AlN*-on-silicon) insures high Q resonators with low motional impedance [24].

Table 2-3 : 76.8 MHz resenator with different single crystal silicon's orientations

	5 µm Si (100)	5 µm Si (110)	5 µm Si (111)
Frequency (MHz)	76.8	76.8	76.8
Unloaded Q	8400	9700	10500
Rm (Ω)	170	230	125
TCF (ppm/˚C)	0.87	0.456	0.825
SiO_2 height (µm)	1.4	1.83	1.66
Device width (µm)	47.5	50	52
Electrode length (µm)	18	23.3	23.3

2.8. Resonator performance optimization

As shown in Figure 2-21, *AlN* thickness shows a big effect over the motional resistance value, and Q. The thinner the film is, the higher the Q, and the lower the Rm achieved, this was proved theoretically using Equation 2.37. Although better temperature stability can be achieved by using 0.3 µm *AlN*, 0.1µm thickness is chosen when compared to the rest of devices in this work paying the cost of high capacitance which will only affect the oscillator's power consumption slightly. Figure 2-22 shows the effect of in-plane dimensions on resonator's performance. These dimensions are optimized for the highest Q and lowest motional resistance value possible at 76.8 MHz; as previously stated the resonator's width is the main frequency settler. Table 2-4 shows the effect of increasing the thickness of Si on resenator's performance, increasing the Si thickness, increases the resonant frequency, and Q.

For 0.825 ppm/˚C TCF, 76.8MHz resonator, the devices have to be redesigned by changing the inplane dimensions and the SiO_2 thickness, the new figures are given in Table 2-5. As shown in Figure 2-23, as the Si thickness increases, a thicker SiO_2 layer for temperature compensation is needed, it is quadratic relation between both thicknesses. Deposition of thick SiO_2 layers may induce stresses on the film surface while manufacturing, decreasing the Q of the resonator; besides the need to work on high temperature for depositing thick layers. For these reasons device 3 is discarded.

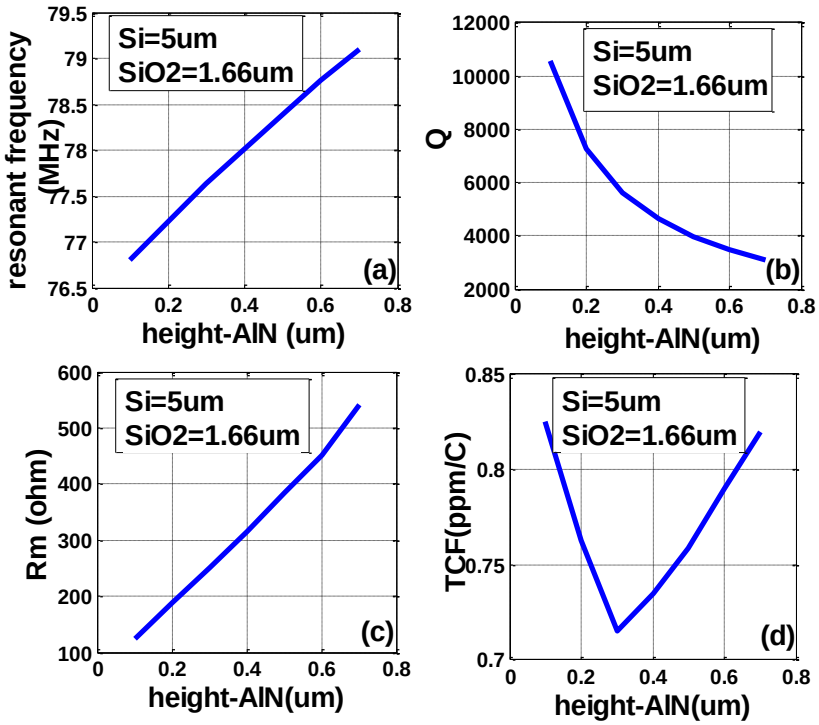

Figure 2-20: effect of *AlN* thickness on resonance frequency (a), Q(b), Rm (c) and temperature stability(d)

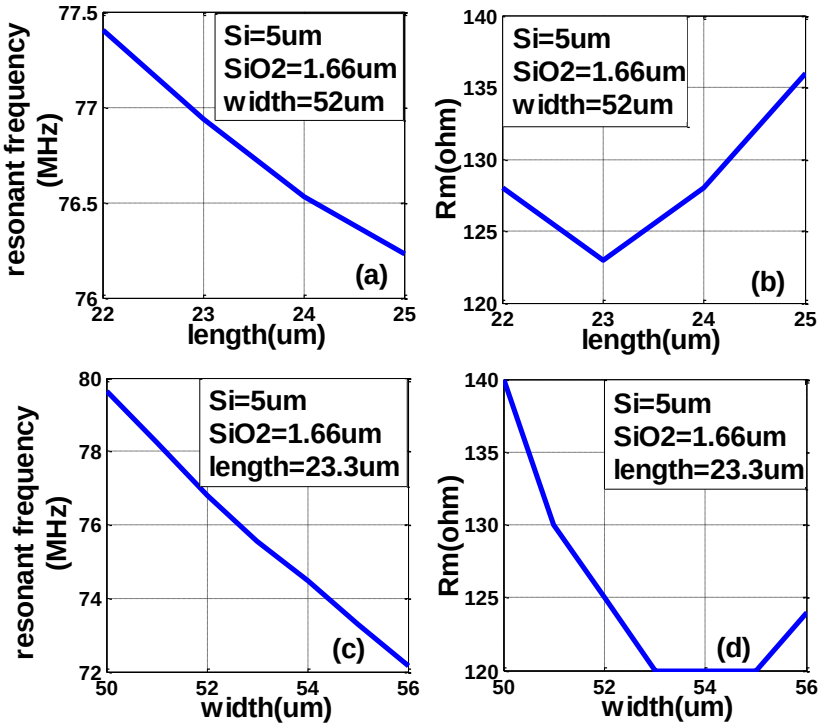

Figure 2-21: effect of electrode's length, and width on frequency (a,c), and motional resistance (b,d)

Table 2-4: Effect of Si thickness on resonator's performance (*AlN* thickness=0.1 µm, $\mathbf{SiO_2}$ thickness=1.66 µm)

Si thickness (µm)	Resonant frequency (MHz)	Q	Rm (Ω)	TCF (ppm/˚C)
5	76.8	9950	125	0.825
10	80.94	17310	117	8.65
15	82.7	24830	115	11.95

Table 2-5: Final 76.8 MHz, 0.825 ppm/˚C TCF resonators design

P.O.C		Design 1		Design 2		Design 3	
Si thickness (µm)		5		10		15	
SiO_2 thickness (µm)		1.66		2.95		3.9	
Width (µm)		52		52.7		52.7	
Electrode length (µm)		23.3		23.3		23.9	
Rm (Ω)		125		160		190	
Thermal mode frequencies (MHz)	Q_{TED} of thermal modes	76.7 77.7	1.63E5 1.06E5	76.6 77.76 77.8	1.89E5 0.72E5 1.26E5	76.3 76.9 77.6	1.07E5 2.31E5 1.63E5
$Q_{anch+AKE}$		10580		14400		16200	
Q_{Total}		9950		13380		15140	

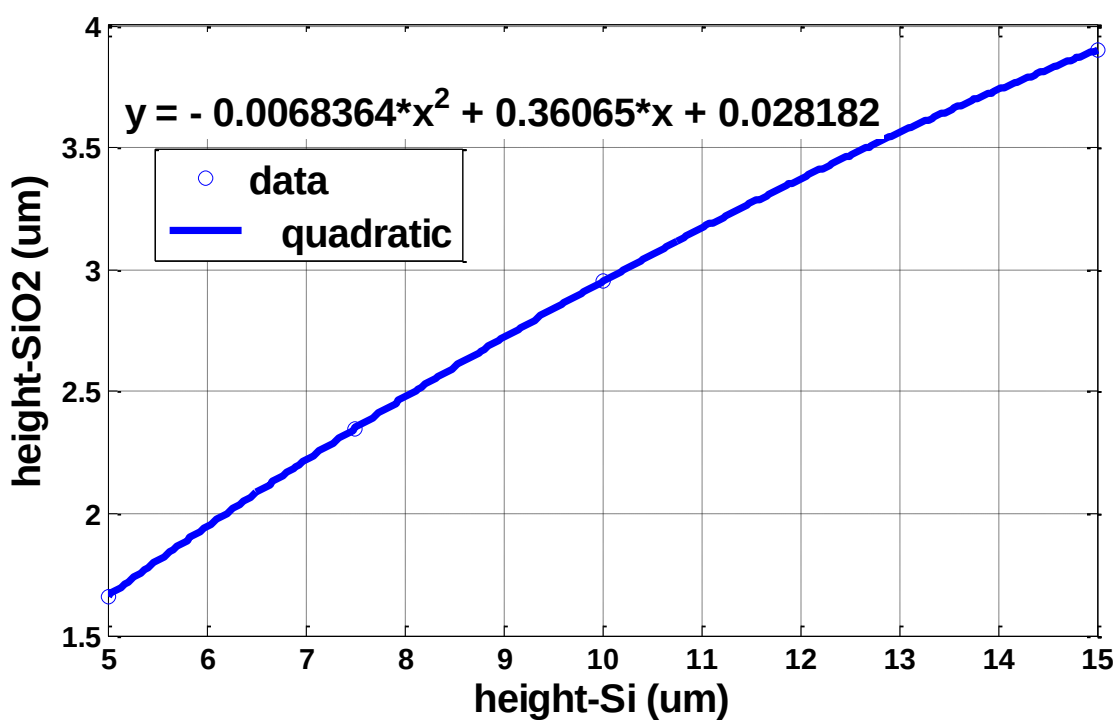

Figure 2-22: SiO_2 thickness for compensating the negative TCF of Si and *AlN*, for TCF of 0.825 ppm/˚C

3.Series Resonance Oscillator

3.1.Concept of Oscillation

Resonator is a lossy element, that when exists alone will never oscillate, it needs sort of energy pumping to the transducer to have mechanical vibration. An amplifier is needed to compensate for the resonator losses and be able to amplify the output signal for signal conditioning. Figure 3-1 shows the concept of the loop oscillator [3].

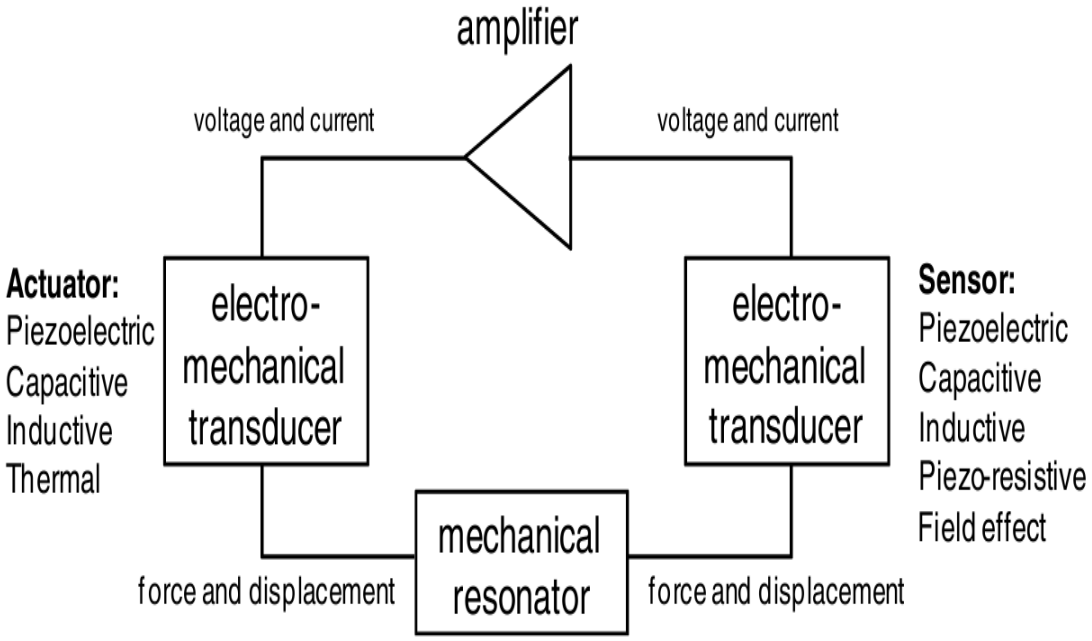

Figure 3-1: oscillator core [3]

As it can be seen from the above figure, there is no input signal to the loop; noise inside the amplifier plays the role of igniting the signal. The noise can be shot, flicker, white noise that circulates around the loop, got filtered with the resonator to have the specific resonance frequency and back to the amplifier to be amplified. The loop will goes on amplifying the noise till reaching a non linearity limit whether inside the amplifier or the

resonator. The power capability of the resonator is a top important requirement for low power and small floor noise inside the oscillator, which translates to high coupling factor η.

There are several conditions that have to be fulfilled for getting a proper oscillation [3]. Equations 3.1 and 3.2 are the famous Barkhausen criteria to ensure real value of gain greater than one and closed loop gain phase of zero. Equation 3.3 deals with the amplitude stability, which ensures that the amplitude of the oscillation is self-limiting; i.e., the loop gain decreases when the amplitude increases. Equation 3.4 deals with phase stability, and states that when the loop phase increases, the frequency should decrease.

$$\mathrm{Re}(G(w_s, a_s)) = 1 \tag{3.1}$$

$$\mathrm{Im}(G((w_s, a_s)) = 0 \tag{3.2}$$

$$\frac{\partial |G|}{\partial a}\Big|_{w_s, a_s} < 0 \tag{3.3}$$

$$\frac{\partial (\arg G)}{\partial w}\Big|_{w_s, a_s} < 0 \tag{3.4}$$

Where G is the oscillator's closed loop gain, w_s is the frequency of oscillation, a_s is the amplitude of oscillation.

If the circuit is strongly nonlinear with a large bandwidth, it results in a relaxation oscillator, the waveform of which is far from being sinusoidal. On the opposite, if the circuit has a narrow bandwidth, the system becomes a harmonic oscillator and the oscillatory signal is approximately sinusoidal [62]

3.2. Theory of High Q Oscillators

The best way to analyze the behavior of any high Q oscillator is to split it conceptually into the motional impedance Z_m and circuit impedance Z_c containing all electronic components [63], including resonator's parasitic capacitors C_{12}, C_{10} and C_{20} as shown in

Figure 3-2. The active circuit impedance at fundamental frequency $Z_{c(1)}$ is defined in Equation 3.5.

$$Z_{c(1)} = \frac{V_{(1)}}{I_c} \tag{3.5}$$

Where, I_c is the current out of resonator to the circuit, and $V_{(1)}$ is the fundamental component of voltage V.

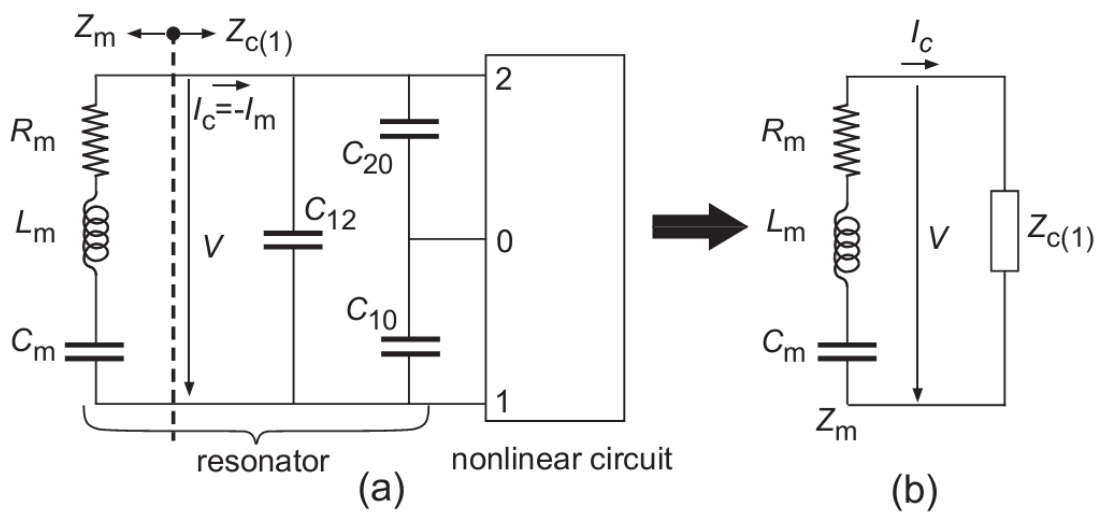

Figure 3-2: (a) general form of oscillator, (b) splitting impedances to Zm, and Zc(1) [62]

As long as I_c is small, the circuit remains linear, the voltage V remains sinusoidal with a complex value $V_{(1)}$=V, and $Z_{c(1)}$ is equal to the small signal impedance Z_c of the circuit. Re (Z_c) should be negative to be able to compensate the losses of the resonator.

When the current is large enough to produce harmonic components of V, the amplitude of its fundamental component $V_{(1)}$ is reduced, thus reducing the negative real part of $Z_{c(1)}$. Excess current may produce so much nonlinearities that the real part of $Z_{c(1)}$ becomes positive [62].

Any oscillation will decay exponentially with a time constant τ

$$\tau = -\frac{2L_m}{R_m + \mathrm{Re}\left(Z_{c(1)}\right)} \tag{3.6}$$

So for positive τ, the amplitude can grow exponentially setting criteria for stable oscillation:

$$\mathrm{Re}\left(Z_{c(1)}\right) = -R_m \text{ corresponding to } \tau = \infty \tag{3.7}$$

Also imaginary part has to be equal giving a general equation for stable oscillation

$$Z_{c(1)} = -Z_m \tag{3.8}$$

Using Equation 2.41, and equating the imaginary part of $Z_{c(1)}$ to that of $-Z_m$, we get the amount of frequency pulling at stable oscillation.

$$p_s = \frac{-\omega C_m}{2} Im\left(Z_{c(1)}\right) \tag{3.9}$$

The above equation shows the relative difference between the oscillation's frequency and the mechanical resonant frequency. The oscillator should be designed with very small value of p_s in order to have the highest loaded Q and the best possible close in phase noise [62].

3.3.Oscillators Based on Series Resonance and Parallel Resonance

Frequency of oscillation shift from mechanical resonant frequency totally depends on the circuit impedance seen by the resonator. Bulky Crystal oscillators are mainly pierce (Figure 3-3), which is parallel resonance oscillator [63]. Smaller MEMS resonators work at frequency closer to the mechanical frequency, using series resonance oscillator topology [62]. Most of the published MEMS oscillators are TIA based ring oscillators [11, 18, 19, and 21]. Our oscillator is a cross coupled series resonance topology, chosen for its inductive impedance seen across the resonator as will be discussed in the following sections.

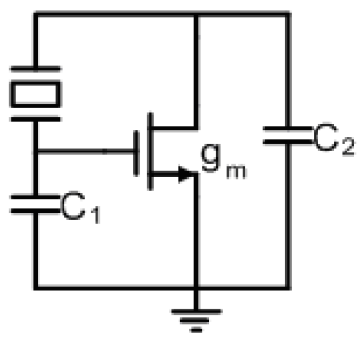

Figure 3-3 pierce oscillator

3.4.Cross Coupled-Series Resonance Oscillator

Series resonance's Q is less sensitive to resonator's size shrinkage because of the lower device capacitance. Working near series resonance rather than parallel resonance (as in quartz) guarantees maximum loaded Q and maintains phase noise performance [64]. A very small pulling from the mechanical resonant frequency is required to minimize the frequency dependence on electrical parameters, thus enhancing the frequency stability of the oscillator. The series resonant oscillator shown in Figure 3-4 consumes less power ($\alpha\ 1/P_c$) than parallel resonant one ($\alpha\ 1/{P_c}^2$) for the same pulling value P_c making it suitable for the more demanding cellular phone platforms. The small signal loop gain is

$$Gain \approx \left(\frac{g_m(R_L/2||2C_L)}{1+g_m(Z_s||C_s)/2}\right)^2 \tag{3.10}$$

Where Z_s is the resonator impedance, and $C_s = C_p/2$.

Source degeneration reaches a minimum value at series resonance, introducing a unity loop gain and oscillation at this frequency. Equivalent circuit of oscillator is shown in Figure 3-5.

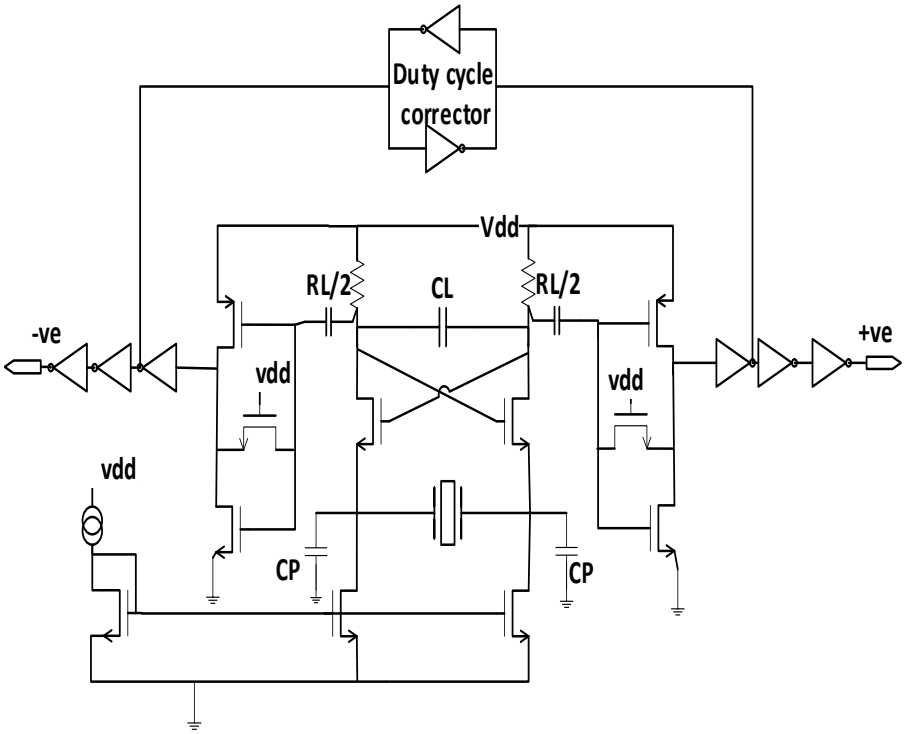

Figure 3-4: MEMS series resonance oscillator

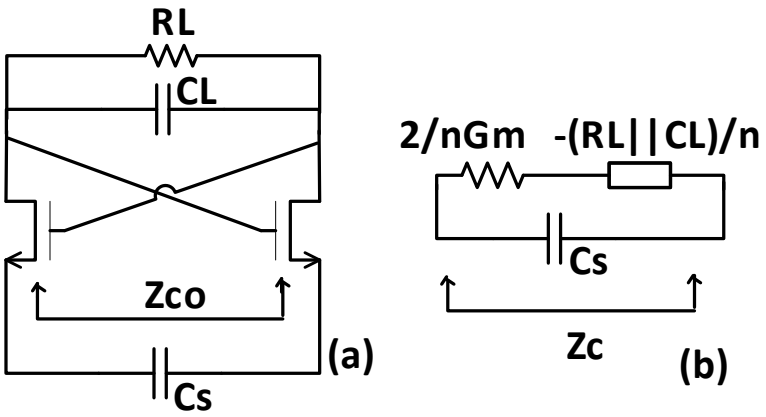

Figure 3-5 : (a) Impedance seen by resonator. (b) is the equivalent circuit of (a)

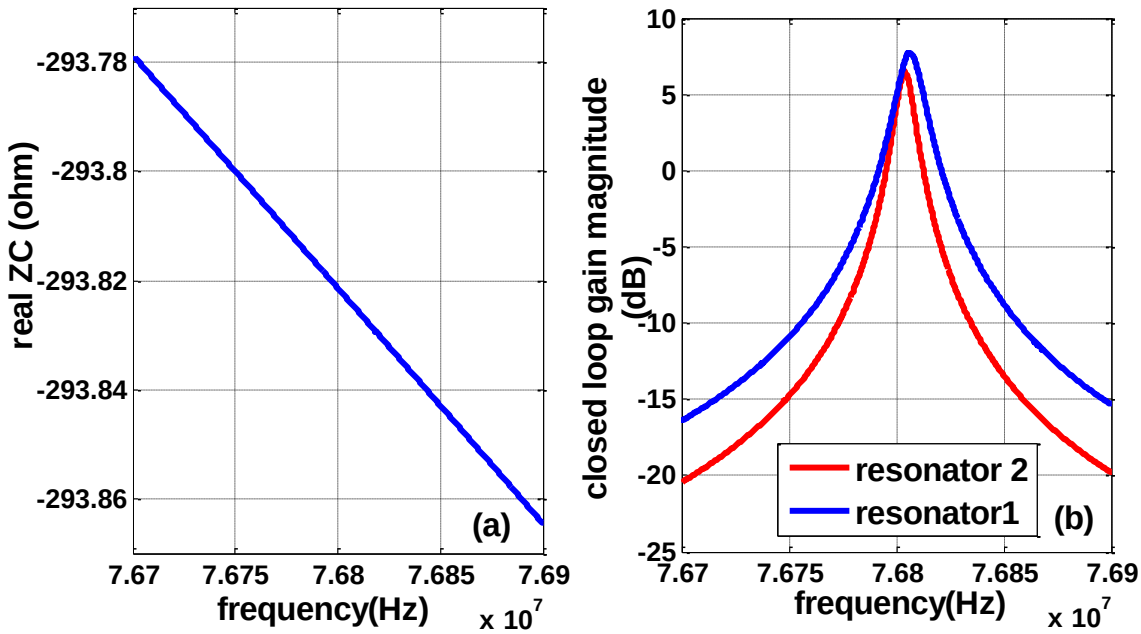

Figure 3-6: real Zc versus frequency (a), closed loop gain magnitude (b)

The circuit impedance Z_{co} as shown in Equation 3.11 is always inductive thus pulling values is always negative, where the oscillation frequency is less than mechanical frequency. The real part of Zc across frequency is shown in Figure 3-6a. This resistance has to be negative and of absolute value greater than resonator's motional resistance for oscillation startup. C_P can induce parasitic oscillation at a frequency which satisfies Equation 3.12, therefore Equation 3.13 is a necessary condition for preventing parasitic oscillations (AC stability) where C_L with R_L act as low pass filter [64].

$$Z_{co} = \frac{2}{nG_m} - \frac{R_L/n}{1+(\omega C_L R_L)^2} + j\frac{\omega C_L {R_L}^2/n}{1+(\omega C_L R_L)^2} \tag{3.11}$$

$$\mathrm{Im}(Z_{co}) = {}^{1}/_{\omega C_s} \tag{3.12}$$

$$C_L > \frac{C_s}{n}\left(1 - \frac{2}{R_L G_m}\right) \tag{3.13}$$

where n is the ratio between source transconductance G_{ms} and gate transconductance G_m. The series load impedance $2/G_m$ seen by resonator's tank (assuming no loading from the tail current sources) should be much less than R_m to

prevent loading and Q degradation, where the loaded Q is given in Equation 3.14. By maximizing Q_L, better close-in phase noise can be achieved. All active devices are IO devices (0.18μm) running on 1.8 volt supply for Electrostatic discharge (ESD) considerations in 32nm Technology kit.

$$Q_L = \frac{R_m}{R_m + R_{in} + R_{out}} . Q \tag{3.14}$$

Where R_{in} and R_{out} are the loaded resistors on the resonators.

For fair comparison with state-of-the-art MEMS oscillators, a standard FOM for oscillators is used [11]:

$$FOM = 10 \log \left[\left(\frac{f_o}{\Delta f} \right)^2 . \frac{1}{L(\Delta f) . p_{dissipated|mW}} \right] \tag{3.15}$$

where f_o is the carrier frequency, Δf is the offset frequency from the carrier, $L(\Delta f)$ is the phase noise atΔf, and $p_{dissipated|mW}$ is the power dissipation in milli-watts.

Two resonators (5 and 10 μm Si thickness) are connected to oscillator to compare their performance. Large R_m value of the 2nd resonator leads to smaller closed loop gain when compared to 1st resonator case (Figure 3-6b). Such smaller gain affects the phase noise floor, where design 2 has a higher floor by 1.5 dB when compared to design 1; this is a result of smaller signal swing to the squaring buffer, and thus smaller slew rate signal to the input of the cascaded inverters, which is translated to inverter's higher static current (the time where both NMOS and PMOS transistors are on is increased). Design 2 consumes 930 μA for the same transistors sizing used in design 1 which consumes 850 μA.

2nd Resonator's higher Q translates to better 3dB in close-in phase noise when compared to 1st resonator (Figure 3-7). This higher Q with lower close loop gain negatively impacts the oscillator's startup time to reach 650μs instead of 250 μs as the case of 1st resonator. FOM of 1st and 2nd designs are 216, and 215 dB respectively at 100 kHz offset frequency. Integrated rms jitter calculated from 10 kHz to 20 MHz for 1st and 2nd oscillators are 106 fs, and 125 fs, respectively. Both oscillators (active circuit) showed a maximum pulling effect of 78.5 ppm over the industrial temperature range, which should be added to

resonator's TCF for accurate judgment of temperature stability. It is clear that design 1 overweight design 2 in terms of FOM, jitter, power consumption, and startup time. Design 2 shows better 3dB phase noise values for frequency offsets smaller than flicker corner.

3.5. Results Discussion and Comparison with Previous Work

Table 3-1 compares the proposed design to other published papers. [18, 19] use electrostatic resonators. Those are characterized by a very high Q due to the usage of single crystal silicon as only device material; this helps lowering the power consumption despite the resonator's high motional resistance (kilo Ohms) that leads to high phase noise. On the other hand, *AlN* bulk resonators [12, 65] are characterized by small motional resistance because of the superior η however they suffer from low Q due to abandoning the low acoustic loss Si. Our work combines *AlN* and Silicon in a composite structure resulting in low motional resistance and high Q; which is the same solution offered in [11].

However targeting 1GHz resonance frequency [11] using contour mode resonator results in lower Q than ours due to damping issues (as shown in Equation 2.4); moreover high power consumption is needed for 1GHz oscillator.

Our work is the first to target low resonance frequency oscillators using *AlN* on silicon thus saving power through high Q, high η resonator, and simpler circuitry. Connecting the resonators on the sources of cross coupled transistors helps to maintain the resonator's unloaded Q and avoid degrading it, which explains the superior close-in phase noise results when compared to capacitive high Q resonators that are combined with noisy high gain multistage amplifiers to overcome resonator's losses modeled as R_m [18, 19]. Superior phase noise floor was a result of carefully designed duty cycle corrector and inverter buffers for the smallest rise and fall time durations, which is enhanced using 32 nm kit technology. [11, 12] have similar FOM to our work relying on

very high resonance frequency (Equation 3.15); yet worse phase noise levels at all frequency offsets.

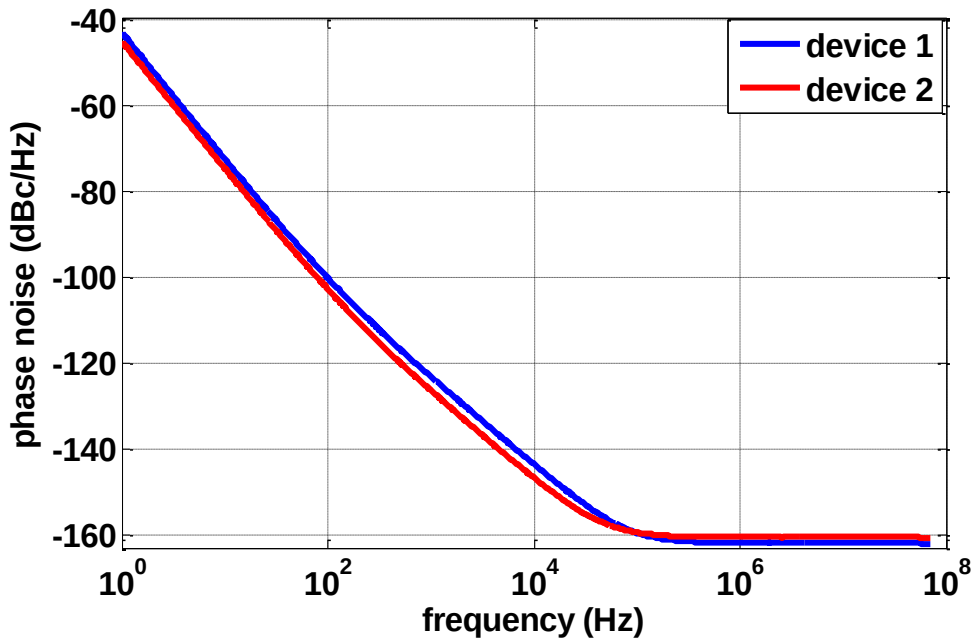

Figure 3-7: phase noise plot

3.6.IBM- 65nm Tapeout

The design is ported to IBM-65nm. Using 1.8 V IO devices, post layout phase noise results are shown in Figure 3-8. Worst phase noise case is for the lowest gain oscillator (high temperature, slow transistor, minimum resistance, maximum capacitance, and minimum supply), and the best phase noise for the highest gain conditions (low temperature, fast transistor, maximum resistance, minimum capacitance, and nominal supply). The oscillator consumed 900 μA, with FOM (@ 100 kHz) = 215.

When compared to 32nm design, porting to 65nm worsens the oscillator's FOM as more 50 μA is consumed. The new design gives a lower 3dB phase noise levels at all frequency offset lower than 100 kHz.

Layout is shown in Figure 3-9, occupying only 0.032 mm^2.

Table 3-1: Performance summary

Spec		**This work**		[64]	[18]	[11]	[19]	[65]	[12]	[23]
CMOS process		**32 nm I/O (0.18µm)**		0.13µm	0.6 µm	0.18µm	0.35µm	0.35µm	0.5µm	-
MEMS Resonator		***AlN* on silicon**		FBAR	capacitive	*AlN* on silicon	capacitive	*AlN* Bulk	*AlN* Bulk	ZnO on silicon
		Design1	**Design2**							
Frequency(MHz)		**76.8**	**76.8**	600	5.5	1006	61.2	78.79	1000	90.4
power (mW)		**1.53**	**1.67**	5.6	1.9	7.2	0.78	11.8	3.5	-
RMS jitter (fs) (10k-20MHz)		**106**	**125**	50	-	-	-	-	-	-
FOM(@100kHz)		**216**	**215**	208	-	214	-	-	215	-
Q		**9950**	**13380**	-	$>10^5$	7100	48000	1061	1450	4100
R_m (Ω)		**125**	**160**	-	10k	150	1.5k	790	82	500
PN (dBc/Hz)	10Hz	**-72.2**	**-75**	-	-66	-	-	-	-	-
	100Hz	**-100.3**	**-103**	-69	-92	-	-	-	-	-
	1kHz	**-123**	**-126.5**	-98	-112	-94	-110	-80.8	-81	-
	10k Hz	**-143**	**-146.4**	-126	-	-122	-128	-	-	-
	100kHz	**-159.5**	**-159.5**	-140	-	-	-132	-	-140	-
	Floor	**-162**	**-160.5**	-150	-135	-154	-	-	-146	-
TCF (ppm/˚C)	material	**0.825**		-	-	-	-	-	-	-
	electronic	**-**		-	0.39	-	-	-	-	-

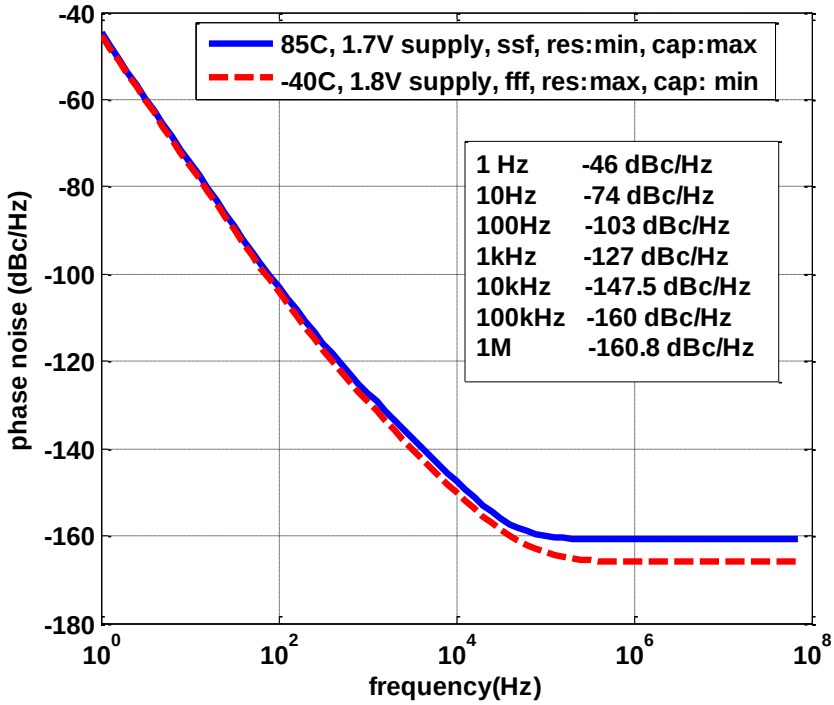

Figure 3-8: post layout phase noise for 65nm node

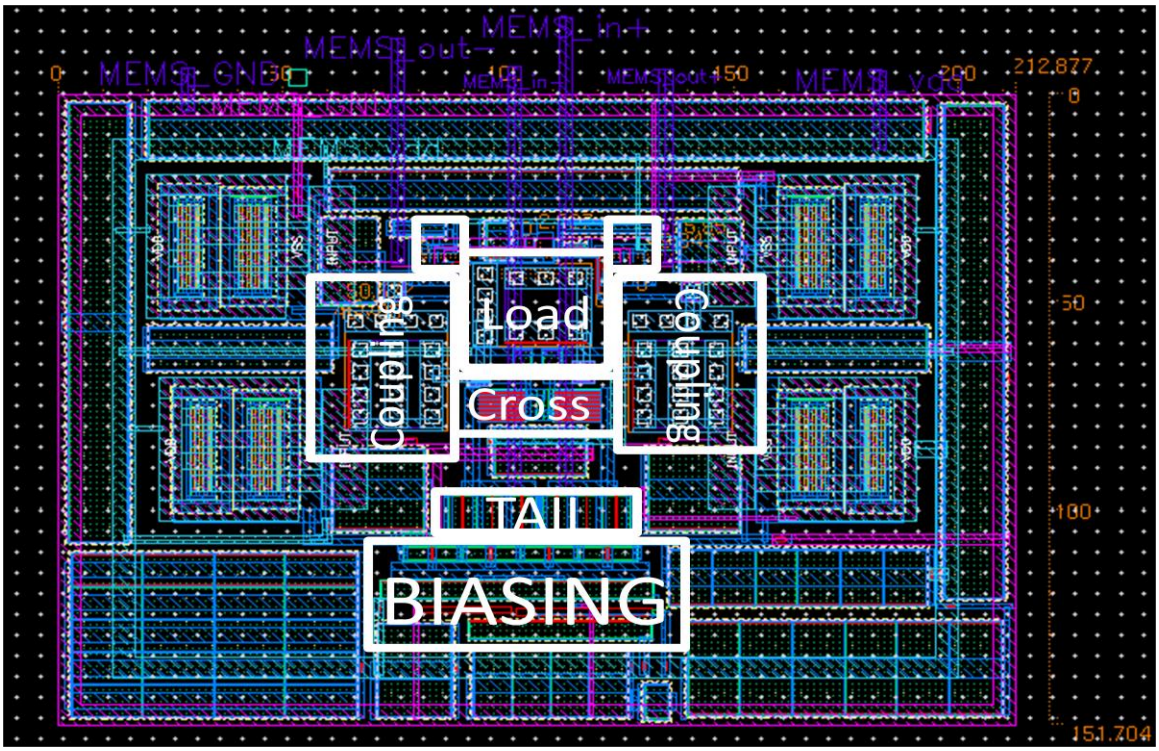

Figure 3-9: Layout (65nm node)

4.Temperature to Digital Converter

Reference oscillators have to be very high short-term and long-term accurate to meet the stringent requirements for modern radio transceivers. The short-term accuracy is related to phase-noise and unwanted spurs, the long-term accuracy needs an accurate temperature compensation solution [25].

In Chapter 2 we discussed the material temperature compensation which helped in enhancing the MEMS resonator temperature stability from -3000 ppm to about 105 ppm across temperature range of -40˚C to 85˚C. Material compensation doesn't help in compensating fabrication tolerances, urging for electronic compensation [66-74] which may reach to (±8000ppm) [67]

Electronic temperature compensation platform is needed to reach the required temperature stability for LTE standards (less than 2.5 ppm over the temperature range) [15]. Any temperature compensation system should include the basic blocks shown in Figure 4-1. The system essentially consists of temperature sensor (Thermistor or band gap front end circuitry + converter (ADC or FDC)), compensation circuitry (analog or digital) and frequency tuning mechanism. The temperature sensor presented in this chapter is based on substrate PNP BJT transistors. Sigma–delta ADC is used to digitize the temperature dependent voltages generated from the band gap circuitry front-end.

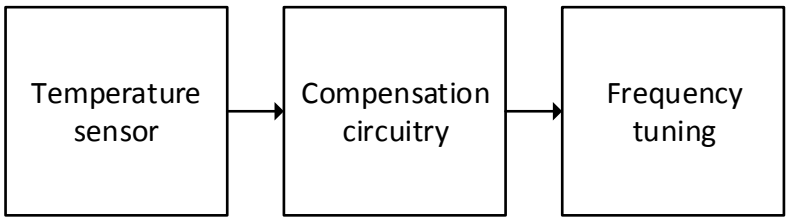

Figure 4-1: Essential blocks in any temperature compensation system

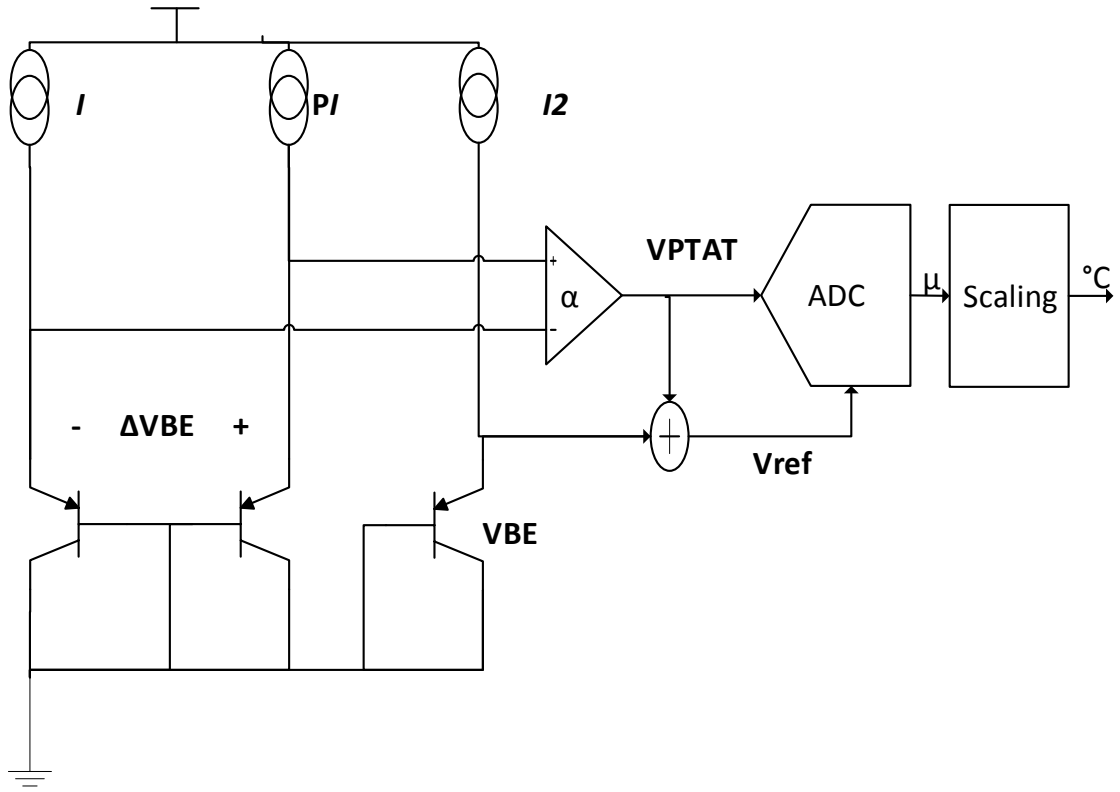

Figure 4-2: TDC system level

A CMOS smart temperature sensor [75-81] consists of voltage-temperature dependent and independent generators and ADC to digitize the output. The voltage needed can be generated from thermistor, or Band gap reference circuits that are famous of using substrate PNP bipolar transistor in CMOS process. Thermistor is more accurate than bipolar temperature sensing, especially when we are targeting SIP solution for the MEMS oscillator [71], the MEMS die can include a thermistor to sense the MEMS die temperature, while the sensor interface circuits and ADC are included on the CMOS die. A Band gap circuitry will sense CMOS die's temperature not the MEMS die's which is not accurate; moreover, the accuracy will be limited by how the two dies are connected. Moreover, band gap references usually have low effective signal to noise ratio due to the small temperature-to-voltage signal generated (PTAT, and CTAT), which complicates efforts of achieving an extremely low-noise temperature to digital converter. However in

this thesis, the thermistor option will be neglected for the sake of a more standardized CMOS platform for the MEMS oscillator, as it is fairly costly to integrate high-quality bipolar devices on the MEMS die as desired for best thermal tracking of the MEMS resonator [71].

The band gap circuitry front-end and Sigma-delta ADC are presented in this chapter in both system and circuit levels. Accuracy, noise and power consumption are analyzed and settled the main specifications of the sensor.

4.1.High System Level

4.1.1. Temperature measurement using bipolar transistor

We are mainly interested in two voltages, the difference in base-emitter voltages ΔVBE, and an absolute base-emitter voltage VBE [54, 75]. In principle, these voltages can be generated using two transistors, or using a single transistor to which different bias currents are successively applied. To separate the accuracy issues related to ΔVBE from those related to VBE; three transistors are used in the conceptual Figure 4-2.

$$\Delta VBE = \frac{KT}{q}\ln(p) \tag{4.1}$$

From Equation 4.1, one can notice that ΔVBE is independent of the absolute bias current and saturation current of transistors, it only depends on the current ratio.

VBE is generated using the third bipolar transistor. VBE given in Equation 4.2 depends on the absolute value of the saturation current I_s and the bias current I_2.

$$VBE = \frac{KT}{q}\ln\left(\frac{I_2}{I_s}\right) \tag{4.2}$$

VBE extrapolated value at 0K is typically 1.2V (the silicon bandgap energy), from where it decreases linearly by typically − 2mV / ˚C (Figure 4-3). In practice, VBE suffers from non-linearities with temperature, this is called the curvature of VBE and it can be corrected via different ways, however this is out of thesis scope. Vref can be generated as given in Equation 4.3

$$Vref = VBE + \alpha \cdot \Delta VBE \tag{4.3}$$

Where α is chosen in such a way that the temperature coefficients of VBE and α ΔVBE have an equal magnitude and opposite signs to have an independent temperature voltage Vref. Thus,

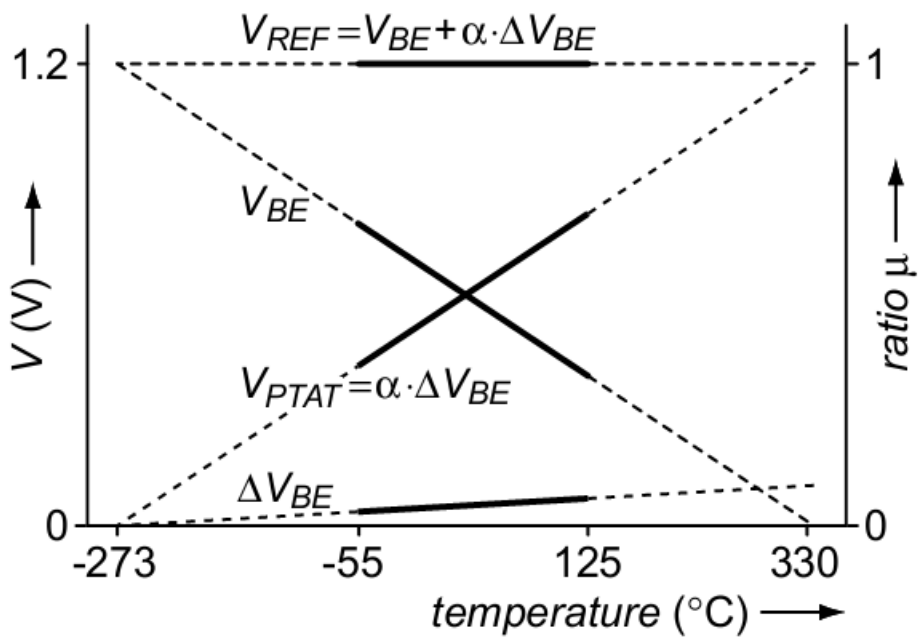

Figure 4-3: temperature dependency of needed voltages [75]

$$\alpha = -\frac{\partial VBE}{\partial t}\frac{q}{k\ ln(p)} \tag{4.4}$$

With ∂VBE /∂T= −2mV / ˚C, typical current density ratios p are between 3 and 16, thus the value of α should range between 8 and 20.

ADC digitizes the temperature signal, it takes VPTAT = α ΔVBE as input and VREF as reference. The output μ of the ADC is as follows

$$\mu = \frac{VPTAT}{Vref} = \frac{\alpha \cdot \Delta\mathrm{VBE}}{\alpha \cdot \Delta\mathrm{VBE} + \mathrm{VBE}} \tag{4.5}$$

Which is PTAT also since Vref is temperature independent. Finally the output of ADC should be scaled to get the final temperature sensor output in degrees Celsius D_{out}.

$$D_{out} = A\,\mu + B \tag{4.6}$$

Since μ is a fraction thus it ranges from 0 to 1, the full scale temperature has to cover μ range. A is typically 600k, and B is -273k as shown in Figure 4-3. Circuits generating A, and B will be covered in this chapter. However we are interested in the industrial temperature ranges that start from -40 ˚C to 85 ˚C. This is almost 20% of the full scale temperature.

The most critical parameters in the system are VBE, ΔVBE, and α. Therefore, it is useful to calculate the expected temperature error generated due to errors in the above parameter values. Sensitivity of D_{out} can be calculated by differentiating it with respect to VBE, ΔVBE, and α as shown below and sketched in Figure 4-4.

$$\mathrm{S}D_{out|VBE} = \frac{-T}{Vref} \tag{4.7}$$

$$\mathrm{S}D_{out|\Delta VBE} = \frac{A-T}{Vref}\alpha \tag{4.8}$$

$$\mathrm{S}D_{out|\alpha} = \frac{T}{\alpha}\left(1 - \frac{T}{\mathrm{A}}\right) \tag{4.9}$$

Figure 4-4 can be used to translate maximum error required in sensor's output ΔT (System's specification) to maximum error in VBE, ΔVBE and α

$$|\text{max error (VBE)}| < (3\text{mv}/^{\circ}\text{C}) \cdot \Delta\mathrm{T} \tag{4.10}$$

$$|\text{max error } (\Delta\text{VBE})| < (3\text{mv}/^{\circ}\text{C}) \cdot \Delta\mathrm{T}/\,\alpha \tag{4.11}$$

$$|\text{max error } (\alpha)| < (\tfrac{2}{3}\%/^{\circ}\text{C}) \cdot \Delta T \quad (4.12)$$

$$|\text{max error } (A)| < (0.25\%/^{\circ}\text{C}) \cdot \Delta T \quad (4.13)$$

$$|\text{max error } (B)| < \Delta T \quad (4.14)$$

The above values are calculated using Vref=1.2, and A=600k.

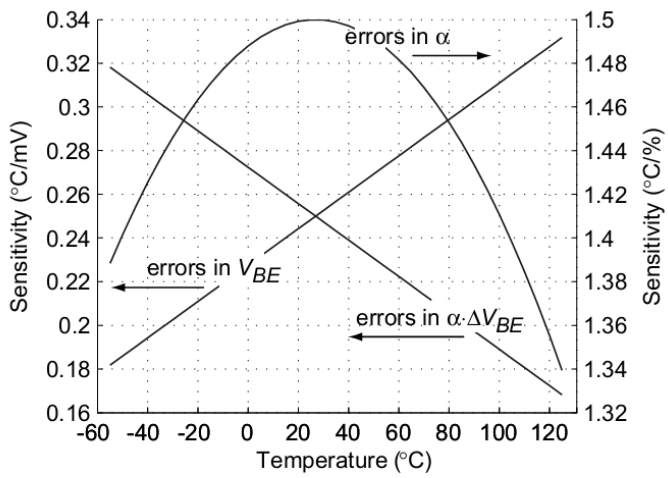

Figure 4-4: sensitivities of temperature sensor output to different parameters errors [75]

4.1.2. Analog to digital Converter

ADCs used in sensor applications usually require high absolute accuracy, high resolution, low power consumption, and good linearity. Offset and gain errors cannot be tolerated. The realization of high resolution nyquist rate converters becomes very expensive when the resolution exceeds 16 bits. ΣΔ modulation [82-84], utilizing oversampling and noise shaping, is a well known technique incorporated in incremental ADCs [85-87]. These ADCs deliver good sample-by-sample conversion performance. In sensor applications the goal is to digitize individual samples or the average value of a noisy dc signal with very low power consumption, unlike telecommunications where a running waveform needs to be digitized continuously, and mainly the spectral behavior of the signal is important.

The resolution required at the output of the ADC should be high enough to make quantization noise insignificant compared to the accuracy requirement of the sensor in order to accurately sense the absolute temperature of the environment. A sensor with a required inaccuracy of ±0.1˚C, a resolution of ±0.01˚C makes quantization errors negligible.

As mentioned earlier, Equations 4.10-4.14 showed the maximum error in VBE and ΔVBE for a given maximum temperature error ΔT. By principle the ADC should not add to these errors, thus one should make sure that ADC's offset, gain errors and non-linearity have to meet the same requirements. To make it clearer let us consider this example, for a maximum temperature error of ± 0.01˚C and a value of α =10, the maximum input-referred offset that the ADC can add to ΔVBE is only ± 3 μV, as shown in (4.11).

The ENOB of the ADC is usually a figure of merit for the AC performance; this term will be used in this thesis to quantify the DC performance [75]. It will be used to express the fact that an ADC's peak quantization error over its DC input range (including offset errors, gain errors, non-linearity) equals that of an ideal ADC with the same number of bits, knowing that the quantization error of an ideal ADC is <±0.5 LSB. ENOB is expressed as

$$ENOB = \log_2\left(\frac{D_{FS}}{\max\left|D_{out-}D_{out_{ideal}}\right|}\right) - 1 \tag{4.15}$$

Where D_{FS} is the full scale temperature, and $D_{out-}D_{out_{ideal}}$is the resolution required. As discussed previously, our temperature range of interest is −40˚C to85˚C which roughly corresponds to μ=0.36 to μ=0.59. About 23% of the ADC's temperature full scale (600 ˚C) is used. A maximum quantization error of ±0.01˚C leads to ENOB of 14.9 bits. This ENOB specification has to be met over the part of the voltages input range that is actually used. Smart temperature sensors bandwidth is typically limited by the thermal properties of its package, and is in the order of 10 Hz; this condition settles the minimum value of the ADC bandwidth. Thus the sensor should take 10 readings per second [15].

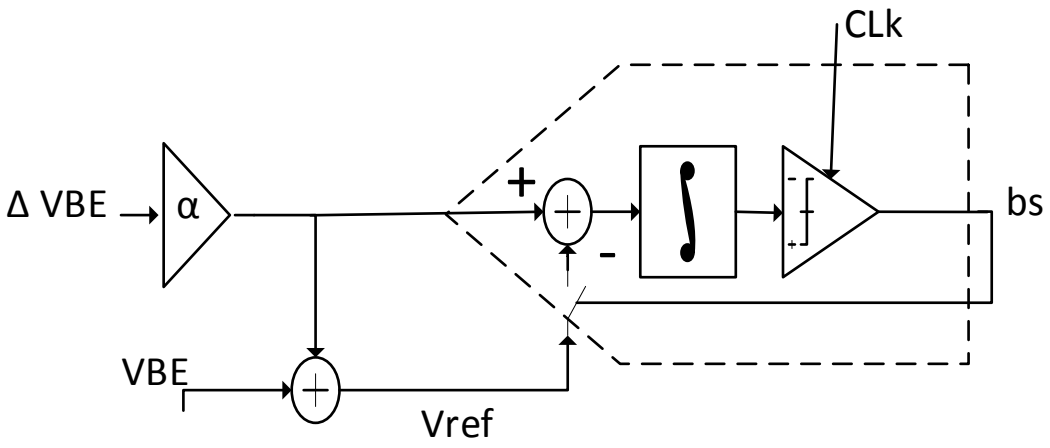

Figure 4-5: Conceptual diagram for the sigma delta modulator

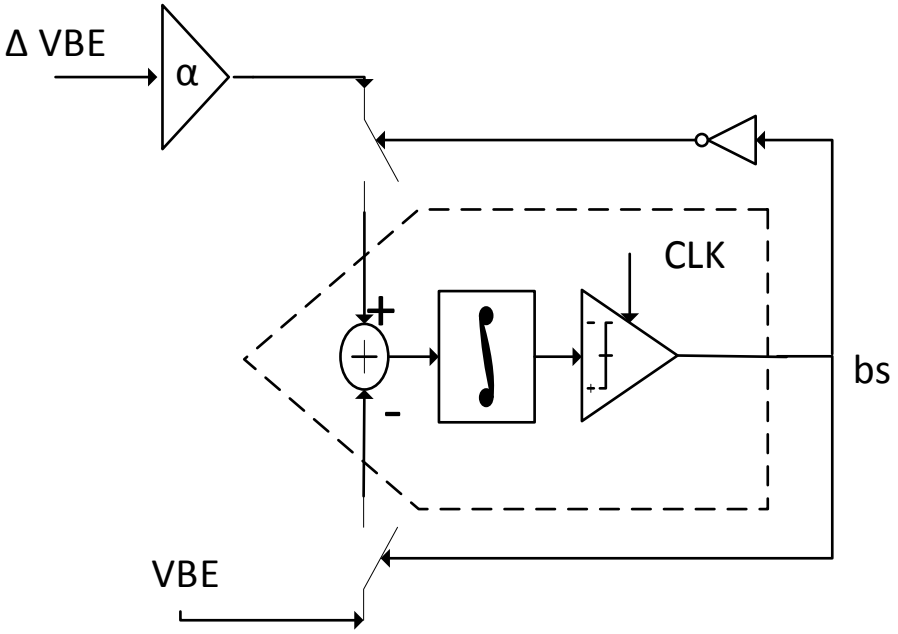

Figure 4-6: Alternative way for charge balancing concept

The conversion from the voltage domain to the time domain using sigma-delta ADC is done by a modulator (the hashed box outline in Figures 4-5 and 4-6), which typically consists of at least one integrator and a comparator [82].

To generate μ (the average value of ADC output) according to Equation 4.5, the input of ADC should be $\alpha \cdot \Delta VBE$ and the reference is $\alpha \cdot \Delta VBE + VBE$, if this is applied to ADC as shown in Figure 4-5, the input to the integrator should be $\alpha \cdot \Delta VBE$ if bs=0 or –VBE if bs=1. The same output can be generated using a simpler system as shown in Figure 4-6. In this case, either $\alpha \cdot \Delta VBE$ or –VBE is applied to the integrator according to the comparator output (bs). An accurate reference voltage Vref is not needed anymore which will heavily ease the design.

4.1.3. Errors in sensor readings

Noise and accuracy specifications are the most important specifications in any read-out circuitry. As it is known in circuit design, the noise and accuracy performances of a sensor can be improved at the cost of higher power consumption. However power consumption, cannot be increased indefinitely, leading to self-heating, which in turn results in a measurement error. This error depends on many factors, such as the die size, the type of package, and the way the package is mounted [75]. The maximum current supply for the whole system can be calculated using the following equation

$$I = \frac{\Delta T}{\theta_{JA} \cdot V_{DD}} \tag{4.16}$$

Where $\theta_{JA}$is the thermal resistance from the die to the environment (junction to ambient), ΔT is the steady state temperature rise. According to [75] for most packages, the supply current has to be limited to a few tens of μA in order to keep the self-heating in the order of 0.01 K., one has to mention that this problem can be mitigated by powering down the sensor between measurements rather than continuous operation.

Noise is mainly generated from the bipolar transistors, integrator, and switches in case of Switched cap ΣΔ ADC. Noise is accumulated in the system due to integration process, either during a complete ΣΔ conversion or individual ΣΔ cycle. The final temperature

noise standard deviation formula is given in Equation 4.17, the proof can be found in [75].

$$\sigma_T = A \cdot \frac{q_{n,\Delta VBE}}{Q_{\Delta VBE} + Q_{VBE}} \sqrt{\frac{1-\mu}{N}} \tag{4.17}$$

Where $q_{n,\Delta VBE}$ is the accumulated noise charge associated with ΔVBE, N is number of ΣΔ clock cycles needed for generation of required charges, and A is the gain needed to convert bit density μ to degrees Celsius. The above equation represents the output referred noise of given readout circuit; this noise can be calculated by estimating the noise charges($q_{n,\Delta VBE}$) integrated during a single ΣΔ cycle in which ΔVBE is integrated

$$q_{n,\Delta VBE} = \alpha \sqrt{\frac{2kT}{gm} t_{clk}} \tag{4.18}$$

Where gm is transconductance of bipolar transistor carrying the smaller current gm = (I·q/K·T), and t_{clk} is the one cycle period.

Submitting 4.18 into 4.17, we get

$$\sigma_{T,bipolar} = A \cdot \frac{\alpha}{Vref} \sqrt{\frac{2kT(1-\mu)}{gm \cdot N \cdot t_{clk}}} \tag{4.19}$$

Equation 4.19 computes the output referred noise due to bipolar front end. This noise can be reduced by increasing the gm and thus the current consumption in the bipolar transistors; making sure that we never hit the self heating current consumption limit. Increasing conversion time (Nt_{clk}) will reduce noise too, moreover reducing the gain α will decrease the noise but this has to be compensated with higher p current ratio in ΔVBE bipolar transistors (Figure 4-2). To have some sense to the values, let us consider this example for example, if tconv = 100 ms, α =10, and I=1 µA, A=600, Vref=1.2, and μ=0.5, thus σT =0.16 mK. This small value shows that the noise generated by the bipolar

transistors is negligible. The output noise will be mainly determined by quantization noise and thermal noise of ADC.

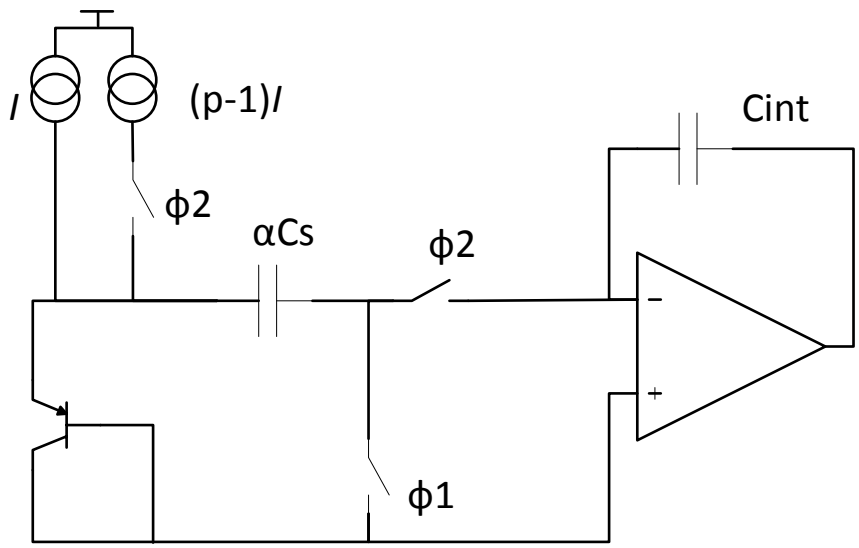

Figure 4-7: integrator circuit implementation

As shown in Figure 4-7, the integrator is implemented in switched capacitor circuitry [84] which is well known in CMOS circuits. The input voltage is sampled on a capacitor Cs and the accumulated charge is integrated using capacitor Cint. Either CTAT or PTAT voltages are sampled in a single ΣΔ modulator's clock cycle depending on the modulator's output bitstream as discussed earlier. The integrator uses 2 non overlapping clock phases ($\varphi 1$ and $\varphi 2$) for sampling and integration respectively. Figure 4-7 shows how ΔVBE is integrated. During phase φ1, VBE is sampled. In phase φ2, the bias current is increased to a total of pI, thus, the voltage across Cs increases by ΔVBE, where the transferred charges are accumulated on Cint. The gain α is realized using a larger Cs for sampling ΔVBE, for the sake of equating ΔVBE and VBE voltages TCF. Matching between αCs used for ΔVBE sampling and Cs used for sampling VBE is critical for accurate α . Matching in the order of 0.1% can be obtained via precise common centroid layout which is insufficient for temperature sensors circuits. Dynamic element matching can then be used to average out mismatch errors [75].

Offset error of the Op-amps adds directly to the ΔVBE error (Equation 4.11). Most of CMOS Op-amps typically have offsets in the mV range; thus offset cancellation techniques are required like autozeroing.

The incomplete settling of the voltage across Cs affects greatly the accuracy of α. The SC ADC should therefore be designed such that settling errors are negligible. Usually settling and slewing effects are related with power consumption, Equation 4.20 gives the minimum bias current of the PNP transistors to overcome settling problem, the proof can be found in [75]

$$I > \frac{kT}{q} 2\alpha \cdot C_s \cdot \frac{N}{t_{conv}} \cdot ln\frac{1}{\varepsilon} \tag{4.20}$$

Where ε is the max settling error needed for max temperature error (ε=0.006% for 0.01K temperature error according to Equation 4.12). If fclk =10 kHz, α =10, Cs =10pF and ε =0.006%, the minimum bias current is 0.5 µA.

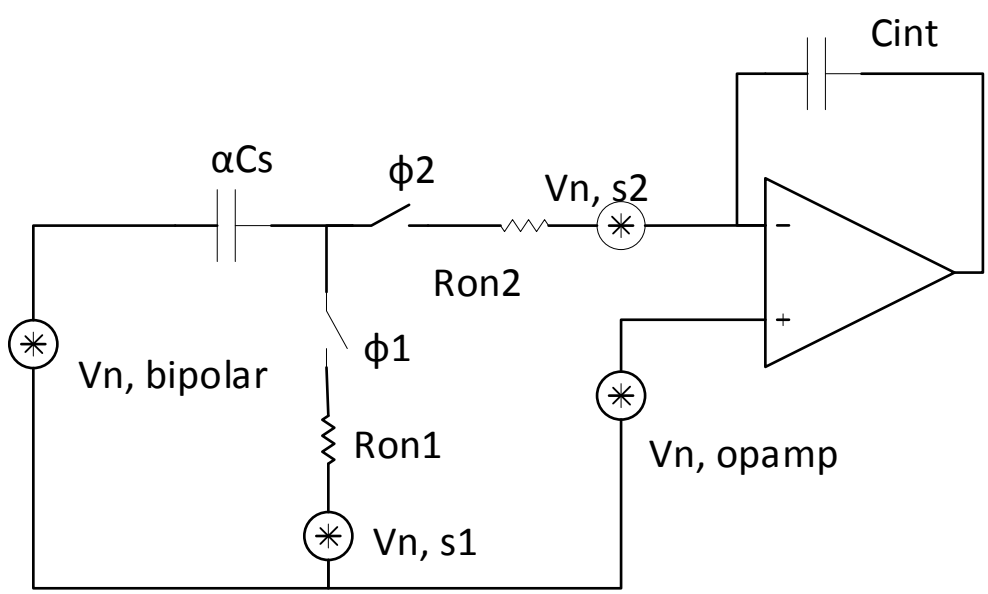

Figure 4-8: noise sources in SC integrator

Figure 4-8 shows the noise sources associated with switched capacitor integrator. The 1st noise source is $V_{n,bipolar}$ which models the noise associated with the bipolar transistor ($\sqrt{4\mathrm{kTB/gm}}$), the 2nd noise source is the thermal noise of switches (4kTRon), the 3rd noise source is the OP-amp noise.

The output referred temperature noise of the SC integrator is proved in [75], and the final formula is given in Equation 4.21

$$\sigma_{T,SC} = \frac{A}{Vref}\sqrt{\frac{3 \cdot kT \cdot \alpha \cdot (1-\mu)}{Cs \cdot N}} \tag{4.21}$$

The output noise is independent of the bias current levels. Higher bias currents reduce the voltage noise, but this is compensated for by an equal increase in the noise bandwidth, thus the rms noise remains the same.

For A=600K, Vref=1.2, μ=0.5, T=300 K, N=1000, α=10, and $\sigma_{T,SC}$= 1mK, the minimum sampling capacitance Cs is 15.9 pF.

The noise specification sets a limit on the minimum value for N·Cs to ensure that the kT/C noise is low enough. For a given t_{conv}, N·Cs determines the minimum bias current needed for the bipolar transistors and the integrator to meet settling specifications (Equation 4.20)

One has to mention that ΣΔ ADC's quantization noise settles the minimum number of clock cycles N as will be shown in the coming sections. According to the quantization noise requirements, the size of Cs can then be derived. N can be increased to reduce the capacitor size thus reducing the area but this comes at the expense of more charge injection errors.

4.2.PTAT and CTAT Generation

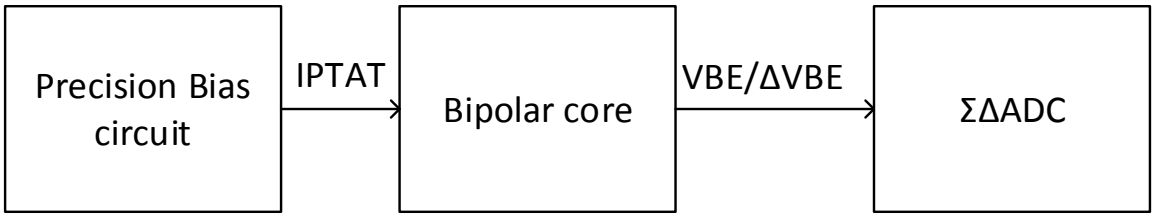

Figure 4-9: bias current and temperature dependent voltage generation

The front end sensor circuitry consists of two main blocks, a precision biasing circuit for PTAT current generation and a core circuit that decides whether to produce VBE or ΔVBE according to ΣΔ modulator output as shown in Figure 4-9 and Figure 4-10. The bias circuit is based on a textbook architecture for high precision applications [84], where PTAT current is generated using 2 PNP transistors of different PNP transistor areas (P). The bias circuit is implemented in standard cascode topology to reduce the curvature and inaccuracy due to process corners [54]. PTAT current generated is the bias current for the bipolar core part.

A single pair of PNP transistors is used to generate both VBE and ΔVBE. Bias currents for these transistors are provided by a set of 8 current sources. Via switches, these currents can either be directed to the left or the right transistor, thus 1:7 bias current ratios (P) are implemented to produce ΔVBE. The full front-end circuitry is shown in Figure 4-11. All switches used in this circuit are of minimum sizes. A combination of transmission gates and pass gates are used in the design.

In order to find the minimum current in the PNP transistor for certain output noise level (Equations 4.19-4.21), we have to develop a MATLAB system level for the modulator to settle all the unknown variables in the needed equations; like N and fclk, this takes us to the modulator design.

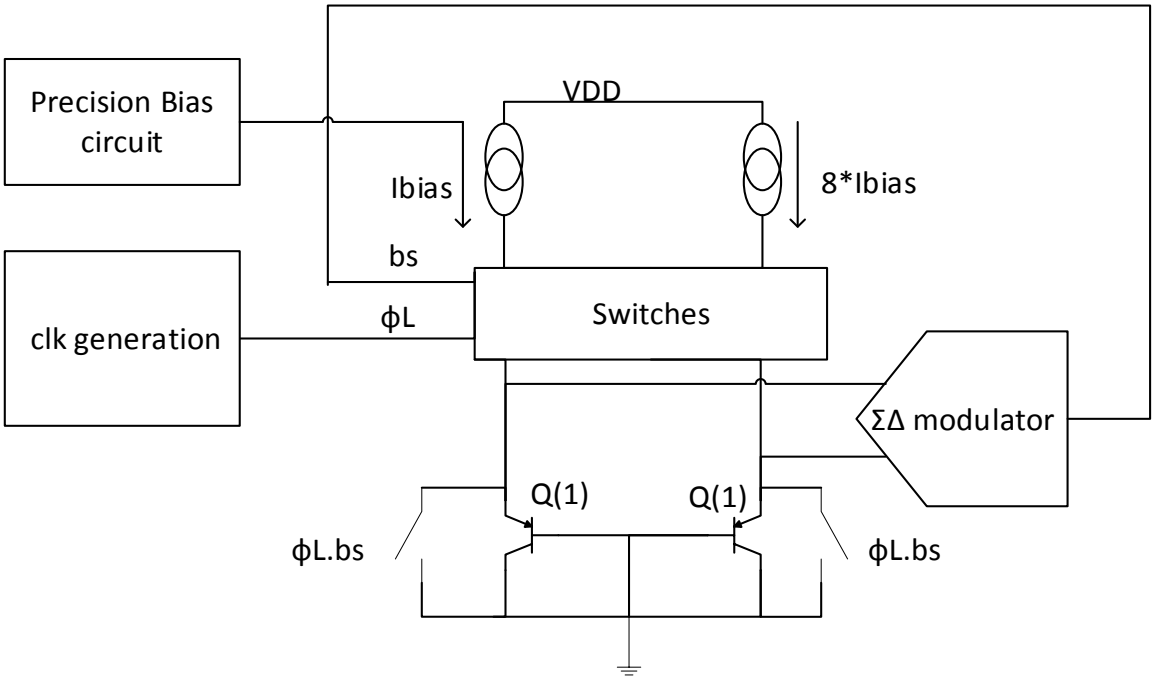

Figure 4-10: band gap circuitry core

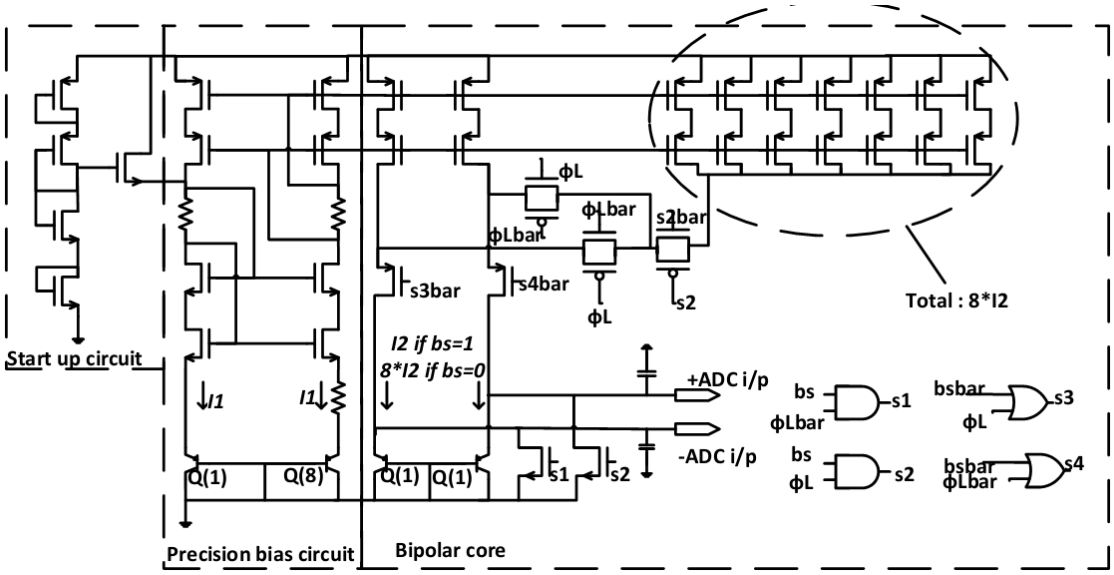

Figure 4-11: Full circuit for temperature dependent generation

4.3.2nd Order CIFF, 1 bit quantizer Sigma-Delta Modulator

In contrast with the usual continuous operation of sigma-delta ADCs that is used in wireless communications, the temperature sensor requires a “one-shot” type of operation. This type is known as incremental ADC, where the converter is powered up, produces a single conversion result, and powers down again to save power. This has implications for both the modulator, and the decimation filter. After powering up, the modulator is brought into a well-defined state by resetting the integration capacitors [78]. Both analog integrators and digital filter must be reset at the beginning of each conversion cycle.

A conceptual block diagram of a higher order incremental converter is shown in Figure 4-12. The converter consists of SC modulator, digital filter and control circuit.

Cascade-of-integrators, feed-forward (CIFF) topology [82, 85-87] with input signal fed right to the input of the 1-bit quantizer is chosen to implement the modulator as shown in Figure 4-13. CIFF architecture output has a lot of advantages for sensors applications:

- The STF of modulator is 1; the input signal is not modified in the loop.
- The signal is not processed by the integrators, easing the nonlinearity specifications on integrator’s op-amp
- Integrator’s signal swing is smaller, leading to lower scaling coefficients, faster conversion time, and lower integrator’s capacitor ratios
- Output quantization noise is independent on the input signal.

Delaying discrete time integrators are used in the linear z-model. The gain factors (a_1, a_2 and b_3) control the pole-zero map of the noise transfer function (NTF), while gain factors (b_1, c_1 and c_2) are the scaling coefficients that control the maximum integrator swing and stability. Usually b_2 is set to zero. The above advantages can be proved mathematically where output Y(z) = U(z) +NTF(z)·E(z). The integrator in the loop process only the quantization noise where U(z)-Y(z) = -NTF(z)·E(z) [85].

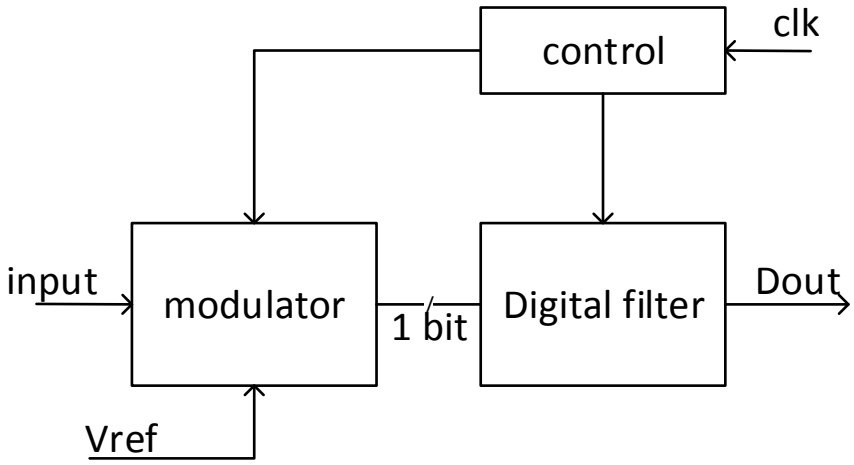

Figure 4-12: Incremental ADC

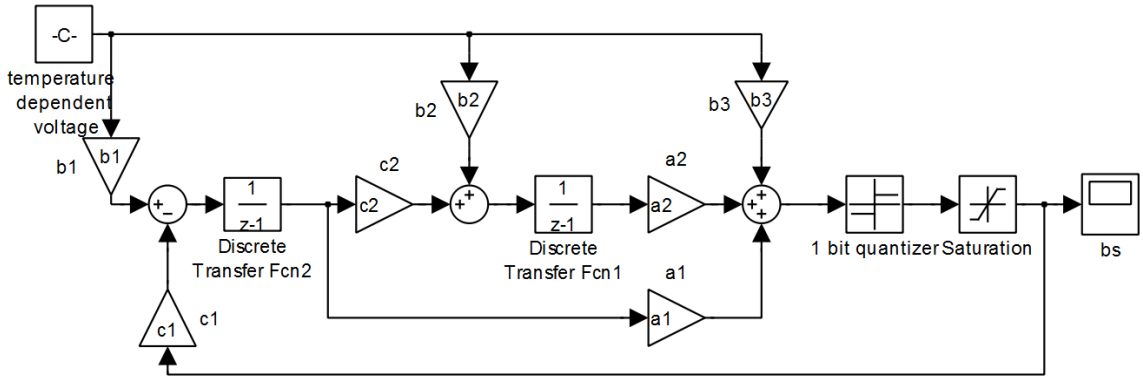

Figure 4-13: A general linear z-model for CIFF sigma delta modulator

1-bit quantizer (comparator) is used to enhance the modulator linearity, no needs for high accurate DAC to feedback the reference signal. Multi-bit feedback DAC may cause degradation in the output that is mitigated using complex linearization techniques [85]. Though comparator eases the design complexity, yet stability becomes an issue for 1-bit quantizer high order modulators, because of the ill-defined comparator's gain value. Special care must be taken when specifying the scaling coefficients to insure a stable loop. This also poses a limit on the maximum input signal level to the modulator,

maximum advised value as fraction of vref is 0.67 to insure stable operation for 2nd order modulators.

The LSB voltage, relative quantization error (q), the ENOB and SNDR of such architecture are given in equations 4.22, 4.23, 4.24 and 4.25 respectively, a proof can be found in [85]

$$V_{LSB} = \frac{2}{N(N-1)} \frac{1}{b_1 c_2} V_{ref} \tag{4.22}$$

$$q = \frac{V_{average} - V_{in}}{V_{LSB}} = 0.5 b_1 c_2 \sum_{l=0}^{m-1} \sum_{k=0}^{l-1} d_k - 0.5 b_1 c_2 \frac{N(N-1)}{2} \frac{V_{in}}{V_{ref}} \tag{4.23}$$

$$ENOB = \log_2\left(\frac{2\max(V_{in})}{V_{LSB}}\right) = \log_2\left(b_1 c_2 \frac{\max(V_{in})}{V_{ref}} \frac{N(N-1)}{2}\right) \tag{4.24}$$

SNDR=6.02*ENOB+1.76 (4.25)

Where N is the number of clock periods per conversion, d_k is the binary comparator output.

The system level design starts with finding the smallest value of N that satisfies the required resolution. ENOB increases rapidly with N (Equation 4.24) for unscaled modulator. However as $b_1 \leq 1$ and $c_2 \leq 1$ are held, ENOB decreases significantly depending on these scaling factors values. Scaling factors can't be chosen high because of the instability issues in 2nd order modulator, we should insure that the output of the last integrator doesn't exceed the reference signal. The larger the N, the smaller the scaling coefficients must be, to avoid overloading the integrators. Both scaling coefficients and N heavily depend on the maximum input signal, limiting the input signal reduces N. However large reduction of input signal will limit the dynamic range of the ADC and the achievable SNDR due to the analog noise present in the SC-converter, resulting in larger capacitor usage to reduce the noise. An optimum choice of N is necessary.

Regarding the digital filter, we chose sinc filter for implementation to suppress periodic noise. An efficient implementation, using a cascade of integrators and differentiators was introduced in [88, 89] for $\Delta\Sigma$ decimation.

An Lth-order sinc-filter with a decimation ratio of M has the FIR transfer function

$$H(z) = \frac{1}{M^L}\left(\frac{1 - z^{-RM}}{1 - z^{-1}}\right)^L \tag{4.26}$$

where $z = e^{j\omega/fs}$, L is the order of the filter, M is the decimation ratio., R is the differential delay

The Cascaded integrator comb (CIC) filter is functionally equivalent to a cascade of L uniform FIR filter stages. A conventional implementation consists of a cascade of L stages each requires RM storage registers and one accumulator [88]. The filter has zeros at frequencies kf_s/M, k=1, 2, 3,…, M-1, while the edge of the stop-band of the filter is f_s/M. If the output of the filter is decimated by M, the folded noise will be centered around f_s/M and its integer multiples, and hence will get suppressed by the notches of the filter response. Decimation filters for incremental converters are of the same modulator's order or higher by one [85].

The incremental converter usually operates in a transient mode. Analog and digital transient signals must settle accurately to achieve the specified accuracy. All memory elements in the decimator must be filled with valid data to get a correct digital output, where the CIC filter's length is L·M [88]. There are two constraints on the minimum number of N during which the converter must be operated to achieve a specified resolution. The analog modulator set a constraint on Nmin using (Equation 4.24), and the CIC filter set a constraint too which is N≥L·M. For higher order filters, the Nmin is usually determined by L·M condition.

According to [85] and Figure 4-13, the output of CIFF modulator is

$$Y(z) = U(z) + NTF(z)E(z) = U(z) + \frac{(1 - z^{-1})^{La}}{D(z)}E(z) \tag{4.27}$$

Where the D(z) represents the poles of the NTF, these poles are needed to stabilize the CIFF 1-bit modulator, control the loop gain and the NTF. They are usually arranged in Butterworth low pass configuration. The digital output after the CIC filter is

$$Dout = Y(z)\frac{1}{M^L}\left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^L = \left(U(z) + \frac{(1-z^{-1})^{La}}{D(z)}E(z)\right)\frac{1}{M^L}\left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^L \quad (4.28)$$

Thus the merged NTF of the system is

$$merged\ NTF = \frac{(1-z^{-1})^{La}}{D(z)}\frac{1}{M^L}\left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^L \quad (4.29)$$

And for a 2nd order modulator: La= 2, L=3:

$$merged\ NTF|2nd\ order = \frac{1}{D(z)}\frac{1}{M^3}\frac{(1-z^{-M})^3}{1-z^{-1}} \quad (4.30)$$

This filter transfer function is a product of pure 2nd order system FIR filter and IIR 1/D(z) filter. In time domain the convolution of the 2 impulse responses gives the required operation length which is 3M+m, where m is the length of transient IIR filter [86]., however when using CIC filters we only have access to 3M, 4M, etc, thus the transient length of the digital filter is neglected specially that M>>m.

Here are general steps for designing the ADC:

- Choose the analog modulator order L_a, thus CIC filter's order $L = L_a + 1$.
- Find Nmin settled by the analog modulator using Equation 4.24, increase Nmin until it becomes devisable by L
- Let decimation ratio M=OSR=Nmin/L
- Simulate the whole system and check the achievable ENOB.
- The clock frequency f_s is found based on t_{conv} of temperature sensor using Equations 4.19-4.21, and thus BW of temperature input DC signal can be found where OSR=f_s/2*BW, also 2*BW is found to be the first notch frequency of CIC filter as mentioned above.

- Thermal noise, capacitor sizes are found using Equations 4.19-4.21, and the scaling coefficients.
- Increase f_s until the desired SNDR is achieved, if calculations give large capacitors to use. Thermal noise will be limiting ENOB rather than quantization noise.

The modulator is designed using the Delta-Sigma Toolbox in MATLAB [82]. Design specifications are found below:

- Quantization noise of $\pm 0.075^{\circ}$C
- 12 bit ADC is required according to equation 4.15
- SNDR=74 dB according to Equation 4.25
- 2nd order modulator, 1 bit qunatizer according to [82]
- 3rd order CIC filter
- For peak SQNR of 80 dB, an OSR of 64 is needed [82]→ N=64*3=192 cycles
- Butterworth high pass NTF filter has a maximum gain of 1.5
- NTF zeros are located at DC [85]
- maximum input signal is $0.67V_{ref}$
- CIFF realization of the modulator to get the required NTF.
- Conversion time of 0.1 seconds
- Clock frequency = 1920 Hz
- BW of the input signal = 15Hz

Using the above specifications, the targeted NTF is as follows,

$$NTF = \frac{(z-1)^2}{(z^2 - 1.225z + 0.4415)} \tag{4.31}$$

This means that there are 2 zeros at DC for better suppression of noise at low frequencies, the pole-zero map, and the NTF are shown in Figure 4-14 and 4-15 respectively. Table 4-1 list the modulator scaled coefficients.

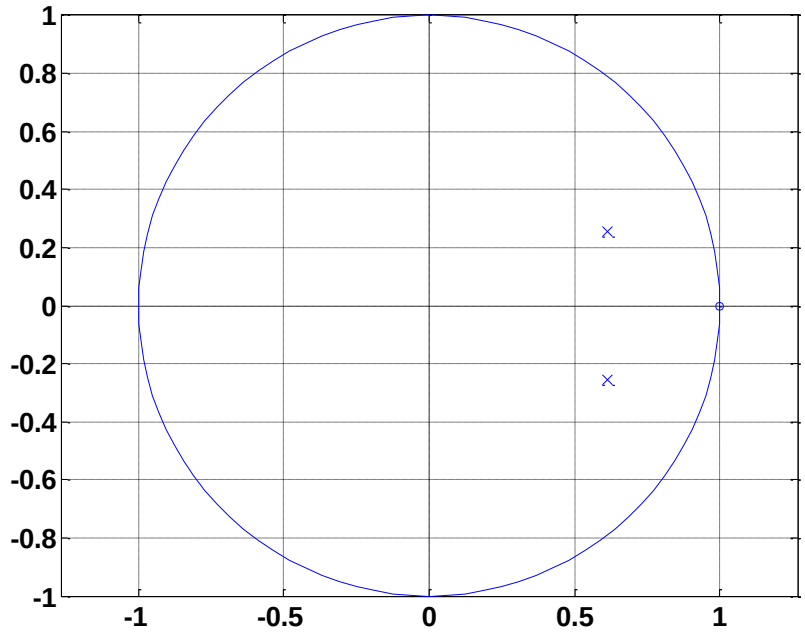

Figure 4-14: pole-zero map for NTF

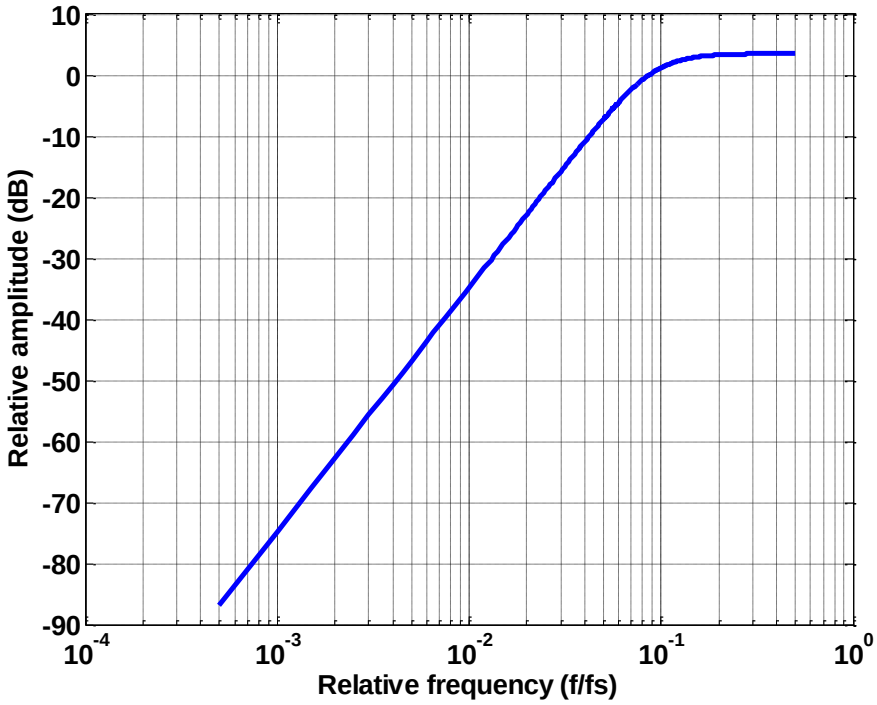

Figure 4-15: Noise transfer characteristics of 2nd order sigma delta modulator

Table 4-1: CIFF 2nd order modulator scaled coefficients values based on maximum input=0.67 vref

coefficients	a1	a2	b1	b2	b3	c1	c2
Un-scaled	0.7749	0.2164	1	0	1	1	1
Scaled	0.9694	0.5927	0.7993	0	1	0.7993	0.456
Used in design	1	0.6	0.8	0	1	0.8	0.5

After setting the current and noise specification of the bipolar font end, the simulations results can be presented. The ΔVBE, VBE temperature behavior is shown in Figure 4-16. The temperature slope of the ΔVBE is about 174 μV/ºC, while that of VBE is - 2mV/ºC, and according to Equation 4.4, α=11.5, thus vref=1.2.

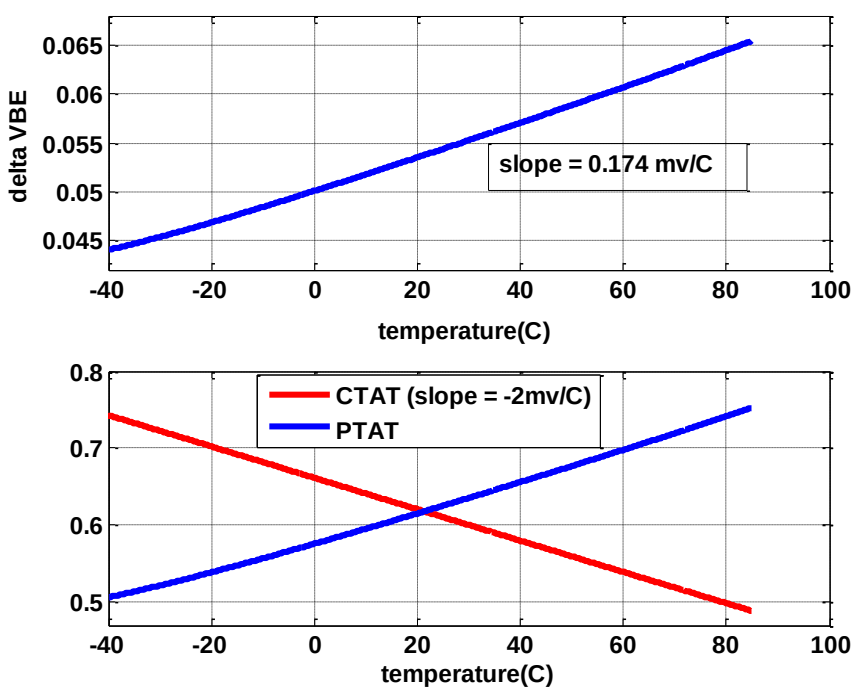

Figure 4-16: PTAT and CTAT temperature behavior

According to the above specifications [N=192, vref=1.2, A=600, α=11.5, Cs=1pF, μ=0.5, fclk=1920 Hz, $\varepsilon = 0.05\%\ for\ \pm 0.075^{\circ}$C resolution] and Equations 4.19-4.21, we get a

minimum I= 8.7 nA, $\sigma_{T,Bipolar|8.7nA} = 2\ mK$, and $\sigma_{T,SC} = 9.65\ mK$ at 300 K. it is clear that noise at the temperature sensor front end is less than that of sigma delta modulator. The current consumed in each branch of bias generator circuit is 0.2 μA, which is large enough to ensure that the saturation current of the PNPs does not significantly degrade the accuracy of the desired 1:7 current ratio. Although a smaller ratio would further reduce the power, it decreases the sensitivity of ΔVBE (now 0.174mV/°C at room temperature), which increases the requirements on the precision of the SC ΔΣ modulator and necessitates a larger gain factor α [80]

Figure 4-17 shows the modulator as realized with switched capacitor circuits. All switches are of minimum size to enhance OP-amps linearity, and to decrease the loading on the OP-amps. Switches at the output of the OP-amps are implemented as transmission gates, and as pass N-MOS gates at the inputs of the OP-amps. Care should be taken while designing the first Op-amp as it settles the ENOB specifications of the modulator. The design of the 2nd Op-amp is much easier as its noise will be of less effect due to the NTF function of the 1st stage. Figure 4-18 shows the non-overlapping clock generation circuitry to generate the needed clocks for SC operation. Figures 4-19 and 4-20 shows the OTAs used in designing the 2 OP-amps.

Both OTAs are folded cascode. The first OTA uses SC CMFB for the sake of a larger swing; the 2nd OTA uses the conventional CMFB circuitry. Each OTA consumes 1.5 μA, with DC magnitude gain of 71 dB (Figure 4-21). This current is needed for complete charging and discharging of the capacitors. The size of the sampling capacitors is a trade-off between settling time on the one hand and kT/C noise and charge injection errors on the other [80].

Table 4-2: Sampling and integration capacitances

$C_{\text{sampling1}}$ = 1.5 pF	$C_{\text{integeration1}}$ = 7.5 pF
$C_{\text{sampling2}}$ = 1 pF	$C_{\text{integeration2}}$ = 2 pF

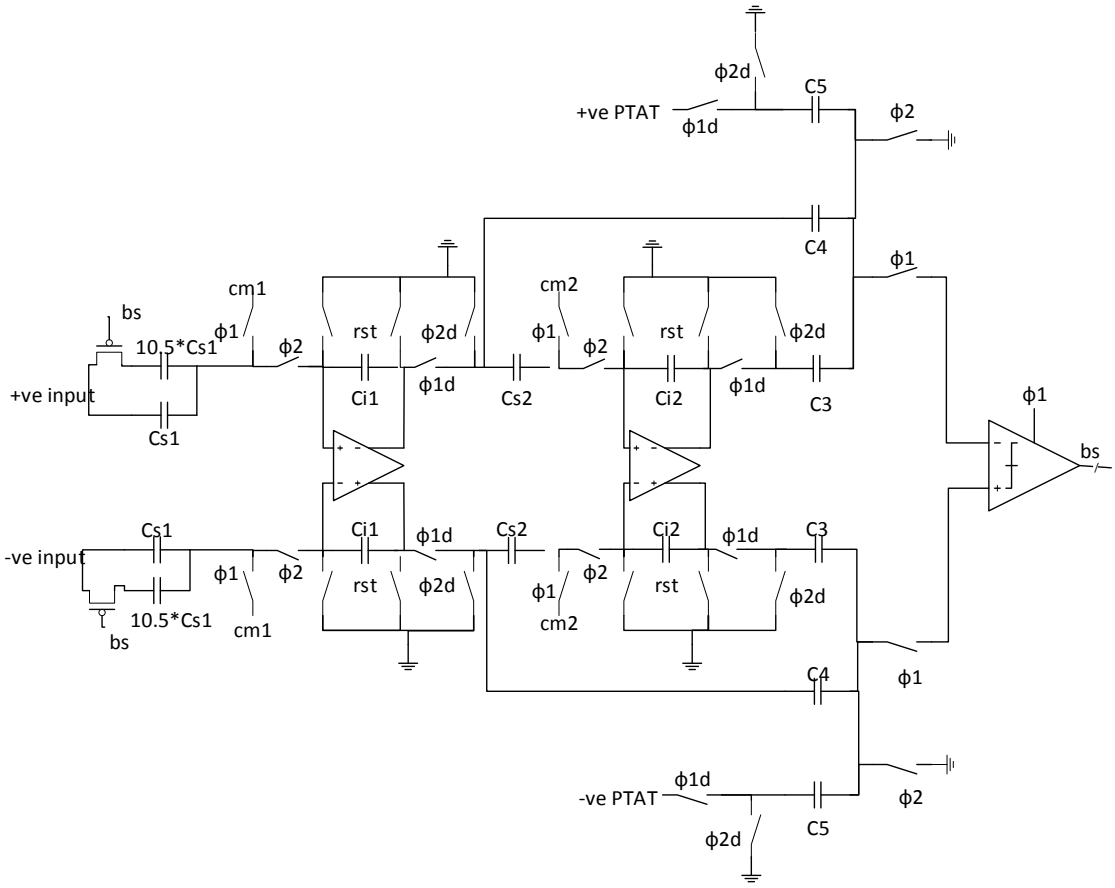

Figure 4-17: A simplified realization of 2nd order, 1 bit CIFF sigma delta modulator as fully switched capacitor circuit.

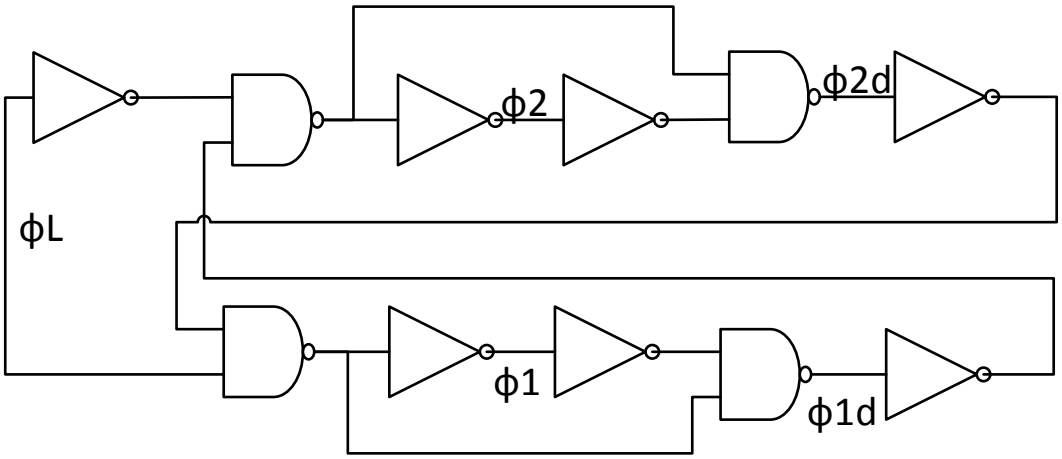

Figure 4-18: non overlapping phases clock generation

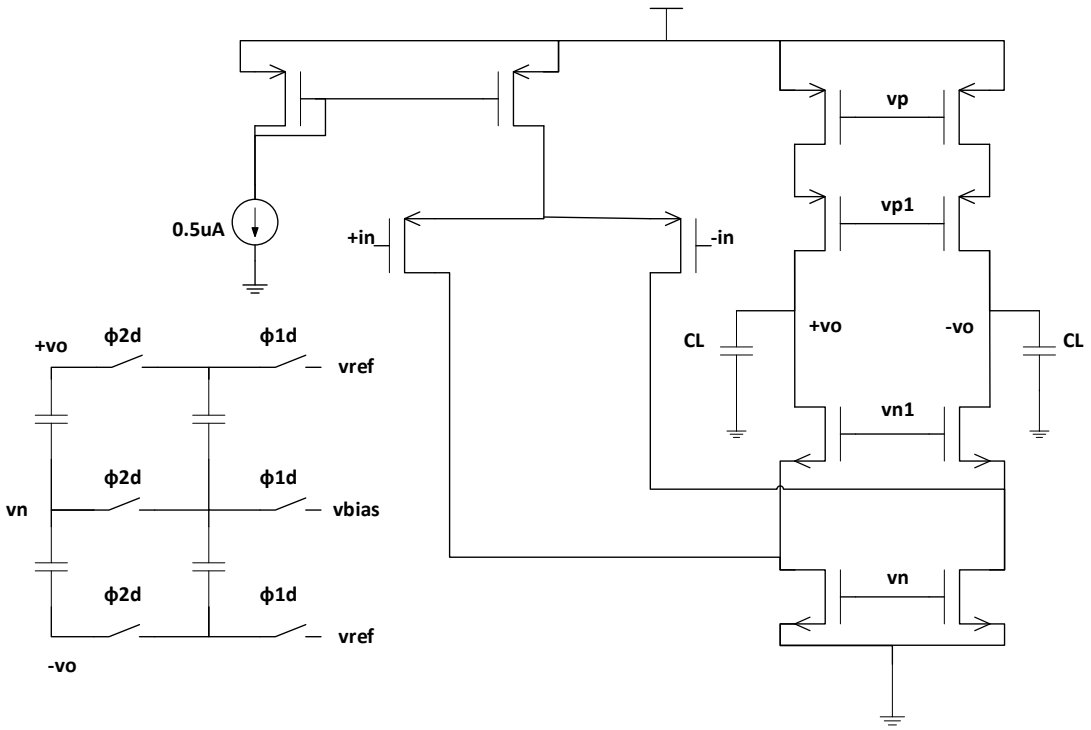

Figure 4-19: folded cascode OTA for 1st OTA

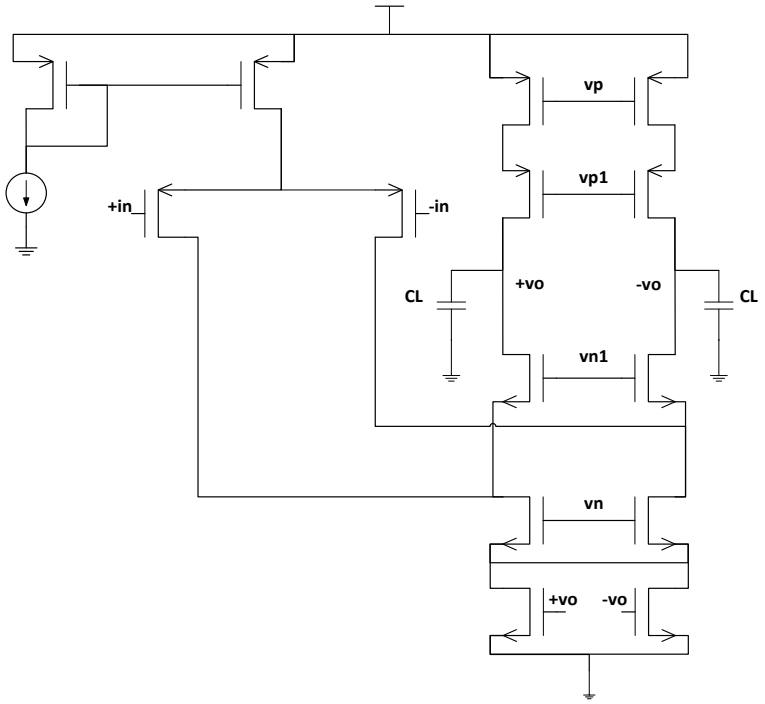

Figure 4-20: folded cascode for 2nd OTA

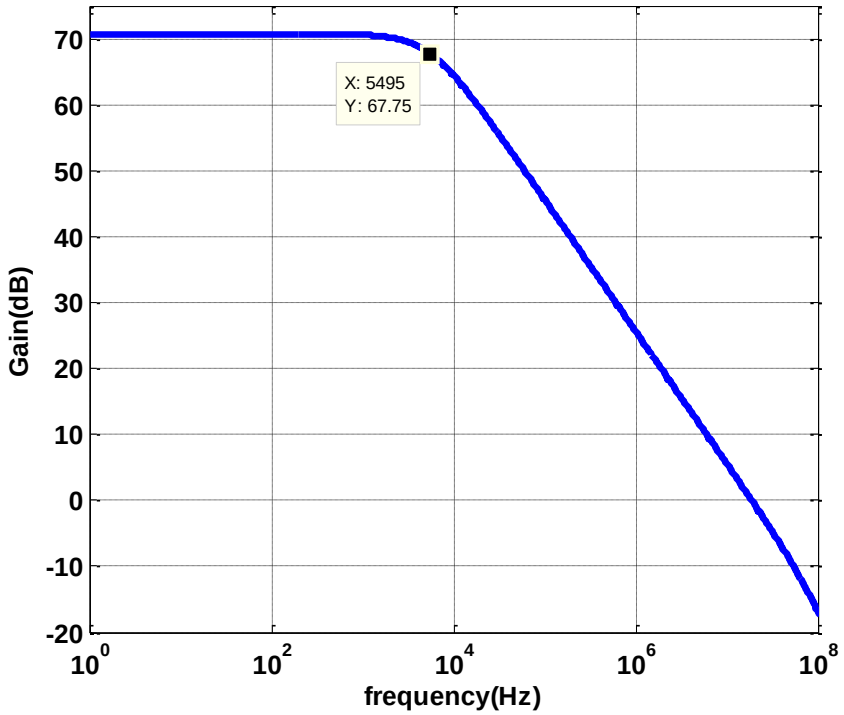

Figure 4-21: Gain of 1st OTA

The comparator consists of comparator latch and RS latch, where the comparator latch generates the result, and the RS latch hold the result (Figure 4-22).

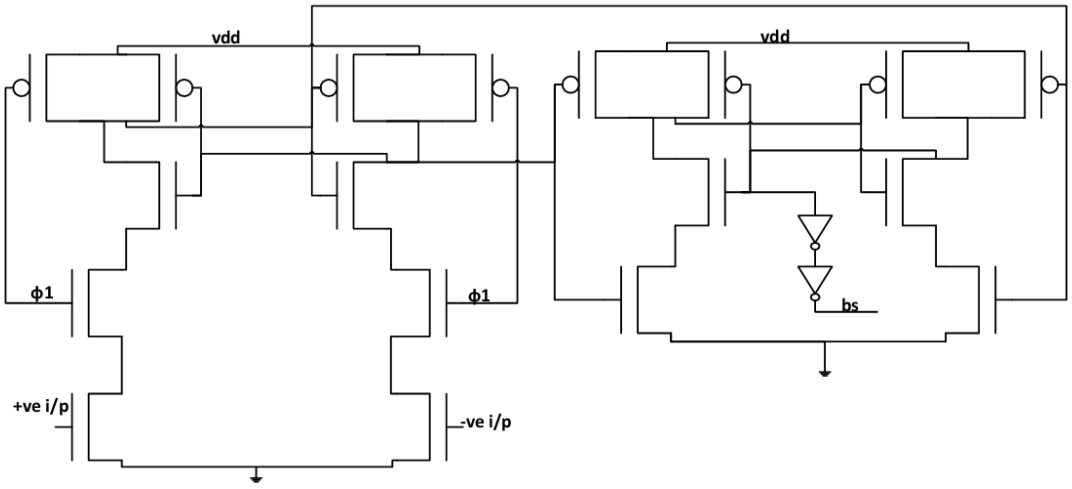

Figure 4-22: comparator schematic

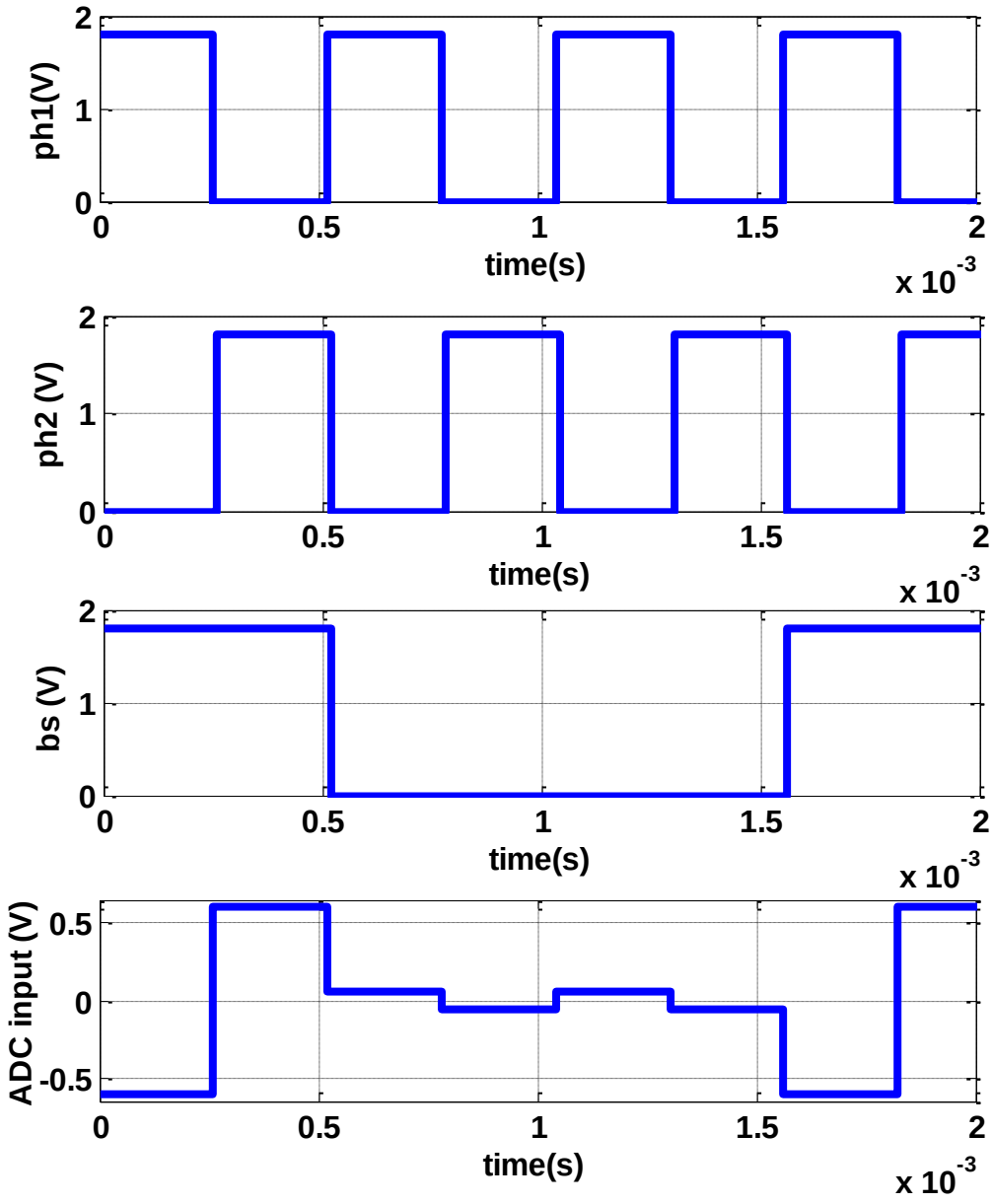

Figure 4-23: Time waveforms of different voltages

Figure 4-23 shows the time waveforms of controlling clocks, modulator input and output. It is clear that when bs=1, the ADC differential input is either VBE or –VBE according to ph1 and ph2. When bs=0, the ADC differential input is either PTAT or –PTAT according to ph1 and ph2. The wave form clearly shows the charge balancing concept previously discussed.

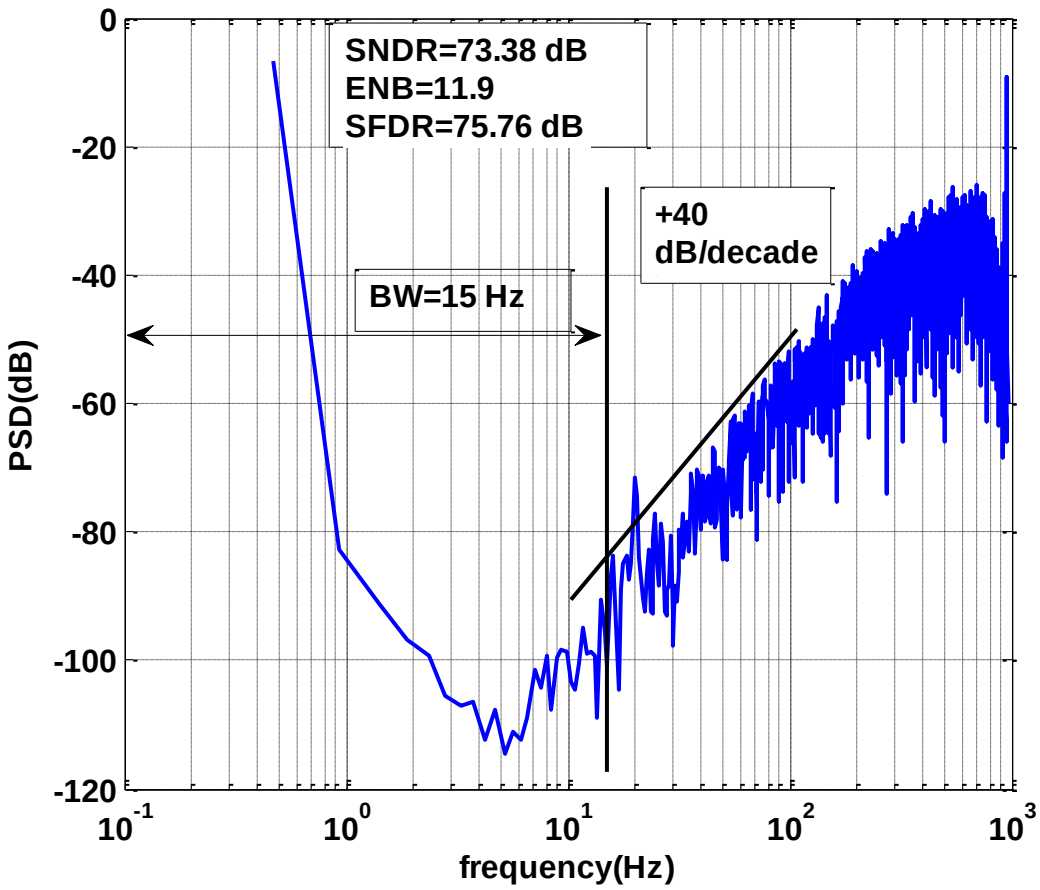

Figure 4-24: PSD of ADC running in ΣΔ modulator

Figure 4-24 shows the Power spectral density of the modulator output running in $\Sigma\Delta$ modulator mode. +40 dB/decade slopes is shown which was expected for 2nd order modulator. SNDR of the modulator is 73.38 dB which gives an effective number of bits of 11.9. The running frequency of the modulator is 1920 Hz and the signal BW is 15Hz. The FFT number of samples is 4096, running for 32/15 seconds. For IDC (single shot) operation, the signal is time limited, thus frequency response of the modulator is complex. The output must be analyzed in time domain.

Table 4-3 shows the modulator average output versus temperature, the simulated results perfectly match the theoretical Equations, Figure 4-25 translates Table 4-3, and the output is PTAT as expected. Table 4-4 summarizes the modulator performance.

Table 4-3: Modulator average output across temperature

Temperature (˚C)	Modulator average o/p, runs over 1.8v supply (mv)	input to CIC, runs over 1v supply (V)	αΔVBE (mv)	VBE (mv)	$\frac{\alpha \cdot \Delta VBE}{\alpha \cdot \Delta VBE + VBE}$
-40	0.721582	0.400879	505.9358	743.068	0.40507
-30	746.4267	0.416015	520.9667	722.9817	0.4188
-20	0.748827	0.431885	538.0253	702.5796	0.43372
-10	0.805957	0.447754	556.2653	682.1313	0.449
0	0.835399	0.464111	575.2748	661.6621	0.4651
10	866.9591	0.480713	594.8111	641.1873	0.4812
20	0.865283	0.497070	614.7349	620.7169	0.4976
30	0.924609	0.513672	634.7496	600.4833	0.5138
40	0.954932	0.530518	655.274	580.0438	0.5304
50	0.985253	0.547363	676.0961	559.6308	0.5471
60	1.016015	0.564453	697.2536	539.2523	0.5639
70	1.047656	0.582031	718.5731	519.1410	0.581
80	1.081494	0.600830	740.6136	498.8608	0.5975

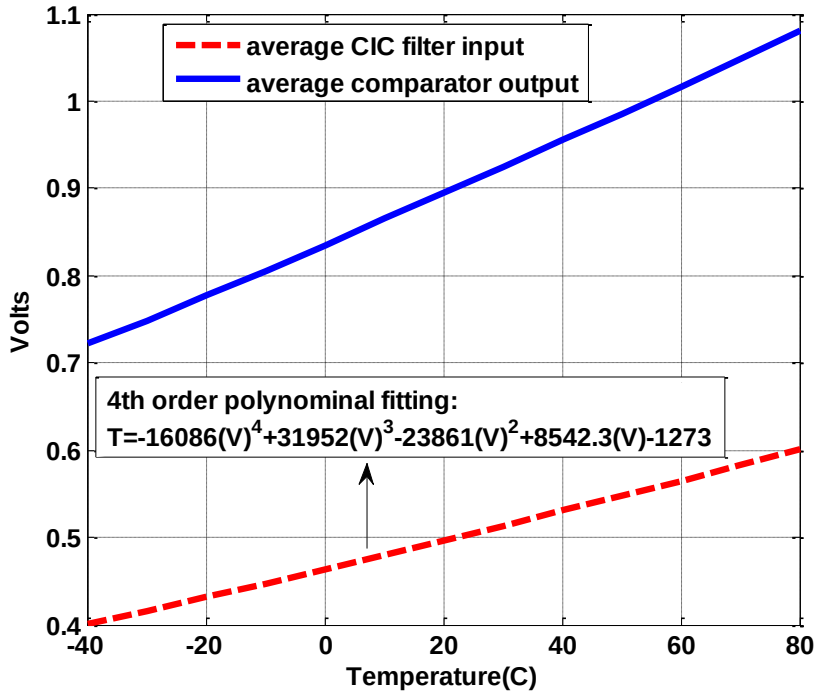

Figure 4-25: Modulator output across temperature (comparator runs on 1.8V, digital filter runs on 1V)

Table 4-4: Modulator performance summary

2nd order CIFF incremental SC ADC		
Sampling frequency		1920 Hz
N		192 cycles
Conversion time (s)		0.1
ENOB ($\Sigma\Delta$ operation)		11.9
Current consumption (μA)	1st OTA 2nd OTA Total	1.5 1.5 3.2

4.4. Temperature output: Decimation filter and Scaling

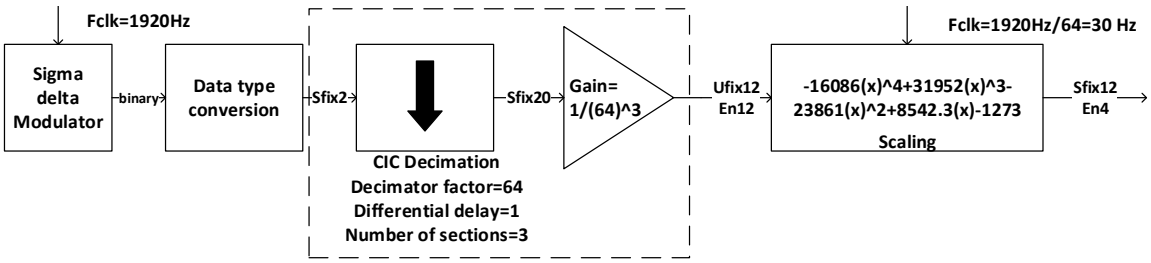

Figure 4-26: top level diagram for CIC decimation filter and scaling

Once the modulator has reached its steady state, the bit stream is fed into a decimation filter, which produces a single conversion result. Usually, the order of a sinc decimation filter is chosen one higher than that of the loop filter as previously mentioned, which implies a 3rd order filter for our 2nd order modulator for ΣΔ operation, and a filter order same to modulator's for single shot operation. In this thesis 3rd order is used for better noise attenuation.

A data type conversion block is required to change the Boolean (1 and 0) modulator output to signed 2 bits output for CIC processing. A 4th order polynomial scaling block is required to generate the temperature in degrees Celsius. The top level diagram of the ADC digital part is shown in Figure 4-26. Figure 4-27 shows the CIC filter response

using 8192 FFT points. Discrete time FIR multi-rate filter is realized by 6 adders, 6 states, no multipliers.

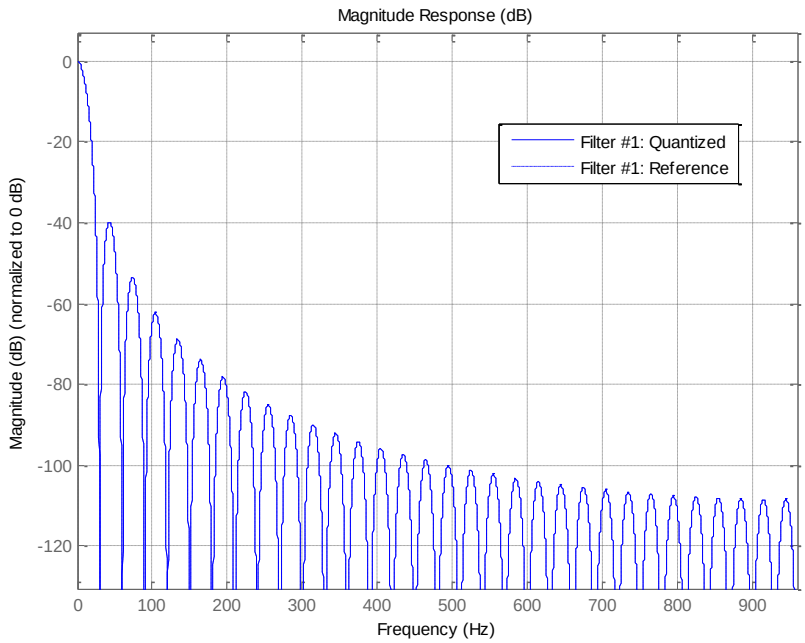

Figure 4-27: CIC decimation filter Magnitude response with 8192 FFT points

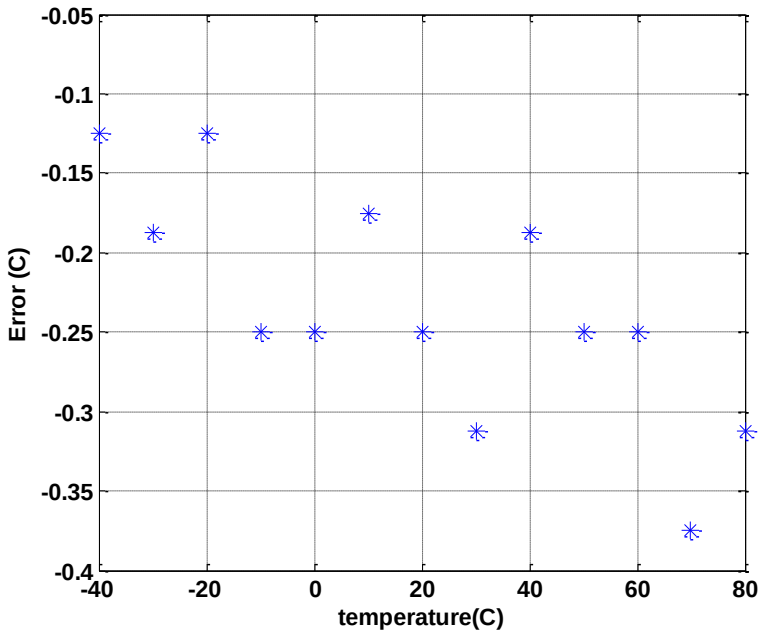

Figure 4-28: Error in temperature output

Figure 4-28 shows the Error in temperature output after 4th order polynomial scaling; the error has an average of -0.25˚C with variations of $\pm$0.125˚C. The maximum absolute error is 0.375˚C at temperature 70˚C. Error can be reduced by increasing the ADC's ENOB.

4.5. Performance Summary

A single FOM is useful to facilitate the comparison of different types of smart temperature sensors. A smart temperature sensor is actually a temperature to digital converter thus ADCs FOM could be used, the product of energy per conversion and resolution (in Kelvin) [81]. However, the sensitivity of most CMOS temperature sensors is low as previously mentioned (174 μV/˚C in this design) thus their resolution is often limited by thermal noise not quantization noise. As a result, a better FOM is the product of energy/conversion and the square of resolution [90].

In some applications, a FOM based on accuracy rather than resolution may be more convenient. The inaccuracy may be specified over different temperature ranges urging the need for a normalized metric for a fair comparison, relative inaccuracy (the peak to peak inaccuracy divided by the corresponding temperature range) can be used as a normalized metric of inaccuracy. The resolution FOM is used in this thesis as the accuracy FOM requires temperature measurements over several samples after fabrication which is affected by many parameters like packaging, calibration, and trimming.

$$Resolution\ FOM = \frac{Energy}{Conversion} \cdot Resolution^2 \tag{4.32}$$

Table 4-5 compares our temperature to digital converter (TDC) design with recent BJT based publications. Authors in [79] used 16 bit 2nd order $\Sigma\Delta$ ADC to get resolution of 0.01˚C. 16 bit ADC is necessary as the full scale temperature input to the ADC is 600˚C (Equation 4.15) using $\alpha\Delta$VBE as ADC input. And thus ADC's average output is μ=1 where $\alpha\Delta$VBE = Vref = 1.2 V at full scale temperature 600˚C. This design is a one of the

basic TDC designs. Our TDC also relies on full scale temperature of 600˚C, and after doing the math, it is just the resolution of 12 bit ADC that limits the resolution of the TDC to 0.075˚C. [77] is similar to [79] but realized in more power efficient way.

Zoom ADCs are presented in [76 and 81] for the sake of better power efficiency, authors used both 5 bit SAR for course conversion and 10 bit $\Sigma\Delta$ ADC for fine conversion. The zooming concept helped in scaling the reference voltage of the $\Sigma\Delta$ ADC to enhance the resolution where full scale temperature reported was 18˚C. Such enhancement eased the design of $\Sigma\Delta$ ADC to be only first order in [81]. Authors in [76] used 2nd order $\Sigma\Delta$ for the sake of faster conversions and thus better resolution.

Intel's work in [91] was targeting PC platforms. They focused on miniaturization to spread large number of sensors on hot and cold spots inside the CPU. Their work gives a resolution of 0.19˚C for a temperature insensitive application. FDC was used for fast conversions (0.5 ms), consuming 2.7 mA.

Authors in [74] used the conventional concept of 600˚C full scaled 2nd order $\Sigma\Delta$ ADC introduced in [79], however they relied on very high sampling frequency (262 kHz) to shorten the conversion time to 6 ms and so they enhanced their temperature resolution metric.

Table 4-5: Comparison with BJT sensing based previous work

		This work	[79] 2005	[81] 2011	[76] 2013	[77] 2013	[91] 2013	[74] 2015
Temp range(˚C)		**-40→85**	-55→125	-30→125	-55→125	-70→130	20→100	-40→85
Technology		**(1.8V-IO) in 32nm CMOS**	0.7 μm CMOS	0.16μm CMOS	0.16μm CMOS	0.7 μm CMOS	32nm CMOS (1.4 V)	0.18 μm CMOS
ADC type		**2nd order 12 bits $\Sigma\Delta$ ADC**	2nd order 16 bit $\Sigma\Delta$	coarse 5 bit SAR and fine 10 bit 1st order $\Sigma\Delta$ ADC	Coarse 5 bit SAR and fine 10 bit 2nd order $\Sigma\Delta$ ADC	2nd order $\Sigma\Delta$ ADC	FDC Voltage to frequency converter	2nd order $\Sigma\Delta$ ADC
Supply current (μA)	Front end	**1.4**	37	-	-	5	-	1.5
	ADC	**3.2**	-	-	-	-	-	1.7
	Total	**4.6***	75	4.6	3.4	25	2700	4.5
Resolution(K)		**0.075**	0.01	0.015	0.02	0.025	0.19	0.025
Conversion time (ms)		**100**	100	100	5.3	100	0.5	6
Resolution FOM(nJ˚C ^{2})		**4.65**	1.9	0.17	0.011	3.9	68	0.024

*Excluding the digital filter and clock generation circuits.

5.Initial Offset and Temperature Compensated LTE Signal

This chapter focuses on the electronic compensation system platform to mitigate the MEMS resonator's initial frequency offset, and the frequency-temperature drift issue. The chapter starts with analyzing different electronic frequency compensation methods, summarized in Figure 5-1, and then introduces our system-level design (MATLAB and Verilog) for our digital compensation system. The chapter also focuses on the RF-LTE Phase locked loop system that produces compensated LTE signals referenced by MEMS oscillators.

5.1.Overview

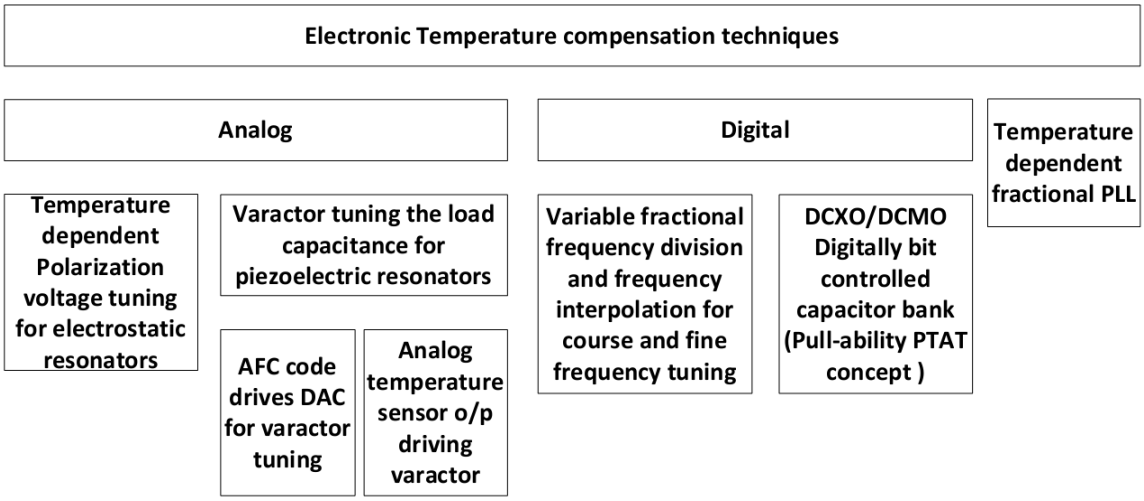

Figure 5-1: Electronic temperature compensation techniques

5.1.1. Analog Compensation

Analog compensation in [18] relies on the fact that for electrostatic transduced resonators (Figure 5-2), the resonance frequency decreases with increasing the polarization voltage. So, if the polarization voltage has an appropriate negative temperature dependence (VBE from Band gab reference circuitry), the change in frequency with temperature is offset by a change due to the polarization voltage. The author found a relation between polarization voltage, temperature and resonance frequency and implemented this relation in circuits.

The same technique was used in [54] but for piezoelectric resonators. Here we have to mention that electronic compensation techniques for piezoelectric MEMS oscillators is more complicated than there capacitive counterparts; this is due to the limited tuning range available through electronic frequency tuning. Unlike in electrostatic actuated MEMS oscillators [18] where a change in polarization voltage produces a shift in the resonance frequency, the piezoelectric oscillator's designers are forced to rely on small voltage tuning for temperature and process compensation. Varactors are used for analog frequency tuning. There is no need here for high voltage charge pump operation due to the usage of piezoelectric transduction that doesn't need high voltage operation as described in chapter 2 [3].

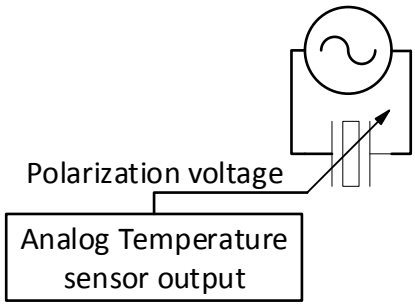

Figure 5-2: Polarization voltage compensation for electrostatic resonators

For TCXO [66], part of the off-chip load capacitance CL is implemented on chip using a varactor. Temperature sensor digital signal is converted to an analog signal using a DAC

to drive the varactor for frequency-temperature compensation (Figure 5-3). This approach has many disadvantages:

- The varactor capacitance-voltage (C-V) relation is nonlinear so as the capacitance to frequency transfer function. Furthermore, the varactor C-V curve is a strong function of PVT conditions. The nonlinear frequency versus DAC output transfer function complicates the compensation loop design and increase the DAC resolution requirement.
- The limited Cmax to Cmin capacitance ratio of the analog varactor limits the achievable frequency tuning range. Varactor gain should be high to have the required tuning range.
- Control line noise degrades the phase noise of the oscillator.
- DAC in the analog approach needs reference buffer, and band-gap reference.

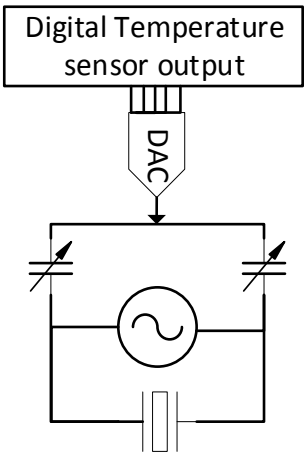

Figure 5-3: Analog compensation using DACs and varactors

5.1.2. Digital compensation

Usually digital compensation is more complex when compared to analog solution, yet more accurate. In the digital approach, binary weighted switched capacitor bank is used

for frequency tuning [4, 68]. The frequency stability control is done by first converting the serial digital signal coming from temperature sensor to a parallel digital signal, which is applied to the switched capacitor bank (Figure 5-4). This approach overweighs the previous one in many aspects:

- The capacitance versus code transfer function is linear
- The Cmax to Cmin ratio is limited only by the parasitic capacitance and is normally much larger than what an analog varactor can achieve.
- All the digital bank capacitors are MIM capacitors for better noise immunity.

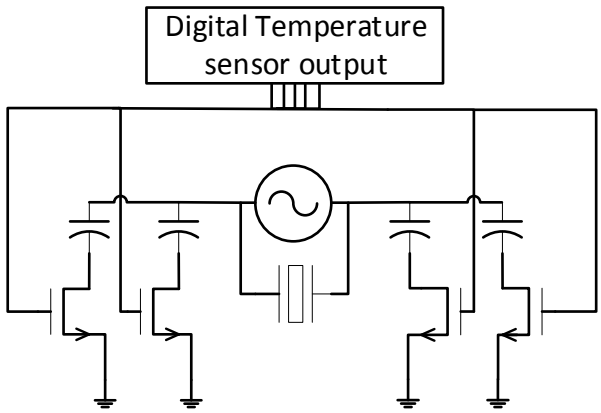

Figure 5-4: Temperature compensation using capacitor bank

[4 and 68] use the idea of the ability to get a PTAT frequency behavior by decreasing the load capacitance with temperature (as temperature increases, the load capacitance decreases linearly and thus the frequency increases). Pull-ability is a specification for the change in operating frequency as a function of change in the load capacitance. The temperature sensor generates a voltage signal used to reduce the load capacitance to make the pull-ability behavior PTAT

In [69 and 70] the compensation is based on the combination of inhibition and frequency interpolation techniques that both have the advantage of an all-digital implementation providing linear frequency tuning. Coarse tuning can be achieved by N variable division

that is similar to the inhibition method and that means compensation of the divided signal over an arbitrary large temperature and initial frequency adjustment. Frequency interpolation can be obtained by varying the load capacitance of the piezoelectric resonator (or the polarization voltage for capacitive resonator) with a variable duty cycle *dc* so as to generate two different frequencies spaced by an amount of ΔF_{HL} leading to mitigating resonator's temperature drift problem as shown in Figure 5-5.

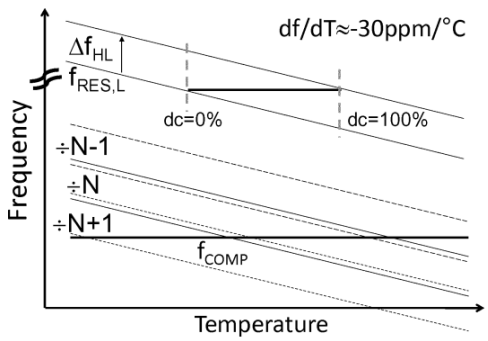

Figure 5-5: digital compensation scheme used in [69, 70]

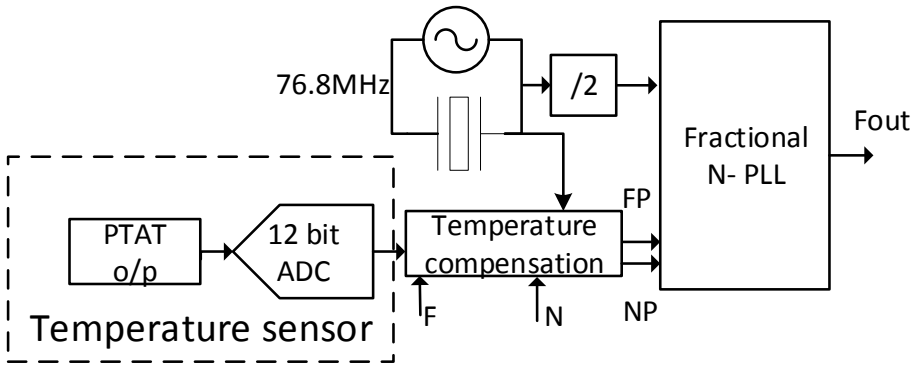

Figure 5-6: fractional N-PLL solution

5.1.3. Fractional N-PLL Solution

Previous work used fractional N-PLL for temperature and initial frequency compensation [71-74]. It is the most accurate way for compensation and been used by state-of-the-art

solutions yet complex and power hungry. $\pm 0.5ppm$ frequency stability can be achieved from -40˚C to 85˚C. For the above reasons, the thesis focuses on the implementation of TCMO platform using fractional N-PLL for temperature compensation. Figure 5-6 shows the complete high level system for our platform.

5.2. Digital Compensation Algorithm

A composite compensation factor that combines both the process spread of $\pm$8000 ppm [67] and the temperature drift of MEMS reference oscillator frequency is generated. This factor is used for frequency compensation via adjustment of the fractional N-PLL frequency division factors as shown in Figure 5-6. The factor is determined by the MEMS resonator's reference signal, resonator's operating temperature, and the required output signal frequency

If integer N-PLL is used, the trimming accuracy will be determined by a comparison source frequency. So in order to achieve 10 ppm accuracy for an output frequency of 150 MHz for example, an integer N-PLL would require a comparison frequency of 1.5 KHz. As a result, the lock-time can become very large. The trimming accuracy of a fractional N-PLL on the other hand, can be very small even when maintaining a high comparison frequency and a wide loop bandwidth; thus, locking time is reduced.

The temperature compensation logic showed in Figure 5-6 and 5-7 implements the temperature compensation algorithm. The algorithm modifies the PLL division factor to correct the resonator frequency shifts due to both fabrication process and temperature drift. The output frequency is determined by the resonator frequency f_{MEMS} and the PLL division factors N, F. Any error in the output frequency due to a change in f_{MEMS} is compensated by modifying the factors N and F to NP and FP such that the error between the actual output frequency and the required frequency is better than certain threshold.

$$fout_{before\ compensation} = \frac{f_{MEMS}\left(N + \frac{F}{2^f}\right)}{2} \tag{5.1}$$

$$fout_{required} = 76.8 * \frac{10^6\left(N + \frac{F}{2^f}\right)}{2} \tag{5.2}$$

$$N_{Total} = N\frac{fout_{required}}{fout_{before\ compensation}} \tag{5.3}$$

$$N_p = fix(N_{Total}) \tag{5.4}$$

$$F_p = round\left(\left(N_{Total-}N_p\right) \cdot 2^f\right) \tag{5.5}$$

$$fout_{after\ compensation} = \frac{f_{MEMS}\left(N_p + \frac{F_p}{2^f}\right)}{2} \tag{5.6}$$

$$fout_{error|ppm} = \left(\frac{fout_{after\ compensation} - fout_{required}}{fout_{required}}\right) * 10^6 \tag{5.7}$$

In the above equations, f_{MEMS} is the MEMS oscillator center frequency combining both initial and temperature errors to be solved for, f is number of bits of PLL-sigma delta modulator, N is the integer division ratio, F is the sigma delta input word, where F/2f represents the fraction division. $fout_{before\ compensation}$ is the PLL output frequency including the errors, $fout_{required}$ is the required PLL output frequency, and $fout_{after\ compensation}$ is the output compensated frequency.

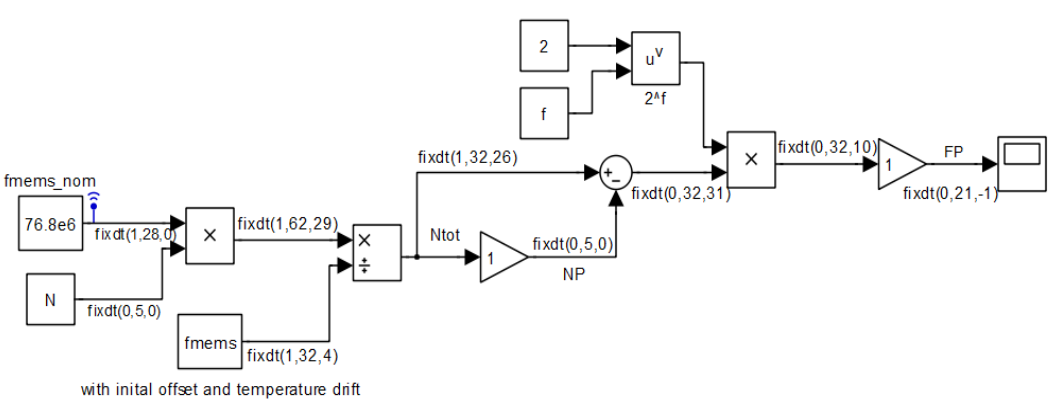

Figure 5-7: digital compensation circuitry

Figure 5-7 shows how the algorithm and Equations 5.4 and 5.5 can be implemented on silicon. The system level includes some multipliers and adders to compensate for both initial offset and temperature drift errors. Care should be taken when specifying the word length of each bus in the system for highly accurate output, MEMS Oscillator frequency f_{MEMS} should be sensed and this is easily done by digital circuits using a faster clock to count the number of rising edge in the MEMS clock signal.

The system has been tested using Verilog for 2 temperatures (-40˚C and 30˚C). The N and f values used for both tests are 19 and 21 respectively; the clk frequency is 1920Hz. For the 1st test shown in Figure 5-8, the input to CIC filter is PTAT (shown as "in") which resembles an average of -1642 (Stored integer); i.e., $1642*2^{-12}$ = 0.4V. The temperature output "temp" is -642 (Stored integer); i.e., -642*2^{-4} = -40.125˚C. (2^{-4} is used here as the temperature is implemented as (1,12,4) fixed point implementation). The algorithm gives NP of 18, and FP of 1786730.

For the 2nd test shown in Figure 5-9, the input to the filter resembles an average of 2104 (SI); i.e., 0.5137V. The temperature output is 475 (SI); i.e., 29.6875˚C. The algorithm gives NP of 18, and FP of 1783802. The Verilog outputs for both tests were double checked with MATLAB output, and it is clear that the temperature and the compensation parameter (FP) are generated in 0.1 second as targeted. In the above tests, we assumed the values of N and f.

In order to find out the needed values and ranges for N and f required by the system, we need to shed lights to the RF-LTE system, frequency plan, and system phase noise requirements.

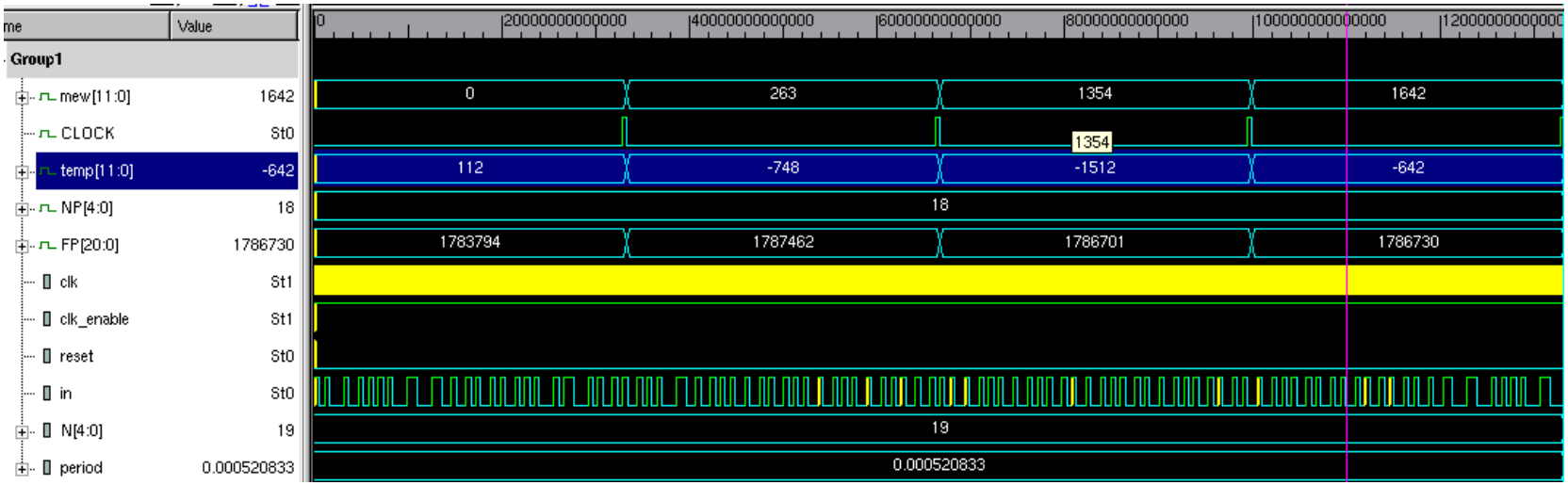

Figure 5-8: compensation system inputs and outputs for -40˚C

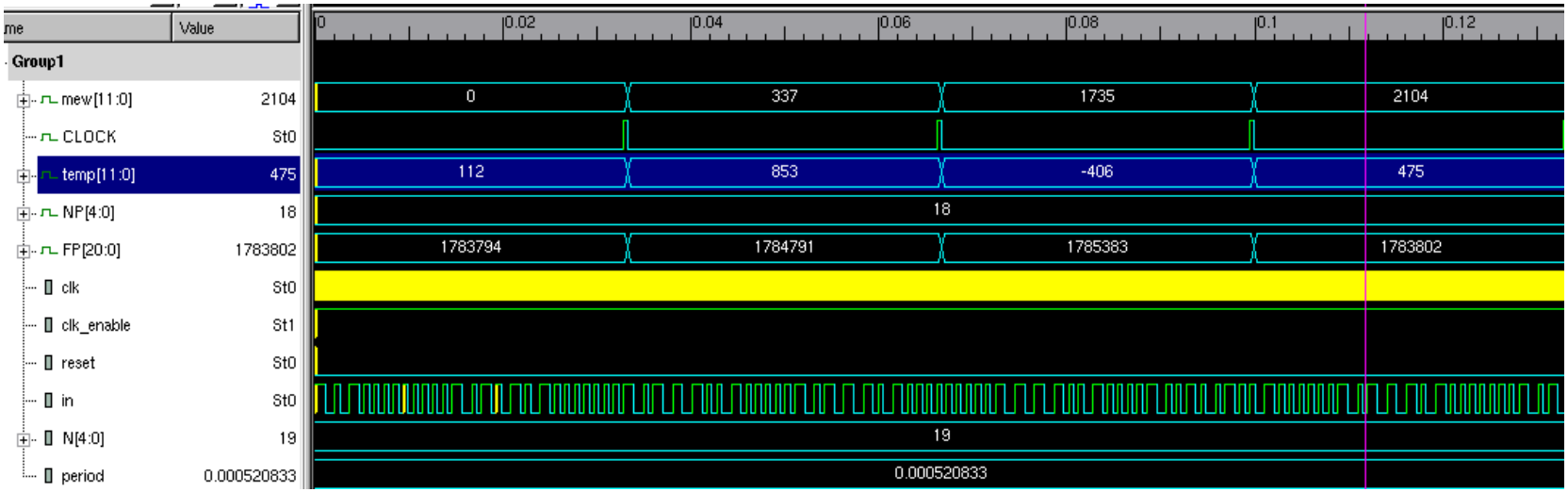

Figure 5-9: compensation system inputs and outputs for 30˚C

5.3. LTE Phase Locked Loop

Frequency synthesizers are the key block for any system's performance. Advanced wireless communications like LTE were introduced with different frequencies in each country. SOC solution, low power dissipation, small chip size and high performance per cost are highly desirable.

Most synthesizers are realized by phase locking concept to achieve high frequency accuracy [94-98]. In wireless applications, ΔΣ fractional-N PLLs are preferred as frequency synthesizer due to their fine frequency resolution and wide bandwidth. Unlike their counterparts integer-N PLLs, that need a low reference frequency to guarantee fine frequency resolution. The PLL loop bandwidth is usually settled below Fref/10 to avoid any instability [94]. The main problem that rises from wide bandwidth fractional-N PLLs is the ΔΣ modulator's quantization noise. Therefore the bandwidth has to be narrow enough to ensure that the instantaneous charge errors at the CP output can be greatly suppressed before it disturbs the VCO. However small loop bandwidth will slow the PLL response down.

Our PLL should have the following broad specifications:

- Low phase noise
- FDD: Uplink and downlink operation, both operating at the same time, wth different frequencies; thus 2 PLLs should be used, one for Tx, and another for Rx. [98]
- Fine frequency resolution which supports the minimum channel spacing in LTE.
- PLL For a direct conversion transceiver (zero IF)
- Rx Modulation : QPSK

PLL's frequency range is one of its most important specifications. This is a very fundamental property which is gaining more attention in modern wireless standards and globalization of wireless devices due to limited spectrum. Another specification is the output frequency resolution which is known as the minimum frequency step that the PLL

can sense. Usually high resolution is guaranteed using fractional-N phase-locked loops. Synthesizer's settling time affects the transient behavior, thus the switching and correcting speeds [98]. PLL phase noise affects the quality of the received signal, eventually affects the Bit error rate of the signal in case of a receiver. In zero and low IF transceivers, the PLL should generates in-phase and quadrature-phase reference signals (I/Q). Care should be taken because any imbalance between these two signals will degrade the received signal quality.

There are strict design rules and guidelines for RF IC designers, as they have to meet electrical industry standards such as 3GPP for Europe [99, 100] or IEEE for USA. The standards assign frequency bands to different telecommunication systems to avoid interference. It imposes limits to important RF system parameters like phase noise, linearity, frequency allocation, BER, and error vector magnitude EVM. Frequency plan, modulation, blocking, spurs, and phase noise requirements are stated in [99-101]. Previous work in LTE PLLs can be found in [102-105].

LTE provides an uplink speed up to 50 Mbps and a downlink speed up to 100 Mbps [102]. Channel bandwidth is scalable from 1.4MHz to 20MHz [99]. This suits the needs of different network operators that have different bandwidth allocations. LTE improves spectral efficiency in 3G networks, allowing carriers to provide more data and voice services over a given bandwidth.

EVM is a critical specification and it is used to describe the modulation quality of the transmitted signal [102]. Poor EVM reduces the ability of a receiver to properly recover the transmitted signal. Oscillator's phase noise in both transmitter and receiver is the main contributor to poor EVM. Therefore, LTE transceivers usually have stringent specifications for the frequency synthesizer in terms of integrated phase noise, frequency resolution and lock time.

5.3.1. Frequency Plan

Practically both FDD and TDD should be targeted when setting the PLL system requirements [105], however to ease the design only FDD is considered, this will ease the system level spec on PLL settling time, bandwidth. To accommodate all FDD LTE frequency bands, a wide-range fractional-N PLL is implemented. It consists of PFD, CP, LPF, VCO, a programmable divider, and SDM.

QPSK Sensitivity and targeted LTE bands are summarized in Table 5-1, while Table 5-2 shows the frequency plan, and Figure 5-10 shows the frequency plan system implementation.

The usage of 2 VCOs is to relax the tuning range requirements and to cover the whole LTE bands. VCO1 is working on twice the carrier frequency to avoid the injection pulling for bands 1, 2, 3, 4, 5, 8, 9 and 10. Bands 11, 12, 13 and 14 also don't suffer from injection pulling due to high VCO center frequency. Yet band 7 may suffer from pulling because it is output directly from VCO2.

As shown in Figure 5-10, IQ dividers are needed for zero IF Transceivers; the system satisfies FDD LTE band requirements

Table 5-1: available FDD bands and their QPSK reference sensitivity

Modulation type	Band	TX (MHz)	RX (MHz)	Relations with VCO	Available channel BW(MHz)	Duplex distance (MHz)	QPSK Ref. sensitivity
FDD	1	1920-1980	2110-2170	VCO1/2	5 10 15 20	190	-100 -97 -95.2 -94
	2	1850-1910	1930-1990	VCO1/2	1.4 3 5 10 15 20	80	-102.7 -99.7 -98 -95 -93.2 -92

	3	1710- 1785	1805- 1880	VCO1/2	1.4 3 5 10 15 20	95	-101.7 -98.7 -97 -94 -92.2 -91
	4	1710- 1755	2110- 2155	VCO1/2	1.4 3 5 10 15 20	400	-104.7 -101.7 -100 -97 -95.2 -94
	5	824- 849	869- 894	VCO1/4	1.4 3 5 10	45	-103.2 -100.2 -98 -95
	7	2500- 2570	2620- 2690	VCO2	5 10 15 20	120	-98 -95 -93.2 -92
	8	880- 915	925- 960	VCO1/4	1.4 3 5 10	45	-102.2 -99.2 -97 -94
	9	1749.9- 1784.9	1844.9- 1879.9	VCO1/2	5 10 15 20	95	-99 -96 -94.2 -93
	10	1710- 1770	2110- 2170	VCO1/2	5 10 15 20	400	-100 -97 -95.2 -94
	11	1427.9- 1447.9	1475.9- 1495.9	VCO2/2	5 10	48	-100 -97
	12	699- 716	729- 746	VCO2/4	1.4 3 5 10	30	-101.7 -98.7 -97 -94
	13	777- 787	746- 756	VCO2/4	5 10	31	-97 -94
	14	788- 798	758- 768	VCO2/4	5 10	30	-97 -94

Table 5-2: Frequency plan

VCO1 center=3850 MHz Tuning range=33.77%		LTE Bands	N ranges	Instantaneous N after considering SDM (-3→4)	Geometric mean for Phase noise estimation
VCO2 center=2845 MHz Tuning range =27.7%					
VCO ranges (MHz)	Band ranges (MHz)				
VCO1 (3200→4500)			21→29	13→33	
VCO1/2 (1600→2250)	1710→2170	1,2,3,4,9,10			25
VCO1/4 (800→1125)	824→960	5,8			23
VCO2 (2450→3240)	2500→2690	7	16→21		16
VCO2/2 (1225→1620)	1427.9→1495.9	11			19
VCO2/4 (612.5→810)	699→798	12,13,14			19

Where tuning range= (Vmax-Vcenter)*2*100/Vcenter.

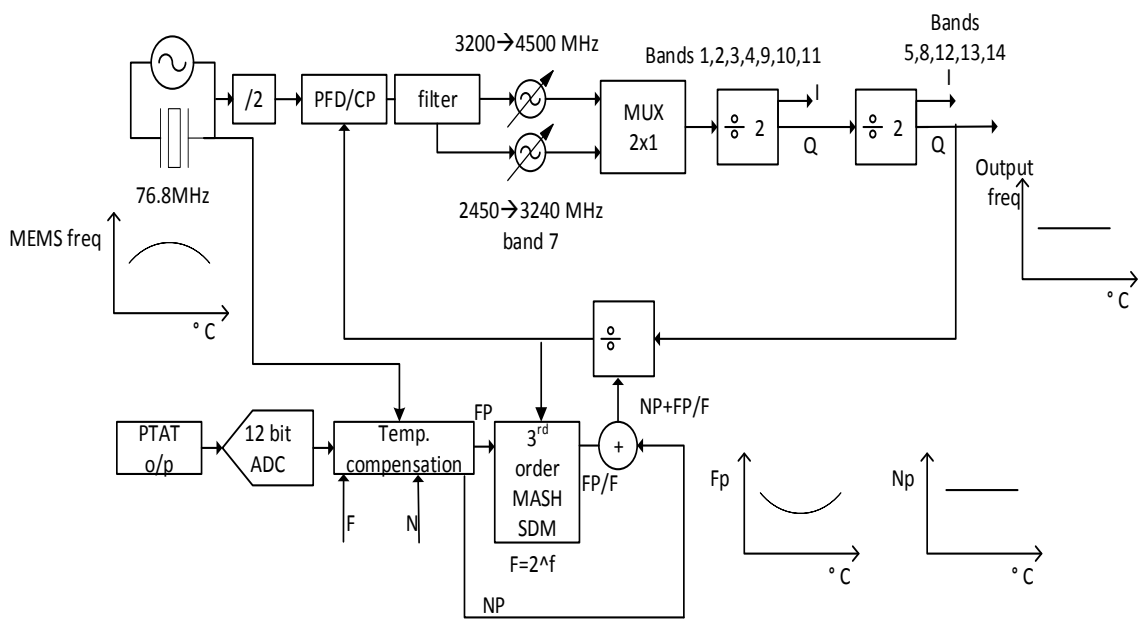

Figure 5-10: Complete system for generating programmable LTE compensated frequencies

- For bands 1, 2, 3, 4,5,8,9 and 10:

The maximum number of N is settled by 2170 MHz band frequency, where 2710/2/38.4=28.25. Thus maximum N required is 29. As a check: 29*2*38.4= 2227.2 MHz (> 2710 MHz).

On the other hand minimum N is settled by 824 MHz frequency where 824/38.4=21.45. Thus minimum N required=21. As a check: 21*38.4 =806.4 MHz (< 824MHz).

Therefore N ranges from 21→29. Making VCO1 frequency ranges from 3200→4500 MHz, with center frequency of 3850 MHz and tuning range of 33.77%.

The instantaneous multi modulus division ratio can vary from -3 to 4 around its average division ratios using 3rd order MASH 1-1-1 SDM. Thus we need to have a divider ratios at least 3 less than the minimum number, and 4 greater than the maximum number, resulting in MMD division range of N= 18→33.

- For bands 7, 11, 12, 13 and14:

The maximum number of N is settled by 798 MHz band frequency, where 798/38.4=20.78. Thus maximum N required is 21. As a check: 21*38.4= 806.4 MHz (>798 MHz).

On the other hand minimum N is settled by 2500 MHz frequency where 2500/38.4/4= 16.27. Thus minimum N is 16. As a check: 16*2*238.4 =2457.6 MHz (<2500).

Therefore N ranges from 16→21. Making VCO2 frequency ranges from 2450→3240 MHz, with center frequency of 2845 MHz and tuning range of 27.7%.

Using 3rd order MASH 1-1-1 SDM results in MMD division range of N= 13→24.

So, N ranges from 13→33 to cover all LTE frequencies.

According to [98], geometric mean values of N was used to calculate the PLL's phase noise and jitter, the geometric mean values of N for each band is shown in Table 5-2 and is calculated as follows :

- Bands 1, 2,3,4,9 and10:

$$\frac{\sqrt{1710 * 2170}}{38.4 * 2} = 25$$

- Bands 5 and 8:

$$\frac{\sqrt{824 * 960}}{38.4} = 23$$

- Band 7:

$$\frac{\sqrt{2500 * 2690}}{38.4 * 2 * 2} = 16$$

- Band 11 :

$$\frac{\sqrt{1427.9 * 1495.9}}{38.4 * 2} = 19$$

- Bands 12, 13, and 14:

$$\frac{\sqrt{699 * 798}}{38.4} = 19$$

- For all bands

$$\sqrt[5]{25 * 23 * 16 * 19 * 19} = 20$$

Of course this is 1 scheme of many others to cover the whole LTE bands. Other solution may be in using 3 VCOs. This will help to ease the tuning range requirements, shields band 7 from pulling (using a double center frequency VCO). However it increases the MMD division values needed, which by turn worsens the MEMS and CP phase noise at the output; added to that the larger chip area, and power consumption.

Table 5-3: SNR required for each channel BW

BW_{freq}(MHz)	Modulation power added (dB)	Maximum fraction throughput (%)	SNR (dB)
1.4	6	70	18.6
3	6	70	18.8
5	6	70	18.6
10	6	70	18.8
15	7	70	18.7
20	9	70	19.7

5.3.2. Phase noise specifications

As previously mentioned, Transmitter EVM is greatly impacted by the transmitter's PLL phase noise, and it is well know that the receiver sensitivity is heavely dependent on PLL phase noise. VCO introduces small frequency and phase random variations and jitter, these variations is known as phase noise. Reciprocal mixing is one of the serious problems caused by PLL's phase noise, where it occurs when the reciever's LO phase noise mixes with a strong interfering signal (blocker) producing a signal which falls inside the pass-band of the receiver [102]. Figure 5-11 shows LTE in-band and out-of band blocking specs. Receiver sensitivity is defined as the minimum detectable power at the receiver input for a specified minimum BER at the receiver output [100]. LTE reciver sensitivity at differnet channel BW are shown in Table 5-1.

Phase noise specifications for the PLL were derived from the LTE standard [99-101], SNR is listed in Table 5-3 for every channel BW, and the PN is calculated in Table 5-4. Equation (5.8) is used to calculate the Phase noise at different frequency offsets [101]

$$L(\Delta f) \leq P_{REFSNS} + 6{,}7{,}9dBm - SNR - P_{Blocker}(\Delta f) - 10\log(BW) \quad (5.8)$$

Where $P_{Blocker}$ is power found in blockers and shown in Figure 5-11. $6{,}7{,}9dBm$ are the added modulation power and is listed in Table 5-3 for every channel BW. Table 5-5 shows that the Toughest phase noise specs are for LTE bands 1, 4, 10, and 11 with 10 MHz channel BW.

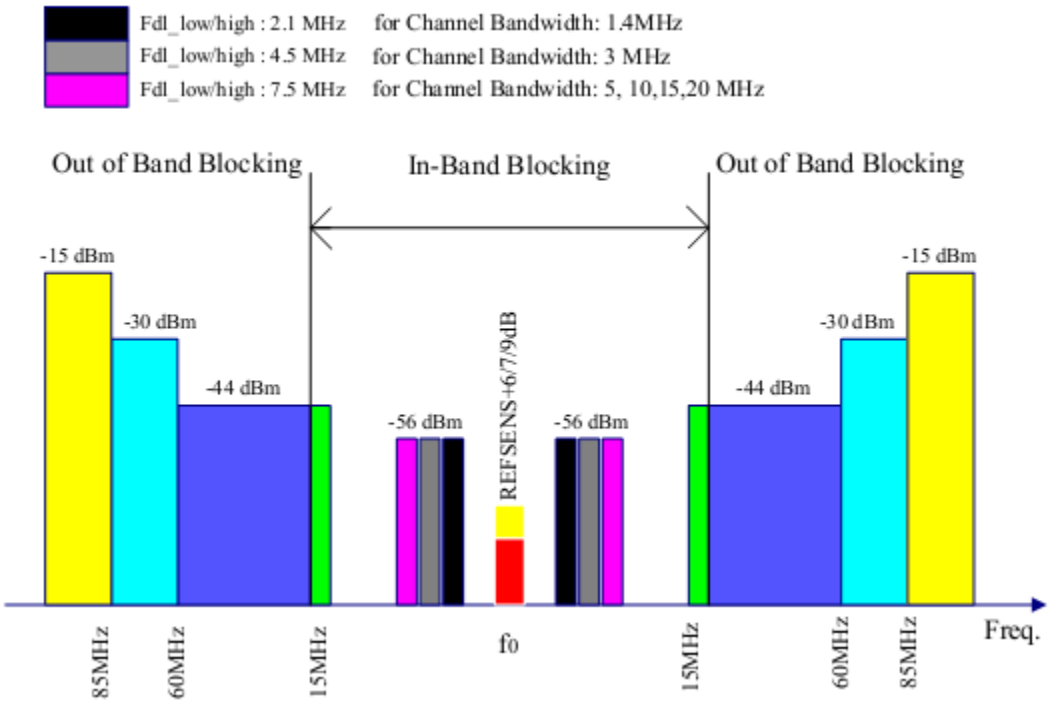

Figure 5-11: blockers profile

Table 5-4: Phase noise specifications

Band	BW (MHz)	QPSK P_{REFSNS} (dBm)	PN ($7.5MHz$) (dBc/Hz)	Band	BW (MHz)	QPSK P_{REFSNS} (dBm)	PN ($7.5\ MHz$) (dBc/Hz)
1	5	-100	-123.59	8	1.4	-102.2	-120.26
	10	-97	-123.8		3	-99.2	-120.77
	15	-95.2	-122.66		5	-97	-120.59
	20	-94	-121.71		10	-94	-120.8
2	1.4	-102.7	-120.76	9	5	-99	-122.59
	3	-99.7	-121.27		10	-96	-122.8
	5	-98	-121.59		15	-94.2	-121.66
	10	-95	-121.8		20	-93	-120.71
	15	-93.2	-120.66				
	20	-92	-119.71				
3	1.4	-101.7	-119.76	10	5	-100	-123.59
	3	-98.7	-120.27		10	-97	-123.8
	5	-97	-120.59		15	-95.2	-122.66
	10	-94	-120.8		20	-94	-121.71
	15	-92.2	-119.66				

	20	-91	-118.71				
4	1.4 3 5 10 15 20	-104.7 -101.7 -100 -97 -95.2 -94	-122.76 -123.27 -123.59 -123.8 -122.66 -121.71	11	5 10	-100 -97	-123.59 -123.8
5	1.4 3 5 10	-103.2 -100.2 -98 -95	121.26 -121.77 -121.59 -121.8	12	1.4 3 5 10	-101.7 -98.7 -97 -94	-119.76 -120.27 -120.59 -120.8
7	5 10 15 20	-98 -95 -93.2 -92	-121.59 -121.8 -120.66 -119.7	13 14	5 10 5 10	-97 -94 -97 -94	-120.59 -120.8 -120.59 -120.8

LTE is on based on OFDM systems; the multi carrier scheme differs significantly from single carrier schemes due to PLL's PN profile that is replicated at every subcarrier within each channel. The integrated phase noise should be calculated starting from one tenth the subcarrier spacing and ending in one half the channel bandwidths. [98]

Table 5-5: Most stringent phase noise specifications

Channel BW (MHz)		10
Modulation power added (dB)		6
SNR (dB)		18.8
Worst case Phase noise (dBc/Hz)	L(7.5MHz) =-97+6-18.8+56-10log(10e6) L(15MHz) =-97+6-18.8+44-10log(10e6) L(60MHz) =-97+6-18.8+30-10log(10e6) L(85MHz) =-97+6-18.8+15-10log(10e6) *L(1 kHz) *L(10 kHz) *L(100kHz)	-123.8 -135.8 -149.8 -164.8 -71 -100 -100

* Values taken from [98] based on LTE Rx system simulations.

- OFDM : 12 subcarrier in 180KHz → Resource Block spacing=15kHz
- Max channel BW =20MHz
- Jitter is calculated between RB spacing/10 to channel BW/2
- Jitter is calculated from 1.5kHz to 10MHz
- FDD maximum frequency settling time = 50 us [98]

- TDD maximum frequency settling time = 5 us [98]

First we have to determine the required LPF bandwidth and CP current to build a linearized phase domain model on MATLAB. Therefore we can figure out the phase noise specifications for each block in our targeted PLL. Filter components are shown in Table 5-6, and calculated according to [106]. The passive filter is shown in Figure 5-12

Table 5-6: Loop filter components value

Filter components	Values
C1	110 pF
C2	1.1 nF
C3	11 pF
R2	3.25 KΩ
R3	555 Ω

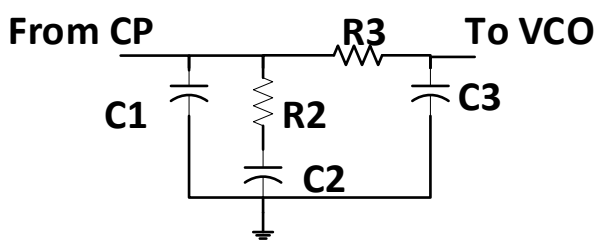

Figure 5-12: passive loop filter

- BW= 150 KHz
- ICp= 500uA
- KVCO=50MHz/V (low gain for low VCO phase noise)
- Phai= 56˚
- Feedback divider N=20 (geometric mean) for phase noise calculations.
- 3rd order Mash 1-1-1 is used for its unconditional stability and simplicity

$$Resolution = \frac{f_{ref}}{2^f} = ppm\ required * \ Output_{\min frequency} \tag{5.9}$$

For output min frequency = 612.5 MHz, f_{ref}=38.4 MHz, 0.1 ppm resolution gives f=20. For f= 21, the final resolution is 0.03 ppm. As shown the resolution specification is

settled by the VCO min frequency. Higher frequency LTE bands are expected to have better resolution than 0.03 ppm.

Since both VCOs have a wide tuning range, their sensitivities will vary around 50 MHz/V. To solve this problem a digitally-programmable CP should be used. Programmable CP compensates for VCO sensitivity variation. The CP current will vary with VCO sensitivity. It is well known that the CP current within the PLL transfer function is proportional to the square of the VCO sensitivity. The higher the sensitivity, the lower the CP current required. Figures 5-13 to 5-17 show the phase noise specification on MATLAB for different LTE bands.

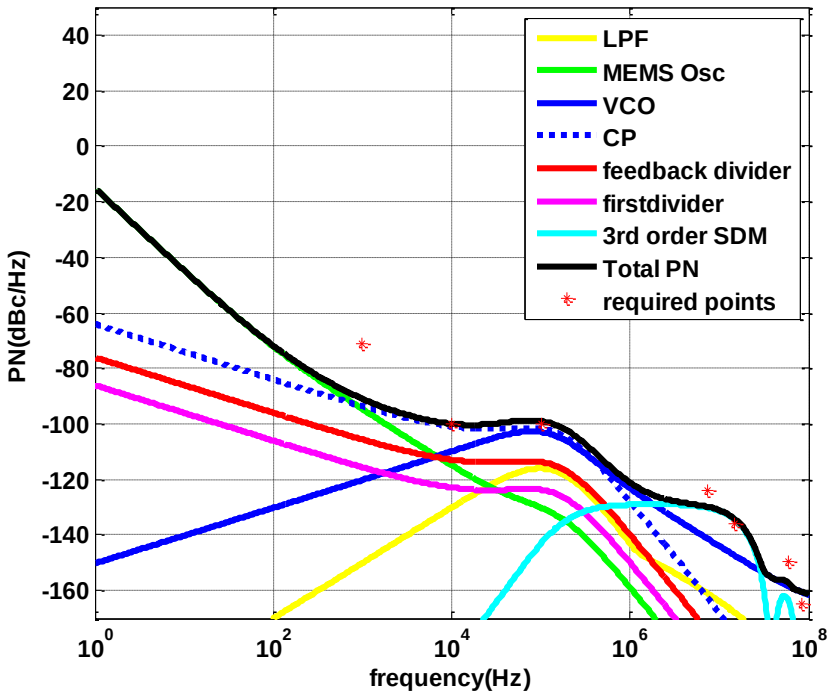

Figure 5-13: phase noise at the output of PLL (1920 MHz) using geometric mean N=25

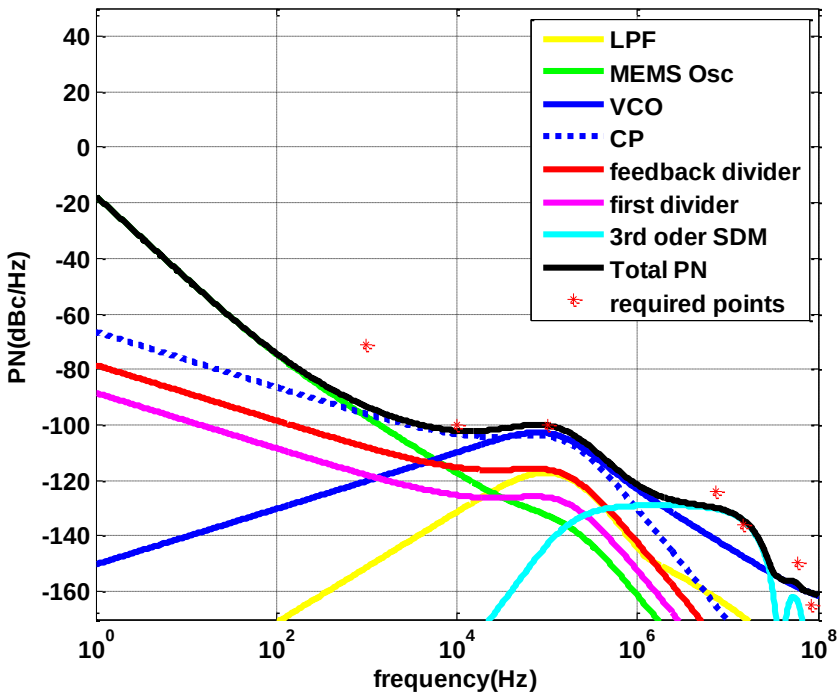

Figure 5-14: phase noise at the output of PLL (1459.2 MHz) using geometric mean N=19

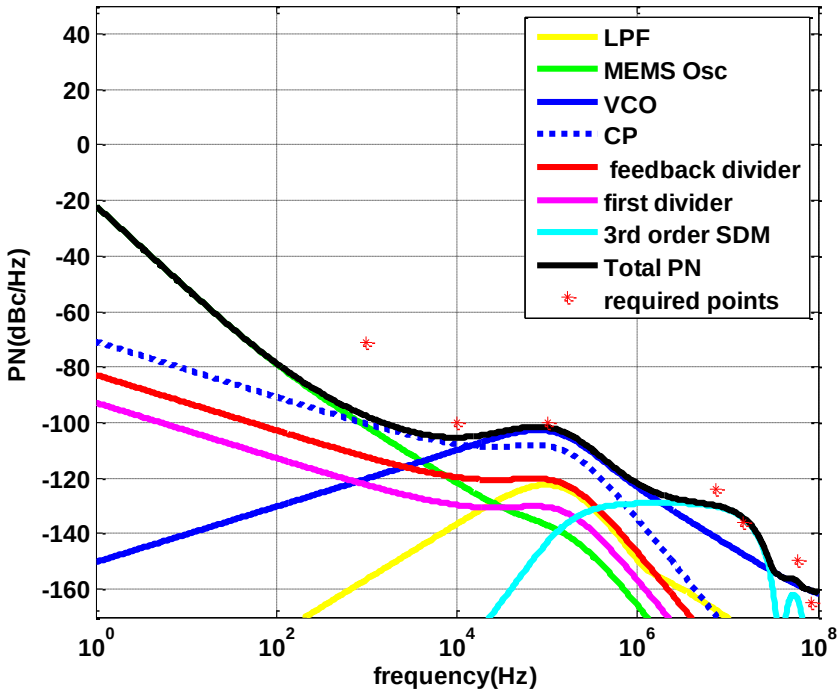

Figure 5-15: phase noise at the output of PLL (883.2 MHz) using geometric mean N=23

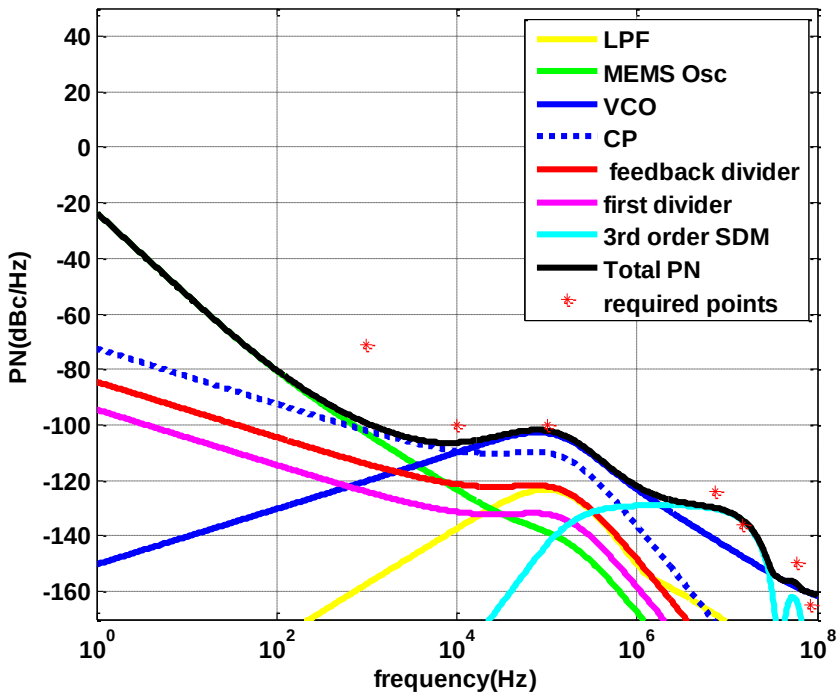

Figure 5-16: phase noise at the output of PLL (729.6 MHz) using geometric mean N=19

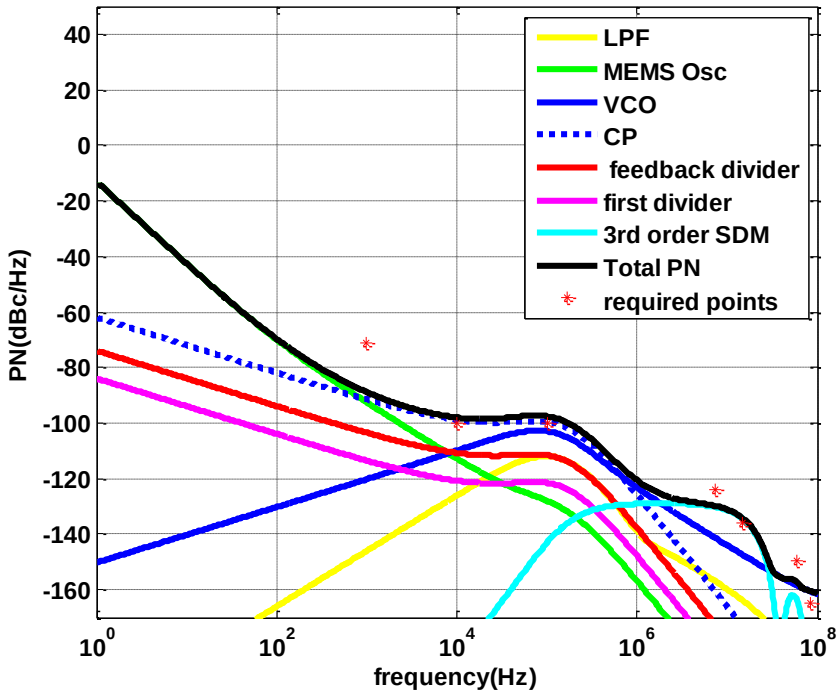

Figure 5-17: phase noise at the output of PLL (2457.6 MHz) using geometric mean N=16

Table 5-7: jitter calculated from 1.5 kHz to 10 MHz

Bands	Frequency (MHz)	Jitter (ps)
1, 2, 3, 4, 9 and 10	1920	0.46
5 and 8	883.2	1.06
7	2457.6	0.614
11	1459.2	0.6
12, 13 and 14	729.6	1.29

Table 5-7 lists the PLL output's rms jitter of maximum 1.29 ps for 729.6 MHz, and a minimum of 0.46ps for 1920 MHz.

5.4.Integration of Compensation System (MATLAB and Verilog Level)

Table 5-8: division ratios used for different LTE bands in the compensation algorithm

LTE Bands	N used in algorithm	$(N+F/2^f)$ used in algorithm	Fout required (MHz)
1,2,3,4,9,10	25	$(25+F/2^f)*2$	1920
5,8	23	$23+F/2^f*1$	883.2
7	16	$(16+F/2^f)*4$	2457.6
11	19	$(19+F/2^f)*2$	1459.2
12,13,14	19	$19+F/2^f*1$	729.6

*1→ Fout is generated from VCO/4, *2 → Fout is taken after from VCO/2, *4→Fout is generated directly from VCO

Back again to Equations (5.1-5.7), after settling the N, and f; we now can test the digital circuitry algorithm described in the beginning of the chapter. Starting with the passive temperature compensated MEMS oscillator output (chapter 2) characterized by the known parabolic shape with 105 ppm frequency shift across industrial temperature ranges as shown in Figure 2-10. We have to account for $\pm$8000 ppm as initial frequency error due to process spread and further reduce the temperature drift error. Table 5-8 lists the division ratios for LTE bands used in compensation algorithm, while Figures 5-18 to 5-25 shows the results of the algorithm for 729.6 MHz as band 12, 13 and 14 are characterized

by the lowest frequency output which settles the resolution specification assuming infinite resolution of TDC.

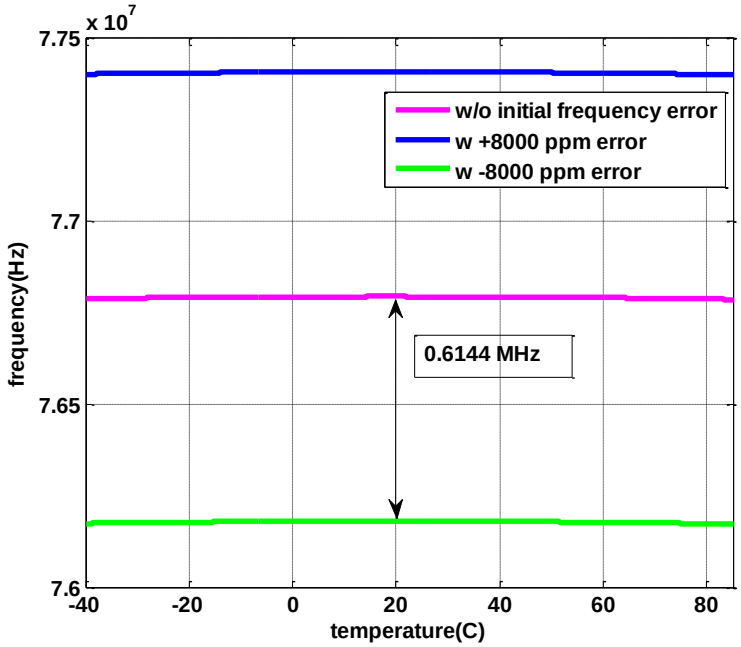

Figure 5-18: MEMS resonance frequency versus temperature with and without process variations

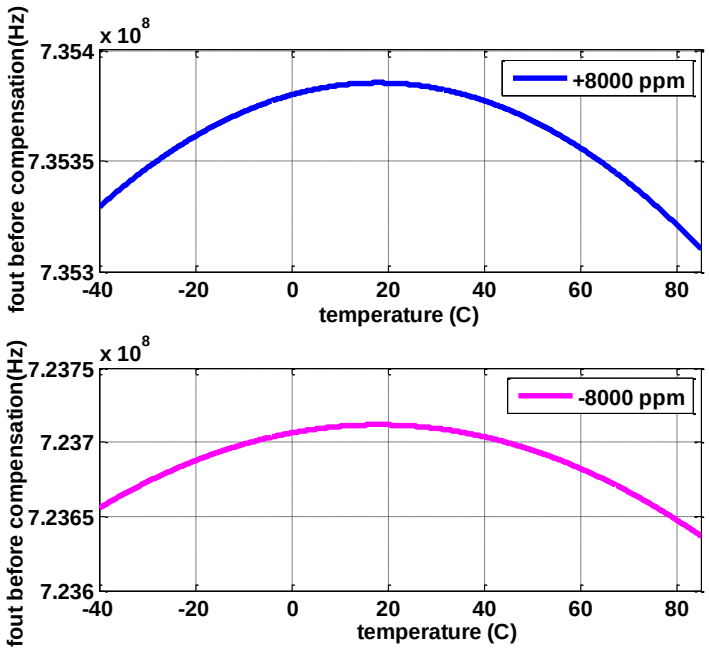

Figure 5-19: PLL output frequency before compensation vs temperature

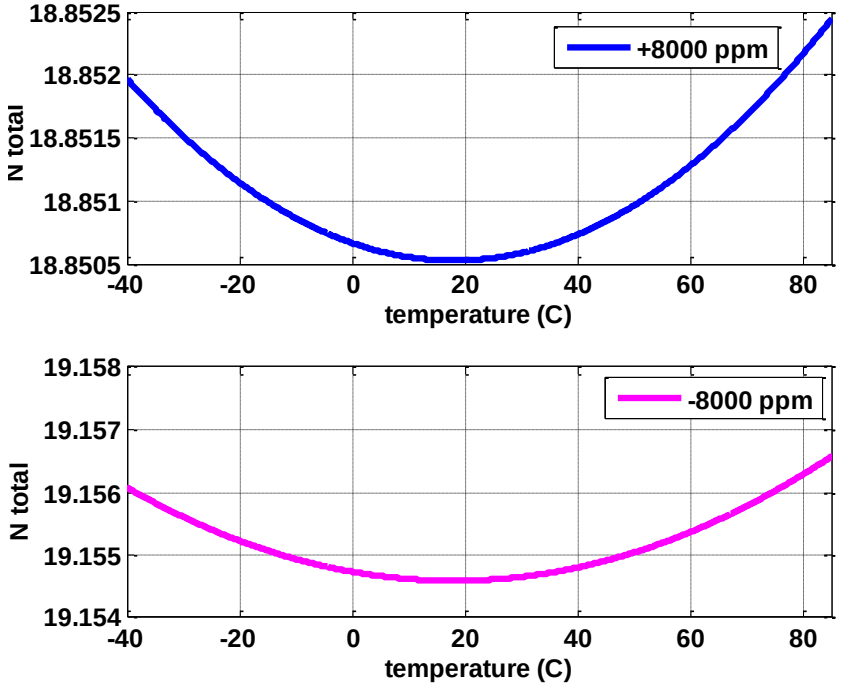

Figure 5-20: fractional N vs temperature

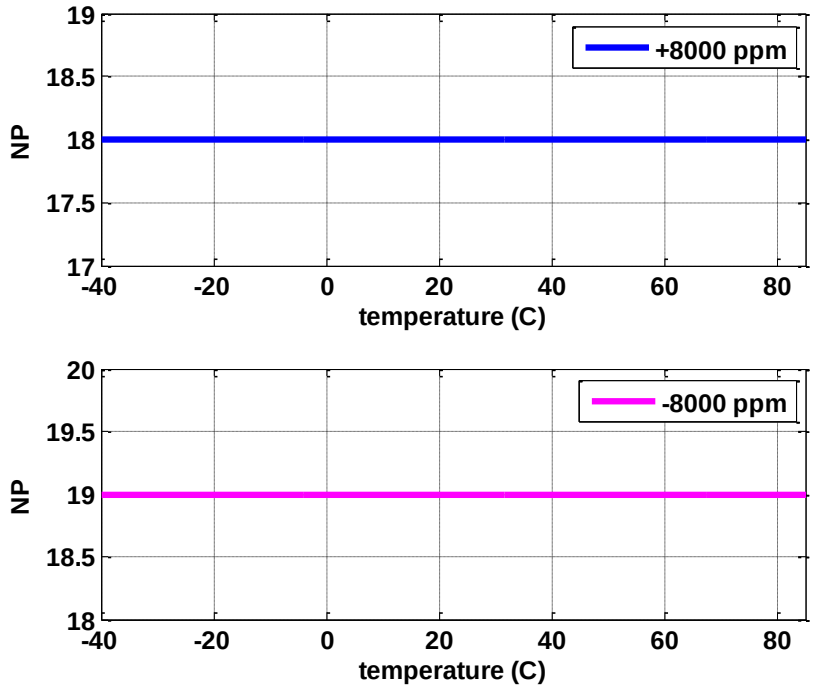

Figure 5-21: output integer N from temperature compensation circuitry vs temperature

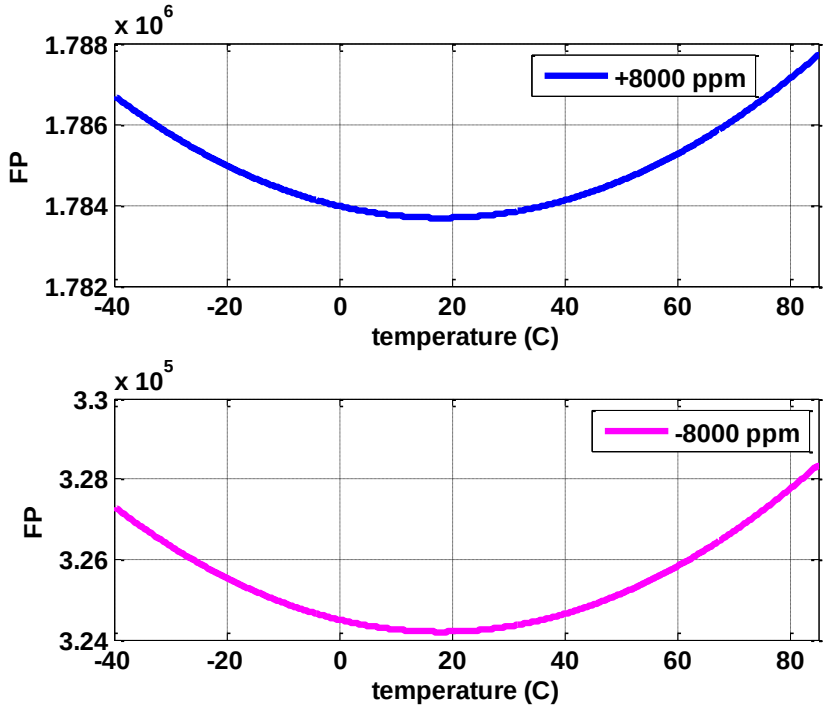

Figure 5-22: output word from temperature compensation circuitry vs temperature

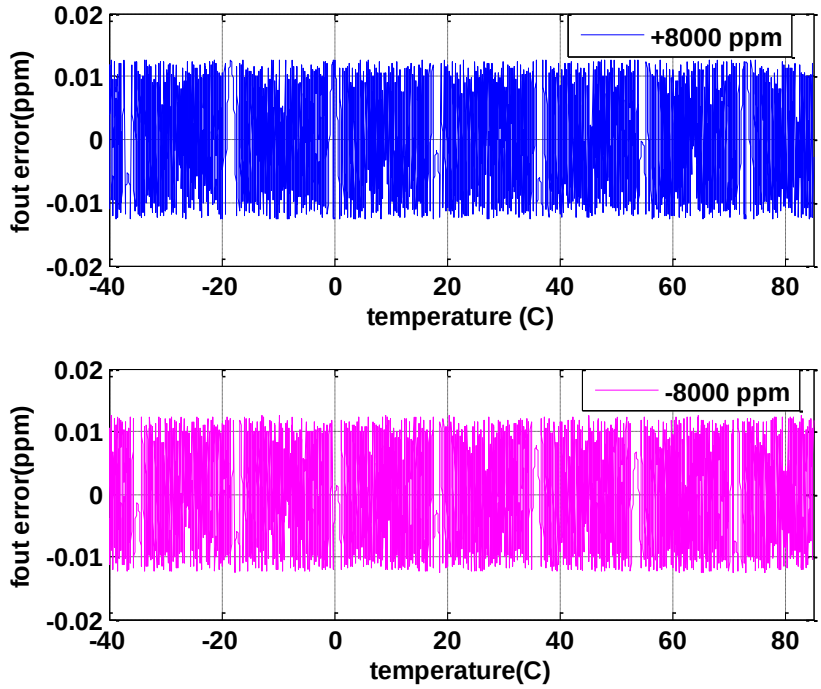

Figure 5-23: Error in PLL output after compensation vs temperature

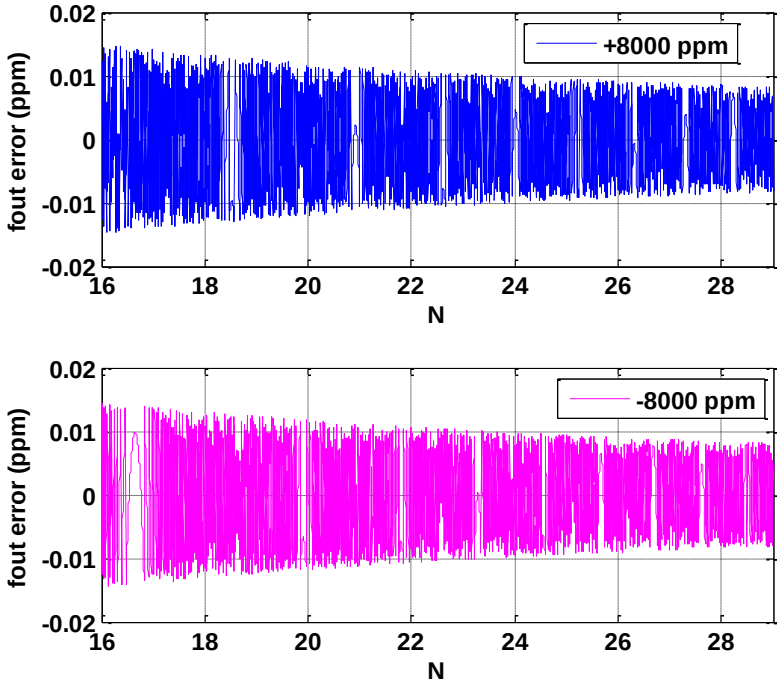

Figure 5-24: PLL output error after compensation vs N

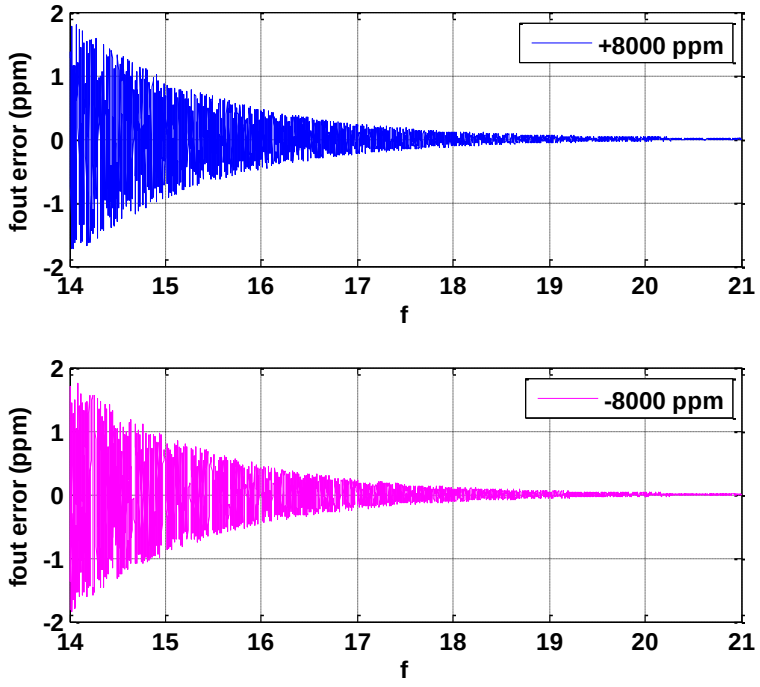

Figure 5-25: PLL output error vs SDM bits

It is clear that the resolution is mainly settled by the SDM block, the larger the number bits, the better the resolution. Resolution is also enhanced by increasing the integer N division ratio but this enhancement is negligible when compared to SDM number of bits effect. Figure 5-26 shows the FP algorithm output when f= 14 bits, it is clear that the output is not sensitive at all to temperature which means low frequency resolution and low frequency stability. Figure 5-27 shows the error in compensation factor FP after considering the TDC errors; the FP error increases with the absolute temperature. Notice that the sensitivity of FP to temperature is not constant. i.e., temperature error of 0.125˚C at -40˚C gives FP error of -13, while temperature error of 0.25˚C at 20˚C gives only FP error of 1. Figure 5-28 shows the sensitivity of FP to TDC errors. The sensitivity is Vshaped – trend due to the effect of the parabolic material compensation. FP ranges from 1783682 to 1787692 across temperature of -40˚C to 85˚C, assuming ±8000 ppm initial frequency offset. Thus FP full scale is only 4010, with maximum error of 34 at 70˚C (Figure 5-27)

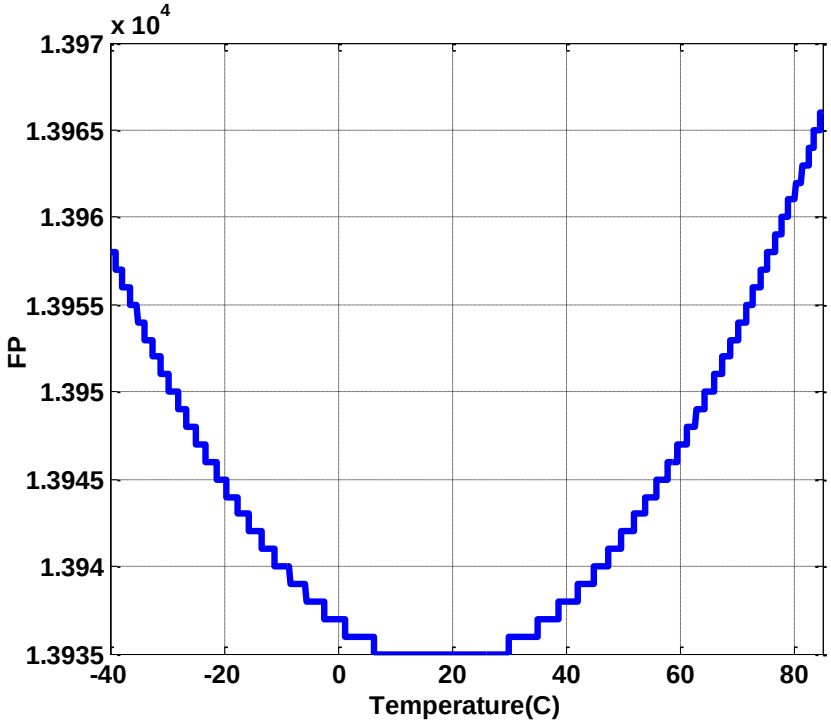

Figure 5-26: FP when using 14 bits SDM (f=14)

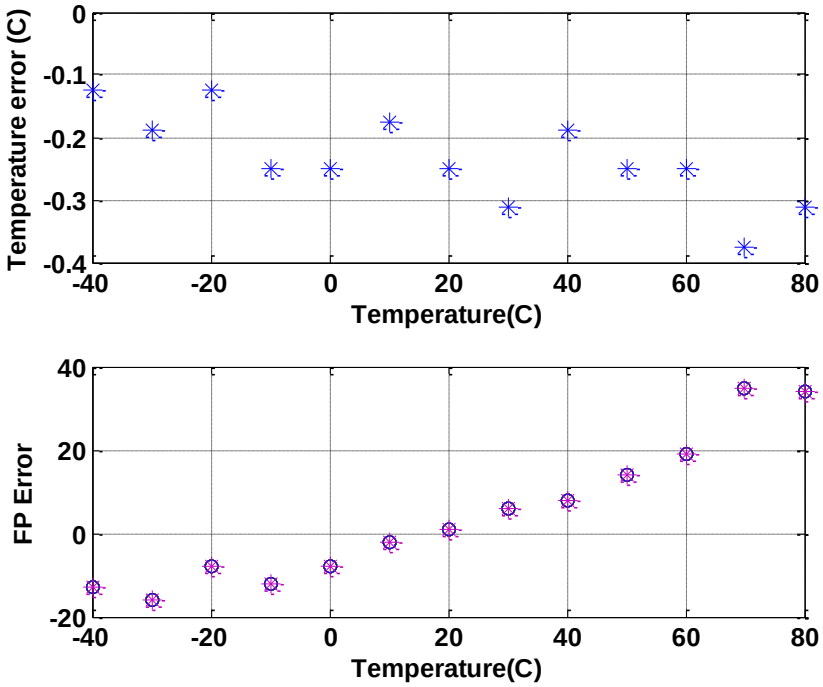

Figure 5-27: Error in compensation factor due to TDC limited resolution

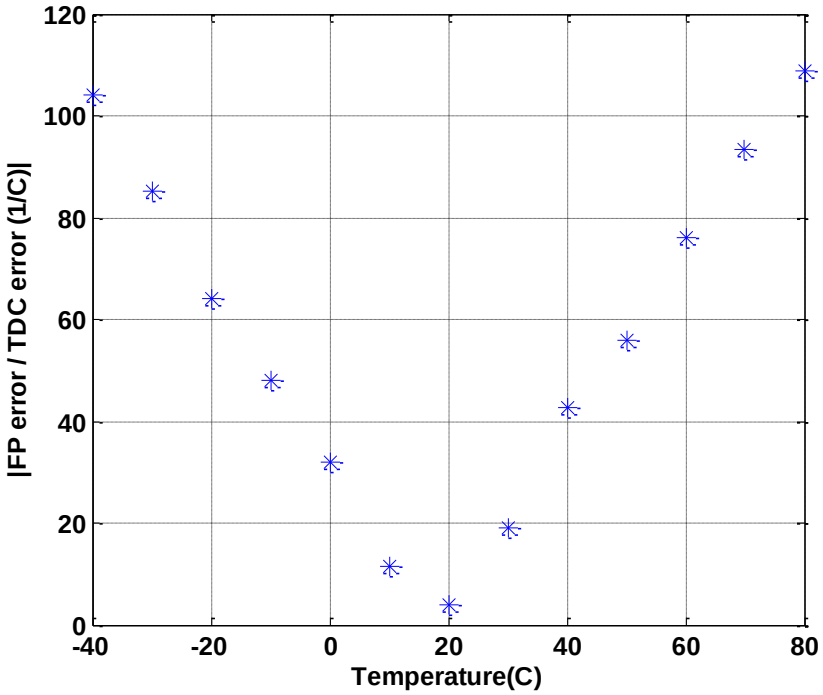

Figure 5-28: sensitivity of FP to temperature error

5.5.Transient (Verliog-A Simulations)

The above results considers the PLL as an ideal multiplying block without any non idealities, in this section a verilog-A model was built for the system to investigate on the settling and the VCO line ripples due to the instantaneous change in division ratio as a result of SDM operation. Figures 5-29 and 5-30 show the settling of PLL output frequency at 30 ˚C. Compensated frequency usually requires a longer settling time when compared with ideal reference source. The frequency resolution across temperatures is shown in Figure 5-31. The frequency output is averaged over the LTE settling time specification (50 μs) to get the resolution figures.

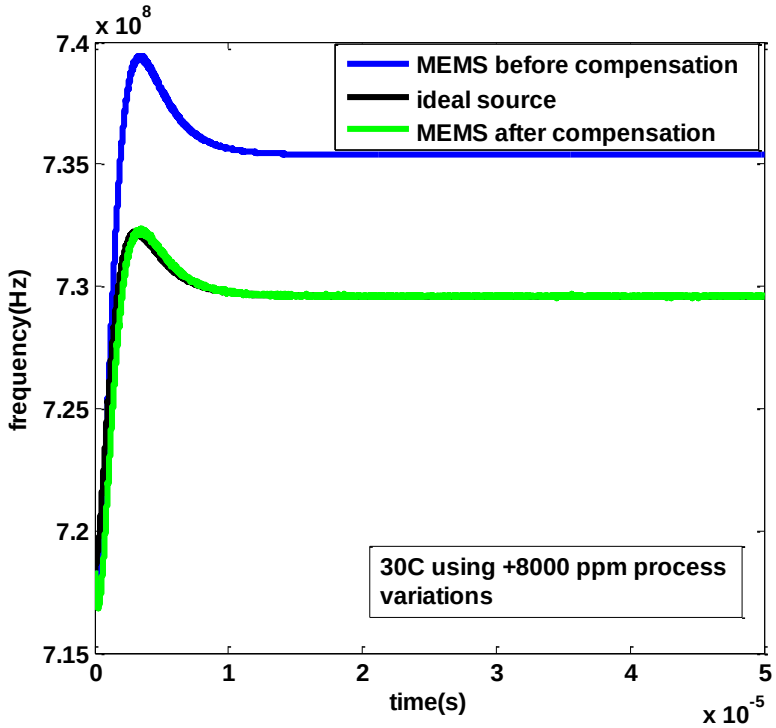

Figure 5-29: output frequency before compensation, after compensation, and using ideal source at 30˚C

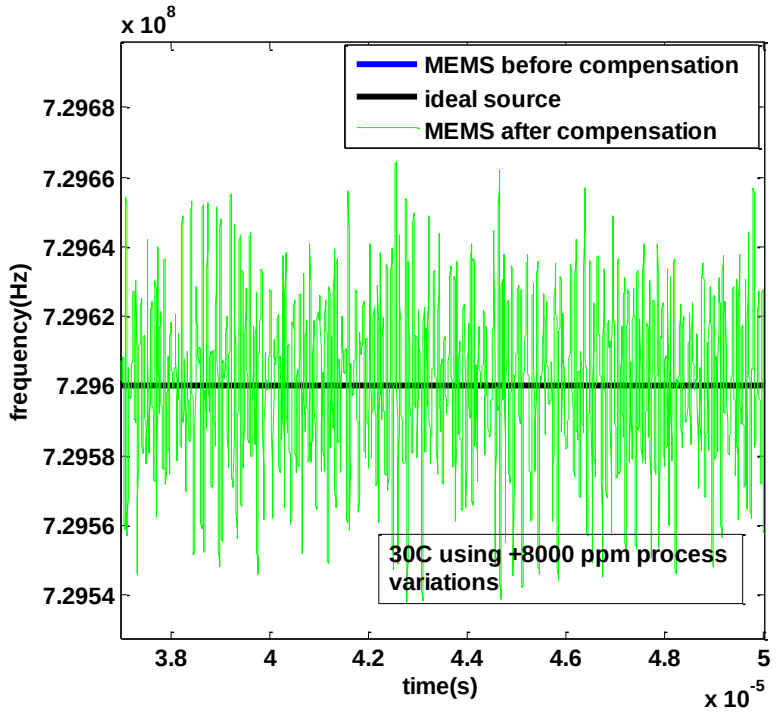

Figure 5-30: Figure 5-29 zoomed, instantaneous changes in division ratio are shown due to usage of SDM

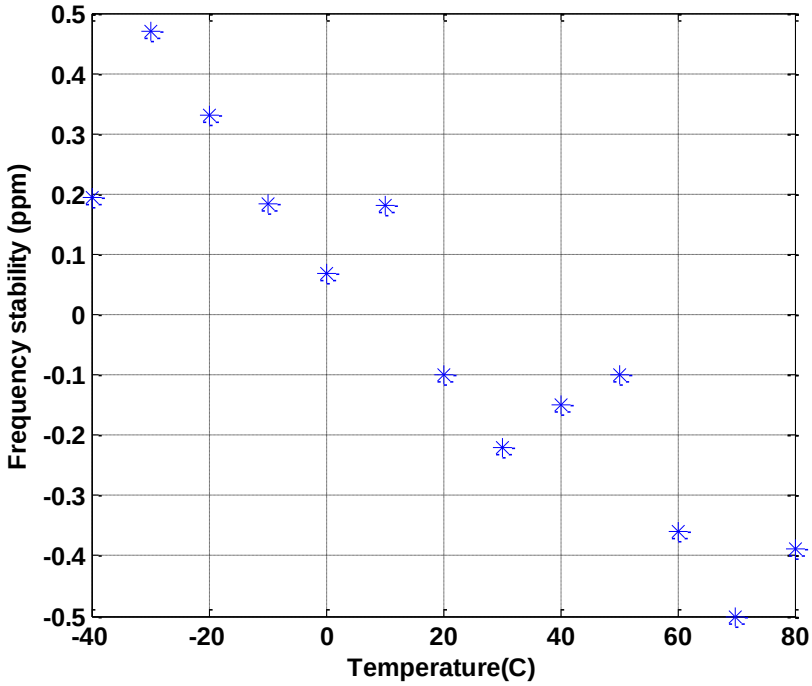

Figure 5-31: Output frequency resolution for 729.6 MHz (bands 12, 13 and 14 are the worst among all bands)

5.6. Performance Summary

Table 5-9 compares our work with the-state-of-art work in three main streams; the first is the MEMS core oscillator. The table lists all the important specifications from the resonator type, Q, motional resistance, power and phase noise specifications. The table focuses also on the temperature to digital converter block, comparing our performance to previous work in terms of the sensing device used, power consumption, and output the temperature resolution. At last the table compares the frequency compensation method used, and the output frequency stability metric of the oscillator.

Authors in [69] were targeting a real time clock based on AlN-on-silicon resonator driven at 1MHz with Q of 140,000 in vacuum, 200 ohm motional resistance, a current consumption of 3.2 μA and 3 ns rms jitter. The TDC is based on thermistor front end and a frequency to digital converter consuming 30 μA with resolution of 0.04 K, in 7.5ms conversion time. The frequency stability is $\pm$10 ppm (0→50˚C) for 32 kHz output frequency. Compensation is done in digital fashion using dividers and counters. It is clear that although the very high Q, only -110 dBc/Hz phase noise was achieved at 10 kHz, due to very low power consumption.

Authors in [92] were targeting a GPS reference oscillator based on quartz resonator driven at 40MHz. GPS imposes a stringent specification on the thermal frequency drift to be less than 50ppb/˚C affecting the choice of the TDC. The frequency compensation scheme has to be very fast to sense the frequency changes while temperature ramps. The TDC is based on thermistor front end and a 12 bit SAR consuming 800 μA with resolution of 0.05 K, in 2ms conversion time. The frequency stability is $\pm$0.5 ppm (-10→80˚C) for 40 MHz output frequency. Compensation is done in digital fashion using LUT and capacitor banks.

Authors in [54] were targeting a reference oscillator for wireless communications based on AlN-on-silicon resonator driven at the 5th tone 427 MHz with Q of 1400 in vacuum, 180 ohm motional resistance, and a current consumption of 7.2 mA. The temperature

sensor is based on BJT front end and some analog circuitry. Material temperature compensation achieves frequency stability of $\pm$390 ppm, where electronic compensation further reduces this value to $\pm$35 ppm (-10→70˚C).

Authors in [71] were targeting a reference oscillator for 4G and GPS applications based on all-silicon resonator driven electrostatically at 48 MHz with Q of 140,000 in vacuum, and a current consumption of 2 mA. The chip frequency output is programmable ranging from 0.5MHz to 220MHz. The temperature sensor is based on thermistor front end and 2nd order ΣΔADC characterized by resolution of 0.1 mK in 100 ms, while consuming 3.97 mA. Electronic compensation is based on fractional N-PLL with frequency stability of $\pm$0.5 ppm (-40 →85˚C) at 100 MHz and jitter of 0.573ps at the same frequency output was achieved.

Authors in [74] were targeting real timing keeping applications based on all-silicon resonator driven electrostatically at 524 kHz with Q of 52,000 in vacuum, motional resistance of 90 kΩ, and a current consumption of 0.24 μA. The chip frequency output is programmable ranging from 1Hz to 32 kHz. The temperature sensor is based on BJT front end and 2nd order ΣΔADC characterized by resolution of 0.025K in 6 ms, while consuming 4.5 μA. Electronic compensation is based on fractional N-PLL with frequency stability of $\pm$3 ppm (-40 →85˚C) was achieved.

Our work targets wireless communications applications. The MEMS oscillator is based on AlN-on-silicon resonator driven at the 1st tone 76.8 MHz with Q of 9950 in vacuum, 125 ohm motional resistance, a current consumption of 0.85 mA, and rms jitter of 106fs. The temperature sensor is based on BJT front end and 12 bit 2nd order ΣΔADC characterized by resolution of 0.075K in 100 ms, while consuming 4.6 μA . Material temperature compensation achieves frequency stability of 105 ppm, where electronic compensation based on fractional N-PLL further reduces this value to $\pm$0.5 ppm (-10→70˚C) at 729.6 MHz LTE output.

Table 5-9: Comparison with the-state-of-the-art

	P.O.C		**This work**	[69] 2010	[92] 2010	[54] 2012	[71] 2013	[74] 2014
	Technology		**1.8 V in 32nm CMOS**	0.18μ CMOS	2.5V/1V in 45nm CMOS	0.18μ CMOS	3.3 V in 0.18μ CMOS	1.5V – 4.5V in 0.18μ CMOS
MEMS core oscillator	MEMS resonator		**AlN-on-Silicon**	AlN-on-silicon	Quartz	AlN-on-silicon	Electrostatic Silicon	Electrostatic Silicon
	frequency (Hz)	MEMS	**76.8 M**	1 M	40MHz	427 M	48 M	524 k
		Chip o/p	**LTE 699M→2690M**	32.768 k	40MHz	427 M	0.5M→220M	1 →32kHz
	Mode of operation		**1st**	1st	1st	5th	1st	1st
	Qunloaded		**9950**	140,000 (vaccum) 20,000 (air)	-	1400	140,000	52,000
	Rm Ω		**125**	200	-	180	-	90,000
	Core oscillator PN(dBc/Hz)	1 kHz 10 kHz Floor	**-123** **-143** **-162**	- -110	-	-82 - -147	- -140 -	- - -
	RMS jitter (ps)	Oscillator	**0.106**	3000	-	-	-	-
		Chip o/p	**1.29 @ 729.6 MHz**	-	-	-	0.573@ 100 MHz	-
Temperature to digital converter	Temp range(˚C)		**-40→85**	0→50	-10→80	-10→70	-40→85	-40→85
	Temperature sensor front end		**BJT**	Thermistor	Thermistor	BJT	Thermistor	BJT

	Temperature to digital converter		**2nd order 12 bits ΣΔ ADC**	FDC	12bit SAR	-	2nd order ΣΔ ADC	2nd order ΣΔ ADC
	Supply Current (μA)	Oscillator	**850**	3.2	-	7200	2000	0.24
		TDC	**4.6**	30	800	-	3970	4.5
	TDC Resolution(K)		**0.075**	0.04	0.05	-	0.0001	0.025
	TDC Conversion time (ms)		**100**	7.5	0.002	-	100	6
	TDC Resolution FOM(nJ˚C ^{2})		**4.65**	0.36	-	-	0.013	0.024
Compensation	Electronic Compensation		**Fractional N-PLL**	Digital	Digital LUT+ cap. Banks	Parabolic-analog	Fractional N-PLL	Fractional N-PLL
	Output frequency resolution	Material	**105 ppm**	-	-	±390 ppm	-	-
		Electronic	**±0.5 ppm @ 729.6 MHz**	±10 ppm	±0.5 ppm	±35 ppm	±0.5 ppm @ 100 MHz	±3 ppm

6.Conclusions and Future Work

6.1.Conclusion

The thesis presents a platform for MEMS reference oscillators targeting wireless applications. LTE is taken as an example to implement the platform for its stringent specifications on phase noise and frequency resolutions. The thesis justifies the need to replace bulky crystal oscillators with MEMS oscillators for the sake of cost and area in mobile devices. The thesis solves the two main challenges to implement MEMS reference oscillators for wireless communications, which are resonator's initial frequency offset due to process tolerance ($\pm 8000\, ppm$) and resonator's temperature drift ($3000\, ppm$). Initial offset is solved using electronic compensation. While temperature drift problem is mitigated by using both material and electronic compensation.

6.2.Future Work

- A number of research areas can benefit from high frequency MEMS reference oscillators. GHz resonators will ease system level specifications of phase locked loops and thus RF transceivers.
- Studying nonlinear operation of resonators, and its effect on phase noise.
- Investigations on single-resonator multi-frequency operation for multi-standard receivers.
- Studying the performance of widely tunable micromechanical resonators array.
- Intensive study can be carried on low power - low phase noise series resonance oscillators to reduce the system power.
- Thermistor usage instead of band-gap front end circuitry for temperature sensing for more accurate results.

- Investigations on low power techniques in ΣΔ ADC.
- Study different dynamic element matching techniques, ADC system chopping for better accuracy results
- Effect of TDC on phase noise of output
- Transferring the system to silicon.

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