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Design of Reliable Analog DMTL Phase Shifter with Improved Performance for Ku Band Applications

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ABSTRACT

An analog phase shifter based on distributed MEMS transmission line (DMTL) is designed for Ku band applications. Traditional RF MEMS phase shifter comprising 6 switches has limited phase shift of 37.75° due to instability region. A new concept of stopper is incorporated to achieve high phase shift. In the present paper, optimisation of the analog phase shifter is done to increase its phase shift upto 88.63°. Phase shift is a strong function of capacitance ratio which is increased from 1.75 to 2.95. The maximum operating voltage and mechanical resonant frequency for the phase shifter are 16 V and 8.3 KHz, respectively. The switching time is calculated to 56 µs. The simulated insertion loss of the phase shifter is -1.75 dB with return loss of -20.49 dB at 17 GHz. The simulated results are verified with analytical modelling which are in close match.

Keywords: RF MEMS, DMTL, phase shifter, varactor, Ku band applications

1. INTRODUCTION

Radio frequency micro-electro-mechanical-system (RF MEMS) is an emerging sub-area of MEMS technology which offers wide range of benefits. It enables radar, sensors and broadband communication devices for various military and commercial applications[1-2]. MEMS switch promises to combine useful properties of both mechanical and semiconductor switches e.g. low loss and DC power consumption, reduced size, weight and cost[3]. RF MEMS switches or varactors are the essential blocks of RF MEMS phase shifter[4-6]. Employing, capacitive switches in phase shifters can considerably reduce losses, size, therefore scaling down the area of phased array antenna where thousands of phase shifters are mounted[7-14].

Depending on the application, design approach of phase shifter is classified into two categories viz., analog and digital. In analog approach, continuously varying phase shift is obtained from 0 to 360° and fabricated using MEMS varactors while in digital approach, discrete set of phase delays are obtained and fabricated using MEMS switches[14].

The various ways of implementing analog phase shifter have been reported in literature. Barker et al.[15] reported capacitance ratio of 1.15 with pull-in of 26 V. The measured phase shift/decibel loss, insertion, and return loss were 70°/dB (75 GHz to 110 GHz), -2.5 dB, -11 dB at 94 GHz, respectively. N. Scott Barker[17] discussed capacitance ratio (1.5) and phase shift (360°) with insertion loss: -4 dB at 60 GHz and -5 dB at 100 GHz. W Palei[11] presented true time delay (TTD) phase shifter for Ku band with measured return loss (S_{11}): -15 dB and average loss: -2.3 dB/phase shift of 250° at 20 GHz.

According to the literature reviewed, there is a major issue of controlling bridge height by regulating voltage precisely which provides the maximum capacitance ratio of 1.5:1(electrostatic force at center of MEMS bridge) before snap down with a very small phase shift. But for commercial applications, high reliability and better response are prime concerns. To mitigate above issues, a new concept of stopper is introduced in the design.

2. DESIGN OF MEMS BRIDGE

Amongst various actuation mechanisms, electrostatic actuation technique is often preferred due to almost zero power consumption, small electrode dimensions, ease of fabrication steps and better compatibility with IC fabrication techniques. The reliability of an analog phase shifter primarily depends on the actuation of MEMS bridge which works as a varactor. In terms of performance, the tuning range of MEMS bridge must be within the limit of instability. Most of the phase shifters available in literature have been designed using fixed-fixed beam, where force is applied at the center[15-16]. In this case, the bridge can travel maximum ≈33.33 per cent of its initial height, resulting in a maximum capacitance ratio 1.49:1. In order to increase maximum travel range and capacitance ratio, force can be evenly distributed along the ends of the beam as shown in Fig. 1. Accordingly, the maximum travel range and capacitance ratio is increased to ≈ 43.33 per cent and 1.75:1 respectively as shown in Fig. 2(a).

The major drawback of analog phase shifter is instability of MEMS bridge. To solve this issue, stopper has been incorporated in the mechanical design of unit cell for preventing a snap down of the bridge as shown in Fig 1.

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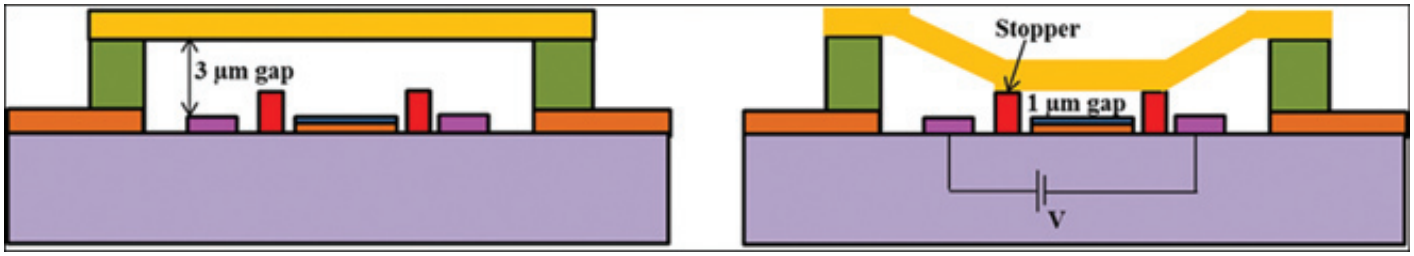

Figure 1. Proposed design of unit cell with stopper.

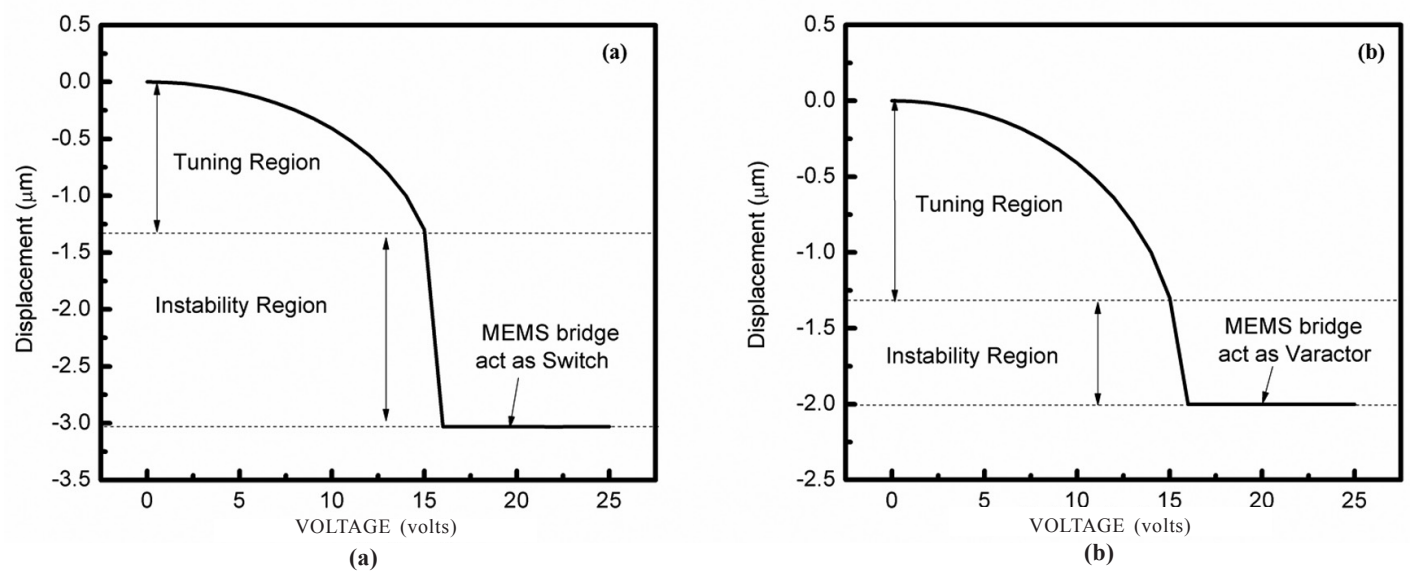

Figure 2. MEMS bridge instability: (a) without stopper and (b) improved by incorporating stopper.

The design parameters of MEMS bridge are mentioned in Table 1. Electromechanical simulations were performed on 3D FEM based software tool i.e., CoventorWare©. Initially, the MEMS bridge is at 3 µm which becomes instable at 1.70 µm from bottom on applying maximum operating voltage of 16 V as shown in Fig. 2(a). Thus for achieving height of 1 µm from bottom of the transmission line is next to an impossible task as MEMS bridge snaps down at 1.70 µm height.

Unlike the switch, the two floating stoppers are designed and placed adjacent to the central capacitive area at a distance of 10 µm as shown in Fig 3. This creates a smaller gap of 1µm between the MEMS bridge and central capacitive area of transmission line as shown in Fig 4. And this way MEMS bridge acts as a varactor by traveling maximum range (66.66 per cent of its initial height) with high capacitance ratio (2.95: 1). Finally, deflection and capacitance ratio is increased by 1.54 and 1.68 times, respectively, compared to the design without stopper.

Table 1. Summary of design parameters of MEMS bridge for analog phase shifter

Design parameters	Values
Capacitive area	150x110 µm^2
Total bridge length	580 µm
Bridge thickness	1.5 µm
Dielectric thickness(SiO_2)	0.1 µm
Bridge initial gap	3 µm
Stopper height from transmission line	1 µm

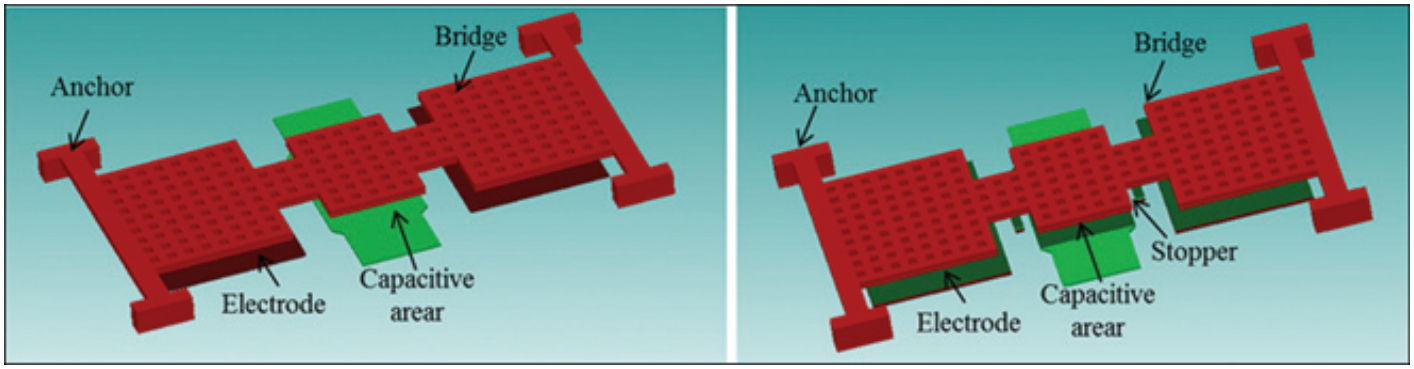

Figure 3. Design of MEMS Bridge without stopper and with stopper.

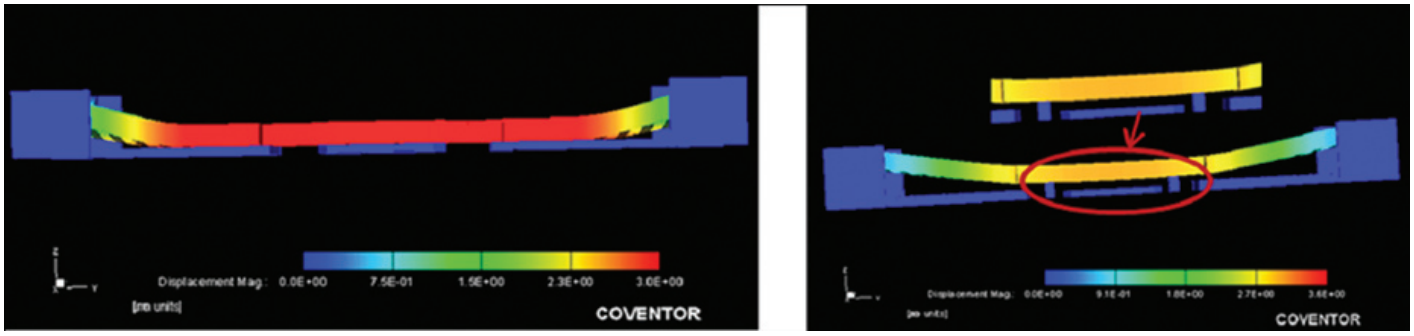

Figure 4. Actuation at pull-in without stopper and with stopper.

The simulated resonance frequency is 8.3 KHz. The calculated switching time is 56 µs for an applied voltage of 20 V from Eqn (1).

$$t_s = 3.67\left(\frac{V_p}{V_s \omega_0}\right) \quad (1)$$

where t_s is the switching time, ω_0 resonant frequency, V_p is the pull-in voltage, V_s is the applied voltage.

3. UNIT CELL OPTIMISATION

The design of DMTL phase shifter requires specification: dielectric constant of substrate, characteristic impedance of unloaded transmission line and Bragg frequency. One of the advantages of using silicon as substrate is that the phase shift ($\nabla\varphi$) is directly proportional to $\sqrt{\varepsilon_{eff}}$ as shown in Eqn (6). The other advantage of using silicon substrate is that fused quartz or glass substrate offers poor thermal properties as compare to silicon substrate. For example: silicon substrate has 111 times higher thermal conductivity compare to fused quartz[18]. Therefore, DMTL phase shifter on Si substrate gives more phase shift per unit length as well as improves power handling capability compared to quartz substrate[18].

Three types of unit cells are designed on silicon substrate with different characteristic impedances of 70 Ω, 65 Ω and 50 Ω, where (W+2G) are 410,330,196 µm, respectively. The design parameters of unit cells are shown in Table 2. Electromagnetic simulations were performed on 3D FEM based software tool i.e. High Frequency Structural Simulator© (HFSS). The length of each unit cell is 800 µm. It is necessary to maintain loaded line impedance within the range of 60 Ω – 42 Ω to maintain the return loss below -10 dB. The simulated results of each unit cell are shown in Fig. 5. Unit cell-I has better performance than others in term of low insertion loss – 0.56 dB and return loss -14.18 dB with 15.76° phase shift at 17 GHz.

Table 2. Summary of design parameters of unit cells for analog phase shifter

Design parameters	Unit Cell I	Unit Cell II	Unit Cell III
Co-Planar waveguide (CPW) impedance	70	65	50
W+2G (µm)	410	330	196
Bragg frequency (GHz)	$2f_0$	$1.8f_0$	$1.7f_0$
Number of switches	1	1	1
Unit cell length (µm)	800	800	800
S_{12} @ 17GHz	-0.56 dB	-0.61 dB	-0.68 dB
S_{11} @ 17GHz	-14.18 dB	-12.37 dB	-10.69 dB
Phase shift(°)	15.76	14.80	13.57
Z_{lu}-Z_{ld} (Ω)	58-44	53-42	43-34

The other parameter, gap variation has a significant effect on desired phase shift; higher gap difference in two states gives higher phase shift. The two simulations have been carried out for all three CPW impedances for optimising maximum gap differences of 3 µm – 1 µm and 3 µm – 0.5 µm. The losses degrade at 3 µm – 0.5 µm as shown in Fig. 6. Thus, the maximum optimised gap is 3 µm – 1 µm for minimum loss in a single unit cell.

4. RESULTS AND DISCUSSION

4.1 Analytical Modelling

The DMTL phase shifter based on CPW configuration comprises of a high impedance (> 50 Ω) transmission line and loaded periodically with MEMS bridges (work as varactor). The distributed transmission line is connected to 50 Ω input and output lines for testing purpose. By changing distributed capacitance of the MEMS bridge results in variation in phase velocity, v_l , of the electromagnetic wave on the loaded CPW, as given by relation:

$$v_l = \frac{1}{\sqrt{L_u[C_u + (C_{MEMS}/s)]}} \quad (2)$$

where L_u and C_u are inductance per unit length and capacitance per unit length of the unloaded CPW, respectively[19-20]. C_{MEMS} is the variable capacitance between MEMS bridge and transmission line and s is the periodic spacing between the MEMS bridges.

$$L_u = C_u Z_0^2, \quad (3)$$

$$C_u = \frac{\sqrt{\varepsilon_{eff}}}{cZ_0} \quad (4)$$

where Z_0 is the characteristic impedance of unloaded transmission line. ε_{eff} is the effective dielectric constant of the unloaded transmission line i.e. CPW.

The loaded line impedance, Z_l, is given by relation:

$$Z_l = \sqrt{\frac{L_u}{[C_u + (C_{MEMS}/s)]}} \quad (5)$$

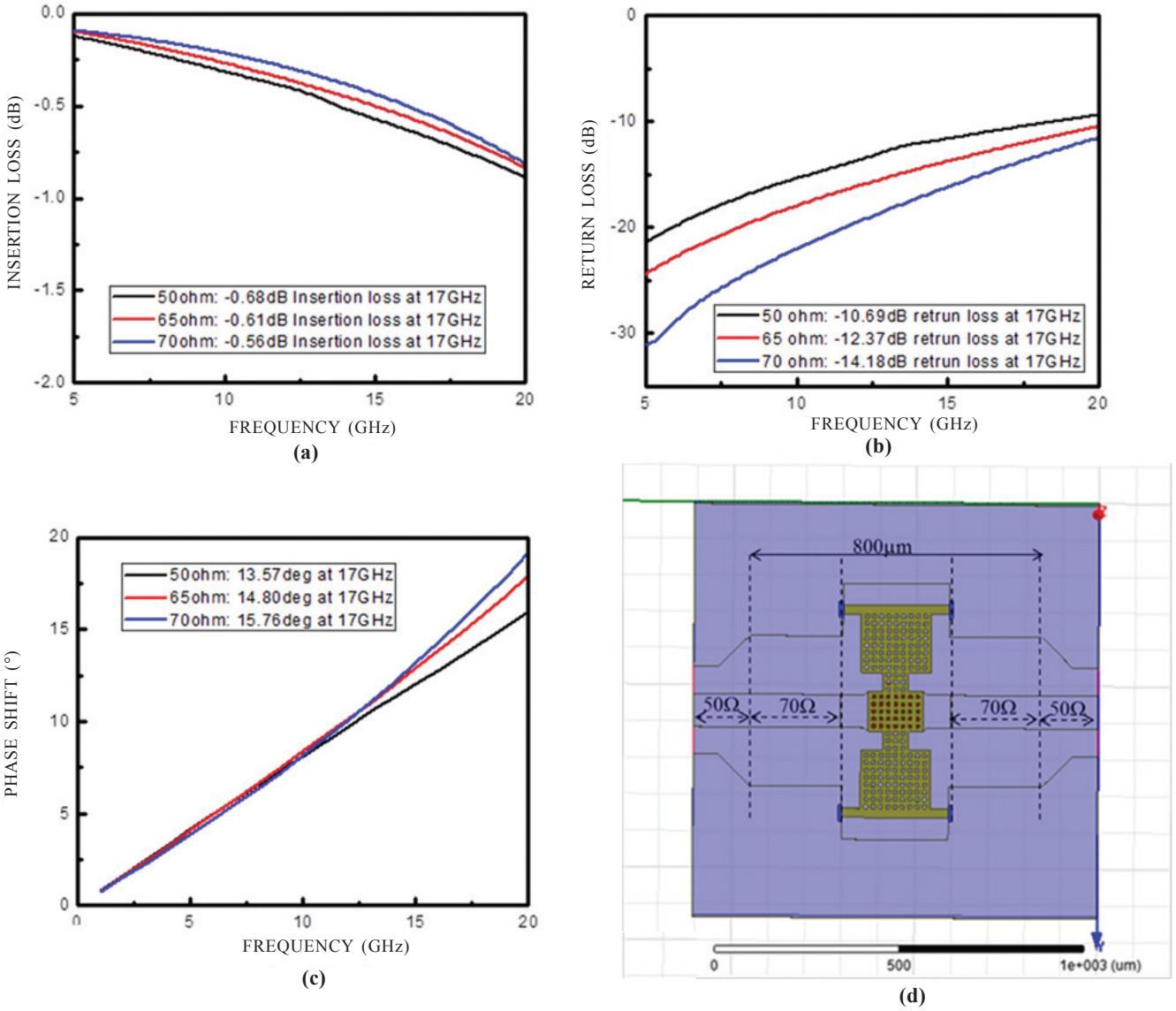

Figure 5. Simulated results of three types of unit cell at 1µm gap: (a) insertion loss (dB), (b) return loss (dB), (c) phase shift, and (d) Unit cell of phase shifter.

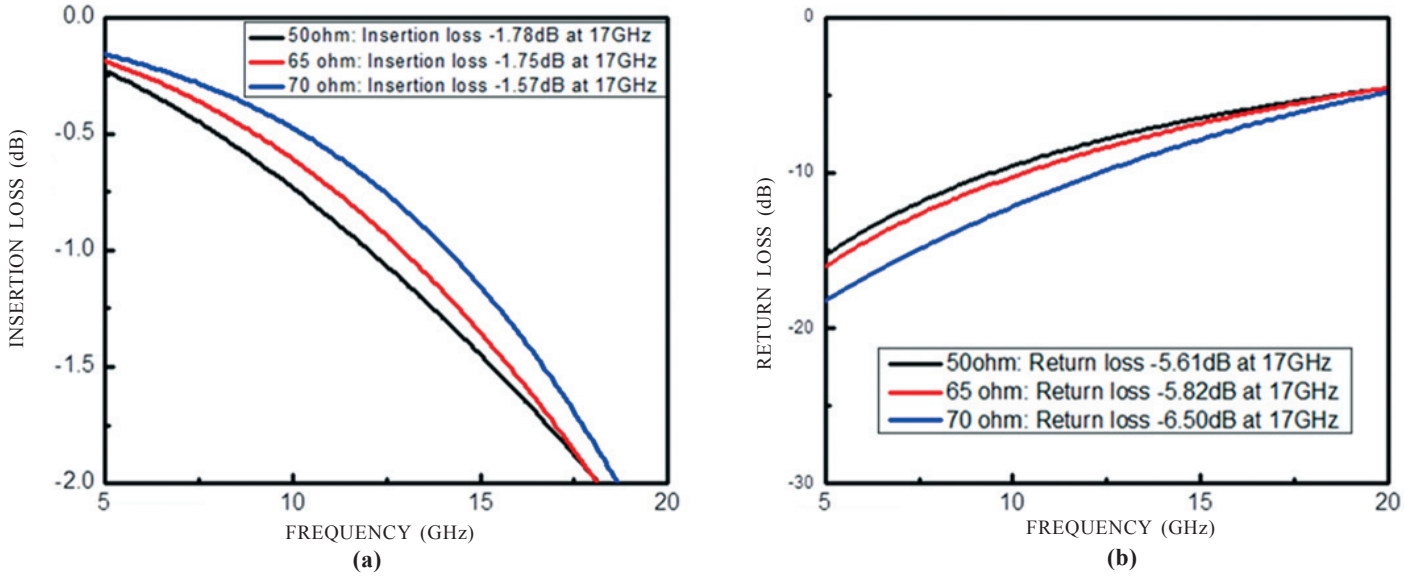

Figure 6. Simulated results of three types of unit cell at 0.5 µm gap: (a) insertion loss and (b) return loss.

From Eqn. (5) by increasing, C_{MEMS}/s, the phase velocity will be decreased by keeping all parameters constant. If v_{l1} and v_{l2} are the phase velocities at two variable gaps, then the differential phase shift $\nabla\varphi$ in degree per meter assuming $v_{l1} > v_{l2}$ is

$$\nabla\varphi = 360 f\left(\frac{1}{v_{l2}} - \frac{1}{v_{l1}}\right) \text{deg/ } meter\ ,$$

Or

$$\nabla\varphi = \frac{360 f Z_0 \sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{l2}} - \frac{1}{Z_{l1}}\right) \text{deg/ } meter, \quad (6)$$

where f is the operating frequency. Z_{l1} and Z_{l2} are the loaded line impedances at two variable gaps.

The periodic configuration has maximum frequency limit due to the Bragg reflection.

$$f_{Bragg} = \frac{1}{\pi s\sqrt{L_u[C_u + (C_{MEMS}/s)]}} \quad (7)$$

$$\varepsilon_{effl} = \frac{c\sqrt{(sL_u(sC_u + C_{MEMS}))}}{s} \quad (8)$$

where, f_{Bragg}, is the bragg frequency at which no power is transmitted through transmission line because loaded line impedance goes to zero. ε_{effl} is the effective dielectric constant of the loaded line.

4.2 3-D FEM Simulation

The unloaded line impedance of 70 Ω is optimised with an effective dielectric constant of 5.98 for phase shifter. Fig. 7 shows the simulated results of insertion (S_{21}) and return loss (S_{11}) at 3 µm (at 0 bias voltage) and 1 µm gap (at 16 bias voltage). It is seen from the return loss that the S_{11} at 1 µm gap has more closely spaced nulls signifying that the transmission line is electrically longer than 3 µm gap. Since the physical length of the DMTL is not changed from Eqn (2) increasing C_{MEMS}/s, the phase velocity decreases; keeping all parameters constant, as expected. According to Eqn (5) the upstate

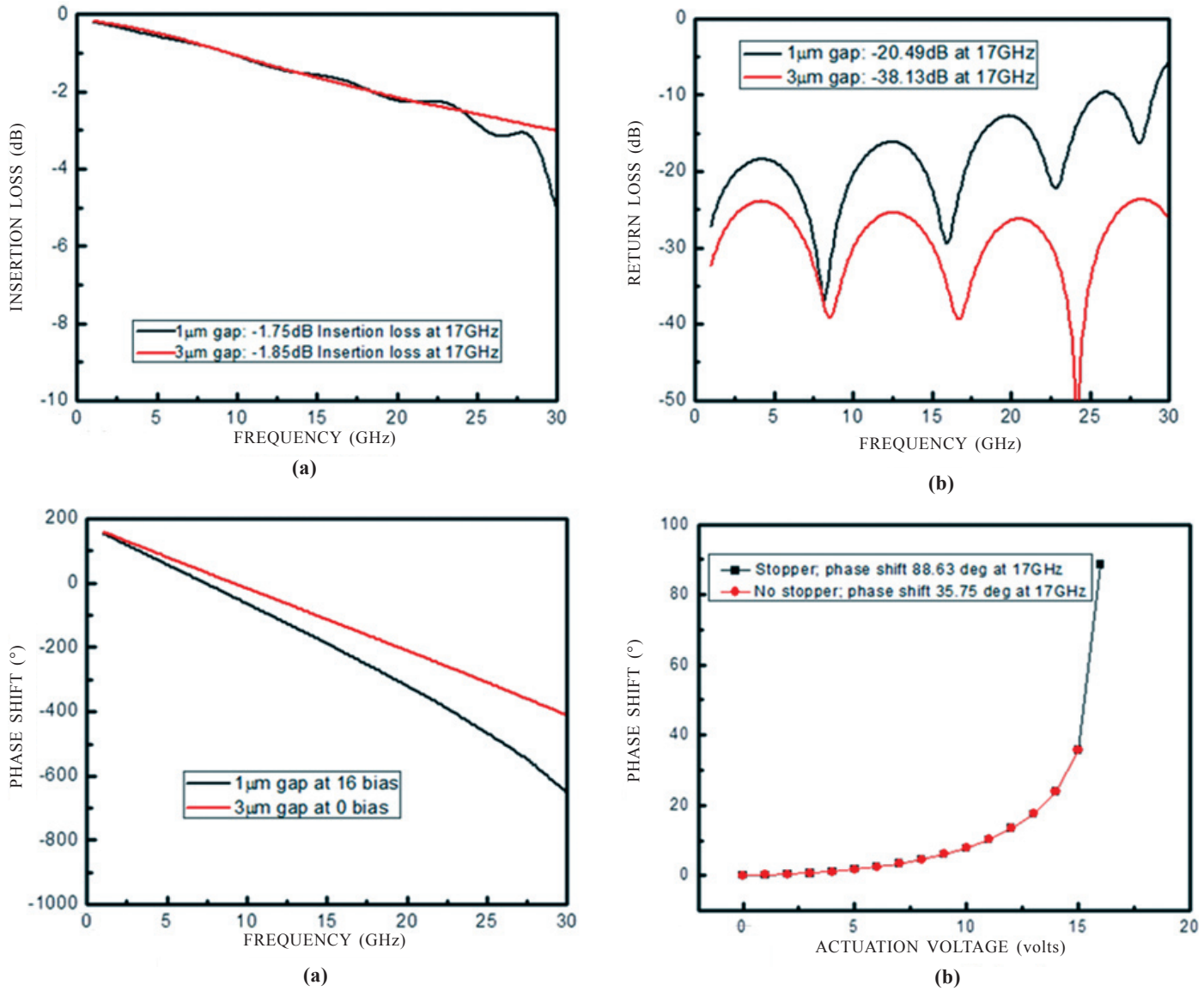

Figure 7. Simulated results of analog phase shifter with 6 unit cells (a) insertion loss, (b) return loss, (c) phase shift versus frequency, and (d) phase shift *vs* actuation voltage.

characteristic impedance is 56.81 Ω and in down state 41.12 Ω. However, the loaded line impedances ($Z_{lu} = 56.39\Omega$ and $Z_{ld} = 44.33\Omega$) are determined from the first peak in return loss at 4.3 GHz from Eqns (9) and (10). At 4.3 GHz frequency, the loaded transmission line is performed as a quarter-wave transformer. The smaller variation in loaded line impedance is due to an effect of the feed line at both ends of the distributed transmission line which adds small inductance.

$$Z_{lu} = Z_0\sqrt{\frac{1+S_{11}}{1-S_{11}}} \tag{9}$$

$$Z_{ld} = Z_0\sqrt{\frac{1-S_{11}}{1+S_{11}}} \tag{10}$$

where, Z_0, Z_{lu} and Z_{ld} are unloaded and loaded (in both states) line impedances. S_{11} is return loss. The calculated effective dielectric constant for the loaded transmission line with $C_{bu} = 40fF$ is $\varepsilon_{effl} = 9.08$ from Eqn (8). The effective dielectric constant ($\varepsilon_{effl} = 9.79$) is also confirmed from the adjacent nulls in the simulated S_{11}.

As seen from the Fig. 7(c), phase shift ($\nabla\varphi$) increases linearly with frequency as expected for a true time delay type phase shifter having $C_r = 2.95$. There is deviation from the linearity at approximately 30 GHz which is a result of move towards the Bragg frequency (calculated Bragg frequency is 30.69 GHz). The maximum simulated phase shift for 6 MEMS bridges is 88.63° with insertion loss: -1.75 dB and return loss: -20.49 dB at 17 GHz. The improved design with stopper shows the increased phase shift to 88.63° from 37.75° (one without stopper) as shown in Fig. 7(d). The phase shift versus capacitance ratio is as shown in Fig. 8. The parameters, extracted from analytical modelling using Eqns (2)-(8) are shown in Table 3.

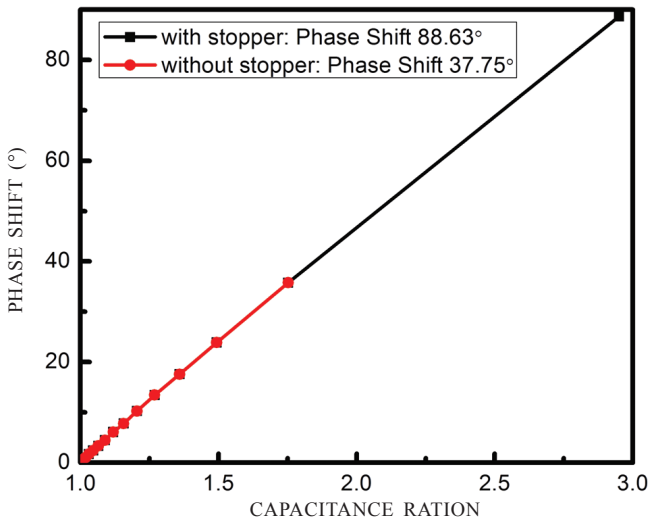

Figure 8. Phase shift versus capacitance.

Table 3. Summary of calculated and simulated parameters for analog phase shifter

Design parameters	Calculated	Simulated
Characteristic impedance	70Ω	--
Effective dielectric Constant of unloaded line	5.98	
Bragg frequency (GHz)	(1.8 f_0) 30.69 GHz	(1.76 f_0) 30 GHz
Z_{lu}-Z_{ld}(Ω)	56.81 & 41.12 Ω	56.39 & 44.33 Ω
Effective dielectric Constant of loaded line	9.08	9.79
Number of switches	6	6
S_{12} @ 17GHz	--	-1.75dB
S_{11} @ 17GHz	--	-20.49dB
Phase Shift (°)	85.71°	88.63°

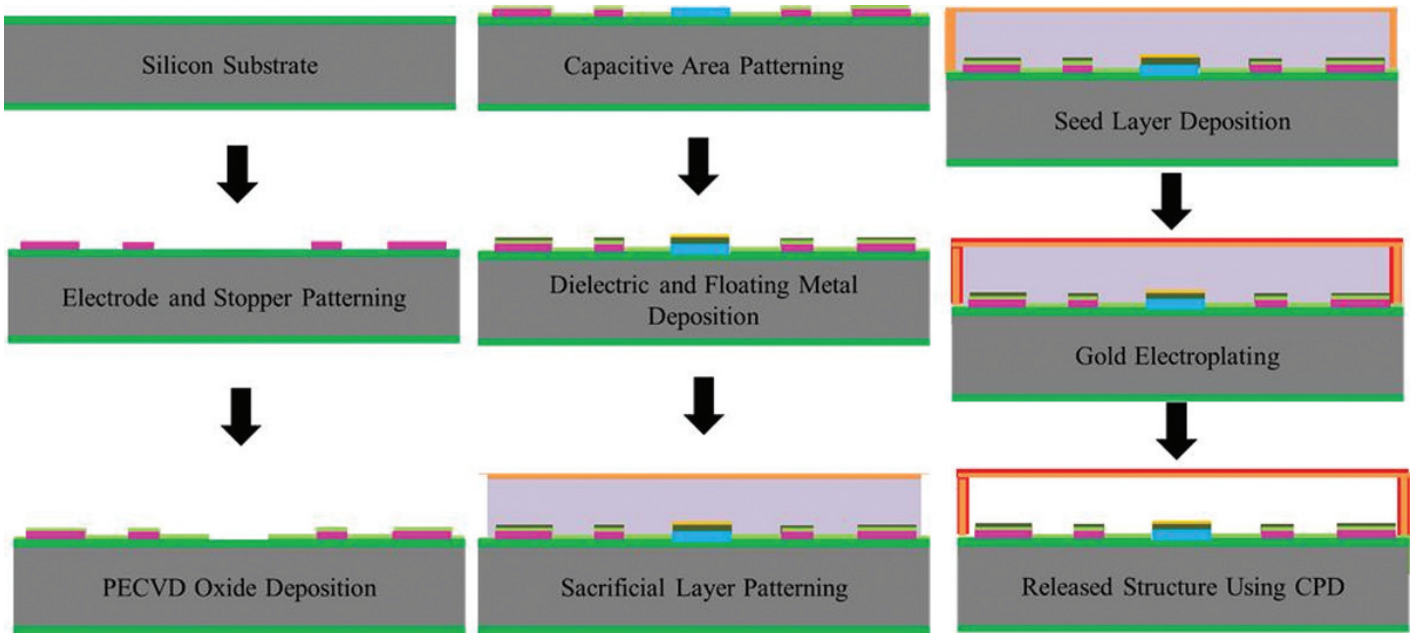

Figure 9. Proposed process flow of RF MEMS DMTL analog phase shifter.

5. PROPOSED FABRICATION PROCESS FLOW

The fabrication process of DMTL phase shifter is similar to symmetric toggle switch[4-5], begins with 250 µm - 300 µm thick high resistivity (>5 kΩ-cm), p-type <100> single side polished silicon substrate. The relative permittivity of substrate is 11.9 and proposed process flow is shown in Fig. 9. Silicon wafer is preferred for its process compatibility with semiconductor fabrication techniques. Initially, 1 µm thick thermal oxide (to reduce cpw/electrical losses and provides better Q at higher frequencies) is followed by patterning of electrode and stopper of poly-*Si* thin film (deposited using low pressure chemical vapour deposition (LPCVD) technique and doped with n-type dopants). Plasma enhanced chemical vapor deposition (PECVD) oxide, which acts as a passivation layer, is deposited to pattern contact holes. After this, underpass area (*Ti/TiN/Al/Ti/TiN*) of transmission line is patterned. Further 0.1 µm dielectric (SiO_2) is deposited using PECVD. Sacrificial layer (3 µm) is patterned for metallic structures such as fixed-fixed beam, cantilevers and other structures. The sacrificial layer is then covered with seed layer (*Cr/Au* ≈10/30 nm). The subsequent lithography defines mold of (+) ve photo resist for electroplating. CPW and bridge, both are incorporated in same mask to reduce mask levels. Finally mold is removed in acetone, *Au/Cr* seed layer is etched out in selective *Au* and *Cr* etchants. Later sacrificial layer of hard photoresist is removed in mild piranha, further released in critical point drying (CPD).

6. CONCLUSION

The reliability of an analog MEMS phase shifter is improved by incorporating stopper in the mechanical design of MEMS bridge. The deflection and capacitance ratio is increased by 1.54 and 1.68 times, respectively, compared to the design without stopper. The maximum operating voltage is 16 V. The phase shifter is designed with insertion and return loss -1.75 dB and-20.49 dB, respectively with 6 MEMS bridges at 17 GHz. The simulation results are in close match with analytical modelling.

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Ms Prachi Jhanwar received BSc and MSc in electronics and communications from Banasthali University, India, in 2009 and 2011, respectively. Currently, she is pursuing her doctoral research with the Sensor and Nanotechnology Group in CSIR-CEERI and engaged in research and development of MEMS. Her major research activity includes design and development of RF MEMS capacitive, ohmic contact switches, high k dielectrics, and high power handling of RF MEMS.

Dr Seema Verma obtained her Master and PhD degree in Electronics from Banasthali University, in 1999 and 2003. She is currently working as Associate Professor of Electronics and Head, Department of Aviation Sciences at Banasthali University. She is Fellow of IETE, Life Member of Indian Science Congress, Life member of International Association of Engineers, (IAENG). She has many projects from UGC (under R7D Major research project Scheme, UGC Innovative Course Scheme) & AICTE to her credit. She is currently into the editorial board of many international journals in the field Wireless Communication and Coding. Her research areas are coding theory, TURBO codes, wireless sensor networks, Aircraft Ad-hoc networks, network security and VLSI design.

Mr Kamaljit Rangra received his ME from Birla Institute of Technology & Science, Pilani, and his PhD from the University of Trento, Povo, Italy. He has been involved in analytical instrumentation, electron beam lithography, semiconductor process simulations, and vacuum microelectronics. His current research interests include RF MEMS for telecommunication applications, and related MEMS technologies. He is a fellow of IETE and secretary of the Semiconductor Society of India, Pilani Chapter.