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Status of Uncooled Infrared Detector Technology at ULIS, France

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ABSTRACT

The high level of accumulated expertise by ULIS and CEA/LETI on uncooled microbolometers made from amorphous silicon enables ULIS to develop uncooled infrared focal plane array (IRFPA) with 17 µm pixel-pitch to enable the development of small power, small weight and power and high performance IR systems. Key characteristics of amorphous silicon based uncooled IR detector is described to highlight the advantage of this technology for system operation. A full range of products from 160 x 120 to 1024 x 768 has been developed and we will focus the paper on the ¼ VGA with 17 µm pixel pitch. Readout integrated circuit (ROIC) architecture is described highlighting innovations that are widely on-chip implemented to enable an easier operation by the user. The detector configuration (integration time, windowing, gain, scanning direction), is driven by a standard I²C link. Like most of the visible arrays, the detector adopts the HSYNC/VSYNC free-run mode of operation driven with only one master clock (MC) supplied to the ROIC which feeds back pixel, line and frame synchronisation. On-chip PROM memory for customer operational condition storage is available for detector characteristics. Low power consumption has been taken into account and less than 60 mW is possible in analogue mode at 60 Hz. A wide electrical dynamic range (2.4V) is maintained despite the use of advanced CMOS node. The specific appeal of this unit lies in the high uniformity and easy operation it provides. The reduction of the pixel-pitch turns this TEC-less ¼ VGA array into a product well adapted for high resolution and compact systems. Noise equivalent temperature difference (NETD) of 35 mK and thermal time constant of 10 ms have been measured leading to 350 mK.ms figure of merit. We insist on NETD trade-off with wide thermal dynamic range, as well as the high characteristics uniformity and pixel operability, achieved thanks to the mastering of the amorphous silicon technology coupled with the ROIC design. This technology node associated with advanced packaging technique, paves the way to compact low power system.

Keywords: Uncooled microbolometer, long wave infrared, amorphous silicon technology, infrared focal plane array

NOMENCLATURE

CTIA	Capacitance trans-impedance amplifier
Ea	Activation energy
IRFPA	Infrared focal plane array
I²C	Inter integrated circuit link
NETD	Noise equivalent temperature difference
NUC	Non uniformity correction
OTP	One time programmable
PROM	Programmable read only memory
PLP	Pixel level package
ROIC	Read out integrated circuit
TWS	Thermal weapons sight
TEC	Thermo electric cooler
VGA	Video graphic array (640 x 480 pixels)
WLP	Wafer level package
XGA	Extended graphic array(1024 x 768 pixels)

1. INTRODUCTION

For some years the infrared sensors market tends to follow the evolution observed in the past for visible imaging sensors. It is particularly true for cost decreasing, to address high volumes applications, while more and more performances are expected from the sensors. Indeed with smaller pixel pitch, higher resolution and easier system integration, microbolometer infrared sensors intend to address military application but also new low-cost/high-volume applications such as thermography, security/surveillance and automotive driver vision enhancement. A ¼ VGA sensor has been designed taking into account up to date 17 µm pixel-size technology and high reliability packaging technique. We will first describe the interest of amorphous silicon for microbolometer applications regarding material properties, simplified technological process and simplified sensor operation. The ¼ VGA sensor will be described in terms of ROIC architecture, packaging and performances.

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2. AMORPHOUS SILICON BASED UNCOOLED INFRARED FOCAL PLANE ARRAY

Amorphous silicon presents attractive properties for micro bolometer applications. The amorphous silicon bolometer resistance R variation versus temperature is described by Arrhenius law, in Eqn. (1), in which activation energy E_a depends on the sensitive material.

$$R=R_0.exp(E_a/kT) \quad (1)$$

As amorphous silicon is not an alloy, every pixel has the same activation energy (standard deviation on mean value < 0.04%) leading to a high spatial uniformity of pixels temperature behaviour. Moreover, amorphous silicon activation

energy E_a remains essentially constant throughout a large range of operational temperature[1]. The microbolometer resistance distribution stems essentially from resistance geometry distribution, while remaining stable regarding focal plane temperature variation. As a consequence, microbolometers' pixel resistances follow a simple and spatially uniform Arrhenius law and hence are fully predictable, leading to easier TEC-less operation with only one gain table for non uniformity correction (NUC) to cover a broad IRFPA temperature range. It's also being very predictable to simplify the algorithms required for thermography and shutter-less operation. Moreover, it leads to the use of simplified system calibration process saving manufacturing cost for high volume system production. Thanks to its physical properties, amorphous silicon is easy to be monolithically integrated onto silicon substrates at temperature compatible with CMOS integrated circuit. Several key technology improvements are required to successfully scale the pixel from 25 µm down to 17 µm or less. One of which is the call for 0.5 µm lithography processing. Advanced lithography in connection with thinner films embodiment clearly gives an edge to maintain, and even to improve, thermal insulation when scaling the pixel to 17 µm while keeping a simple one-level micro bridge structure (as shown in Fig. 1) which leads to high operability and high manufacturing yield. This approach allows to continue to scale down a single level micro bolometer architecture, taking advantage of a very simple process flow and cost saving. Amorphous silicon offers the opportunity to design a rather undemanding micro bridge structure without any extra features than the bare minimum required for the bolometer functionality. This leads to a reduced number of technological operations and results in a little number of photolithographic layers. The mere arrangement of the micro bridge leads therefore to a fast sensor, featuring pixel time constants largely below the common figures known elsewhere. NETD of 56 mK (f/1, 300 K, 30 Hz) with a thermal time constant lower than 7 ms have been already achieved on 12 µm pixel size at R&D level[2]. To our knowledge, it is the best result ever measured on 12 µm pixel size at this date.

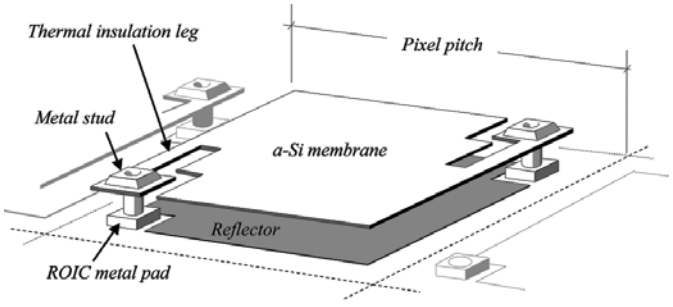

Figure 1. Schematic of the amorphous silicon microbolometer pixel.

3. PACKAGING TECHNIQUES

3.1 Metallic package

Metallic package has been developed for 17 µm XGA detector in order to offer for this high-class detector a possibility to use the package flange as a mechanical reference on which sub part could be integrated (lenses barrel, and/or shutter mechanism).

3.2 Ceramic Package

To enable compact and lightweight system for smaller format detectors, ceramic packages have been developed. High performance ¼ VGA detector is therefore packaged in a compact (24.13 x 24.13 x 3.57 mm^3), low weight (< 6 g) and TEC-less ceramic package. Regarding the environmental tests, this package design is compliant with the automotive AEC- Q - 100 / Grade 3 standard. Particularly, the detector can withstand high level thermal shocks (-50°C/+125°C - 500 cycles), high temperature storage life test (HTSL 125 °C – 1000 h) as well as thermal weapon sight shock and vibration tests.

Moreover, high combined temperature/humidity tests (95 °C – 95 % RH) have been successfully achieved. Several aging and storage tests in progress on similar packages (> 700 days @ 170 °C) are demonstrating a very good package vacuum behaviour as computed reliability reaches > 93 % after 15 yr.

3.3 Silicon Packages

3.3.1 Wafer Level Package

Taking advantage of the silicon technology used for amorphous silicon thermometer integration on CMOS wafer and of the MEMs technology expertise, a new wafer level packaging (WLP) technique is under development to address high volume applications. Figure 2 shows first WLP prototypes integrated either onto PCB (a) or in a standard JEDEC package (b). These products are developed under AEC_Q100 Grade 3 qualification program.

Figure 2. WLP ¼ VGA IRFPA onto PCB or in QFP (not at same scale).

3.3.2 Pixel Level Package

The cost objectives for small sensors (alarm sensors or abandoned sensors) however require a technological breakthrough, particularly in regard to the vacuum packaging of these components, which remains an adverse cost driver for any microbolometer technologies. In this context, CEA-LETI has proposed the PLP technology development for some years[3-5] . According to this unique technology, each bolometer pixel is sealed under vacuum directly at the wafer level, using an IR transparent thin film deposition. This technology leads to an array of hermetic micro boxes or microcapsules each containing a single microbolomètre pixel.

PLP process consists in the manufacturing of IR transparent microcapsules that cover each microbolometer (i.e. each pixel) of the focal plane array (Figure 3). Process flow chart starts with a sacrificial layer, which is deposited above microbolometers followed by a trench etched around each

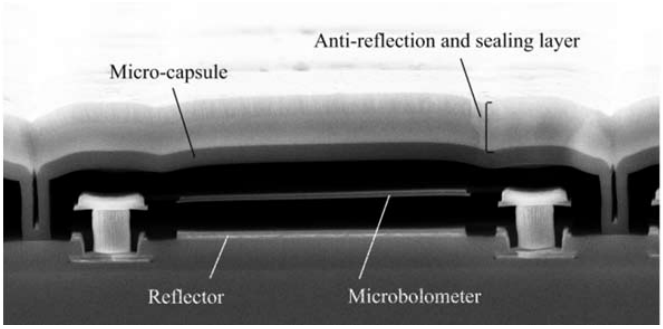

Figure 3. SEM profile view of a bolometer from a PLP test device.

pixel. An IR transparent thin film is then deposited as a liner of the structure in order to form the microcapsule structure. Exhaust holes are etched through the top of the microcapsule and the enclosed sacrificial layer is removed through these exhaust holes. Finally, the sealing and anti-reflecting layer is deposited under high vacuum to finalize the hermeticity of the microcapsule.

To be efficient, the micro cap has to be hermetically sealed under vacuum. Vacuum level in the 10^{-3} mbar range is requested for providing uncooled IRFPA nominal operation. The main point (regarding high volume objectives) is that the PLP process is thoroughly carried out directly on the IRCMOS readout circuit, in a fully collective way.

4. READOUT INTEGRATED CIRCUIT DESIGN

4.1 General Considerations

The bolometer layers are processed directly onto dedicated imaging CMOS ASIC wafers. The goal of the readout integrated circuit (ROIC) associated to the sensor is to measure the thermometer resistance value of each pixel.

The readout is operated in rolling shutter mode. Each imaging pixel is addressed through an injection TMOS and is coupled with a skimming blind bolometer. As described in Fig. 4 to remove a large part of the useless offset current going through the bolometer. To supply voltage samples of each pixel in video output signal, a low noise capacitive trans-impedance amplifier (CTIA) is used in the input stage of the readout

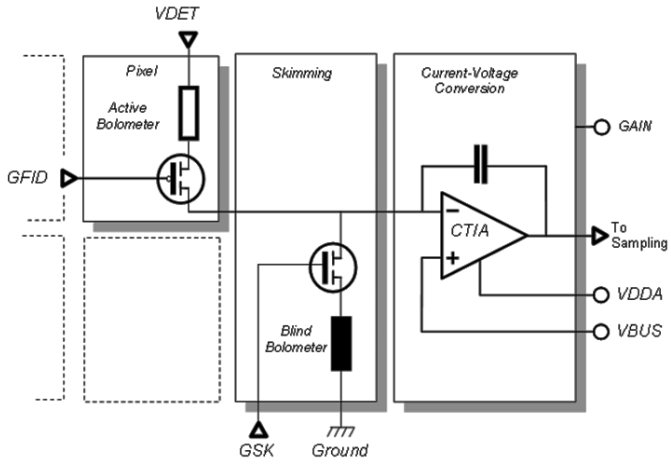

Figure 4. Pixel readout architecture.

integrated circuit (ROIC). This stage converts the current in the bolometer to a voltage value, and size the ROIC gain with the couple C_{int} and T_{int}, respectively integration capacitor and integration time. Thus the main characteristic of the bolometer sensor is the responsivity R, expressed as

$$\Re = \frac{V_{pol}}{R_0} * \frac{E_a . A . R_{th} . \Delta\phi}{k . T^2} * f(T_{\text{int}}, C_{\text{int}}) \qquad (2)$$

where E_a (activation energy), A (membrane area), R_{th} (thermal insulation of the membrane) and R_o (electrical resistance of the thermometer), are parameters that depend of the bolometer design, and particularly of the membrane area. We can observe also with this Eqn. (2) that the only electrical parameter the responsivity depends on, is the bolometer polarization V_{pol}. As activation energy E_a is identical for every pixel in an array, it means that the focal plane temperature behaviour is highly uniform and predictable leading to easier device modelling and therefore easier TEC-less and shutter-less operation.

4.2 ¼ VGA ROIC Design

Focal plane array with 384 x 288 pixels and a pixel pitch of 17 µm has been designed with 3.3 V analogue power supply and 1.5 V digital power supply. Special readout design enables to achieve halving the power consumption from 110 mW for ¼ VGA/25 µm to only 55 mW in analogue video output mode for this ¼ VGA/17 µm. A wide electrical dynamic range (2.4V) is maintained despite the use of an advanced CMOS node. The very low noise ROIC video output allows reaching of very high performances of the bolometer sensors, in particular for NETD and image quality. Many features were integrated in the ROIC to simplify the detector system integration. This is a real evolution towards the standardization of the IR detectors interfaces with digital processing systems. Therefore, a 14 bits ADC is integrated in the readout circuit and the digital data is supplied on an 8 bits multiplexed bus; in this mode the ROIC power consumption reaches less than 175 mW[6]. The detector configuration (integration time, windowing, gain, scanning direction) is driven by a standard I²C link. Like most of the visible arrays, the detector adopts the HSYNC/VSYNC free-run mode of operation driven with only one Master Clock (MC) supplied to the ROIC which feeds back pixel, line and frame synchronizations. Due to 7 MHz PSYNC pixel clock the detector can work at 60 Hz frame rate. On-chip one time programmable (OTP) memory for customer operational condition storage is also available for detector characteristics. For instance the bolometer bridge biasing can be stored during a factory configuration. OTP parameters stored during ULIS sensor manufacturing process support an easier integration in camera system while uploading specific biases from sensor memory.

5. ELECTRO-OPTICAL PERFORMANCES

The specific appeal of this new product lies in the high uniformity and easy operation it provides. It completes the 17 µm detector catalogue which is addressing a full range of products from ¼ VGA, VGA to XGA detectors. The reduction of the pixel-pitch turns this TEC-less ¼ VGA array into a product well adapted for high resolution and compact systems,

achieving at sensor level NETD value equal to 35 mK at F/1 in front of a 27 °C black body temperature, with respect of a 50 Hz frame rate compatibility and scene dynamic over 100 °C typically, such as - 20 °C to + 80 °C. Corresponding results of measurement are presented in Fig. 5(a) for responsivity map in mV/K and Fig. 5(b) for NETD histogram in mK. The thermal time constant measurements of 17 µm pixels give values under 10 ms (range from 8.8 ms to 9.3 ms has been measured on the first VGA/17 µm batches[7]) fully compatible with 30 Hz or higher frame rate operation.

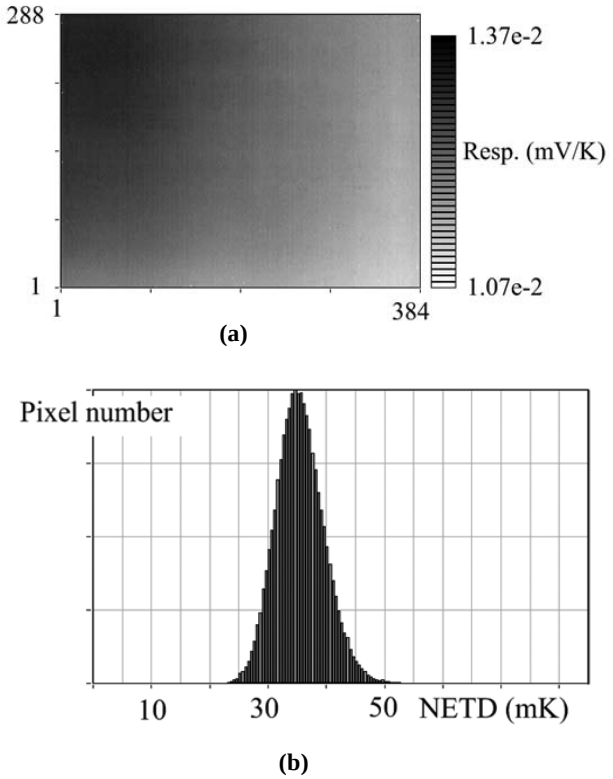

Figure 5. Electro-optical characterisation of ¼ VGA 17 µm (a) Responsivity map (mV/K) (b) NETD histogram (mK).

Regarding VGA 17 µm, the main characteristics are measured at an ambient temperature of 303 K. The overall output range dynamic is 3 V. In the standard operational mode, the responsivity mean value stands at 12.1 mV/K (operated @ 4 pF Gain), hence offering a scene dynamic higher than 150 K. The FWHM DC output voltage distribution is less than 150 mV which represents only 5 % of the output dynamic. The resulting mean NEDT value, @ 303 K of focal plane temperature, stands at 46 mK. Residual fixed pattern noise (RFPN) for this component (in TEC-less operation) reaches 295 µV that is 75 % of the RMS noise.

6. SYSTEM BENEFIT

For a given field of view, the pixel pitches reduction lead to a more compact system due to the size reduction of the FPA. Indeed, the focal length will decrease proportionally to the pixel pitch reduction, i.e by 47 % from 25 µm to 17 µm and more than a factor of 2 from 25 µm to 12 µm. The weight of the system will follow accordingly. ULIS succeed to keep the same level of FPA performance (NETD and dynamic range) while decreasing the pixel pitch, consequently the range performance for a given field of view is maintained.

Therefore, at system level, a possibility will consist of keeping the same system size (same focal length and F/ number) to improve the system detection range as mentioned on the Fig. 6, taking profit from pixel size reduction. Another way to read the curve below is, for a given targeted range, to know the necessary focal length. The range achievement used here is based on Nyquist approach.

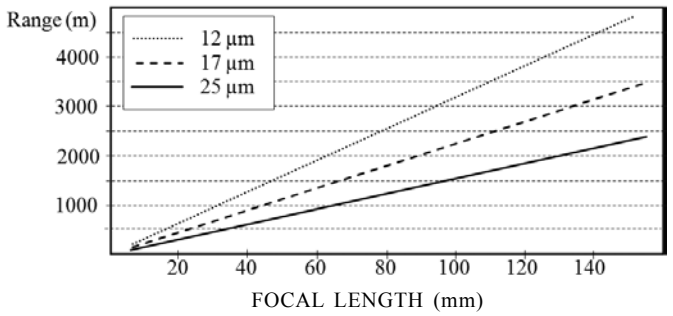

Figure 6. Recognition range performance for ¼ VGA with different pixel pitches (NATO target 2.3 m x 2.3 m).

7. CONCLUSION

Latest state-of-the-art developments and technologies roadmap have been presented, regarding detection material, pixel pitch reduction, and vacuum package or readout integrated circuit functionalities improvements. After having developed the first amorphous silicon XGA arrays with 17 µm pixel-pitch with high uniform performance, we have shown that it can be translated in a high performance (45 mK) VGA format sensor well adapted to more compact system with a low thermal time constant (9 ms) enabling 60 Hz frame rate operation. The new product ¼ VGA 384 x 288 focal plane array 17 µm pixel pitch take benefits of those latest technology improvements, achieving NETD performances of 35 mK at F/1, 50 Hz frame rate, compliant with the requirement of IR imaging systems for thermal weapon sights (TWS), ground vehicle situation awareness, long-range surveillance, handheld goggles and UAV.

Beside these state-of-the-art performances, amorphous silicon detection material associated to improved ROIC functionalities enable to reduce manufacturing time and calibration process currently required by all LWIR thermal system. Packaging technology such as wafer level package will also open new application opportunities in the automotive field, based on an additional cost reduction step in the offer of LWIR sensors. ULIS is as far as we know, the only one company able to provide sensor from 80 x 80 to 1024 x 768 pixels made from the same technology.

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CONTRIBUTORS

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Mr Patrick Robert received an engineering degree in microelectronics from ENSERG at Grenoble, France, in 1988. He worked with Thomson-EFCIS in the analog design of telecommunication circuits and also at Dolphin Integration for ADC design. He has been involved with infrared readout circuits design first at SOFRADIR and now at ULIS. He is now in-charge of the ROIC designers team of ULIS and recognized as Expert at ULIS.

Mr Alain Durand graduated from the Engineering School of Physics of Grenoble in 1997. He joined the French Atomic Energy Commission where he worked on nuclear radiation detector systems and also at LETI on MCT based and a:Si bolometer infrared detectors developments. Presently he is working at ULIS, where he is now responsible for the test, characterization and simulation of product under development.

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Mr Emmanuel Bercier has received Engineer diploma in Optronics at POLYTECH at Faculty of Science of Orsay (Paris XI) and the College of Optics (ESO) in 1998. He joins the SOFRADIR Company as scientist, where he occupied engineer R&D's position in characterization of components. Later he joined ULIS to occupy the management of Professional Products Line dedicated to the large volumes, where he takes the responsibility of the offer and its development specifically adapted to the sectors of the thermal imaging, safety/security, surveillance and transportation.

Mr Arnaud Crastes received his engineering diploma from Institut d'Optique Graduate School and MSc (Electro-optical system design) with honors in the same year in 1995. He worked earlier at Sagem Defense and Security (Paris) as electro-optical R&D manager and THALES where he is involved in space product development as program manager, follow by an experience in business development in MOEMS and imager based on extended InGaAs technology. Presently working as to customer support manager at ULIS. He is technical expert for ULIS and for National Research Agency as well. He has several patents and more than 35 publications in different conferences.