Automatic Target Handing Over System

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ABSTRACT

The image seen by the airborne seeker and the image (of the same scene) seen by the operator through the high resolution sensor (thermal sight) are different in spatial resolution. In order to establish the correlation between these two images, the thermal sight image needs to be resampled and made similar to the seeker image by applying a preprocessing technique. The preprocessing is carried out by a handing over system (HOS) that resamples the thermal sight image making it compatible with seeker image and hands over the resampled image to the seeker.

This paper discusses the implementation of the suitable handing over algorithm. (Boland, J.S. *et al.* Automatic target hand using correlation techniques. Technical report, Auburn University, Alabama, 31 January, 1977, pp. 57-63). Emphasis is laid on developing suitable hardware and software and tests to match the two images obtained by two different sensors of the same scene. The hardware and software-have been evaluated with different sets of images. The H/W is designed around iAPX 86 family of processor and software is developed in PL/M. Hardware also includes the recording facility on a standard VCR, to record the performance of handing over electronics (HOE) during testing/flight trials. Evaluation of the system by realistically simulating the field scenario in the laboratory has shown that the HOS is functioning satisfactorily.

INTRODUCTION

Third generation systems of airborne seekers envisage 'fire and forget' capability, demanding autonomous mode of operation. In systems employing lock-on-before-launch concept, the target is recognised using a high resolution sensor and is handed over to the seeker, for further tracking.

Acquisition and recognition of the target depends on field of view (FOV), target size, optics size, sensor resolution, etc. The number of pixels that the target occupies in the image plane depends on target size, maximum range, FOV of the seeker and optics size. Because of limitations on the size of the system for airborne application, the target occupies only a few pixels in the image plane. Schemes like zooming in optics cannot be used for the same reason. As per Johnson's criteria[1], at least 6 to 7 lines through the target are required for recognition. Hence target recognition is not possible through the seeker. Thus there is a requirement of a high resolution sensor such as thermal sight (TS) and handing over system (HOS). Ground-based TS can have bigger optics, narrow field of view, high resolution sensor, etc.

TS and seeker are comounted on the launcher platform (LP). The target acquired by TS is supposed to appear at the centre of the FOV of the seeker. After recognizing the target through TS, the scene around the centre of the FOV can be resampled to make it compatible to seeker image in spatial resolution. The resampled image can be used as a reference image for locating its position in seeker FOV by image correlation techniques. Once the reference area is located in the seeker image, the seeker is automatically trained to bring the located area to the centre of its field of view. Image correlation technique continues updating the reference information at a sufficiently fast rate, typically

tens of milliseconds and thus the seeker keeps tracking the target area. As such the target is located in a given area.

The sensor in the airborne seeker (ABS) and the TS sensor from which the reference is generated have different spatial resolutions. In order to match the two images by correlation, the two images should have the same spatial resolution. To make the two images have the same resolution, a suitable preprocessing technique[2,3] is applied on the high resolution TS image.

This algorithm has been described in a report by Boland[2]. This report, the effect of sensor parameters like number of lines, aspect ratio, field of view and sampling rate on the spatial resolution are discussed in this paper. Each pixel in the low resolution (LR) image falls on a number of pixels in the high resolution image. This preprocessing technique or handing over algorithm averages the gray values of the corresponding each pixel of the LR image. This high resolution (HR) area for each LR pixel contains a number of complete pixels and also fraction of pixels.

The performance of the handing over algorithm has been studied using COMTAL — Micro Vax Image processing system and it is found to be satisfactory[4]. This paper discusses the implementation of handing over algorithm. It also discusses the computational complexity, criticality of the execution time and development of hardware for recording the performance of the HOS on a VCR.

1.1 Handing Over Algorithm and Analysis

Let us consider two images of the same scene, taken by two different sensors: one with HR and the other with LR. In the present case TS has high resolution image and ABS has low resolution image. The two images of the same scene may differ due to differences in,

1. Field of view
2. Sensor resolution (lines per frame)
3. Sensor geometry (aspect ratio)
4. Frame rate
5. Sampling rate

Let W_h be the horizontal scale factor and W_v be the vertical scale factor between the HR and LR images.

1.1.1 Field of View

If the ratio of the LR to HR fields of view is F and all other parameters are identical, then the contribution of the different FOV's to W_h is F and to W_v is F.

1.1.2 Lines per Frame

If the number of video lines per frame in the HR image is twice the number of the lines in the LR image and all other factors are the same including the FOV, then the vertical resolution of the HR image is twice that of LR image and the horizontal resolution is half, as the sampling rate is constant. If the ratio of the number of lines in the LR to the HR images is L and all other parameters are identical, then the contribution of the different number of lines to W_h is L and to W_v is $1/L$.

1.1.3 Aspect Ratio

If the aspect ratios of the LR and HR images are p_1 and p_2 respectively and their ratio $A = P_1/P_2$, then the contribution of the different aspect ratios to W_h is A and to W_v is 1.

1.1.4 Frame Rate

If the ratio of the frame rates of the LR to HR system is R and all other parameters are identical, then the contribution of the different frame rates to W_h is R and to W_v is 1.

1.1.5 Sampling Rate

If the ratio of the sampling rates of HR to LR images is S and all other parameters are identical, then the contribution of the different sampling rates to W_h is S and to W_v is 1.

Therefore, if all the above five cases are present, then the effective horizontal spatial resolution factor

$$W_h = F \times L \times A \times R \times S \qquad (1)$$

and

Effective vertical spatial resolution factor

$$W_v = F/L \qquad (2)$$

For the TS and the seeker considered in this application, the effect of the difference in all the above mentioned sensor parameters results in a vertical scale factor W_v of 14.634 and horizontal scale factor W_h of 14.20.

If W_h and W_v are integers greater than one, then the preprocessing will be averaging the first W_h columns of the first W_v rows of the HR to get LR (1,1) pixel, and the next W_h columns of the first W_v rows are averaged to obtain in the LR (1,2) pixel of the reference array as shown in Fig. 1(a) and the procedure repeats for the other pixels. But, if W_h and/or W_v are real numbers then the problem becomes complex as shown in Fig. 1(b). It can be seen from Fig. 1(b) that LR (1,1) contains 9 full pixels and fractions of neighbouring 6 pixels, whereas LR (2,2) contains only 4 full pixels and
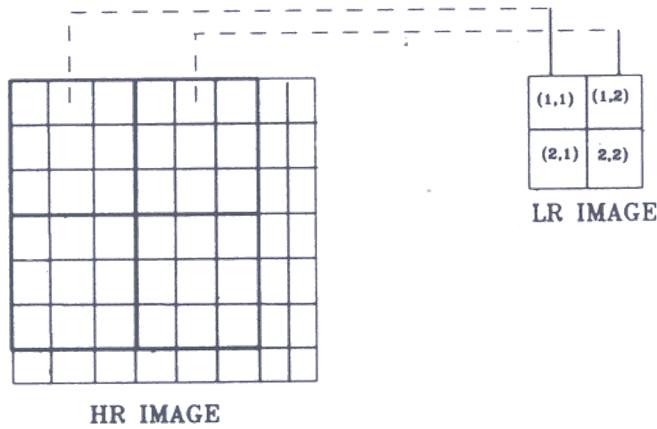

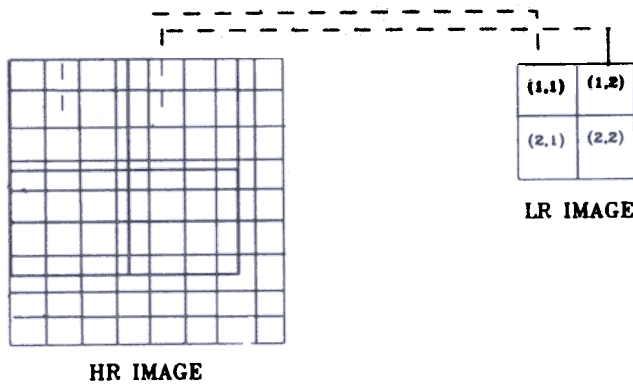Figure 1(a). Preprocessing when $W_h/W_v = 3$ (integer).

Figure 1(b). Preprocessing with $W_h/W_v = 3.25$ (real).

fractions of neighbouring 12 pixels. It can be seen that when 3.25 × 3.25 window is overlayed anywhere on the HR image grid, minimum 4 full pixels would be available in the window.

In a typical window LR (2,2) in Fig. 1(b), there are a few full pixels at the centre and fractions of pixels at the boundary. This window can be represented as shown
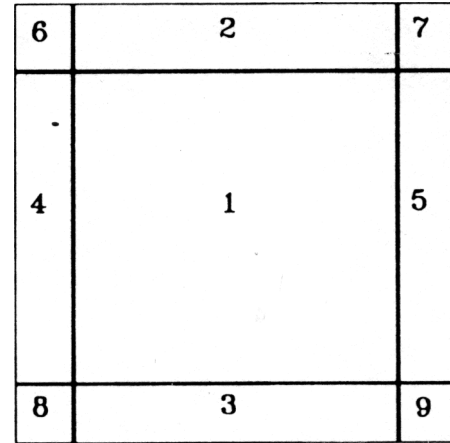

Figure 2. Typical window.

in Fig. 2. The contribution of each part in Fig. 2 is given in the following

corresponds to full pixels and its contribution is

$$A = \frac{-}{W_v\,W_h} \left\{ \sum_{m=u+1}^{x} \sum_{n=v+1}^{y} Hr\,(m,n) \right\} \qquad (3)$$

2 - corresponds to the fraction of pixels which are cut at the top and its contribution is

$$B = \frac{1}{W_v\,W_h} \left\{ \sum_{n=v+1}^{y} Hr\,(u,n)\,[u-(i-1)\,W_v] \right\} \qquad (4)$$

3 - corresponds to similar fraction of pixels which are cut at the bottom and its contribution is

$$C = \frac{1}{W_v\,W_h} \left\{ \sum_{n=v+1}^{y} Hr\,(x+1,n)\,(I\,W_v - x) \right\} \qquad (5)$$

4 - corresponds to fraction of pixels which are cut at the left and its contribution is

$$D = \frac{1}{W_v\,W_h} \left\{ \sum_{m=u+1}^{x} Hr\,(m,v)\,[v-W_h(i-1)] \right\} \qquad (6)$$

5 - corresponds to fraction of pixels which are cut at the right and its contribution is

$$E = \frac{1}{W_v\,W_h} \left\{ \sum_{m=u+1}^{x} Hr\,(m,y+1)\,(W_h j-y) \right\} \qquad (7)$$

6 - Contribution of the left top fraction of pixel and the value is given by

$$F = \frac{-}{W_v\,W_h}\,Hr\,(u,v)\,[u-W_v(i-1)]\,[v-W_i$$

$$(j-1)] \} \qquad (8)$$

7 - Contribution of the right top fraction of pixel and the value is given by

$$G = \frac{\cdot}{W_v \, W_h} \left\{ \; Hr \, (u,y+1) \, [u - W_v(i+1)] \right.$$

$$\left. W_h \, j - y] \; \right\} \tag{9}$$

8 - Contribution of the left bottom fraction of pixel and the value is given by

$$H = \frac{-}{W_v \, W_h} \left\{ \; Hr \, (x+1,v) \, [W_v \, j - x] \, [v - W_h(j-1)] \; \right\} \tag{10}$$

9 - Contribution of the right bottom fraction of pixel and the value is given by

$$I = \frac{\cdot}{W_v \, W_h} \left\{ \; Hr \, (x+1,y+1) \, [W_v \, i - x] \, [W_h \, j - y] \; \right\} \tag{11}$$

Therefore the total average of the complete window is given by

$$Lr \, (i, j) = A + B + C + D + E + F + G + H + I \tag{12}$$

By substituting Eqns (3)-(11) Eqn (12) and simplifying, we get

$$Lr(i,j) = \frac{1}{W_v \, W_h} \left\{ \sum_{m=u+1}^{x} \sum_{n=v+1}^{y} Hr(m,n) + \sum_{n=v+1}^{y} \right\}$$

$$[(u - (i-1)W_v) \, Hr(u,n) + (\, iW_v - x)Hr(x+1,n)] +$$

$$\sum_{m=u+1}^{y} [(v-(j-1)W_h) \, Hr(m,v) + (jW_h - y) \, Hr(m,y+1)]$$

$$+ [\{u - (i-1)W_v\} \, \{v - (j-1) \, W_h\} \, Hr(u,v) +$$

$$(jW_h - y) \, Hr(u,y+1)] + (iW_v - x) \, \{v - (j-1) \, W_h\}$$

$$Hr(x+1,v) + (jW_h - y) \, Hr(x+1,y+1) \tag{13}$$

where,

$$u = \text{Trunc} \, [(i-1) \, W_v + 1]$$

$$v = \text{Trunc} \, [(j-1) \, W_h + 1]$$

$$x = \text{Trunc} \, [iW_v]$$

$$y = \text{Trunc} \, [jW_h]$$

Equation (13) is the final tranformation equation, which converts the $Hr(i,j)$ image into $Lr(i,j)$ image with W_h and W_v scale factors. As we can see, it is computationally complex. This algorithm has to be partitioned into integer manipulation and real number

manipulation. Otherwise, all will be treated as real number computation by the processor and increases the execution time.

2. SYSTEM SPECIFICATIONS

The vehicle borne computer (VBC) is a subsystem in LP, which will interact with all the subsystems present in the vehicle and passes the information to airborne system. The digital scan converter (DSC) converts the non-standard TS signals to standard TV format (composite signal). It also does some preprocessing before sending the signal and generates a few graphics to aid the operator during alignment.

VBC gives a start command to handing over electronics (HOE) and it sends the same to DSC. Then DSC gives the coordinates of the target to HOE. HOE resamples the image around those coordinates and generates LR image which is having same spatial resolution same as that of the ABS. HOE transmits the LR image data to ABS through VBC as show in Fig. 3(a).
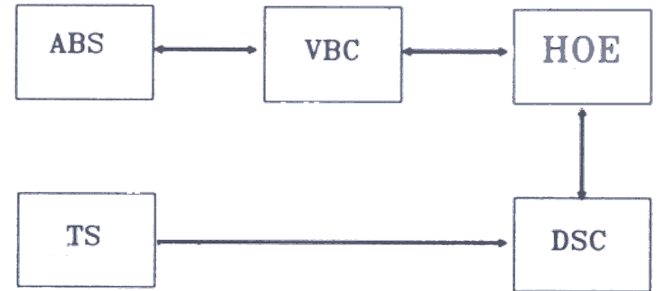

Figure 3(a). Block diagram of data flow.

The detailed interconnection diagram between the HOE, VBC and DSC is shown in Fig. 3(b). HOE has separate RS 232 serial communication links with DSC and VBC. HOE has one input signal for start command and one output line to signal the VBC after completing the LR image data generation.

2.1 Design Considerations

The different considerations in the HOE design are as follows.

1. TS image comes to HOE in the form of composite signal through DSC as shown in Fig. 3(b). In the example considered in this paper, the DSC samples the
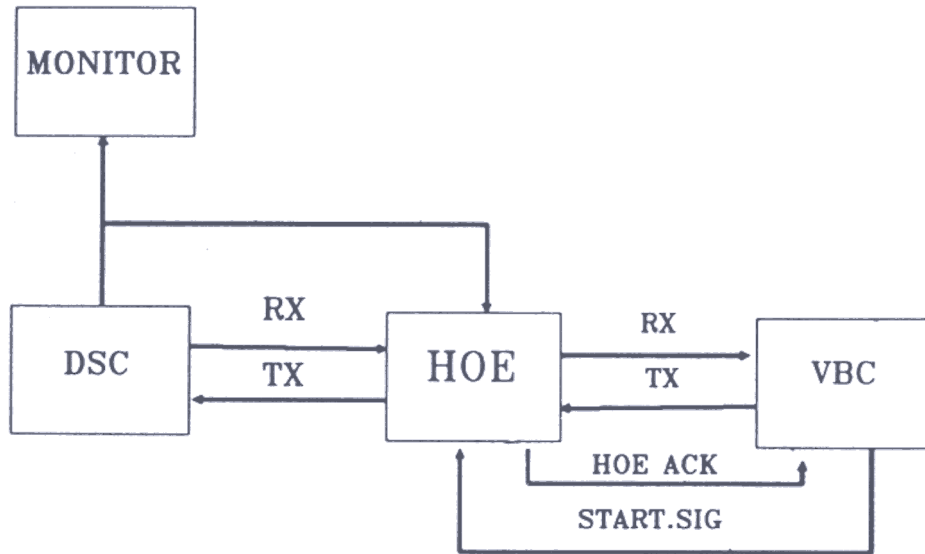
Figure 3(b). HOE interconnection diagram.

TS image at 16 MHz. In order to have same TS/DSC resolution at HOE, the hardware needs to work at 16 MHz.

2. The DSC while converting the TS image of size signal into standard TV format, it repeats the each pixel four times and generates an image of size 710 × 400. Therefore, in HOE hardware instead of considering 710 image pixels in a line, alternate pixels can be considered, i.e. HOE can sample the input video signal at 8 MHz. This reduces the hardware complexity and execution time.

3. For correct image capturing as per the target designate, HOE and DSC should have synchronization with respect to the clock.

4. For distinguishing odd and even frames in the interlaced composite video, a TTL signal has to be generated from the composite video signal.

5. In the system configuration (TS and ABS) the horizontal spatial resolution factor and vertical spatial resolution factor are 14.20 and 14.634 respectively.Generation of a (16 × 16) low resolution image from a high resolution image with these scaling factors, requires 4096 real number multiplications, 139756 integer additions and 12544 real number additions. Thus the handing over algorithm of Eqn (13) is highly complex computationally. From the system point of view, the typical execution time should be a few hundreds of milliseconds. In addition to this, the communication protocols between DSC–HOE and

VBC–HOE would take a few hundred milliseconds more. The HOS design with the above considerations is described in the next Section.

3. HARDWARE DESIGN

3.1 Design Options

The following two possible hardware design options are considered:

(a) The TS-DSC image can be sampled at 16 MHz and stored in a memory in real time. When start signal comes from the VBC, the area around the target of interest can be resampled and sent to the seeker. In this configuration most of the synchronization problems can be eliminated. To reduce the computational complexity, processor and coprocessor combination can be considered[5,6]. After receiving the start command, CPU disables the buffers provided at the memory and reads the data for applying the algorithm. In this configuration, as explained above, sampling has to be done using fast A/D and the remaining logic has to be fast enough to store the image data continuously. To store 710 × 400 image size, we need 284 Kbytes of very fast SRAMs.

(b) After start command comes from the VBC, a gate is generated in the HR image depending on the scale factors and the LR image size. Only the gated image can be stored in memory thereby reducing

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the memory requirement. For this, proper synchronization is required between DSC and HOE. After capturing the image of interest, resampling can be carried out by the processor and coprocessor combination.

Among the two options, the second option is chosen as it requires less storage. Once the TS-DSC image data are availiable in memory, the execution time mainly depends on the processor/coprocessor speed and software. When this project is taken up, the PL/M compiler is the only efficient compiler which gives the optimum machine code. Substantially fewer PL/M statements are necessary for a given application than if it were programmed in assembly language, thereby reducing the software development time.

3.2 Hardware Description

The block diagram of HOE hardware is shown in Fig. 4. The composite video signal coming from DSC consists of horizontal sync (HS), vertical sync (VS) and the video. The sync (HS,VS) signals are separated using the sync separator. The video is sampled at 16 MHz

clock and 8-bit digital data is obtained through a fast A/D converter. In the text, pixel address and line address are referred to as X and Y addresses respectively. For getting X and Y addresses, Fast (F) series digital counters are used and they are initialized by clock, HS and VS signals. The components like counters and buffers used between A/D converter and the memory are of F series to match the input data rate. In a composite video signal, the first equalizing pulse starts at the start of vertical blanking for odd field, and for even field these equalizing pulses come after half a line delay. This half line difference in time between odd and even field continues through all the following pulses, so that vertical sync pulses for successive fields have the time required for odd line interlacing[7].

To generate the TTL signal corresponding to the odd and even field the following procedure is followed. The vertical and horizontal sync signals are given to a processor through input ports. CPU can check the status of the vertical sync signal and when it goes from LOW to HIGH, it starts a counter. It disables the counter/timer as soon as horizontal sync signal goes
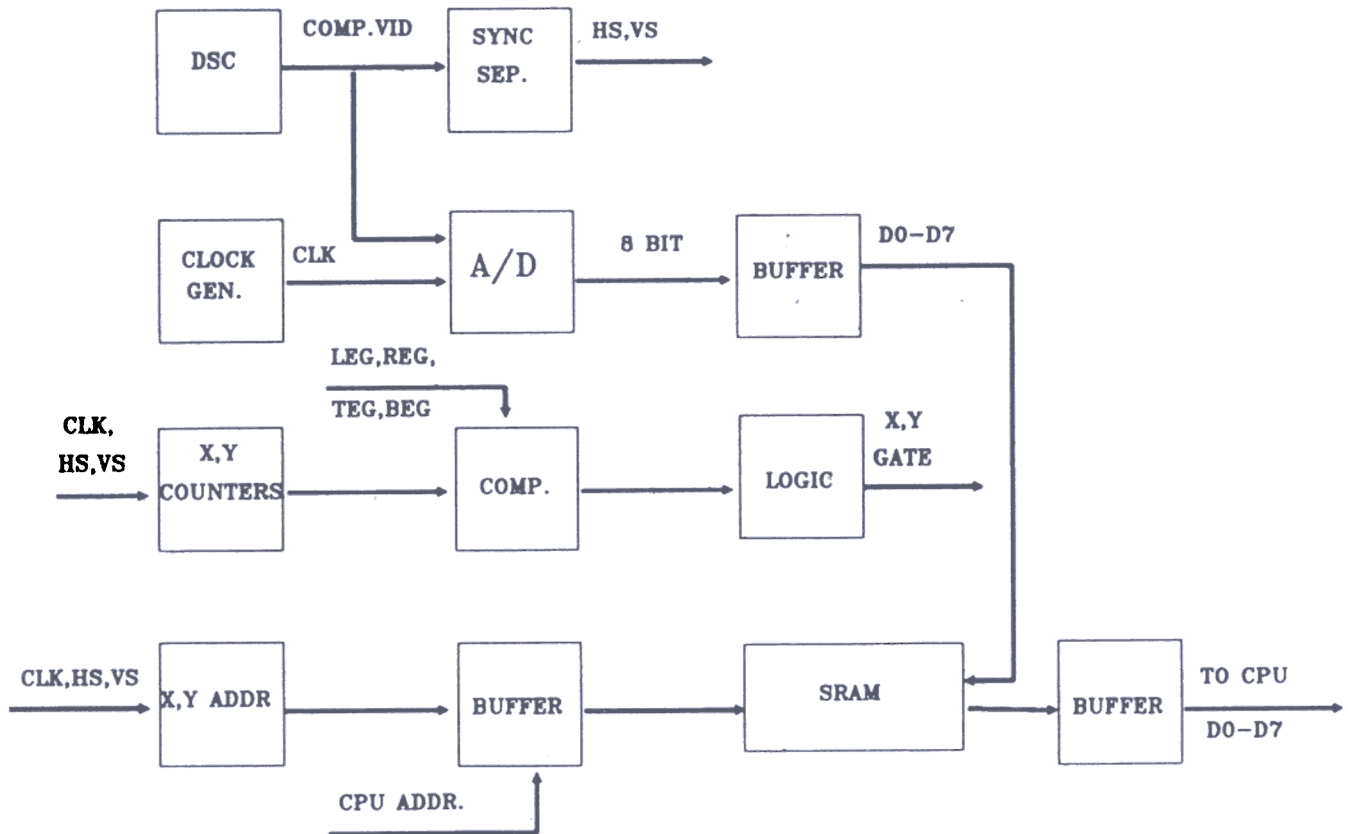

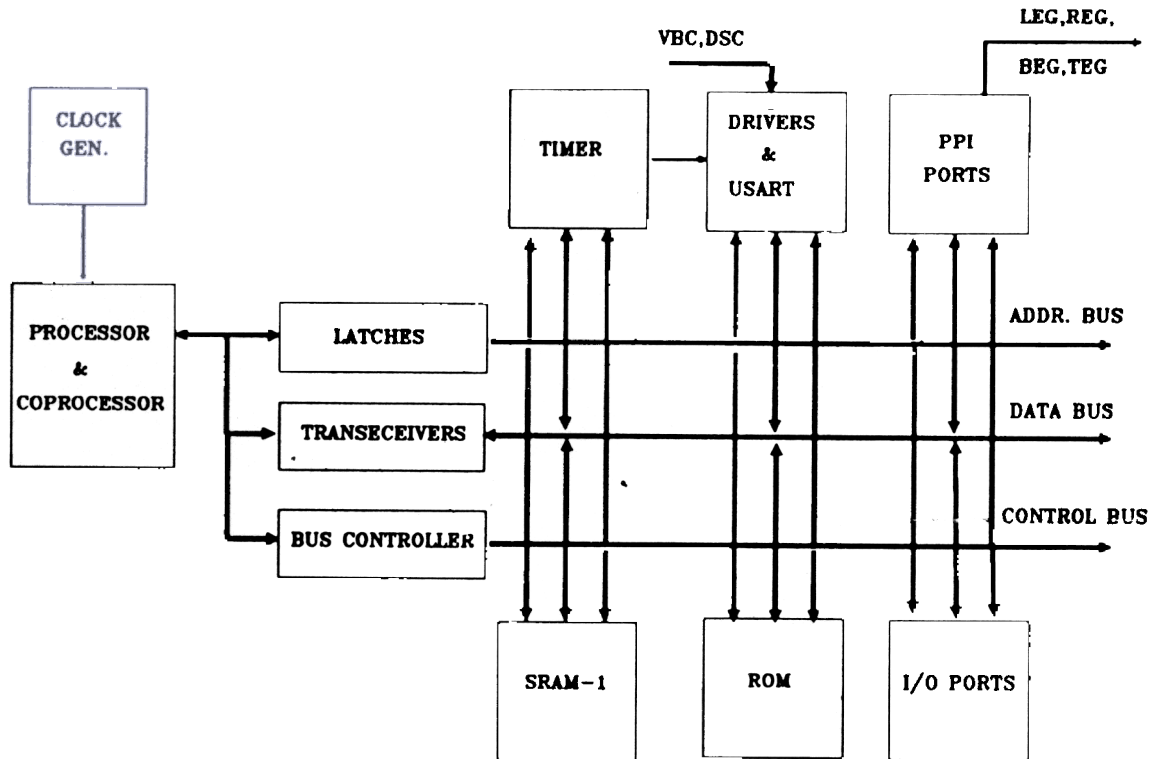Figure 4(a). HOE hardware block diagram.

Figure 4(b). Hardware block diagram (up part).

from HIGH to LOW. If the counter time is > 32 μs, then CPU clears the counter which is clocked by VS. The output of the counter gives the required TTL signal. In this way odd and even fields are distinguished.

The processor receives the target coordinates from DSC and generates the left edge (LEG), right edge (REG), top edge (TEG) and bottom edge (BEG) of a gate around the target and outputs through its ports in synchronization with the frame pulse. The maximum size of the gate can be 256 x 256 which is the limitation of the memory. Each edge is of 16-bit length and thus the hardware contains 64 I/O lines for outputting the target gate edges. The X address and LEG and REG are compared to get X gate. Similarly, Y address and BEG and TEG are compared to get Y gate. Using X gate and Y gate, XY gate signal is generated. This signal is used for enabling the SRAMs.

Separate sets of counters are used for X address and Y address for addressing the memory. The X counters are cleared with gated HS and X gate signal. Similarly, the Y counters are cleared with gated VS and Y gate. These address lines will go to SRAM-1 for addressing different locations. When the processor wants to read

the SRAM-1 it sends the address to the SRAM-1 and reads the data. To avoid the conflict between these two address and data buses, all the address, data lines and control lines are connected through multiplexers/buffers as shown in Fig. 4(a).

The present system is designed and developed around iAPX 86 family of processors and Numeric Data Processor (NDP) 8087 to meet the computational requirement[5,6]. The detailed block schematic is shown in Fig. 4(a). Control bus signals are generated by decoding the status lines using bus controller. To transmit/receive data from DSC and VBC two separate USARTs are used. The outputs are taken through RS 232 line drivers/receivers. Timer is provided for generating the required clock to USARTs. Parallel I/O lines are provided for outputting the target gate edges for generating the X and Y gates. The hardware also contains fast SRAMs of 45 ns. It can store 256 × 256 size of image of 8-bit resolution. For storing firmware, 2 × 8 K × 8 ROM space is provided. Separate I/O ports are also provided for the handshake signals.

The hardware came in three PCBs of standard double euro card of size of 233.4 mm × 160 mm, excluding the mother board.

3.3 Hardware for Recording HOE Performance

To record the performance of HOE hardware during testing and/or flight trials on a standard VCR, a recording hardware has been provided.

The fundamental consideration is that the output image should overlay on the input image (TS-DSC). Neither of them should get affected and the frame as a whole should be recorded on a VCR.

The sync signals are generated separately as explained in Sec. 3.2. The processor, after generating the (16 × 16) LR image, transmits it to ABS through VBC. After above transmission, it will write in a memory (SRAM-2) kept for recording. For reading the SRAM-2, separate address is generated using a set of counters. The readout data goes to a D/A converter and taken for recording. These two address and data buses are taken from buffers/multiplexers and connected to SRAM-2. The processor enables/disables the buffers/multiplexers through the port bits. For recording purpose, the composite video from TS (composite sync) is taken as it is and only during TS video period, a required portion of TS video is disabled and LR video coming from D/A is superimposed. This is illustrated in Fig. 5.

4. SYSTEM SOFTWARE

The main system flow chart is shown in Fig. 6. The present application software is developed in PL/M language (PL/M 86).

On power ON, the USARTs (serial communication interface), Programmable Peripheral Interfaces (PPI) and programmable timer/counter are initialized. Both the USARTs are initialized in async mode, with one stop bit, no parity, eight bit character length, 16x baud rate and enable transmit and receive (DTS and RTS). Programmable timer counter 0 and counter 1 are initialized to get square wave of 9600 baud frequency, required for USART for transmission and reception. The three PPI ports are initialized as output ports.

After initializing all the peripherals in the above mode, the processor waits for the VBC start signal to go from LOW to HIGH. It checks the DSC serial link. Once the serial link test is completed, DSC sends the target coordinates (X and Y) and checksum to HOE. The checksum is the sum of the coordinates. HOE compares the received checksum with the computed one. Then the processor computes the left edge, right edge, bottom edge and top edge of the target and applies the predefined boundary conditions.
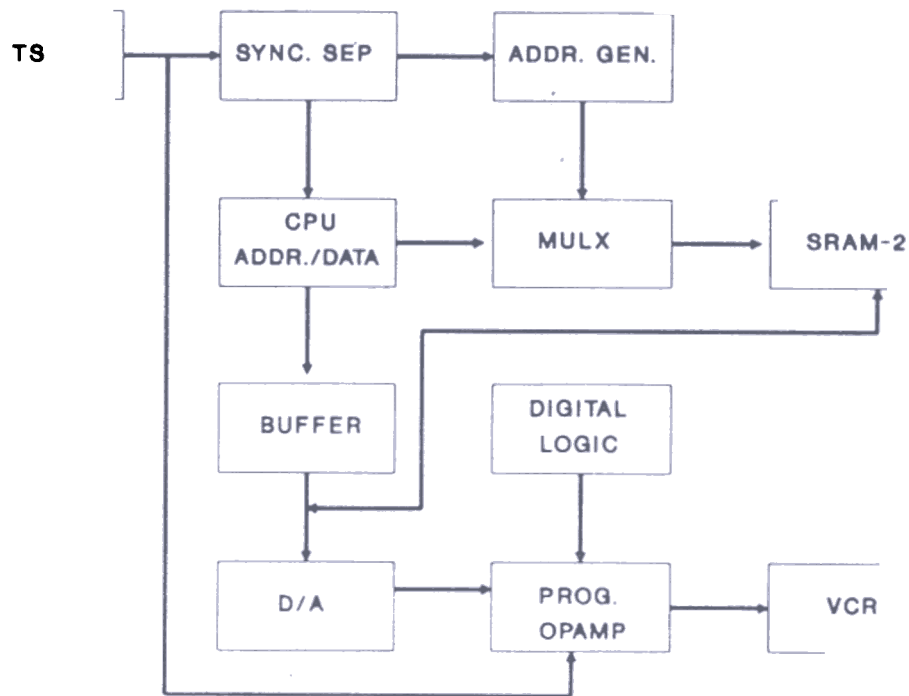

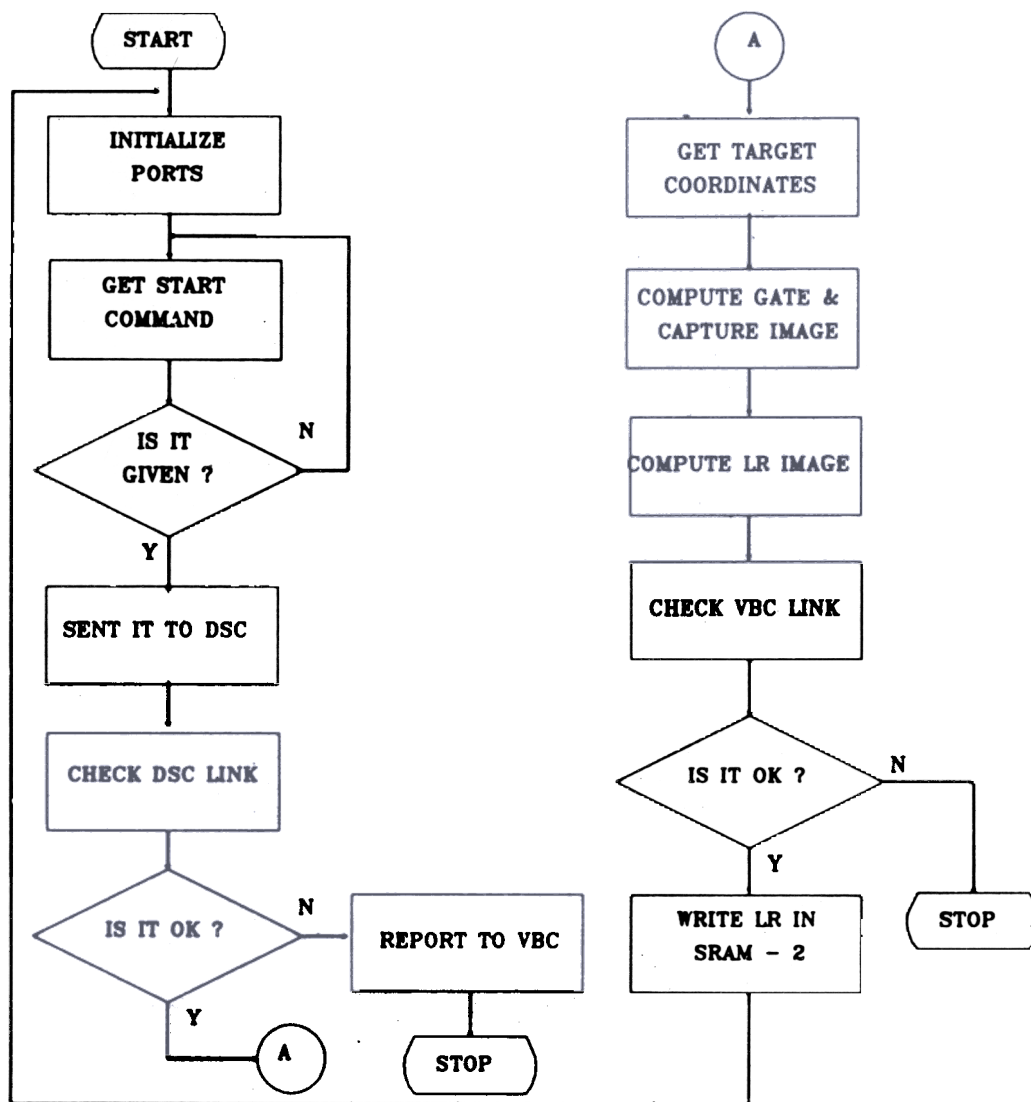Figure 5. Hardware block diagram for recording HOE performance.

Figure 6. Software flow diagram.

The computed target edges are outputted to the comparators through the ports with synchronization with the field pulse. For synchronization, the processor checks the frame pulse (VS), by reading through an input port bit. Here both high and low levels of the pulse are taken into consideration for checking. This avoids the false synchronization. Then the processor waits for 100 ms. During this 100 ms period, DSC disables all its overlay features on the image like cursor, graphics, etc. in the predefined field and displays only raw TS image. HOE waits for five (20 ms × 5) fields. During this time a predefined size of the image around the target will be captured in the SRAM-1. DSC will see the HOE readiness before enabling the cross lines and graphics on the image. i.e. after waiting for 100 ms.

HOE processor computes the LR image data by applying the resampling algorithm. To generate 16 × 16 LR image from a HR image with a horizontal resolution factor of 14.2 and vertical resolution factor of 14.634, there are 4096 real number multiplications, 139756 integer and 12544 floating point additions. While developing the software, the integer number calculation part and floating point calculation part are written as separate modules, so that the compiler can allocate the integer manipulation to the 8086 CPU and floating point manipulation to the coprocessor 8087. Otherwise, compiler treats all computations in the algorithm shown in Eqn (13) as real number computations and generates only 8087 code making 8086 idle for that period. The above method makes use of both the processors in

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parallel. When we have implemented the complete algorithm in a floating point, the processor and coprocessor has taken nearly 19.23 s to generate the LR image of 16 x 16 size. The real and integer manipulation modules took lesser time. The time taken by the processor and coprocessor in this case is 1.5 s for generating LR image of same size. Now, HOE gives ACK signal to VBC through a separate port bit. After establishing link with the VBC, HOE transmits LR data and checksum to VBC. VBC, in turn, transmitts the reference image to the airborne sensor.

The CPU enables the buffers/multiplexers for writing into SRAM-2, for recording purpose. After writing into SRAM-2 buffers/multiplexers are enabled for reading. Both LR and HR images are recorded on a VCR.

5. VALIDATION OF THE ALGORITHM, HARD- WARE AND SOFTWARE

To evaluate the hardware, software and algorithm in the laboratory, a visible video camera and ABS are comounted on a platform, which can be moved. This visible camera is used as substitute for TS-DSC. The image is taken from TS and resampled in HOE hardware. Then the correlation is carried out. This is repeated number of times to validate the system. The testing can be carried out in the following two ways.

(a) The resampled image (LR) can be transmitted from HOE to a PC through RS 232 link (instead of to ABS) and the seeker image can be captured on a PC. Correlation can be performed in software on a PC.

(b) The resampled image (LR) can be transmitted from HOE to an existing correlation tracker, which can correlate the same on the search image.

5.1 Test Procedure and Results

A Javelin video camera is used as high resolution sensor and an existing seeker is used as a low resolution sensor. The image from the camera is captured by HOE H/W and resampled low resolution image is transmitted to a PC. The seeker image is also captured to a PC through a data acquisition card. The parameters like ratio of FOV, ratio of lines per frame and the ratio of aspect ratio of the two sensors are substituted in Eqns (1) and (2). The horizontal and vertical scaling factors are 2.12 and 3.23 respectively.

For illustration purpose, three photographs are presented in Fig. 7. Even though the images are having 256 (8-bit) gray levels, because of PC (EGA card) we can see only 16 gray values as 16 colours. HR image is of 256 × 256 size as captured on HOE hardware. Reference image is of size 16 × 16 generated by the HOE H/W. LR images are 64 × 64 seeker images. The four images under LR images are captured from seeker at different points of time with target at different locations. The white rectangle shown (Fig. 7) in HR image is the area treated as the target area. After capturing on PC, correlation (direct method) is carried out on each seeker image with the same reference image.

The reference image has registered correctly as shown in Fig. 7. The point of registration is shown by a white rectangle. Figure 7(a) is of hills with sky background. A rock, which is protruding outside is taken as a target. Figure 7(b) is the top roof edge of a building with sky background. Figure 7(c) is a window of a building. In all these cases, the generated reference image has matched correctly as long as the target was in the FOV of the seeker. It can also be seen from Fig. 7 that gray level variation of 20 to 30 is present between HR and LR images which also is taken care of by the correlation algorithm.

6. SUMMARY AND CONCLUSION

Simulation study was carried out using the handing over algorithm (HOA) taken from Boland et al^2 and found that the HOA is suitable for our application. This algorithm is implemented using hardware and software. Hardware is designed around iAPX 86 and NDP 8087 coprocessor. The software is developed using PL/M 86 language[8].

The processor takes 1.5 s for the computation of HOE algorithm and another 0.5 s for the communication protocol. Hardware has also been developed for superimposing the resampled LR image on to the HR image in a corner and recording on a VCR. By simulating the field scenario in a realistic way in the laboratory, the system has been evaluated and found to be functioning satisfactorily. For a practical application, the execution time should be less than 1 s. This can be achieved by using faster processors and generating a more optimum machine code using latest versions of C and C^{++} languages. Efforts are also on to reduce the execution time.
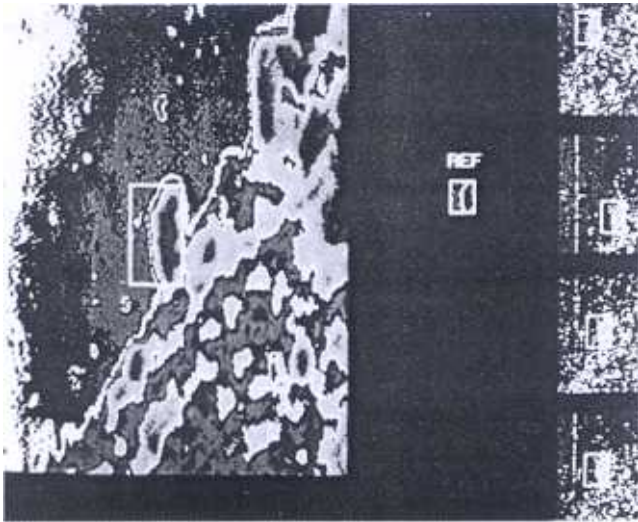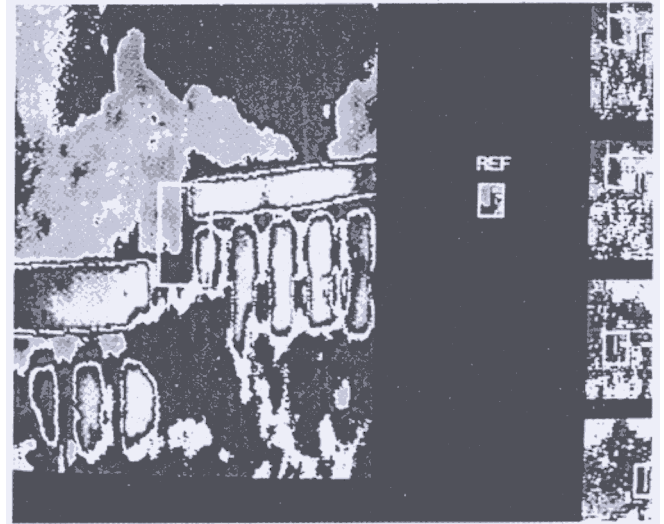
(a)

(b)
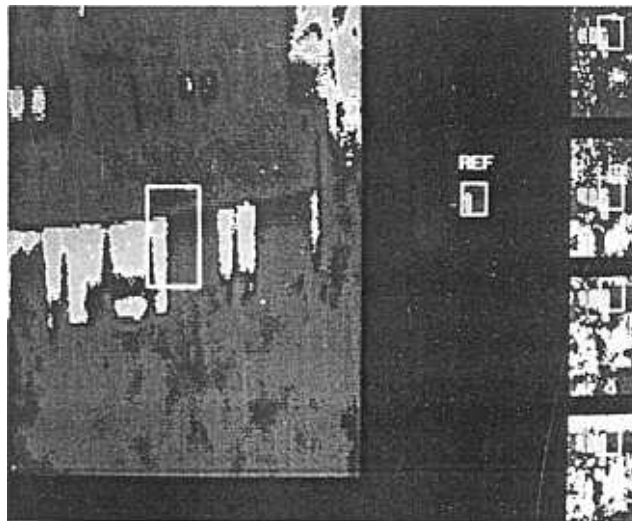
(c)

Figure 7.

ACKNOWLEDMENTS

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