Defence Science Journal, Vol 45, No January 1995, pp 65-68

SHORT COMMUNICATION

Design and Fabrication of 35 GHz *GaAs* Gunn Diodes

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ABSTRACT

The paper describes design and fabrication of *GaAs* 100 mW Gunn diodes for operation at ~ 35 GHz. As the devices have low efficiency, a large amount of input power is dissipated as heat, resulting in temperature rise in the device during operation beyond tolerable limits. Heat from these devices can be removed quickly and efficiently by using gold as integral heat sink (IHS). Further, the temperature of the device can be controlled by monitoring device area. Calculations for heat flow and expected efficiency have been done. Required Gunn structure has been grown by molecular beam epitaxy technique. The devices have been fabricated by IHS-IBR (integral bonding ribbon) technique. From the devices developed, 100 mW of output has been achieved in the frequency range 33-38 GHz with an efficiency of 3-4 per cent.

1. INTRODUCTION

Gunn diode is the most promising source of power at millimeter wave (mm-wave) frequencies. It exhibits low FM noise and provides a wide range of operating frequencies. It is therefore extensively used as a local oscillator in all radar related applications. It is used as transmitter/receiver in radars, beacons, transponders, speed sensors, radio and data links. It also finds application as a power source in preamplifiers, sweepers, intrusion alarms and fuses. Gunn diodes serve as local oscillators and/or amplifiers for communication systems. These diodes are highly reliable devices with practically no restrictions on lifetime. Small size, light-weight and small voltage bias requirements make them superior to low power mm-wave klystrons and backward oscillators. Frequencies from 30-35 GHz which lie in the lower end of mm-wave spectrum are important for radiometry, radars and communication. In this paper, the design of 35 GHz *GaAs* Gunn diodes, operating in the fundamental mode, has been described along with device fabrication details.

2. PRINCIPLE OF OPERATION

The operation of a Gunn diode depends on the transferred electron phenomenon in a special class of semiconductors which have a multivalley structure in their conduction band. Gallium arsenide is the main representative of this class. When a thin sample of this material is biased, the current increases linearly with biasing voltage following Ohm's law. As the bias voltage increases beyond the threshold voltage, the current starts decreasing giving rise to negative differential resistance; and current oscillations in the circuit are observed. The decrease in current is found to be associated with the transfer of electrons from the high mobility, low effective electron mass central valley to low mobility, high effective mass satellite valley. Because of this excitation, the fast moving electrons get slowed down and form a high field domain (comprising accumulation/depletion of electrons) which moves with saturated velocity under the influence of electric field. The high field domain normally nucleates at the cathode end and after traversing the whole length of the sample, annihilates at the anode end, giving a current spike. A new domain is again nucleated and the cycle is repeated.

3. DEVICE DESIGN

Design of a Gunn diode for a particular frequency is governed by a few basic material parameters, such as layer thickness, carrier concentration and device

Received 11 October 1994

geometry. The actual values used depend on the operating frequency, efficiency and the impedance level required of the finished device.

3.1 Frequency of Operation

The frequency of operation depends on the time (t) the high field domain takes to traverse the active length (L_{eff}) of the material[1].

$$\frac{}{t} = \frac{v_{domain}}{L_{eff}}$$

where v_{domain} is the velocity of high field domain and for *GaAs* it is 1×10^7 cm/s. The relationship of frequency of operation (f) and active layer thickness L_{eff} is depicted in Fig. 1. For 35 GHz frequency of operation, the effective length of the active region should be

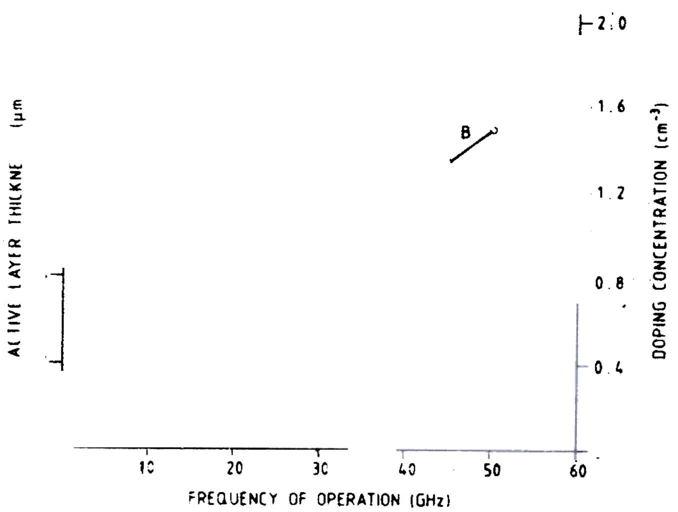

Figure 1. Active layer thickness *vs* frequency of operation (Curve A) and doping concentration *vs* frequency of operation (Curve B).

approximately 2.86 μm. The upper limit of frequency up to which Gunn diode can operate efficiently is imposed[2] by finite electron relaxation time due to the non-instantaneousness of transferred electron effect.

3.2 Carrier Concentration of Active Region

Any space charge instability in the semiconductor grows exponentially in space and time as

$$Q = Q_0 \exp(t/\tau_d)$$

where $\tau_d[=(\varepsilon/\sigma)=(\varepsilon/ne\mu_n)]$ is the magnitude of the negative dielectric relaxation time, ε is permittivity, μ_n is the negative differential mobility, n is doping concentration and σ is the conductivity. The growth factor can be expressed as

$$\exp(t/\tau_d) = \exp(L_{eff}/v\tau_d) = \exp\frac{L_{eff}ne \mid \mu_n \mid}{\varepsilon v}$$

For large space charge growth, $(L_{eff}ne|\mu_n|)\varepsilon v$ has to be greater than unity, which demands

$$nL_{eff} \gg \varepsilon\, v/e \mid \mu_n \mid$$
$$> 1 \times 10^{12}\,\mathrm{cm}^{-2}$$

For stable and efficient oscillations the product of doping concentration and length is kept 3.0-3.5 $\times 10^{12}$ cm^{-2}. With this criterion, suitable range of doping concentration can be estimated. This is illustrated in Fig. 1. The optimum value is 1.0-1.2 $\times 10^{16}$ cm^{-3}.

3.3 Thermal Constraints[4]

The typical Gunn diode structure comprises n^+-n-n^+ *GaAs* layers (Fig. 2). Being a low efficiency device, temperature rise during operation imposes serious limitations on the device dimensions and requires an efficient heat dissipation. As a consequence, heat sir' becomes of prime importance. When the active layer temperature rises, both the overshoot velocity and saturated drift velocity decrease and result in a strong reduction of transit frequency and r.f. performance. The device operating temperature should be limited to 200 °C for good device performance and reliability.

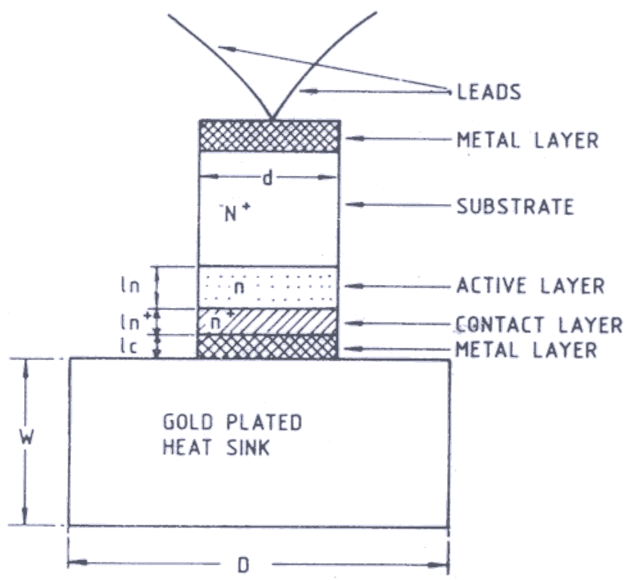

Figure 2. Typical Gunn diode structure.

The maximum attained temperature(T_{max}) can be estimated by considering a simple heat flow model. The following assumptions are made to arrive at an expression for T_{max} :

(a) Heat flow is considered normal to the heat sink,

(b) In the limits $(d/D) < 0.1$ and $0.04 < (W/D) < 4.0$, heat sink is assumed to be semi-infinite,

(c) Joule heating in n^+ layer is neglected, and

(d) Thermal conductivities of n and n^+ layers are approximated by $150/T$ and $120/T$, respectively.

Then

$$T_{max} = \left\{T_0 + Q\left(\frac{d}{2k} + \frac{l_c}{k}\right)\right\} \exp\left\{Q \left(\frac{l_{n^+}}{120} + \frac{L_{eff}}{300}\right)\right\}$$

where, T_0 = Ambient temperature in K

Q = Input heat flux = (Input power/area)

k = Thermal conductivity of gold = 3.88 W/cm^2

l_{n^+} = n^+ layer thickness = 0.3 μm

L_{eff} = active layer thickness

l_c = Ohmic metallisation layer thickness = 0.2 μm

It is advantageous to make the n^+ contact layer and metal bond as thin as possible. T_{max} and expected device efficiency have been calculated for different mesa diameters ($2r$) for 100 mW output power and are shown in Fig. 3. To a first order, the input heat flux varies

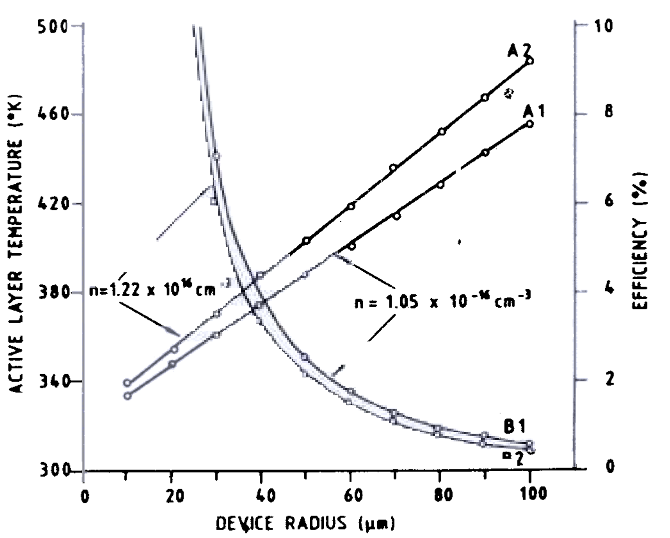

Figure 3. Active layer temperature *vs* device radius (Curves A1, A2) and efficiency *vs* device radius (*r*) (Curves B1, B2).

linearly with position, increasing from zero at the cathode to a maximum value at the anode. This can be analytically modelled using[5]

$$Q = 2JVx/l_n$$

where V is the bias voltage, and $J \approx ne\mu E = \frac{ne\mu V}{L_{eff}}$

The electron mobility μ can be determined as a function of the electric field strength E, the operating temperature and doping concentration n. The variation of input heat flux versus length of the active region (x) is illustrated in Fig. 4 for two different doping concentrations which give a temperature gradient in the device.

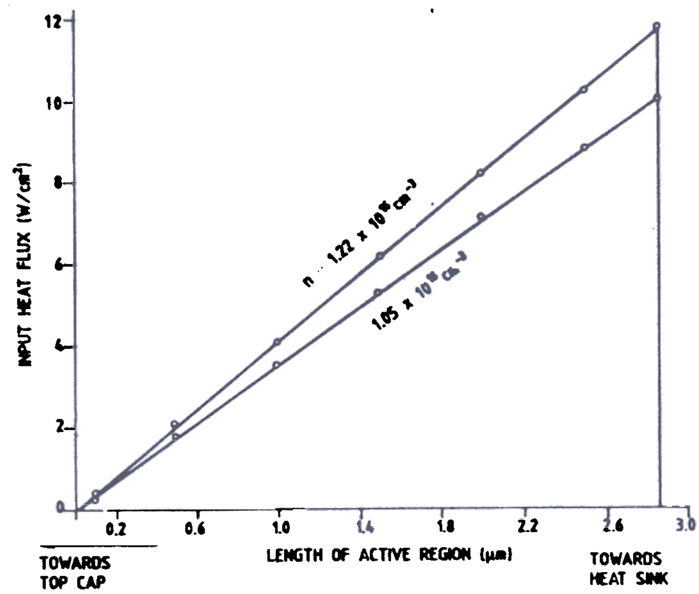

Figure 4. Input heat flux *vs* length of active region.

The contact resistance plays a very crucial role in justifying the assumptions made on operating conditions and the maximum rise in temperature. A reasonable value of one tenth of low field resistance is accepted for ohmic contacts.

For the heat sink region where the lateral heat flow is also important, an effective thickness of heat sink can be defined as $w = gA^{1/2}$ where g is a geometrical factor depending on the form of the device area A. For circular devices $g = \pi^{-1/2} = 0.564$. For 50 micron diameter devices, $w \approx 25$ μm. At high frequencies the current is confined within the skin depth of the surface of the substrate. This results in an increase in the effective resistance of the substrate[6]. Hence, the optimum *GaAs* substrate thickness is about two times the skin depth for uniform current distribution. For 35 GHz, the substrate should be about 17 micron thick.

4. DEVICE FABRICATION

The required epitaxial layers are grown by molecular beam epitaxy (MBE) technique on a conducting

n^+ *GaAs* substrate (*Si* doped) of carrier concentration $\geq 10^{18}$ cm^{-3}. A buffer layer of carrier concentration approximately 5×10^{17} cm^{-3} is initially grown on the substrate with a thickness of 0.5 μm. This screens the imperfections of the substrate. The active layer is next grown to a thickness of about 2.8 micron. Finally, ~0.3 μm thick n^+ contact layer of high concentration ($\geq 10^{18}$cm^{-3}) is grown. This layer is essential for making low resistance ohmic contact to the device. The doping concentrations and thicknesses of different epitaxial layers were determined by using Polaron depth profiler. The devices are then fabricated using integral heat sink-integral bonding ribbon technique[7]. The first step is ohmic contact formation with very low specific contact resistance using the *Ni/Au-Ge/Au* metallisation system followed by alloying. A 20 μm thick gold layer is electroplated on the epitaxial side of the wafer. It serves as integral heat sink and mechanical support for further processing of the wafer. The substrate is thinned down to < 20 μm by chemical-mechanical lapping. Bonding ribbons are formed as integral part of the device. This results in improvement in device bonding and yield. The devices are etched to form mesas (typically 140 μm in diameter) whose area determines the threshold current of the diode which in turn, fixes the operating current. The chips are bonded into standard packages (MA ODS 138 style) by thermo compression[8] bonding technique. The devices are etched further when in package for evaluation of r.f. performance at different currents. Hence the optimum current can be determined with respect to power and efficiency for a particular batch of diodes. The diodes are then finally hermetically sealed using top cap.

The devices are then d.c. tested for ohmicity and low field resistance is determined. For r.f. testing the device is put into the 35 GHz microwave cavity and is tuned for optimum r.f. power output. Typical 100 mW of output power with an efficiency of 3-4 per cent has been achieved in 33-38 GHz region.

ACKNOWLEDGEMENTS

The authors thank their colleagues in the MBE and Microwave Groups for the growth of *GaAs* epitaxial material and r.f. measurements, respectively. The authors also thank the Director, Solidstate Physics Laboratory, for his encouragement and permission to publish this work.

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