SHORT COMMUNICATION

Improved Passivant-induced Shunt Resistance Model for *n-HgCdTe* Photoconducting Infrared Detector

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ABSTRACT

A multilayer model for the majority carrier distribution is employed to calculate the shunt resistance due to passivant-induced electric field in the accumulated n^+ region. The carrier depth profile drops sharply away from the surface, finally attaining the bulk value. The effect of complete sidewall passivation on the shunt resistance is considered. The results show that if the contribution of sidewall passivation is neglected, the total detector resistance is overestimated by ~ 35 per cent. The detector responsivity calculations using the present model are compared with the Siliquini's model and the experimental data of Siliquini. It has been found that the present model yields relatively better agreement with the experimental data in shunt-dominated region.

Keywords: *HgCdTe* photoconductive detectors, shunt resistance model, shunt resistance, surface potential, passivant-induced shunt resistance model

1. INTRODUCTION

The mercury-cadmium-telluride (*HgCdTe*) photoconductive detectors are extensively used in high resolution thermal imaging systems[1]. Apart from the material properties, the performance of a photoconductive detector depends critically on the properties of its passivant and its interface with the semiconductor material. Anodically-grown native oxide passivant, which yields positive fixed charges at the interface, is the most favoured passivant in *n-HgCdTe* photoconductive detector technology[2]. Furthermore, surface recombination due to interface traps at the passivant-semiconductor interface reduces the level of steady state photogenerated minority carriers by lowering the effective minority carrier lifetime, and thereby affecting the performance of the device. The low surface recombination velocity is, therefore, a necessity for high performance device.

The fixed electric field produced by the positive fixed charges at the interface leads to accumulation of electrons at the surface, and thus, enhances surface conduction, giving way to a shunt resistance path at the surface to the current flow in parallel with the bulk detector resistance. This results in lowering of the detector responsivity (R_v).

In a gated *HgCdTe* photoconductor structure, the effects of accumulation on responsivity, shunt resistance and lifetime were studied earlier by varying the gate potential, both theoretically as well as experimentally[3,4]. Bhan[5], *et al.* have studied in detail the effect of these fixed charges on accumulation layer for standard and overlap structures. However, in both of these models (by Siliquini[3] and Bhan[5]), the disagreement with measured responsivities in shunt-dominated detector resistance regions (accumulation regions) was significant.
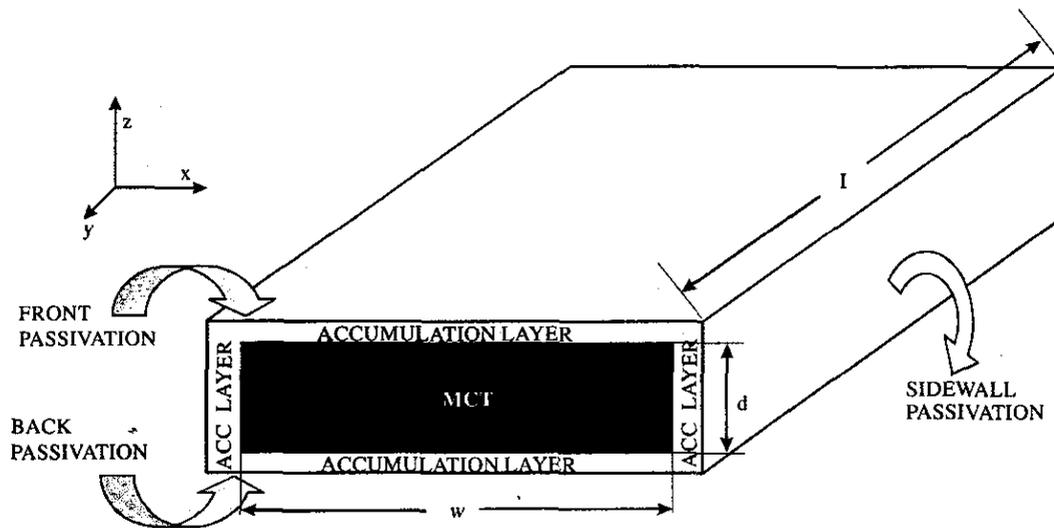
Figure 1. Schematic cross-sectional view of a photoconductor, the sidewalls are also passivated with anodic oxide.

The earlier studies[3-5] have used a step model assuming the accumulation layer to have a constant majority carrier concentration profile, which is far from the actual case. In the present model, the surface layer is rigorously treated as having a concentration profile, which is much closer to real situation. It is assumed that the accumulation layer region is composed of a large number of small sub-layers, each having varying majority carrier concentration. The shunt resistance is calculated, layer-by-layer, till majority carrier concentration reaches the bulk value. Finally, the responsivity is calculated for such a carrier concentration profile in the accumulation layer.

For higher resolution applications, the detector technology demands the use of small active area, which may be comparable to its thickness. Hence, the contributions from the sidewalls to the shunt resistance for small geometry detectors cannot be neglected. There is, therefore, a need to model the device performance, including sidewall contribution, using accurate carrier concentration profile in the estimation of the shunt resistance.

The only reported model, which includes sidewall passivation contribution, is due to Siliquini[6], et al. But here again, a constant majority carrier density was assumed. The shortcomings of aforesaid models are taken into consideration in the present work,

in the sense that profiled nature of majority carrier concentration and contributions from sidewalls to shunt resistance have been included.

2. THEORETICAL MODEL

2.1 Total Shunt Resistance

It is assumed that mainly the fixed surface state charge density, Q_f, due to passivant is responsible for positive surface potential, which accumulates the mercury-cadmium-telluride surface. A cross-sectional schematic diagram of the device model is shown in the Fig.1. The potential ψ is assumed to be zero in the bulk and surface potential, ψ_s, at the surface. To satisfy Gauss law, majority carriers are always attracted to the surface and are confined in one dimension in a thin layer at the surface. However, these are free to move in other two directions under the influence of lateral field, such as E_{bias} along the length of the detector.

The surface state charge density, and majority and minority carrier concentration profiles at the surface, n_s and p_s, respectively are obtained using one-dimensional Poisson's equation and Gauss Law[7]. Now, one needs to relate these carrier profiles at the surface to distance, viz., depth, which is done by numerical integration of surface field as follows:

$$t(\psi) = \int_{\psi_s}^{\psi} \frac{d\psi}{E_s(\psi)} \tag{1}$$

The above equation gives the depth profile for a given ψ_s or Q_f to be later used in the calculations of n_s and layer model of shunt resistance. The detailed expression of E_s is given by Sze[7].

For calculation of surface shunt resistance, R_s, the accumulated region is divided into sub-layers, and resistance is calculated for each layer. In addition, the sidewall passivation and its effect on R_s are also taken into consideration for these calculations. To do that, an identical and uniform accumulation layer on all the four sides (front, back, and both sidewalls) of the detector is considered (Fig. 1). For R_s calculation, one has to know layer thickness, δt, of each layer apart from n_s. Layer thickness is calculated by numerical integration using Eqn (1). Since t and ψ_s are not related linearly, for a given ψ_s, t is calculated for the ith layer, and $t_i - t_{i-1}$ gives the layer width and corresponding n_s. For calibration of the algorithm and the calculation, it was verified and ensured that summation charge densities in each sub-layer is equal to the total charge density given by Gauss Law, ie,

$$Q_s = \sum_{i=1}^{i=n(bulk)} n_s(i) \, \delta t(i) \tag{2}$$

The other details of the calculation procedure are given by Dhar[8], *et al.*

As shown in the Fig. 1, the surface shunt layer is treated as a sheet of length l, width of $2(w + d)$ and thickness equal to the thickness of accumulation layer. This assumption will hold only if the thickness of accumulation layer is much less than the detector's width and thickness. Finally, the total surface R_s due to all the layers is calculated, assuming constant surface mobility, μ_s by adding these in parallel as follows:

$$\frac{1}{R_s} = \sum_{i=1}^{i=n(W_{max})} \frac{1}{R_{layer(i)}} \tag{3}$$

where

$$R_{layer(i)} = \frac{l}{2(w+d)} \frac{1}{q n_s(i) \, \mu_s} \tag{4}$$

While calculating $R_{layer(i)}$, the iteration is terminated when $n_s(i) = n_{no}$, where n_{no} is the equilibrium majority carrier density. After having calculated R_s, the performance parameters namely effective bulk detector resistance R_d and responsivity R_v were calculated.

2.2 Detector Resistance & Responsivity

It has been assumed that detector consists of two parts: (i) bulk core of mercury-cadmium-telluride, and (ii) surrounding sheet of accumulated layer from all the four sides. Having calculated R_s, the remaining bulk (ie, core) resistance of the detector R_b, including sidewall contributions, is estimated as follows:

$$R_b = \frac{l}{(w - 2t_{max})} \frac{1}{q n_{no} \mu_b (d - 2t_{max})} \tag{5}$$

where t_{max} is the maximum accumulation layer thickness at the surface. While calculating majority carrier concentration profile at the surface using $n_s = n_{no} \exp(\beta \psi_s)$, the depth at which the majority carrier concentration profile reaches the bulk value is taken as t_{max}. The factor of $2t_{max}$ is inserted because the bulk region having constant n and μ is the total detector thickness minus surface layers from the front and the back, and width minus surface layers from both the sidewalls (Fig. 1). In actual detectors, all the surfaces (front, back, and sidewalls) are passivated. Finally, the net detector resistance is given as

$$R_d = \frac{R_b R_s}{(R_b + R_s)} \tag{6}$$

To fit the experimental data of gated photoconductor, the relationship between the gate voltage, V_G, and the surface potential, ψ_s, in the presence of interface traps, using metal insulator semiconductor (MIS) theory can be expressed as[3]

$$V_G - V_{FB} = V_{OX} + \psi_s \tag{7}$$

where $V_{FB} = \phi_{ms} - Q_f/C_{ins}$, $V_{OX} = Q_s (\psi_s)/C_{ins}$, ϕ_{ms} is the work function difference between the gate metal and n-type $HgCdTe$, Q_f is the fixed oxide charge for the native oxide/$HgCdTe$ interface, and C_{ins} is the gate insulator capacitance. A change in the gate potential can vary the charge density in the space charge region.

The device voltage responsivity, R_v, following Reine[9], et al. at wavelength λ is given by

$$R_v = \eta \frac{\lambda}{hc} \frac{1}{lwd} \frac{V_b}{n_0} \tau_e \frac{R_s}{R_s + R_b} \qquad (8)$$

where V_b is the bias voltage, h is the Planck's constant, c is the speed of light, d is the thickness of the device, and τ_e is the effective minority carrier lifetime. As discussed in the introduction, the effective lifetime (τ_e), including the contributions from the accumulation layer[6] can be given by

$$\frac{1}{\tau_e} = \frac{1}{\tau_b} + \frac{S_f}{d} + \frac{S_b}{d} + \frac{2S_s}{w} \qquad (9)$$

where τ_b is the bulk minority carrier lifetime, S_f, S_b, and S_s are the surface recombination velocities at the front, the back, and the sidewall boundaries of the semiconductor, respectively, and w is the width of the device.

In this study, it has been assumed that all the surface recombination velocities are identical and equal to S. Assuming that the interface recombination centres are at mid-gap and having a density, D_{it}, the surface recombination velocity at the surface of an n-type semiconductor is related to the surface potential[10] by

$$S = \frac{kTD_{it}}{q} \sigma v_{th} \frac{n_0}{p_s + n_s + 2n_i} \qquad (10)$$

In this equation, D_{it} is the fast interface trap density, σ is the capture cross section, v_{th} is the thermal velocity of the carriers, n_s and p_s are the majority and minority carrier concentration profiles at the surface, and n_i is the intrinsic carrier concentration at the semiconductor surface. The maximum surface

recombination occurs when $n_s = p_s$, therefore, surface accumulation quenches recombination interface traps and reduces the surface recombination velocity. This allows the effective minority carrier lifetime to approach the bulk lifetime in Eqn (9).

The dielectric constant, bandgap, E_g, and intrinsic carrier concentration as a function of composition x and temperature T of the MCT material are calculated following Rogalski[11], et al. and Hansen[12,13], et al. The values of other parameters used in the calculation are given in Table 1.

3. RESULTS & DISCUSSIONS

Table 1 lists all the parameters used in the simulation. The typical distribution of majority

Table 1. Parameters used in simulation

Parameter	A*	B**
Temperature (K)	80	80
x in ($Hg_{1-x}Cd_xTe$)	0.23	0.23
Detector length (μm)	25	250
Detector width (μm)	25	250
Detector thickness (μm)	7	7
Signal wavelength (μm)	--	8.6
Quantum efficiency (η)	--	1
Majority carrier density (n_{no})(cm^{-3})	3E14	7E14
Electron mobility (μ_e)(cm^{2}V^{-1} s^{-1})	1.1E5	1.1E5
Hole mobility (μ_h)(cm^{2}V^{-1} s^{-1})	500	500
Bulk minority carrier lifetime (τ_b)(μs)	4	4
Interface trap density (D_{it})(cm^{-2} eV^{-1})	1E12	1E12
Anodic oxide thickness ($^-$)	800	800
ZnS thickness ($^-$)	2000	2000
Fixed-oxide charge (Q_f) charge/cm^{-2}	2.5E12	2.5E12
Capture cross section (σ) cm^2	1E-11	1E-11
Metal/semiconductor work function difference (ϕ_{ms})(V)	0.1	0.1
Surface recombination velocity (S)(cm s^{-1})	300	300

* Values used for simulation (Figs 2-4)
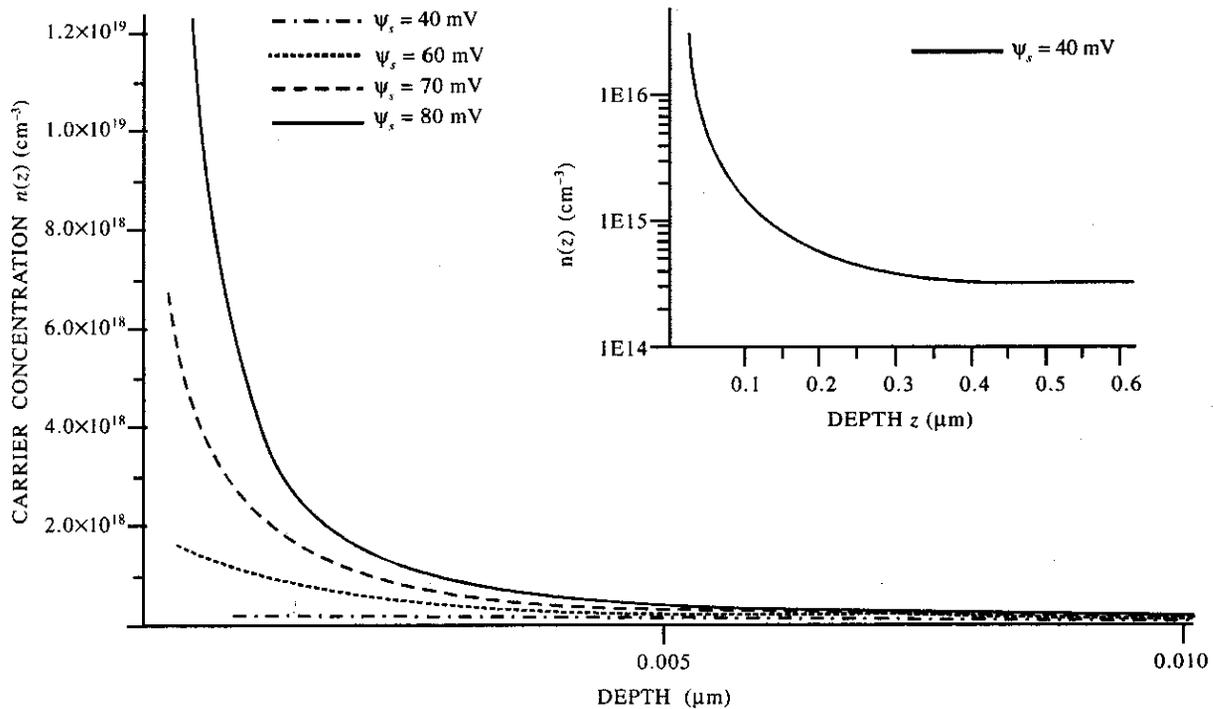** Values used for fitting experimental data (Fig. 5)

Figure 2. A typical depth distribution of surface majority carriers at various surface potentials (40-80 mV). The carrier depth profile drops sharply away from the surface, finally attaining the bulk carrier concentration value, ie, 3E14 cm⁻³. The inset shows the carrier profile for Ψs = 40 mV, wherein the carrier concentration drops to bulk value, as expected.

carriers from surface to the bulk, $n(z)$, is plotted in the Fig. 2 as a function of depth from the surface at various surface potentials (40–80 mV). It may be seen from this figure that the majority carrier concentration at the surface is more than four-orders of magnitudes compared to the bulk value for the highly accumulated case of ψ_s = 80 mV corresponding to Q_f of 2.3E12 charges/cm². Hence in this case, the detector resistance is completely shunt-dominated. Secondly, the carrier profile is sharply rising towards the surface. As shown in the inset, the carrier profile for surface potential, ψ_s = 40 mV, and $n(z)$ finally drops to the bulk value (within 0.03 %), as expected. The depth at which this happens is taken as the maximum thickness of accumulation layer (t_{max}) used in the estimation of bulk resistance [Eqn (5)]. As surface potential is increased, so does the number of majority carriers at the surface. These results clearly show that treating majority carrier density as constant is oversimplification, as done by the earlier workers.

Using the above profile (Fig. 2), the bulk, the shunt, and the total resistances have been calculated

with the sidewall (case 1) and without the sidewall (case 2) at Q_f = 2.3E12 charges/cm² as a function of detector thickness (Fig. 3). The length and width of the detector are assumed to be equal. When the effect of sidewalls is ignored, the bulk resistance, R_b, decreases with an increase in thickness, but R_s remains constant for a fixed value of Q_f. But with sidewall contribution, the R_s decreases with an increase in detector thickness due to the increased sidewall area. The total detector resistance, R_d, for 5 μm thickness of detector is 35.1 ohm and 47.5 ohm for cases 1 and 2, respectively, resulting in a 35 per cent overestimation for case 2. The R_d for 20 μm thickness will be 13.1 ohm and 25.4 ohm for cases 1 and 2, respectively, resulting in a 94 per cent overestimation for case 2. Therefore, it is very clear that the contribution to detector resistance from the sidewalls cannot be ignored and the sidewalls have to be passivated properly to control detector resistance.

Figure 4 shows the plot of the variation of bulk, shunt, and total resistances of detector versus Q_f, keeping the detector dimensions constant.
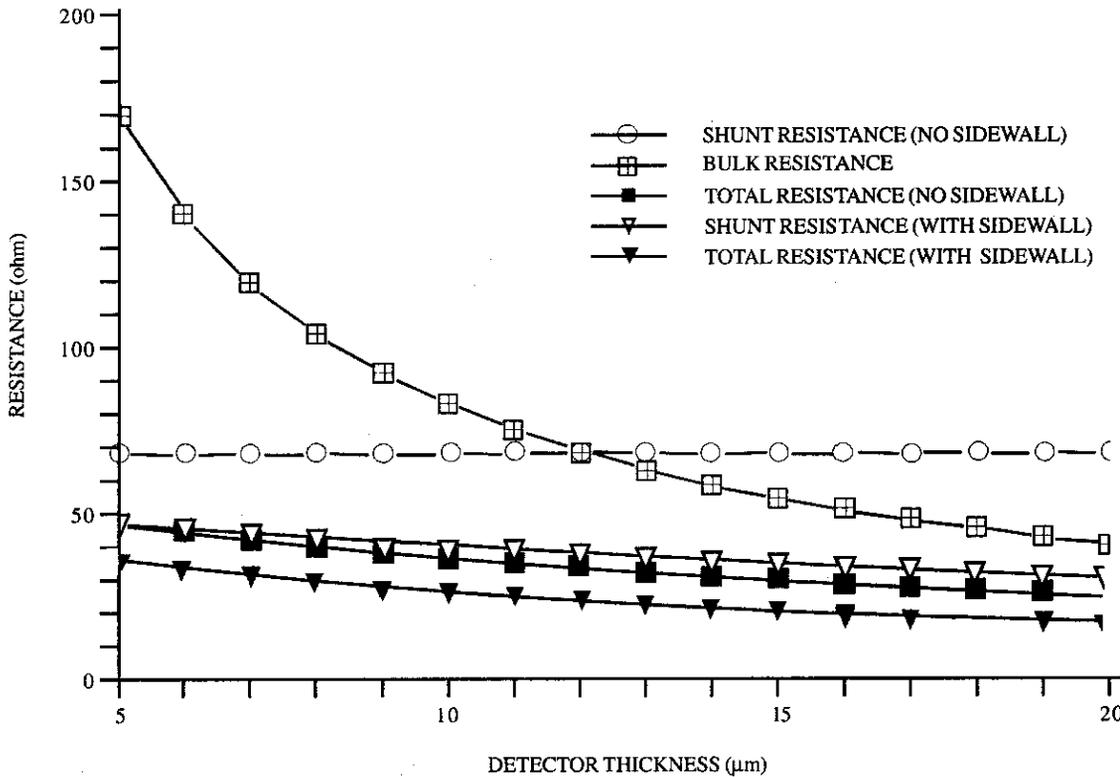
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Figure 3. Bulk, shunt, and total resistances of a detector as calculated using the carrier profile in Fig. 2 as a function of detector thickness with and without the contribution of sidewall passivation. The length and width of the detector are assumed to be equal and Q_f = 2.3 E12 charges/cm².

Additionally, the effect of Q_f on lifetime is also depicted in this figure. As the dimensions are constant, the bulk resistance remains constant at ~ 68 ohm with Q_f, while shunt resistance decreases with increase in the value of Q_f. The total detector resistance, R_d, is close to bulk values at very low values of Q_f (up to ~ 2E11 cm⁻²) because of very high values of shunt resistance. The minority carrier lifetime is low due to the high minority carrier recombination at the oxide/*HgCdTe* interface. However, as the shunt resistance decreases with increase in the value of Q_f, the effect of shunt starts playing a role and R_d is shunt-dominated. The oxide/*HgCdTe* interface becomes more accumulated with negative charges with increase in the value of Q_f, due to the Fermi level at the surface moving closer to the conduction band edge. The surface band bending and corresponding electric field causes the physical separation of electrons and holes at the surface of the semoconductor material, thereby isolating the photogenerated bulk minority carriers from the interface traps. The net effect is lowering of the surface

recombination velocity at the surface and an increase in the effective minority carrier lifetime for heavily accumulated surfaces. The surface recombination velocity decreases with increase in the value of Q_f, which results in increase in effective lifetime until it tapers and reaches almost bulk value[3-5]. A trade-off between shunt factor and lifetime is necessary to obtain optimum responsivity of the detector. From this figure, it is very clear that at Q_f= 1 E12 cm⁻², the shunt starts dominating but the effective lifetime has not reached the bulk value, the optimum Q_f should be between 1-2 E12 cm⁻². Depending upon the growth process[14-15], anodic oxide can yield Q_f from 5 E11 to 1 E12 cm⁻².

4. COMPARISON WITH EXPERIMENTAL DATA

To validate the theory proposed, the Siliquini's theory and his experimental data have been compared for responsivity with the present model. For fitting, the structure of the device is assumed as given by
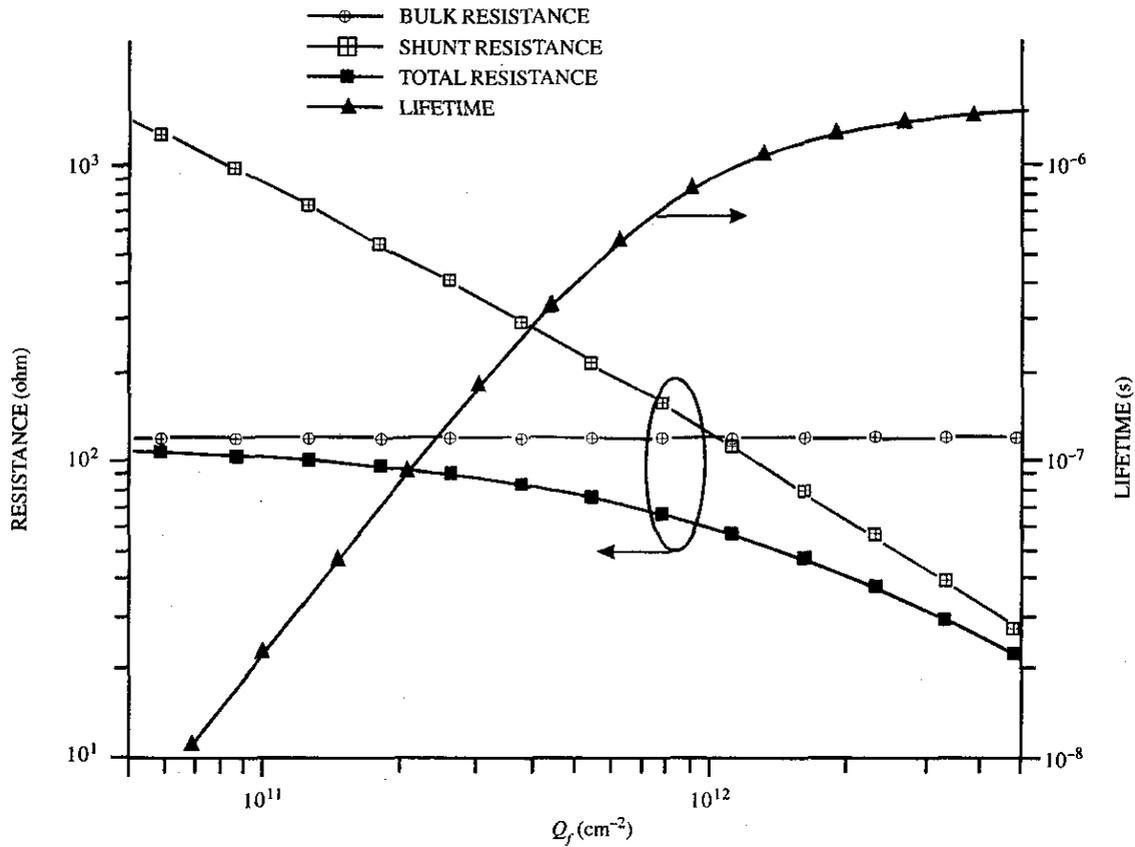
Figure 4. Variation of bulk, shunt, and total resistances of detector vs Q_f keeping the detector dimensions fixed. Additionally, the effect of Q_f on lifetime is also depicted. As the dimensions are kept constant, the bulk resistance remains constant, while shunt resistance decreases with increase in Q_f. A trade-off between shunt factor and lifetime is necessary to obtain optimum responsivity of a detector.

Siliquini and Farone[3]. The experimental values are for gated photoconductor of 250 μm × 250 μm × 7 μm. The effect of shunt from back surface passivation is neglected as the measured data is on mercury-cadmium-telluride epilayer grown on CdZnTe substrate. For calculating contribution of the shunt resistance due to sidewalls, only the effect of fixed-oxide charge, Q_f is considered. In case of the top surface, the variation of gate voltage, V_G, in addition to Q_f is taken into consideration. All these shunt resistances are connected in parallel to bulk. Figure 5 shows

the fit of the developed model with Siliquini's data along with their model. The responsivity, R_v, is plotted as a function of V_G calculated for the profile model along with that of Siliquini's model and experimental values[3]. A measured V_{FB} of -12.5 V, as quoted by the authors[3], was used to shift the gate voltage axis in the Fig. 5. It is evident from this figure that there is a reasonable agreement of the present model with the measured data. Table 2 gives the comparison of rms errors in fitting Siliquini's theory and the present model in different ranges

Table 2. Comparison of Siliquini's experimental data and theory with the present model

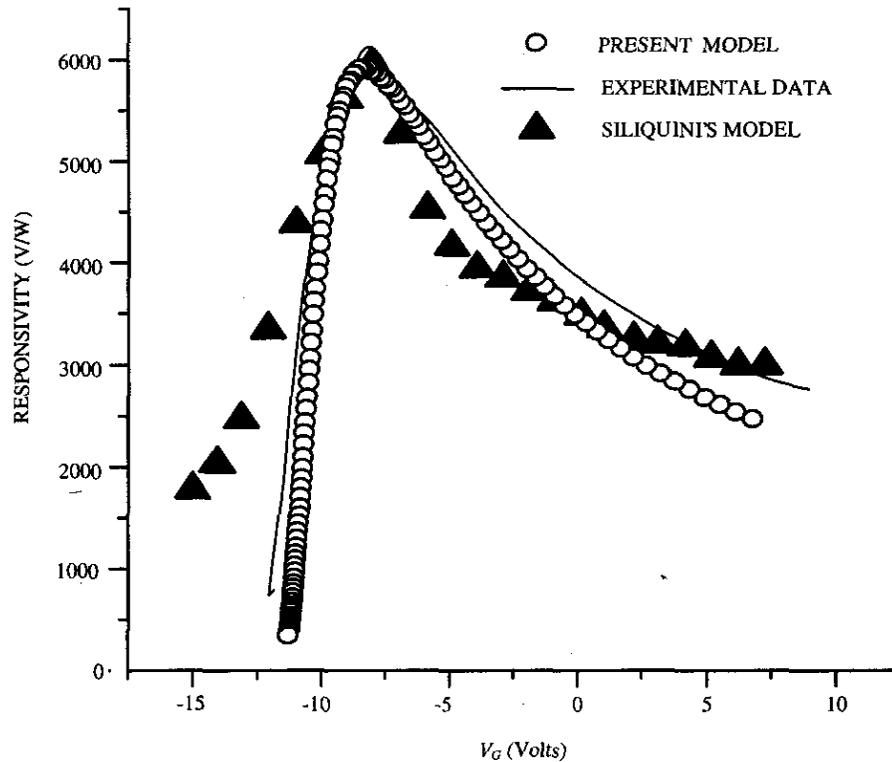| Disagreement (%)	Lifetime-dominated region (V_G from 12.0 V to 7.5 V) (%)	Shunt-dominated region (V_G from 7.5 V to 7.0 V) (%)	Total (V_G from 12 V to 7 V) (%)
Present model	20.38	12	15.89
Siliquini s model	28.01	14	20.63

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Figure 5. The responsivity, R_v plotted as a function of gate voltage, V_G and calculated using carrier profile model along with that of Siliquini's model and the experimental values showing a reasonable agreement of the present model with the measured data. The much better agreement in shunt-dominated region (−7.5 V to +7.0 V) is obtained on account of profile model and sidewall contribution.

of V_G. Evidently the agreement in shunt-dominated region (−7.5 V to +7.0 V) is better. The better fit is obtained on account of using profile model and sidewall contribution. In the surface lifetime-dominated region (−12.0 V to −7.5 V), the agreement of both the models is poor, however the present model relatively shows much better agreement than Siliquini's model[3]. The poor agreement of both the models may be due to the assumption made in calculation of surface recombination velocity due to the presence of interface recombination centres at mid-gap [Eqn (10)]. Under accumulation conditions, the minority carrier effective lifetime tends to approach the bulk lifetime due to the low levels of surface recombination, which directly increases the responsivity (region between −15.0 V to −7.5 V). However, further increase in V_G leads to the stronger accumulation, and hence, in an increase in surface accumulation charge and shunting of the device, thus increasing the total conductance and reducing the responsivity of the detector. Therefore, there will be a trade-

off between effective lifetime and surface accumulation charge. The responsivity will peak at a particular value of the surface potential under accumulation conditions, defined as optimal surface potential for a $HgCdTe$ photoconductive device.

5. CONCLUSIONS

The conventional approach of assuming the distribution of majority excess carriers at the surface due to the fixed surface state charge density to be within the Debye length is far from real condition. The authors have modelled the shunt resistance of a photoconducting detector in a layer-by-layer fashion, considering the profile nature of majority carriers, including the sidewall contribution as well. In the case of small geometry devices, sidewall contribution to total device resistance is very significant and cannot be neglected. The responsivity calculated using the present model shows a better agreement to the experimental data in a shunt-dominated region.

ACKNOWLEDGEMENTS

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