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Dry Etching of *GaAs* to Fabricate Via-Hole Grounds in Monolithic Microwave Integrated Circuits

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ABSTRACT

This study investigates the dry etching of 60 μm dia, 200 μm deep holes for fabrication of through substrate via holes for grounding monolithic microwave integrated circuits (MMICs), on 3-inch dia semi-insulating *GaAs* wafer using RIE and ICP processes with CFC and non-CFC gas chemistry, respectively. The effect of various process parameters on *GaAs* etch rate and resultant etch profile was investigated. Two kinds of masks, photoresist and *Ni*, were used to etch *GaAs* and performance was compared by investigating effect on etch rate, etch depth, etch profile, and surface morphology. The etch profile, etch depth, and surface morphology of as-etched samples were characterised by scanning electron microscopy. The desired 200 μm deep strawberry profile was obtained at 40 mTorr for both RIE and ICP processes with an etch rate of ~1.3 μm/min and ~4 μm/min respectively. *Ni* metal mask was used for RIE process due to poor photoresist selectivity, whereas ICP process utilised photoresist as mask. The vias were then metallised by depositing a thin seed layer of *Ti*/*Au* (1000 Å) using radio frequency sputtering and *Au* (~5 μm) electroplated to connect the frontside pad and back side ground plane. The typical parasitic inductance offered by these via for RIE and ICP processes was ~76 *pH* and 83 *pH* respectively, which is well within the acceptable limits. The developed process was finally integrated to in-house MMIC production line.

Keywords: GaAs, MMIC, Via-hole, ICP, RIE, etching

1. INTRODUCTION

High power *GaAs*-based monolithic microwave integrated circuits (MMICs) are widely used in military, wireless, and space communication systems. The performance of these MMICs is significantly improved using substrate via holes that connect the front and back sides of the wafer. Via connections provide low inductance grounding for circuit elements such as metal semiconductor field effect transistor (MESFET), high electron mobility transistor (HEMT), inductor and capacitor. They also allow increased packing density and ease of layout design due to flexibility in placing grounding structures[1-3]. These holes can provide additional heat sinking to mitigate the relatively low thermal conductivity of *GaAs*[4].

The via connection process consists of the via hole etching step and a subsequent metallisation step. Before etching via holes, devices are fabricated on the front side of wafer and then the wafer is thinned from the back side to a thickness of 100-200 μm as per the requirement. Via hole etching is performed from the backside of the wafer to contact grounding metal pads on the frontside. Dry etching is preferred over wet etching because of its superior uniformity and dimensional control. As via hole etching follows all other device fabrication processes, the process reliability and reproducibility are very important.

To etch very high aspect ratio holes, dry etching process must provide high etch rates, good etch anisotropy, smooth sidewalls, and high selectivity to the masking material and the frontside metal pad. The most common technique that meets the above requirements is reactive ion etching (RIE). High-density plasma etchings techniques, such as electron cyclotron resonance (ECR) and inductively coupled plasma (ICP) have also been reported to give relatively higher etch rate and good anisotropy. Because of these advantages, ICP etching has been replacing conventional reactive ion etching (RIE) for *GaAs* backside via etching in MMICs. ICP etching improves throughput significantly utilising faster etching rates with better control of via profile and surface morphology, repeatability and reproducibility. The surface morphology and profile of via hole are important, not only for the inductance consideration but also for the success of backside metallisation. The smooth morphology of the etched sidewalls provides reliable and good electrical contact with low resistance[5].

Etching is mainly carried out in chlorine/fluorine plasma. A number of gas combinations CCl_2F_2, CCl_2F_2/CCl_4, $SiCl_4/Cl_2$, $BCl_3/Cl_2/Ar$, Cl_2/Ar and Cl_2/BCl_3 have been utilised to fabricate via holes[6]. Each gas combination has its advantages and disadvantages. Cl_2/BCl_3 gas mixture with ICP process is being increasingly used for fabrication of via holes at high etch rates with excellent anisotropy

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and smooth surface morphology.

Generally reported etch depths using ICP/RIE for via hole etching applications in MMIC are < 200µm. In this study, the etching of 60 µm dia. via holes, up to a depth of 200 µm, in 3-inch *GaAs* wafer using RIE with CCl_2F_2/CCl_4 gases have been reported and then this developed etching process has been significantly improved for etch rate, anisotropy with much higher throughput, utilising ICP etching using Cl_2/BCl_3 gas chemistry. Moreover, this Cl_2/BCl_3 chemistry is very much suitable for etching via holes in *AlGaAs*/*GaAs* p-HEMT as these devices involve superlattice buffer layers, which are difficult to etch using fluorine-based chemistry[7].

The initial process study was carried out using less expensive, readily available in-house RIE system with CCl_2F_2/CCl_4 gas chemistry. But the gas used was CFC that is detrimental to ozone layer depletion and is already banned in many countries. Presently all the plasma processing is being carried out worldwide using non-CFC gases due to environment-friendly nature. The authors have also re-optimised and improved the etch process with ICP system using Cl_2/BCl_3 gases.

The substrate thickness was kept ~200 µm considering factors like handling of fragile wafers and electrical losses in MMIC microstrip interconnects on the frontside although it is not easy to etch 200 µm deep holes with suitable profile, good reproducibility, and repeatability. The via hole dia of 60 µm was chosen to have a properly controlled opening, on the frontside, for ensuring good electrical contact to 120 x120 μm^2 ground metal pad. The combination of CCl_2F_2 and CCl_4 gases has been chosen with RIE to derive the advantages of both gases. CCl_2F_2 is attractive because of its excellent selectivity wrt to the frontside *Ti*/*Pt*/*Au* metal pad, in addition to its lack of corrosiveness and toxicity. Higher etch selectivity is required to accommodate the over etch of substrate necessary to take care of thickness non-uniformity and etch rate variation across a 3 inch wafer. This, in turn, enhances the device yield. CCl_2F_2 alone is reported to give very low etch rates and is not suitable for deep etching[8]. CCl_4 is added to CCl_2F_2 to enhance the etch rate that provides more reactive chlorine ions readily available for etching without compromising on the easier handling of gas mixture.

This study initially aims to develop a production viable via hole RIE process using CCl_2F_2/CCl_4 gases compatible with inhouse MMIC production line. Later on this etching process was replaced with new reproducible ICP etching process using non-CFC gas chemistry (Cl_2/BCl_3) without changing existing MMIC designs and mask sets. For the implementation of ICP backside via etching process into any existing RIE etching production line, it is important to understand the impact of ICP process parameters on via profile, etch rate, mask selectivity, sidewall morphology and produce same RIE via etch profile to avoid any changes in via model and circuit design. A slight change in via etch profile would lead to change in via inductance value of grounded source pad. This change in source inductance could affect the circuit performance for higher frequency application.

Dry etching of deep anisotropic holes (~200 µm) need long etching times that are mainly limited by the type of mask used. The etching mask should have high plasma resistance to withstand the plasma conditions for long duration of etch time. The mask also plays significant role in determining the etch rate, etch depth, and surface morphology as well as the etch profile. A number of masking materials have been reported in literature, for example, photoresist, Si_3N_4, *Au*, and *Ni*. The mask choice mainly depends on its plasma resistance, selectivity, and its compatibility with the process in addition to the required etch depth and final etch profile. In this study, two kinds of masks, photoresist and *Ni*, have been used to etch *GaAs* and compared their performances in RIE environment by investigating their effect on etch rate and etch depth with time, etch profile, and surface morphology. Finally the suitable mask was utilised for ICP etching.

2. EXPERIMENTAL

The frontside of (100) oriented, 3-inch S.I. *GaAs* wafers were coated with *Ti*/*Pt*/*Au* (600 Å/300 Å /4100 Å) using e-beam deposition to simulate the frontside grounding metal pad. Then the backside of the wafers was thinned down to ~200 µm by lapping and polishing. Subsequently, the wafer back surface was smoothed and cleaned with $H_2SO_4/H_2O_2/H_2O$-based solution. This was followed by photolithographic patterning of 60 µm dia holes, using either AZ4620 photoresist or 2000 Å thick thermally evaporated *Ni*. The former was spun onto the wafer to give resist thickness of ~24 µm. A Karl Suss BSA aligner was used for lithographic patterning. The patterned photoresist was post baked at 120°C for 30 min to introduce a sloped photoresist profile with improved adhesion. An oxygen plasma descum step prior to etching was utilised in order to remove any residual photoresist in the via hole which would contribute to the roughness of the etched surface.

RIE was performed in a conventional parallel plate reactor. The wafers were placed on the lower electrode to which 13.56 MHz radio frequency power was applied. The temperature of this electrode was maintained at 30°C, using a chiller. The chamber was evacuated to a base pressure of ~8E-6 Torr by a turbomolecular pump, backed by a mechanical pump, before introducing the process gases (CCl_2F_2 and CCl_4) in the chamber. As CCl_4 is liquid at room temperature, it was vapour-transported to the chamber using N_2 gas in a bubbler. The influence of RIE process parameters like gas flow rates, pressure, and power on etch rate and etch profile were studied in detail. The flow rates of CCl_4 and CCl_2F_2 were varied using mass flow controllers, while keeping the total flow constant at 42 sccm. The process pressure was varied from 30 mTorr to 200 mTorr by an automatic throttle value. The plasma power density was varied from 0.14W/cm^2 to 0.36 W/cm^2.

ICP etching was carried out using standard load lock

ICP-RIE system. All test samples were ~200 µm thick, AZ4620 photoresist patterned wafers as in case of RIE, but mounted on 82 mm dia sapphire carrier with wax. This is due to the fact that ICP etching requires cooling of the wafer during etching, which is very difficult without carrier wafer. Plasma of etcher is inductively coupled through a coil at 13.56 MHz, with independent energy control provided by 13.56 MHz RF biasing of the wafer platen. Helium gas was used to cool backside of the wafer. The substrate temperature was set at 20 °C for all test conditions. The etch chemistry was a mixture of Cl_2/BCl_3 through mass flow controlled process gas lines. The chamber was evacuated to a base pressure of 9E-6torr, by a turbo-moleculer pump backed by a dry mechanical pump, before initiating the etch process. The etch gases mixture was introduced through an annular region at the top of chamber lid. ICP process parameters like pressure and platen power were varied in a narrow window, at constant ICP coil power, to reproduce the RIE etched 200 µm deep via profile at a relatively high etch rate.

After etching holes in *GaAs*, the photoresist and *Ni* masks were removed by cleaning in acetone and wet etching in $FeCl_3/H_2O$ solution, respectively. The etch rate, etch depth, etch profile, and surface morphology of via holes were determined by cleaving through the etched features and examining the sample under SEM, model LEO series, with the electron beam oriented normal to the cleaved surface.

3. RESULTS AND DISCUSSION

3.1 RIE Process

(a) *Effect of RIE process parameters with the photoresist mask–CCl_4/CCl_2F_2 flow rate ratio*: Figure 1 shows the effect of CCl_4 to CCl_2F_2 flow rate ratio on the *GaAs* etch rate, at a fixed pressure of 100 mTorr and total flow rate of 42 sccm. As the CCl_4 concentration increases, the etch rate increases, first, due to increase in concentration of reactive *Cl* species in the plasma and second, due to a decrease in the relative concentration of F species which in turn reduces the formation of less volatile GaF_3[9]. The formation of GaF_3 is found to be the rate-limiting step. However high *Cl* concentration results in crystallographic facet etching, due to higher chemical component of etching, which increases undercutting. Hence, etching becomes less anisotropic and leads to increased surface roughness. This is detrimental to achieving the good metal step coverage during the subsequent metallisation step. Hence CCl_4/CCl_2F_2 flow rate ratio of 0.2 was found optimal for obtaining reasonably high etch rates, good surface morphology, and anisotropic profiles.

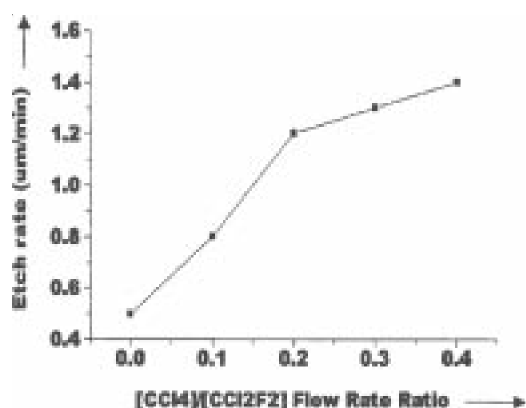


Figure 1. Etch rate variation with CCl_4 to CCl_2F_2 flow rate ratio. (Power = 200 W, Pressure = 100 mTorr).

(b) *Pressure*: Figure 2 shows the effect of pressure on the *GaAs* etch rate at fixed CCl_4/CCl_2F_2 flow rate ratio of 0.2 and 200 W power. As pressure increases, the etch rate increases due to increased density of the reactive species. But there is a fall in anisotropy at higher pressure as the mean free path of reactive species and self-bias reduces, thus decreasing the physical component of etching. Figure 2 also shows the undercut obtained for a 60 min etch corresponding to a photoresist pattern opening of 60 µm dia holes.

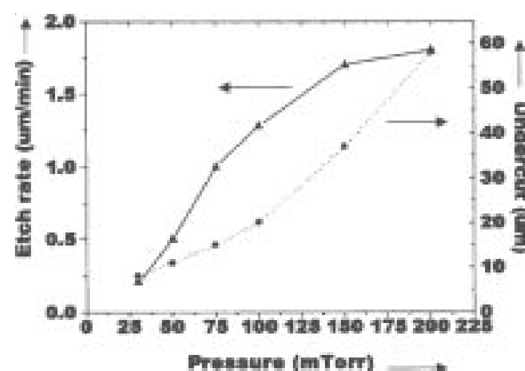


Figure 2. Etch rate variation and undercut obtained with pressure. (Power = 200 W, CCl_4 = 7 sccm, CCl_2F_2 = 35 sccm).

This clearly indicates that at higher pressures, etching tends to be isotropic. Thus, there is a trade-off between etch rate and anisotropy. At low pressure, the etch rate is low due to lower concentration of reactive species as well as due to physical sputtering of the adsorbed reactive species from the surface before they react with the *GaAs* surface.

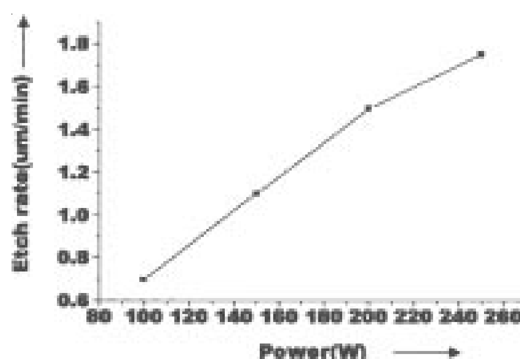
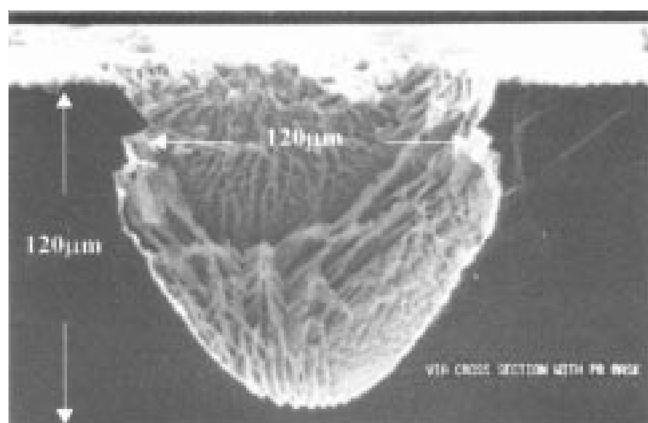


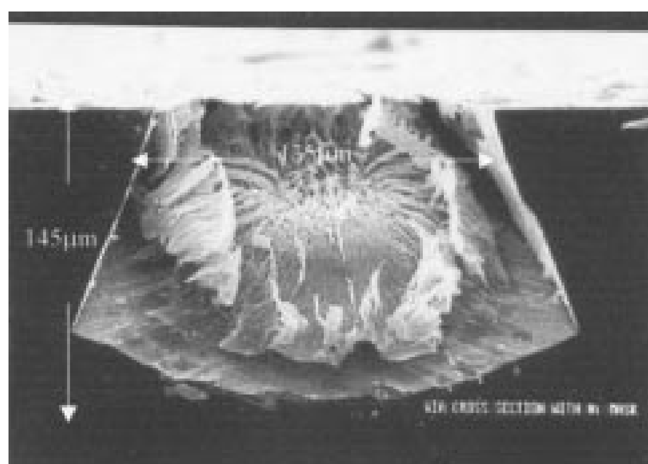
Figure 3. Etch rate variation with power. (Pressure = 100 mTorr, CCl_4 = 7 sccm, CCl_2F_2 = 35 sccm, Time = 60 min).

(c) *Power*: Figure 3 shows the variation of etch rate with power. As power increased, the etch rate increased due to the increase in self-bias and hence ion energy. This increased ion energy enhances physical etching component of etching and promotes anisotropy. Also at higher radio frequency powers, the degree of dissociation of the reactive gas molecules increased, thereby increasing the concentration of reactive species. Although anisotropy was excellent for powers > 250 W, surface morphology was getting degraded making it unsuitable for subsequent metallisation step. Also, the selectivity of the mask, which was strongly dependant on the nature of mask (photoresist and *Ni*) decreased due to higher physical etching component at higher powers.

(d) *Effect of mask*: Figures 4(a) and 4(b) show the etch profiles obtained using photoresist and *Ni* masks, respectively, for 60 μm dia opening, under identical conditions at power = 150 W, pressure = 100 mTorr, and CCl_4 =7 sccm, CCl_2F_2 = 35 sccm. These etch profiles show that at higher pressure (~100 mTorr), etching is anisotropic in nature with photoresist mask and crystallographic with *Ni* mask. This leads one to



(a)



(b)

Figure 4. SEM via cross sections: (a) with photoresist mask, (b) with *Ni* mask.

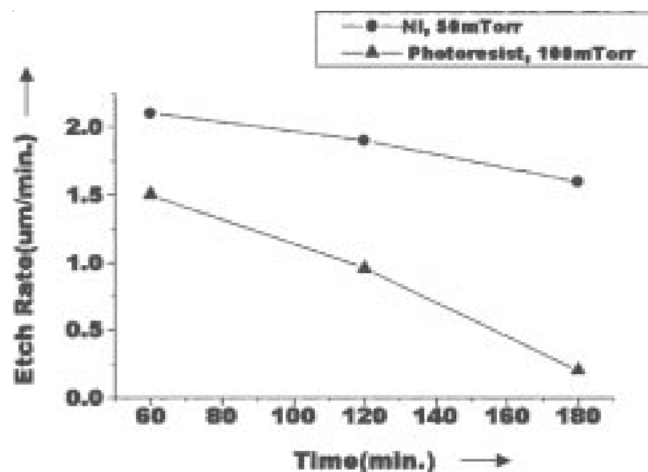


Figure 5. Etch rate variation with time. (power = 200 W, CCl_4 /CCl_2F_2 ratio = 1/5).

conclude that photoresist mask plays an important role in promoting anisotropy. Figure 5 shows the etch rate variation with time wrt photoresist and *Ni* masks at 100 mTorr and 50 mTorr process pressure, respectively, keeping other parameters constant (Power = 200 W, CCl_4/CCl_2F_2 ratio = 1/5). It is seen that for the photoresist mask etch rate reduces drastically after 120 min of etching and so it becomes very difficult to achieve etch depths > 116 μm with controlled etched profile. To achieve etch depths>116 μm with desired profile, the *Ni* mask was thus studied at lower pressure ~40-50 mTorr. At lower pressure, the mean free path increases, which enhances the physical etching component, and hence, anisotropy. It is seen that with the photoresist mask, most of the etching took place during the first 60 min with average etch rate ~1.5 μm/min. The average etch rate decreased to ~0.96 μm/min after 120 min and etching became negligible after a depth of ~116 μm, irrespective of etch time. Experiments have shown an *GaAs* average etch rate of ~3-4 μm/min without any mask. However, in the case of the *Ni* mask, there was a very small reduction in etch rate, from 2.1 μm/min for 60 min to 1.9 mm/min for 120 min. In both the cases, the etch rate decreased as depth increased because of decrease in effectiveness of supplying reactive species and removing etch by products. Less undercut was observed with the photoresist mask as compared to the *Ni* mask.

Appreciable reduction in average etch rate after 120 min. and reduced undercut with the photoresist mask indicates that the photoresist promoted anisotropy but reduced the etch rate possibly due to sputter and re-deposition on the sidewalls of the etched via. In other words, the photoresist mask causes passivation of the sidewalls, after a certain period of etch time, due to polymer deposition[10]. Hence, appreciable lateral etching takes place only in the initial stages of etching. Strawberry shaped etch profile was obtained with the photoresist mask, as

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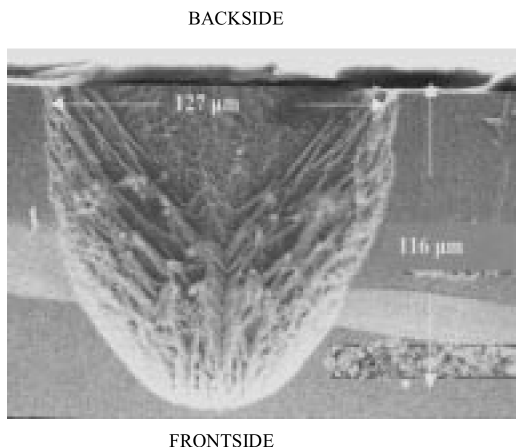


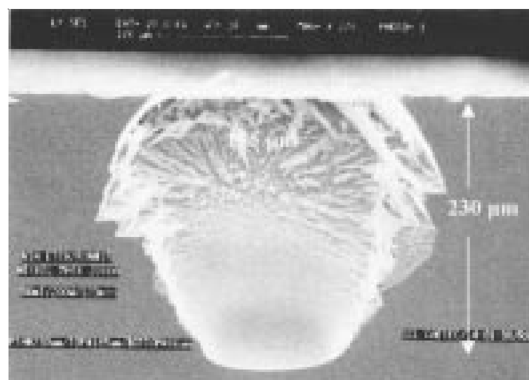
FRONTSIDE

Figure 6. SEM profile obtained with the Photoresist mask after 120 min of etching.

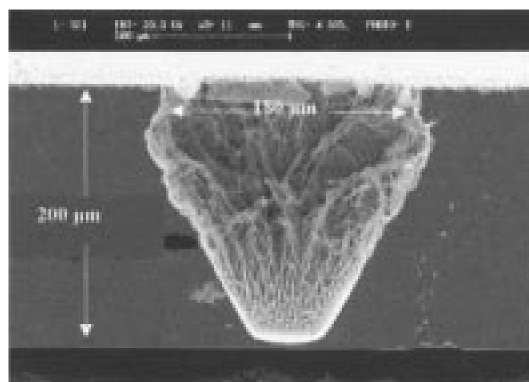
shown in Fig. 6, for etch time of 120 min at 100 mTorr process pressure. This etch profile clearly shows that RIE process with photoresist mask is suitable for etching only 100 µm deep via holes.

Figure 7(a) shows the SEM cross-section of via etched with *Ni* mask at 50 mTorr process pressure. The etch depth obtained at 50 mTorr was >200 µm but the etch profile, with a negative slope in the sidewall, was not suitable for the subsequent metallisation step. It can cause break in metal continuity. The negative slope was due to higher component of chemical etching compared to physical etching. The etch profile in the former is defined by etching along crystallographic planes of the material, which in this case was responsible for the observed sidewall slope. Also, via opening at 200 µm depth was quite high ~86 µm. To enhance anisotropy, the pressure was further reduced to 40 mTorr keeping other parameters same. The desired profile was obtained with controlled undercut as shown in Fig. 7(b) which is strawberry in shape with a top dia ~60 ± 10 µm and bottom dia ~180 ± 10 µm. The average etch rate obtained at 40 mTorr was ~1.35 µm /min for an etch depth of 200 µm. Below 40 mTorr pressure, the anisotropy was very good but the etch rate reduced significantly making deep via etching up to 200 µm depths unpractical. The surface morphology of via holes etched with the photoresist mask was better in comparison to holes etched with the *Ni* mask probably due to polymer re-deposition on the sidewalls. The best selectivity obtained with the photoresist mask for etch depth of ~100 µm was 12:1, at power 200 W, while a selectivity of >200:1 was obtained using *Ni* mask for depths >200 µm with negligible etching of *Ni* at powers up to 250 W.

It is clear from above discussion that *Ni* mask is suitable for 200 µm deep via etching using RIE process that results in very good selectivity, reproducibility, and repeatability. The optimised RIE process parameters were then implemented for etching actual, front side processed 3-inch product wafers. The etched vias were then metallised with a thin radio frequency sputtered seed layer of



(a)



(b)

Figure 7. SEM cross-section of 200 µm deep via hole with the *Ni* mask. (a) At 50 m Torr process pressure, (b) at 40 mTorr process pressure.

Ti/*Au* (1000 Å) for later electroplating. Finally, 5 µm thick film of gold was electroplated to connect the frontside pad and backside ground plane. Figure 8 shows the cross-section of plated via hole with good metal step coverage.The dc resistance measured between the top and bottom surface through the via hole was ~0.5 Ω. These via connections had a parasitic inductance ~76 pH, which is well within acceptable limits[11]. The high selectivity of this process to *Ni* and *Ti*/*Pt*/*Au* pads allowed an over etch of more than 15 % to account for the thickness non-uniformity

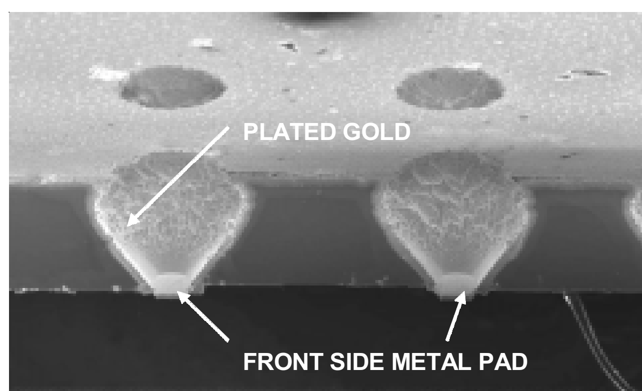


Figure 8. SEM cross-section of 200 µm deep plated via hole with good metal step coverage.

across a 3 inch wafer and to ensure that all vias are opened. The via yield obtained was > 90 % over a 3 inch *GaAs* wafer.

3.2 ICP Process

ICP etching was carried out using only photoresist mask to have less complex process with good etch surface morphology as indicated by RIE process. Process parameters like pressure and platen power were varied in a narrow window, at constant ICP coil power, to reproduce the RIE etched 200 µm deep via profile at a relatively very high etch rate. All the ICP experiments were carried out at near-maximum available coil power and Cl_2/BCl_3 flow rate ratio of 4:3 to have high plasma density[4] and increased

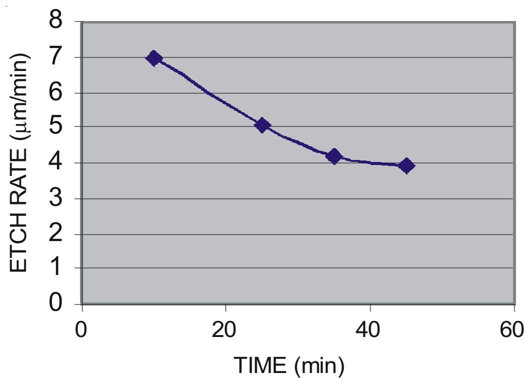


Figure 9. ICP etch rate variation with elapsed etch time. (Coil/Platen, Power = 950 W/65 W, Pressure = 30 mTorr).

concentration of reactive *Cl* species, that resulted in high etch rates with better etch surface morphology. Higher than 4:3 flow rate ratio increased the etch rate but at the cost of surface morphology, whereas lower flow rate ratio decreased the etch rate significantly.

(a) *Total etch time*: Figure 9 shows the etch rate variation with elapsed etch time for ICP process at 950W coil power, 30 mTorr pressure and 65W platen power. It clearly shows that the average etch rate is decreased with etch time, from 7 µm/min for 10 min of etching to 3.9µm/min for 45 min of etching on 3-inch wafer. This is due to increased depth, which reduces the effectiveness of supplying reactive species and removing etch byproducts. Therefore, the average etch rate achieved for 100 µm etch depths is much higher than 200 µm etch depths for same diameter holes. As reported by other groups, the authors also achieved an etch rate of > 6 µm/min for 100 µm depths using ICP process. However, the reduction in average etch rate with etch time was much less for ICP process in comparison to RIE process and etch depths of 176 µm could be achieved in just 45 min at 30 mTorr with controlled undercut. Whereas in case of RIE etch rate reduced to ~1.6 µm/min even at 50 mTorr pressure and etch depth of 95 µm could only be achieved in 60 min of etching using photoresist mask.

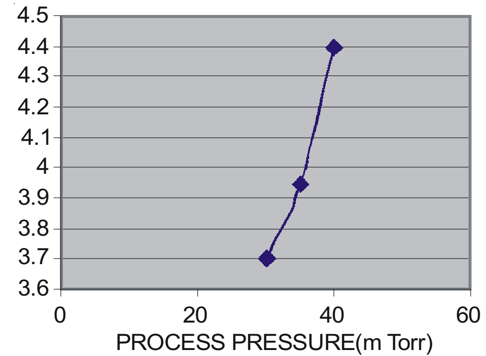


Figure 10. Etch rate as a function of process Pressure. (Coil power = 950 W, platen power = 80 W, etch time = 45 min)

(b) *Process pressure*: Figure 10 shows ICP process etch rate variation with process pressure at 950W coil power and 80W platen power for an etch time of 45 min. The authors worked around 30-40 mTorr with higher etch rate with an aim to reproduce RIE etch profile with higher etch rates. It is evident from graph that etch rate is a strong function of process pressure and is increasing with pressure due to increased density of reactive species but anisotropy is maintained mainly due to very small reduction in ion energy incident on the substrate with 10 mTorr increase in pressure. In other words, physical component of etching is fairly constant over this narrow pressure range. Etch rate is increased to 4.4 µm/min at 40 mTorr from 3.7 µm/min at 30 mTorr, for an etch time of 45 minutes, suggesting that the process is at a reaction rate limited regime in this narrow process pressure window. Figure 11 shows the SEM cross-section of via hole etched with 4.4 µm/min etch rate.

(c) *Platen power*: Figure 12 shows etch rate variation as a function of platen power. Increasing platen power to 90 W at pressure 30 mTorr resulted in reduction in etch rate to 3.6 µm/min from 3.9 µm/min at 65 W platen power for an etch time of 45 min. This reduction in etch rate in turn resulted into better etch sidewall morphology at 90W, because of the higher ion

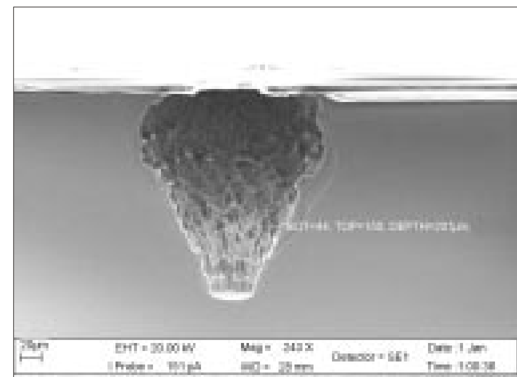


Figure 11. SEM cross-section of via-hole etched with 4.4 µm/min etch rate. (Coil power = 950 W, platen power = 80 W, etch time = 45 min)

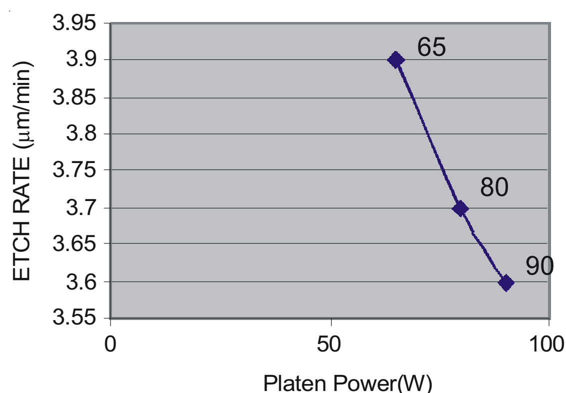


Figure 12. Etch rate as a function of platen power. (coil power = 950 W, pressure = 30 mTorr, etch time = 45 min)

bombardment that may sputter the surface evenly regardless of defects[12].

After a series of experiments, it was concluded that a process pressure of 40 mTorr with platen power of 90 W are suitable for 200 μm deep, 60 μm dia via-hole etching. This is due to the fact that etching process using these values has resulted in high etch rate with similar etched sidewall morphology as compared to RIE process. This indicates that ICP process would give better sidewall morphology in comparison to RIE process at similar etch rates. Figure 13 shows the final etch profile obtained with ICP process at 40 mTorr pressure, 950 W coil power, 90 W of platen power for an etch time of 50 min, with via etch yield of >90% on full wafer. This ICP etch profile is almost similar to the RIE profile (Fig.7 (b)) and is obtained at relatively very high etch rate of ~4 μm/min over a 3-inch wafer with uniformity and reproducibility better than 4 %. The etch selectivity obtained for 200 μm deep vias with photoresist mask using ICP process was >12:1. The etched holes were then seed metallised and gold plated to form via ground connections. Figure14 shows the SEM photomicrograph of gold plated hole from backside with good metal step coverage. The typical dc via-hole resistance measured was ~0.5 Ω and via inductance value measured was ~83 *pH* for ICP process, well within acceptable range. The slightly higher via inductance value obtained for ICP process is mainly due to marginally better anisotropy over 200 μm depth. Table. 1 shows the comparison of process parameters for the ICP and RIE processes for etching 200 μm deep via holes on 3-inch wafer with > 90 per cent via yield. The total etch time has been significantly reduced from 180 min to 50 min for ICP etching, with much simpler process using photoresist mask. Finally, this high-density plasma etching process has been integrated in production line and C-band medium power amplifiers/attenuators were fabricated with high etch rate, without changing the existing MMIC designs and mask sets.

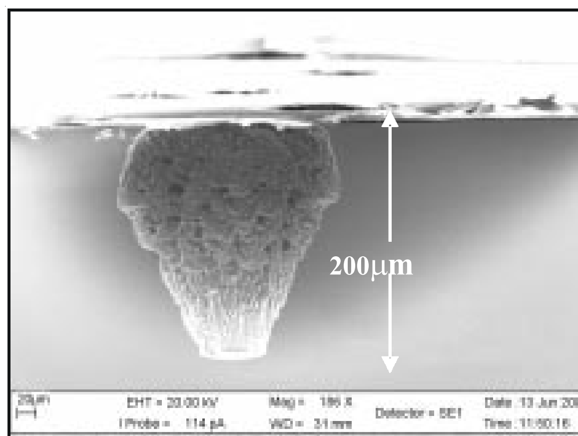


Figure 13. ICP etched via profile at 40 mTorr (coil power = 950 W, platen power = 90 W, etch time = 50 min)

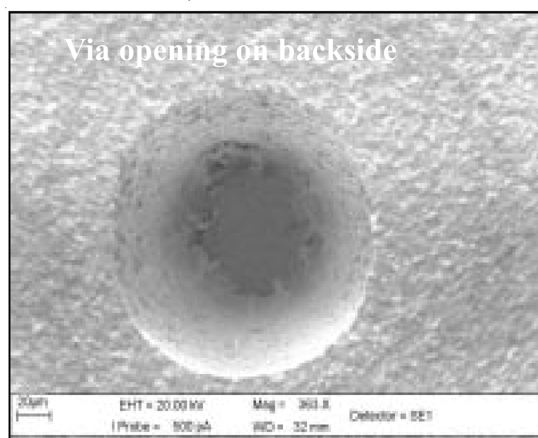


Figure 14. SEM photomicrograph of gold plated via-hole from backside.

CONCLUSIONS

The dry etching process of *GaAs* to etch 200 μm deep via holes for MMICs has been studied in detail. The

Table 1. RIE/ICP optimised process parameters for 60 μm dia, 200 μm deep via-hole etching over a 3-inch wafer

Parameter	RIE	ICP
Mask	Nickel (2000A°)	Photoresist (24 μm)
Gases	CCl_2F_2 /CCl_4	Cl_2/BCl_3
Process pressure	40 mTorr	40 mTorr
Power	200 W	950 W/90 W
Etch rate	~1.3 μm/min	~ 4 μm/min
Selectivity	>200:1	>12:1
Etch time	180 min	50 min

influence of various process parameters was studied for deep anisotropic etching of *GaAs* using RIE with CCl_4/ CCl_2F_2gases. A nickel metal mask was found suitable for achieving 200 µm etch depths with an average etch rate of ~1.3 µm/min and desired anisotropic profile. The process was successfully integrated in the production line and via grounds were fabricated with typical via resistance of ~0.5 Ω and inductance of ~76 *pH*. The device yield was enhanced due to high selectivity of this process to *Ni* and *Ti*/*Pt*/*Au* pads.

The developed RIE process used CFC gas chemistry with much lower throughput for 3-inch wafer. This existing slow etch rate RIE process was subsequently replaced by developing a high plasma density ICP process with photoresist mask, using non-CFC (Cl_2/BCl_3) gas chemistry. Desired anisotropic etch profile for 60 mm dia via hole was obtained at 40 mTorr pressure, 950 W coil power, 90 W of platen power at an etch rate of ~4 mm/min and via etch yield of >90 % over a full wafer, with very good uniformity and reproducibility. The typical dc via-hole resistance measured was ~0.5 Ω and via inductance value measured was ~83 pH well within acceptable limits. The ICP process has resulted in high etch rate with acceptable etched sidewall morphology as compared to the RIE process. Finally, this high-density plasma etching process has been integrated in production line for fabrication of MMIC's with high throughput, without affecting the production using the existing designs and mask sets.

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