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Fin Field Effect Transistors Performance in Analog and RF for High-k Dielectrics

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ABSTRACT

The high-*k* is needed to replace SiO_2 as the gate dielectric to reduce the gate leakage current. The impact of a high-*k* gate dielectric on the device short channel performance and scalability of nanoscale double gate Fin field effect transistors (FinFET) CMOS is examined by 2-D device simulations. DG FinFETs are designed with high-*k* at the high performance node of the 2008 Semiconductor Industry Association International Technology Roadmap for Semiconductors (ITRS). DG FinFET CMOS can be optimally designed to yield outstanding performance with good trade-offs between speed and power consumption as the gate length is scaled to < 10 nm. Using technology computer-aided design (TCAD) tools a 2-D FinFET device is created and the simulations are performed on it. The optimum value of threshold voltage is identified as V_T=0.653V with ε=23(ZrO_2) for the 2-D device structure. For the 2-D device structure, the leakage current has been reduced to 9.47×10^{-14} A. High-*k* improves the I_{on}/I_{off} ratio of transistors for future high-speed logic applications and also improves the storage capability.

Keywords: CMOS, FinFET, nanoscale, high-*k* gate dielectrics, multi-gate devices, high performance semiconductor devices

1. INTRODUCTION

As conventional scaling of classical CMOS is approaching technological limits, interest in non-classical double-gate and triple-gate is growing. These multi-gate devices, which can be fabricated as fin field effect transistors (FinFETs), are potentially scalable to the end of ITRS because of their ultra-thin bodies which suppress short channel effects owing to the simultaneous control of the channel by more than one gate. Here, self-aligned processes have been introduced where the FinFET concept is one of the most promising[1] FinFETs have several advantages, including better current control without requiring increased device size. FinFETs facilitate scaling of CMOS dimensions while maintaining acceptable performance[2].

Alternative dielectric materials other than silicon with a higher dielectric constant, *k*, and thus, larger physical thickness than SiO_2 are required to reduce the gate leakage current and provide high on-currents[3]. The implementation of high-*k* dielectrics to the SOI (silicon-on-insulator) FinFETs improves the scalability and saves chip area. A high-*k* dielectric material needs to provide good electrical stability, that is, the amount of charge trapped in the high-k dielectric material needs to remain at a low level even after extended operation of a transistor. It should also be scalable, that is, it should provide an acceptable level of leakage and acceptable levels of electron and hole mobility at reduced thickness. High-*k* dielectric materials satisfying these conditions may be advantageously employed for high performance semiconductor devices[1-4]. Also the larger physical thickness t_{hk} of the high-*k* dielectric reduces the parasitic gate-source/drain (G-S/D) outer fringe capacitance[5]. Using technology computer-aided design (TCAD) tools, FinFET device models and simulations can be performed to evaluate the performance of FinFETs for high performance, low operating power, and low standby power applications according to International Technology Roadmap for Semiconductors (ITRS) specifications[6]. The performance and characteristics of a FinFET device is created and the simulations are performed on it. High-*k* improves the I_{on}/I_{off} ratio of transistors for future high speed logic applications and also improves the storage capability[7].

2. NANOSCALE FIN FIELD EFFECT TRANSISTORS

The present invention relates generally to the field of semiconductor manufacturing and, more specifically, to a method for manufacturing fin field effect transistors. The push for ever increasing device densities is particularly strong in CMOS technologies, such as in the design and fabrication of field effect transistors (FETs)[8]. Scaling FETs to attain higher device density in CMOS results in degradation of performance and/or reliability[9].

The gate of the FinFET is then formed on one or more sides of the fin. FinFETs have several advantages, including

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better current control without requiring increased device size. FinFETs thus facilitate scaling of CMOS dimensions while maintaining an acceptable performance[9].

FinFET devices need to be isolated from each other, and the source and drain of individual devices need to be isolated to ensure source-to-drain decoupling. For this reason, FinFETs have been typically manufactured from silicon-on-insulator (SOI) wafers to provide isolation between the fins of different devices. The source and drains of individual FinFETs are decoupled from each other by the buried isolation layer.

In recent years, MOSFET devices have been aggressively scaled in combination with a complex design of the channel doping to avoid short channel effects. One approach to avoid gate tunnelling is the use of thicker gate oxides of different materials (high-*k* materials)[10]. Multi-gate MOSFETs have been considered one of the most attractive devices to achieve channel lengths < 20 nm. To completely control the silicon area between the gates, the silicon area must be fully depleted. Short channel effects can be avoided using very thin membranes or fins. The alignment of the gates to each other and to the implanted doping profiles is very crucial for the device performance and constitutes one of the key issues for multi-gate device manufacturing. Therefore, self-aligned processes have been introduced and FinFET devices with gate lengths down to 18 nm and a gate oxide thickness of 2.5 nm have been tested experimentally. Suppression of leakage current and reduction in device-to-device variability are key challenges for sub-45 nm CMOS technologies.

One of the most promising structures is the FinFET with a double gate that is wrapped around a narrow silicon fin, which provides robustness against short-channel effects. A thinner body allows for more aggressive gate-length scaling. Short channel effects can be avoided using very thin membranes or fins. FinFETs have several advantages, including better current control without requiring increased device size. FinFETs thus facilitate scaling of CMOS dimensions while maintaining an acceptable performance[11]. Most of the reported results that describe experiments rely on simplified two-dimensional simulations. Only few three-dimensional investigations have been performed for FinFET structures.

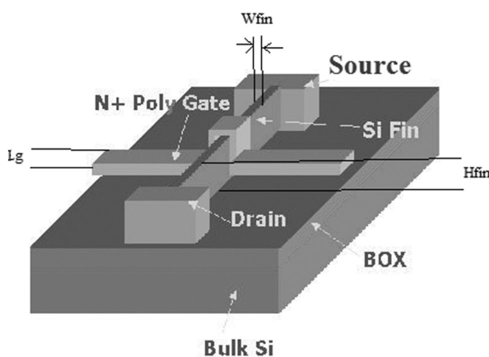

Figure 1. A double-gate FinFET device. (Wfin–fin width; Hfin–fin height; L_g–gate length)

Three-dimensional simulations are, therefore mandatory to properly predict the behaviour of such devices.

2.1 Short Channel Effects

The short channel effects occur when the magnitude of the width of the depletion region between the source and drain is equal to the channel length of the MOSFET. Short channel effect means decrease in threshold voltage as channel length decreases. As the channel length L is reduced to increase both the operation speed and the number of components per chip, short channel effect arises[12]. The short-channel effects are attributed to the following two physical phenomena:

- The limitation imposed on electron drift characteristics in the channel.
- The modification of the threshold voltage due to the shortening channel length.

3. HIGH-*K* DIELECTRICS

To fulfil the scaling scenario as projected in the International Technology Roadmap for Semiconductors (ITRS), it is widely believed that a high-*k* (high permittivity) dielectric is needed to replace SiO_2 as the CMOS gate dielectric to reduce significantly the gate leakage current. As transistors have decreased in size, the thickness of the silicon dioxide gate dielectric has steadily decreased to increase the gate capacitance, and thereby drive current and device performance. As the thickness scales below 2 nm, leakage currents due to tunneling increase drastically, leading to power consumption and reduced device reliability. Replacing the silicon dioxide gate dielectric with a high-*k* material allows increased gate capacitance without the leakage effects. The continued shrinking of the CMOS device size for higher speed and lower power consumption drives the conventional SiO_2 gate oxide approaching its thickness scaling limit[3]. Severe direct tunneling and reliability problem at extremely small thickness will set a barrier for given material. Alternative dielectric materials with a higher dielectric constant, k, and thus larger physical thickness than SiO_2 will be required to reduce the gate leakage current[9] and provide high on-currents. The implementation of high-*k* dielectrics to the SOI (silicon-on-Insulator) FinFETs improves the scalability and saves chip area. A high-*k* dielectric material needs to provide good electrical stability, that is, the amount of charge trapped in the high-*k* dielectric material needs to remain at a low level even after extended operation of a transistor. It should also be scalable, that is, provide an acceptable level of leakage and acceptable levels of electron and hole mobility at a reduced thickness. High-*k* dielectric materials satisfying these conditions may be advantageously employed for high performance semiconductor devices[13]. Different materials similarly have different abilities to hold charge. High-*k* materials, such as hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), and titanium dioxide (TiO_2) inherently have a dielectric constant or k above 3.9, the k of silicon dioxide. Materials for high-*k* gate dielectrics include ZrO_2, HfO_2, other dielectric metal oxides, alloys thereof, and their silicate alloys[14].

The dielectric between the plates passes a small amount of leakage current. The conductors and leads introduce an equivalent series resistance and the dielectric has an electric field strength limit, resulting in a breakdown. voltage Thicker gate layer might be used which can reduce the leakage current flowing through the structure as well as improving the gate dielectric reliability.

For both future silicon and emerging non-silicon nanoelectronic transistors[15,16] high-*k* gate dielectric is required for enabling continued equivalent gate oxide thickness scaling, and hence, high performance, and for controlling gate oxide leakage. In addition, high-*k* gate dielectric is required for successful demonstration of high performance logic transistors on high-mobility non-silicon substrates with high I_{ON} /I_{OFF} ratios.

3.1 Threshold Voltage

The threshold voltage V_T of a MOSFET is usually defined as the gate voltage where an inversion layer is formed at the interface between the insulating layer (oxide) and the substrate (body) of the transistor[16]. Threshold voltage is defined as the minimum voltage that is required to make the transistor ON and the drain to source (I_{ds}) current starts conducting[18]. Threshold voltage in a MOSFET is given by

$$V_T = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}$$

where q = charge of electron (1.6×10^{-19}C), $\varepsilon = \varepsilon_0 * \varepsilon_r$, ε_0 = permittivity of free space (8.854×10^{-12} F/m), ε_r = relative permittivity (3.9 for SiO_2), N_A = doping concentration, C_{ox} = oxide capacitance.

3.2 Transconductance

In field effect transistors, and MOSFETs, trans-conductance, g_m, is the change in the drain current divided by the change in the gate/source voltage with a constant drain/source voltage. Transconductance can be calculated as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\varepsilon_0 \varepsilon_r}{T_{ox}} \eta_n W/L (V_{GS} - V_T)$$

where, μ_n = mobility of electron, ε_0 = permittivity of free space(8.854×10^{-12} F/m), ε_r = relative permittivity(3.9 for SiO_2), T_{ox}=Oxide thickness, W =channel width, L =channel length, V_{GS}=gate-source voltage, V_T=threshold voltage.

3.3 Transit Frequency

Transit frequency is the frequency at which the small signal current gain of the device drops to unity while the source and drain terminals are held at ground.

Transit frequency in a MOSFET is given by

$$C_{gs} = \frac{2}{3}(WLC_{ox})$$

$$f_t = \frac{\varepsilon_0 \varepsilon_r \mu_n W}{2\pi T_{ox} L C_{gs}} (V_{gs} - V_t)$$

where, μ_n = mobility of electron ε_0 = permittivity of free space(8.854×10^{-12} F/m), ε_r = relative permittivity (3.9 for SiO_2), T_{ox}=Oxide thickness, W = channel width, L = channel length, V_{gs} = gate-source voltage, V_t = threshold voltage, C_{ox} = oxide capacitance.

4. SIMULATION AND RESULT ANALYSIS

4.1 Two-dimensional Device Creation

The 2-D device formation and simulations has been done using the Sentaurus Structure Editor of the Technology computer-aided design (TCAD) tool. Figure 2 shows the two-dimensional FinFET device.

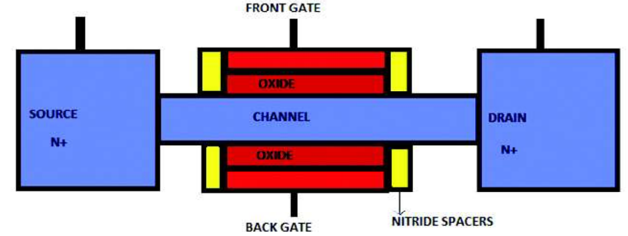

Figure 2. Two-dimensional view of the double-gate FinFET structure.

The structure consists of two gates, gate 1 and gate 2 and also two fins. The simulations were done for gate voltage values of 0.1, 0.2, 0.5, 0.9, 1.0, 1.5, and 2.0 and also for gate dielectric values of 3.9, 7.8,10, and 23.The drain voltage V_{ds} was kept constant at 2v and the $I_d V_g$ curve was obtained. The $I_d V_g$ curve was obtained using Inspect tool.

4.2 Drain Leakage Current

Even though a transistor is logically turned off, there is a non-zero leakage current through the channel at the microscopic level. This current is known as the sub-threshold leakage because it occurs when the gate voltage is below its threshold voltage. Figure 3 shows the variation in drain leakage current with increasing dielectric value and various gate voltages. It is shown that the leakage current is low for high dielectric value, that is, for ε=23(ZrO_2), the sub-threshold leakage current increases dramatically for low threshold devices. A high threshold voltage in the standby mode gives low leakage current (I_{off}).

4.3 Threshold Voltage

Figure 4 shows the variation in threshold voltage (V_T) with increasing dielectric value and various gate voltages. It is shown that the threshold voltage is high for high dielectric value that is for ε=23 (ZrO_2). The optimum threshold voltage is identified as 0.65V. A high threshold voltages in the standby mode gives low leakage current (I_{off}).

4.4 Transconductance

Transit frequency is the frequency at which the small signal current gain of the device drops to unity while the source and drain terminals are held at ground. Figure 5 shows the variation transconductance (g_m) with increasing dielectric value and various gate voltages.

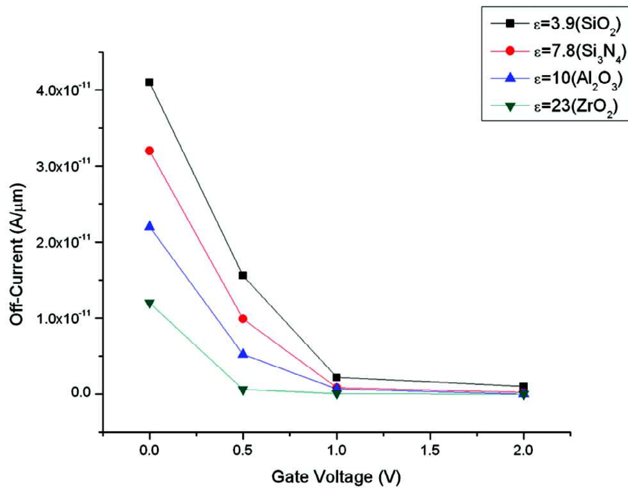

Figure 3. Variation of drain leakage current with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

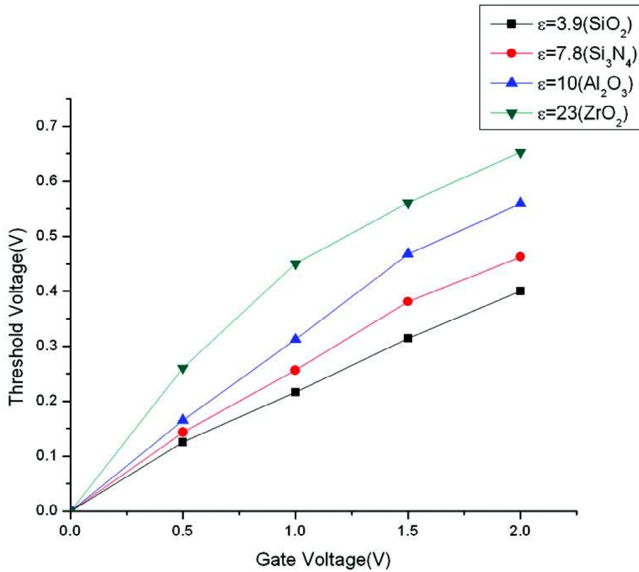

Figure 4. Variation of threshold voltage with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

It is shown that the transit frequency is high for high dielectric value, that is, for ε=23 (ZrO_2), the optimum frequency obtained is 50 MHz.

4.5 Transit Frequency

Transit frequency is the frequency at which the small signal current gain of the device drops to unity while the source and drain terminals are held at ground. Figure 6 shows the variation in transit frequency with increasing dielectric value and various gate voltages. It is shown that the transit frequency is high for high dielectric value that is for ε=23 (ZrO_2), the optimum frequency obtained is 50 MHz.

4.6 Gate Capacitance

Plot shows the variation in transit Gate capacitance (C_g) with increasing dielectric value. It is shown that the

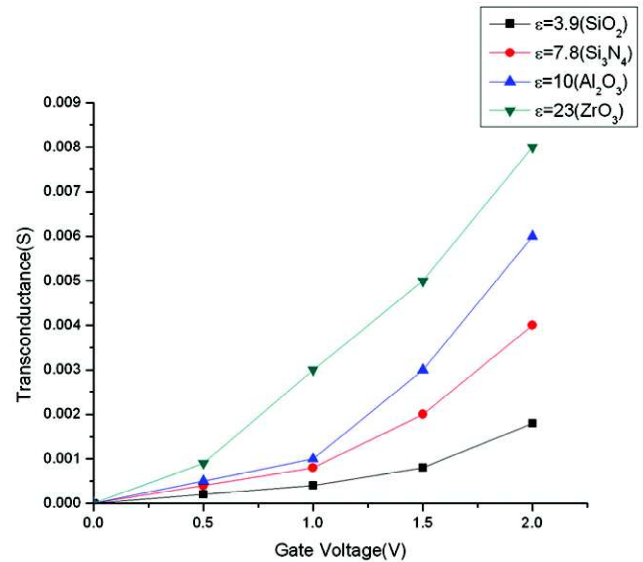

Figure 5. Variation of transconductance with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

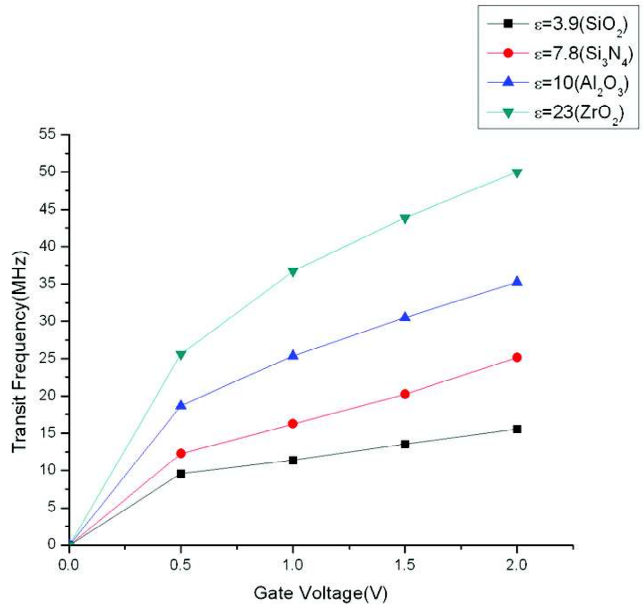

Figure 6. Variation of transit frequency with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

gate capacitance is high for high dielectric value that is for ε=23 (ZrO_2).

4.7 Channel Resistance

Figure 8 shows the variation in channel resistance with increasing dielectric value. It is shown that the channel resistance is low for high dielectric value, that is, for ε=23(ZrO_2).

4.8 Gate Delay

Figure 9 shows the variation in gate delay (T_d) with increasing gate voltage. The optimum gate delay obtained

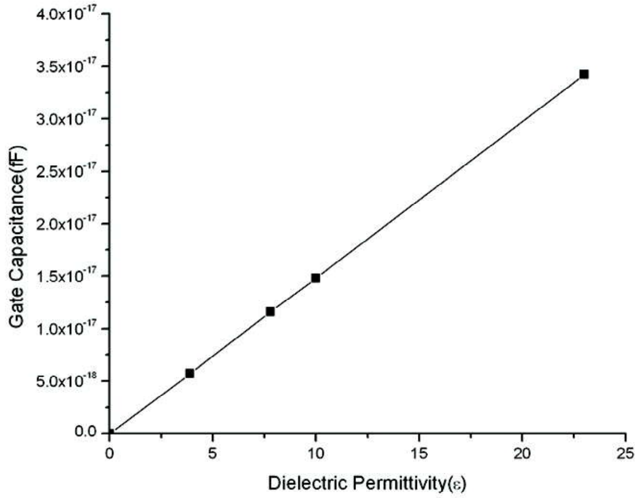

Figure 7. Variation of gate capacitance with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0V).

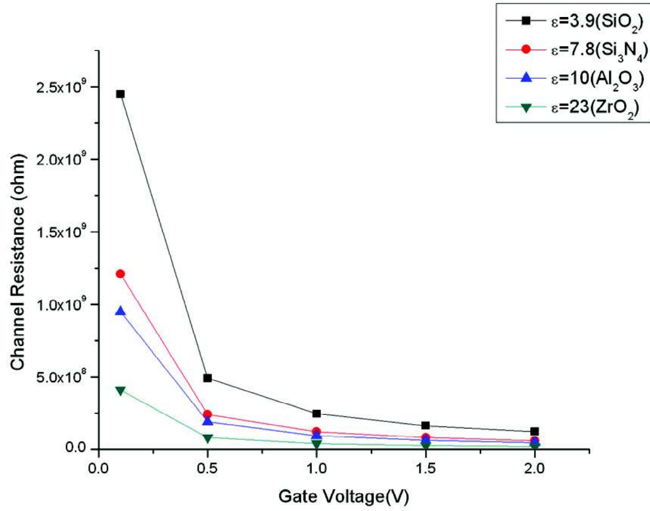

Figure 8. Variation of channel resistance with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

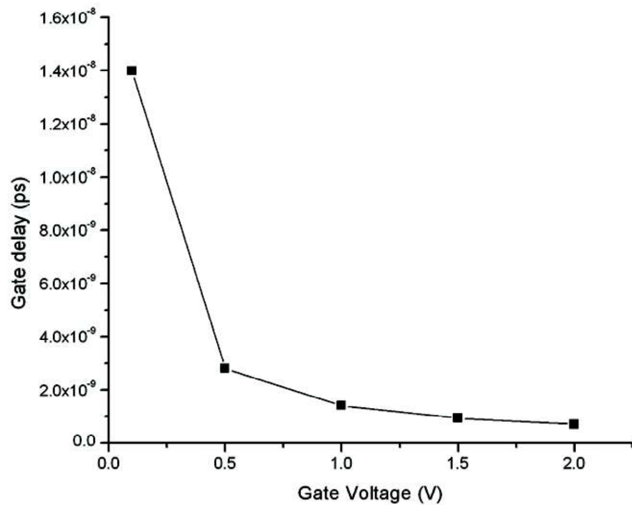

Figure 9. Variation of gate delay with increasing dielectric constant and gate voltage (0.1 V, 0.5 V, 1.0 V, 1.5 V and 2.0) V.

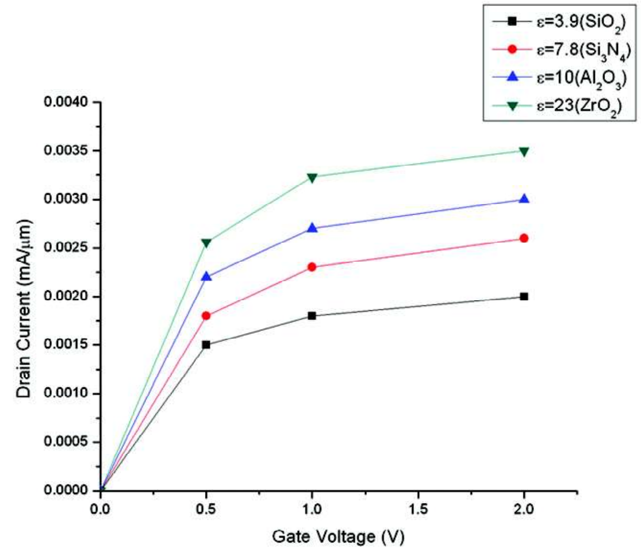

Figure 10. Variation of drain current with increasing dielectric constant and gate voltage (0.5 V, 1.0 V, 1.5 V and 2.0 V).

is 7.0183×10^{-10} ps.

It is shown that the drain current is also high for high dielectric value, that is, for ε=23(ZrO_2).The optimum value of drain current obtained is 0.0035 mA/μm. High-*k* gate dielectrics enhance CMOS scalability as well as storage capability using NAND gate[19] which make it suitable for high speed applications.

5. CONCLUSIONS

Using Technology Computer-Aided Design (TCAD) tools, 2-D device models and simulations can be performed to evaluate the performance of the FinFETs. The optimum value of threshold voltage is identified as V_T = 0.653V with ε=23(ZrO_2) for the 2-D device structure. For the FinFET device the leakage current has been reduced to 9.47×10^{-14} A whereas for ε=23 (ZrO_2). High-*k* gate dielectrics enhance CMOS scalability as well as storage capability which make it suitable for high-speed applications. The gate length of the device has to be scaled down to control the parasitic capacitances and the fin thickness is reduced to suppress the short channel effects (SCEs).

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