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Design of Capacitor Array in 16-Bit Ultra High Precision SAR ADC for the Wearable Electronics Application

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ABSTRACT This paper proposes a 16-bit 6-channel high-voltage successive approximation register (SAR) ADC with an optimized 5 + 5 + 6 segmented capacitor array. The lower 10 bits of the capacitor array are all composed of unit capacitors without any calibration unit. Without calibration, the lower 10 bits of the capacitor array can ensure 10-bit conversion accuracy. Every of the upper 6 bits of the capacitor array contains a linearity calibration unit. The linearity error of the upper 6 bits is calibrated by the linearity calibration unit. The 16-bit is manufactured by a 0.6μm standard COMS process, and the total chip area of 6-channel ADC including pads is 6.6mm × 6.6mm. As for single channel SAR ADC, the area is 0.9mm × 2.0mm. The measurement results show that the effective conversion accuracy of the SAR ADC reaches 13 bits by using novel differential nonlinearity (DNL) and integral nonlinearity (INL) calibration methods. The power is 80mW, corresponding to a Figure of Merit (FOM) of 48 pJ/conv.-step.

INDEX TERMS Segmented capacitor array, SAR ADC, linearity error, calibration.

I. INTRODUCTION

For the wearable electronic devices, low power consumption is its core indicator [1], [2]. Therefore, for its core chips, they all have lower power consumption requirements. As a typical representative of low-power Analog-to-Digital Converters (ADCs), SAR (successive approximation register) capacitor array units have been widely used in the core chips of many wearable electronic devices [3]–[5]. Due to the safety requirements of the wearable device, the analog signals mostly fluctuate within a small range, so the minimum resolution voltage will be significantly lower than that of ordinary application environments. For the core ADC chip, a higher number of conversion bits is required to meet the specification requirements.

SAR ADC is the core of low-power products in wearable devices. Its accuracy is mainly determined by the internal SAR capacitor array. Because the capacitor array is composed of capacitors, its static power consumption is negligible. Because the main working principle of the SAR ADC is: first use charge to scale, and then use the comparator and digital logic unit to perform the bisection [6]. As a result, it can achieve a resolution of more than 16 bits under a medium conversion rate. Therefore, for the current field of

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wearable devices, the analog-to-digital converters in low-power, high-precision applications are mostly designed using SAR-type capacitor array [7], [8].

The biggest challenge lies in the high resolution SAR ADC is the mismatch of capacitor array. Techniques to compensate for the mismatch in SAR converters appeared in the open literature. They mainly belong to the following three categories: foreground calibration, background calibration and averaging. Foreground methods measure the bit weights during calibration and fix bit weight errors in digital domain during normal operation [9]. Recently, the rapid advancement of digital technology motivates the use of digital techniques especially for background algorithms. Background calibration corrects the error during the normal operation, which exists the possibility of non-convergence [10]. Averaging deal with the mismatch errors by performing multiple conversions of the same sample [11]. A novel mismatch calibration method is proposed in this work. The measurement results show that the effective conversion accuracy of the SAR ADC reaches 13 bits.

II. OVERALL FUNCTION

The typical block diagram of the SAR ADC is shown in Fig. 1. The conversion accuracy of the SAR ADC is mainly determined by the SAR capacitor array [12]. The classic capacitor array of an N-bit SAR ADC is shown in Fig. 2.

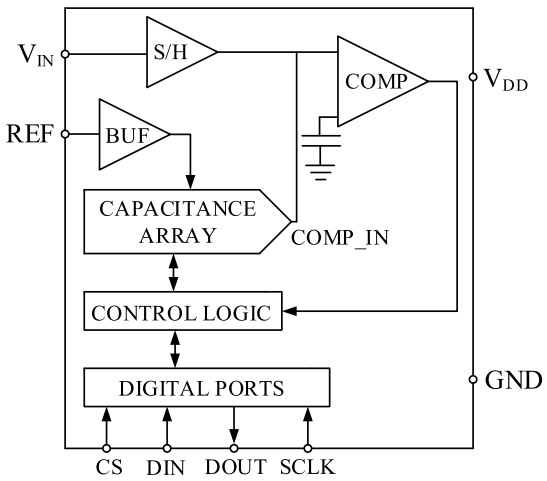

FIGURE 1. The block diagram of SAR ADC.

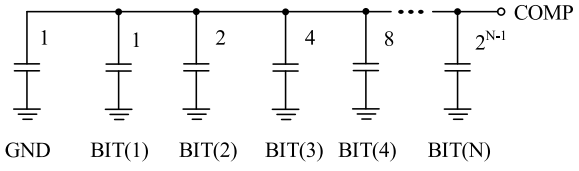

FIGURE 2. Classic capacitor array of N-bit SAR ADC.

It can be seen from Fig. 2 that for the 16-bit ADC, the total number of unit capacitors is $2^{16} = 65536$, and the layout area is too large to achieve. Set the number of unit capacitors used in the N-th weight capacitor to Num(N). According to the basic principles of SAR ADC, for any M bits, when the minimum unit capacitor is used, the following formulas are used [13]:

$$Num\,(M) = 2^{M-1} \tag{1}$$

$$S\,(M-1) = Num\,(1) + Num\,(2) + \cdots + Num\,(M-1) \tag{2}$$

$$S\,(M-1)\,/Num\,(M) = \left(2^{M-1}-1\right)/2^{M-1} \tag{3}$$

Here, $S(M-1)$ represents the summation of all of the lower-bit capacitors before the M-th weight capacitor. For example, considering the 4-th weight capacitor (M = 4), Num(4) = 8, the summation of all of the previous capacitors before the 4-th weight capacitor is: S(3) = Num(1) + Num(2) + Num(3) = 1 + 2 + 4 = 7, finally, which satisfied the Equation (3). In general, in order to meet the N-bit conversion accuracy requirements, the number of unit capacitors applied to any N bits of the capacitor array must satisfy the above formula. Therefore, for a capacitor array with a precision of more than 16 bits, on the premise of satisfying the above formula, a 5 + 5 + 6 segmented capacitor array structure can be applied, as shown in Fig. 3. The number of unit capacitors is $2^7 = 128$.

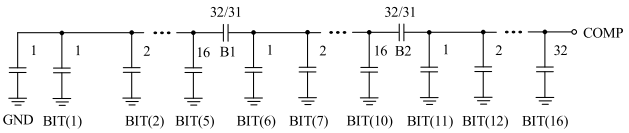

FIGURE 3. 16-bit capacitor array.

As shown in Fig. 3, in order to meet the requirements of Equation (3), the bridge capacitances B1 and B2 must be 32/31 times the size of the unit capacitor, so set B1 and B2 to 32/31.

For the SAR capacitor array shown in Fig. 3, to ensure that the capacitor array meets the 16-bit conversion accuracy, it is necessary to ensure that the relative error of all capacitors is less than $1/2^{16}$. By consulting the current major IC foundry, it can be known that the current natural matching accuracy of the capacitor is about 10 bits, that is, the relative error of the capacitor is larger than $1/2^{10}$, and all capacitors are required to be unit capacitors. If there is a non-unit capacitor in the capacitor array, the matching accuracy will be much lower.

In summary, although the SAR capacitor array shown in Fig. 3 can solve the problem of the excessive layout area, due to the limitation of the manufacture, its conversion accuracy will be far below 10 bits. Therefore, in order to meet the performance requirements of 16-bit ADC, it is necessary to optimize the design of the schematic shown in Fig. 3.

At present, the IC foundries can ensure capacitor units with a natural matching accuracy of about 10 bits. Therefore, if all the capacitors in BIT(1)~BIT(10) are composed of unit capacitors, there is no need to introduce any calibrations for

the lower 10-bit capacitor array. As can be seen from Fig. 3, in the lower 10-bit capacitor array, only the bridge capacitor B1 is not a unit capacitor. Therefore, in this work, the capacitor B1 is firstly normalized to a unit capacitor, so that the lower 10-bit capacitors are composed of unit capacitors, and the calibration range of the SAR capacitor array is minimized.

According to the basic working principle of SAR ADC and the requirements of Equation (3), for the weight capacitor of BIT(1)∼BIT(5), the weight value is $1/2^{6-M}$(M = 1, 2, 3, 4, 5). Therefore, on the premise of satisfying the above weight relationship, by optimizing part of the circuit so that the bridge capacitor B1 in Fig. 3 also becomes a unit capacitor, then the BIT(1)∼BIT(10) bits of the weighted capacitor are all composed of unit capacitors. This meets the capacitor production conditions of IC foundry, making the natural conversion accuracy of the BIT(1)∼BIT(10) meet the 10-bit requirement. According to the above analysis, the optimization schematic diagram of the capacitor array in this work is shown in Fig. 4.

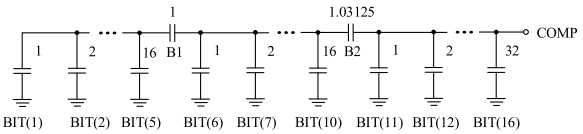

FIGURE 4. The optimization schematic diagram of capacitor array.

In Fig. 4, it can be easily obtained that the BIT(1)∼BIT(5) bits meet the requirements of Equation (3). In the capacitor array shown in Fig. 4, the main transition point is the bridge capacitors B1 and B2. Therefore, the equivalent capacitance analysis is mainly performed on the above two points. The bridge capacitor B1 is a unit capacitor, so the equivalent total capacitance of BIT(1)∼BIT(5) and capacitor B1 is equal to 31/32. Therefore, BIT(1)∼BIT(6) meet the requirements of Equation (3). For BIT(1)∼BIT(10), it can also be easily obtained that BIT(1)∼BIT(10) meet the requirements of Equation (3).

As shown in Fig. 4, the total equivalent capacitance of the BIT(1)∼BIT(10) bits is 31 + 31/32, and the weight capacitance of the BIT(11) is 1. Therefore, in order to meet the requirements of Equation (3), the size of capacitor B2 needs to satisfy the formula:

$$(31 + 31/32) \times B2/\left((31 + 31/32) + B2\right) = 1023/1024 \tag{4}$$

From Equation (4), we can get $B2 = 1.03125$. It can be easily derived from Equation (4) and Equation (3): BIT(1)∼BIT(11) meet the requirement of Equation (3). When BIT(11) meets the requirement of Equation (3), it can be concluded that BIT(1)∼BIT(16) all meet the requirements of Equation (3).

In order to prove that these two capacitor arrays in Fig. 3 and Fig. 4 work similarly during the comparison period, law of conservation of electric charge is used to transform these two segmented capacitor arrays to normal binary capacitor arrays. A voltage excitation Vref is connected to the BIT(5) in the conventional 16-bit capacitor array shown in Fig. 5, the remaining capacitors are connected to the ground.

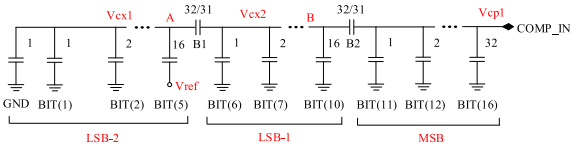

FIGURE 5. A voltage excitation on the BIT(5) in the conventional 16-bit capacitor array..

According to the conservation of electric charge in the node A:

$$\left(V_{cx1} - V_{ref}\right) \times 16 + V_{cx1} \times 16 + (V_{cx1} - V_{cx2}) \times B1 = 0 \tag{5}$$

Based on Equation (5), the value of voltage in the node A is

$$V_{cx1} = \frac{V_{ref} \times 16 + V_{cx2} \times B1}{B1 + 32} \tag{6}$$

The charge stored in the capacitor array LSB−2 is equivalent to the charge stored in the bridge capacitor B1. Therefore, the charge Q_{c1} stored in the bridge capacitor B1 is

$$\begin{aligned} Q_{c1} &= (V_{cx2} - V_{cx1}) \times B1 \\ &= \left(V_{cx2} - \frac{V_{ref} \times 16 + V_{cx2} \times \frac{32}{31}}{\frac{32}{31} + 32}\right) \times \frac{32}{31} \\ &= V_{cx2} - \frac{1}{2} V_{ref} \end{aligned} \tag{7}$$

According to the conservation of electric charge in the node B:

$$(V_{cx2} - V_{cx1}) \times B1 + V_{cx2} \times 31 + \left(V_{cx2} - V_{cp1}\right) \times B2 = 0 \tag{8}$$

Based on Equation (8), the value of voltage in the node B is

$$V_{cx2} = \frac{V_{cx1} \times B1 + V_{cp1} \times B2}{B1 + 31 + B2} \tag{9}$$

The charge stored in the capacitor array LSB−2 and LSB−1 is equivalent to the charge stored in the bridge capacitor B2. Therefore, the charge Q_{c2} stored in the bridge capacitor B2 is

$$\begin{aligned} Q_{c2} &= \left(V_{cp1} - V_{cx2}\right) \times B2 \\ &= \left(V_{cp1} - \frac{V_{cx1} \times \frac{32}{31} + V_{cp1} \times \frac{32}{31}}{\frac{32}{31} + 31 + \frac{32}{31}}\right) \times \frac{32}{31} \\ &= \left(V_{cp1} - \frac{V_{ref} \times \frac{1}{2} + V_{cp1} \times \frac{32}{31}}{\frac{32}{31} + 32}\right) \times \frac{32}{31} \\ &= V_{cp1} - \frac{1}{64} V_{ref} \end{aligned} \tag{10}$$

Therefore, the total charge Q_{ctot1} stored in the capacitor array in Fig. 5 is

$$Q_{ctot1} = Q_{c2} + V_{cp1} \times 63 = V_{cp1} \times 64 - \frac{1}{64} V_{ref} \quad (11)$$

Assume that C_{ilsb2} (i=1,2,3,4,5) represents the capacitor connected to Vref in the LSB−2 capacitor array, then Equation (11) can be rewritten as:

$$Q_{ctot1} = Q_{c2} + V_{cp1} \times 63 = V_{cp1} \times 64 - \frac{C_{ilsb2}}{2^{10}} V_{ref} \quad (12)$$

A voltage excitation Vref is connected to the BIT(10) in the conventional 16-bit capacitor array shown in Fig. 6, the remaining capacitors are connected to the ground.

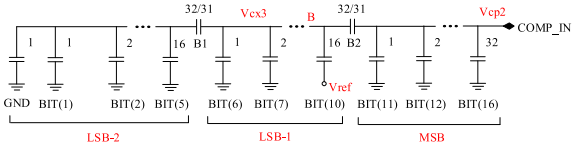

FIGURE 6. Voltage excitation on the BIT(10) in the conventional 16-bit capacitor array..

According to the conservation of electric charge in the node B:

$$V_{cx3} \times (B1||32) + V_{cx3} \times 15 + (V_{cx3} - V_{ref}) \times 16 + (V_{cx3} - V_{cp2}) \times B2 = 0 \quad (13)$$

Based on Equation (13), the value of voltage in the node B is

$$V_{cx3} = \frac{V_{ref} \times 16 + V_{cp2} \times B2}{B2 + 32} \quad (14)$$

The charge stored in the capacitor array LSB−2 and LSB−1 is equivalent to the charge stored in the bridge capacitor B2. Therefore, the charge Q_{c3} stored in the bridge capacitor B2 is

$$\begin{aligned} Q_{c3} &= (V_{cp2} - V_{cx3}) \times B2 \\ &= \left(V_{cp2} - \frac{V_{ref} \times 16 + V_{cp2} \times \frac{32}{31}}{32 + \frac{32}{31}} \right) \times \frac{32}{31} \\ &= V_{cp2} - \frac{1}{2} V_{ref} \end{aligned} \quad (15)$$

Therefore, the total charge Q_{ctot2} stored in the capacitor array in Fig. 6 is

$$Q_{ctot2} = Q_{c3} + V_{cp2} \times 63 = V_{cp2} \times 64 - \frac{1}{2} V_{ref} \quad (16)$$

Assume that C_{ilsb1} (i = 1,2,3,4,5) represents the capacitor connected to V_{ref} in the LSB−1 capacitor array, then Equation (16) can be rewritten as

$$Q_{ctot2} = V_{cp2} \times 64 - \frac{C_{ilsb1}}{2^5} V_{ref} \quad (17)$$

Comparing Equation (12) and Equation (17), the equivalent binary capacitor array shown in Fig. 7 can be derived from the segmented capacitor array in Fig. 3.

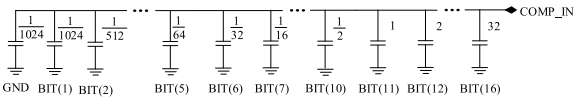

FIGURE 7. The equivalent capacitor array of the conventional 16-bit capacitor array..

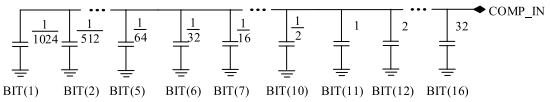

FIGURE 8. The equivalent capacitor array of the optimization capacitor array..

Based on the detailed analysis above, Fig. 8 may be regarded as the equivalent binary capacitor array of the optimization capacitor array in Fig.4.

Compared these two equivalent capacitor arrays (Fig. 7 and Fig. 8), the capacitors all meet the binary relationship. Therefore, these two capacitor array work similarly during the conversion period.

It can be seen from the above that the BIT(1)∼BIT(16) bits can satisfy the Equation (3), and the bridge capacitor B1 has been normalized to a unit capacitor. Therefore, when all the capacitors used in the BIT(1)∼BIT(10) bits are composed of unit capacitors, the lower 10-bit capacitor array can meet the linear capacitor production conditions of the IC foundry. Therefore, for the BIT(1)∼BIT(10) bits, the schematic diagram shown in Fig. 4 can ensure that the natural conversion accuracy is not lower than 10 bits without introducing any calibrations.

In summary, for the BIT(1)∼BIT(10) bits, because they are all composed of unit capacitance, there is no need to introduce any calibrations. However, the bridge capacitor B2 is a non-unit capacitor, so after manufacturing, capacitor B2 usually has a large error, which is equivalent to introducing a mismatch of the BIT(11)∼BIT(16) capacitors. The mismatch introduced by the bridge capacitor B2 will directly reduce the DNL and INL of the ADC. In order to meet the 16-bit conversion accuracy requirements of the ADC, calibration units of BIT(11)∼BIT(16) capacitors are introduced, as shown in Fig. 9.

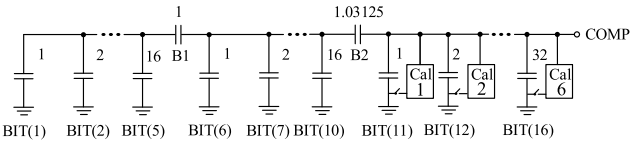

FIGURE 9. The capacitor array with calibration units.

As shown in Fig. 9, the IC foundry can only provide 10-bit matching accuracy, and the bridge capacitor B2 is a non-unit capacitor. The weight capacitors of BIT(11)∼BIT(16) will have an obvious mismatch, and the Cal(N) unit will compensate for the mismatch of the corresponding capacitor.

It can be seen from Fig. 9 that the weight of BIT(11) is 1024LSB, so in order to meet the 16-bit accuracy requirement, the minimum trimming step of DNL should be set to 0.5LSB. According to the basic principle of the AD converter, the corresponding capacitance of 0.5LSB should be $0.5C/1024 = 1C/2048$. Suppose Cal1's trim steps are 0.5LSB and 1LSB, and CalN's trim steps are 0.5LSB, 1LSB, $\cdots$, 2^NLSB. Therefore, the corresponding trimming capacitance of CalN is 1C/2048, $2^1C/2048$, $\cdots$, $2^NC/2048$. The circuit diagram is shown in Fig. 10.

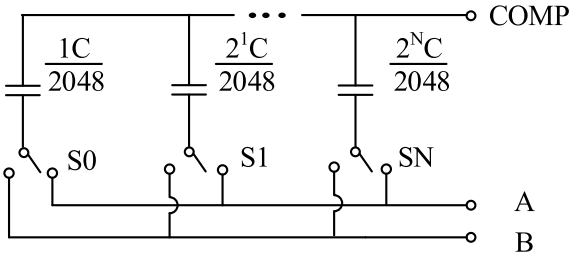

FIGURE 10. The circuit diagram of calibration unit.

In the actual design, the N value in the Cal1 unit is 4. Therefore, the minimum trimming step of the Cal1 unit is 0.5LSB, and the maximum trimming step is 16LSB. By analogy, N in the Cal6 unit is 9. The minimum calibration step of the CalN unit is 0.5LSB, and the maximum trimming step is 512LSB.

As can be seen from Fig. 9 and Fig. 10, even if the foundry can only provide 10-bit matching accuracy, the SAR capacitor array in this work can also ensure that the BIT(1)∼BIT(10) bits have 10-bit matching accuracy. For the BIT(11)∼BIT(16) bits, the mismatch caused by process and bridge capacitor B2 can be calibrated by the calibration unit.

The conversion performance of SAR ADC is usually characterized by two specifications. One is the DNL error, which is defined as the maximum difference between two adjacent codes. This parameter can characterize the linearity of the ADC in a small range; the other is the INL error, which is defined as the maximum deviation of the entire input range from the theoretical curve. INL can be simply expressed as the superposition of all DNL. This parameter can characterize the linearity of the ADC in the full-scale range.

For the current IC foundries, in order to meet the 10-bit capacitor matching accuracy requirements, the size of the single capacitor must be greater than a certain value, and the smaller the layout area of the capacitor array, the better the matching. Otherwise, the gradient effect of the process will cause a gradient mismatch of all capacitors, which usually affects the INL of the final circuit.

During calibration, when the weighted capacitors of the BIT(11)∼BIT(16) bits of the final circuit are calibrated, the theoretical deviation of DNL can be less than 1LSB, so the schematic shown in Fig. 9 can guarantee the DNL performance. However, even if the circuit structure shown in Fig. 9 is used, its overall capacitance still needs at least 64. In order to achieve the best matching accuracy of the process, the overall layout area of the capacitor array may exceed the minimum span area of the linear capacitance of the foundry, resulting in the INL error. Therefore, this paper will introduce an INL calibration method, which can achieve the INL calibration of the final circuit.

By testing multiple high-precision ADCs and statistically analyzing their INL curves, it can be concluded that when the DNL value is adjusted to the minimum, there are three main types of INL waveforms for 16-bit ADCs. The theoretical models are shown in Fig. 11.

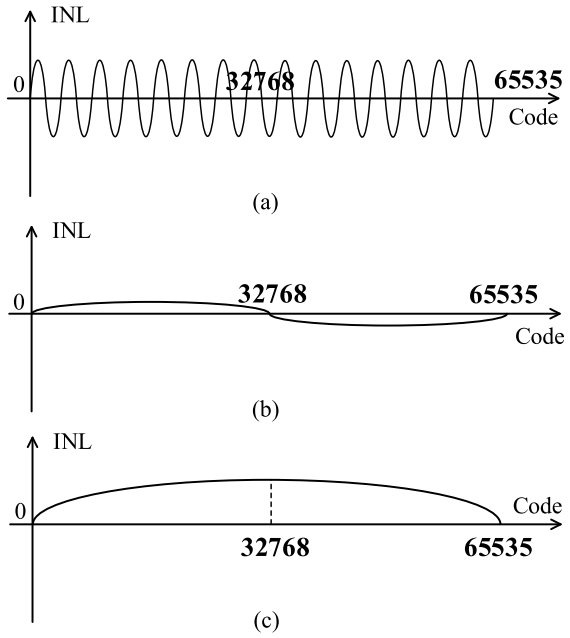

FIGURE 11. Typical theoretical models of INL: (a)model 1. (b)model 2. (c)model 3.

The three cases in Fig. 11 represent three typical INL measurement results, it is possible that there are other results other than these three cases in Fig. 11. As for Fig. 11(a), the error is evenly distributed among all of the codes, which will not lead large error in general. The curve in Fig. 11(c) is a second order curve, the central idea in this design is to produce an opposite second order curve to counteract the error. The curve in Fig. 11(b) can be regarded as two second order curves symmetrical about the midpoint. Its calibration can be similar as Fig. 11(c). We can generate two opposite second order curves to cancel the error. Finally, in this work, we focus on the case in Fig. 11(c).

In Fig. 11(a), the INL waveform indicates that INL is mainly caused by the overall DNL, and the peak value of INL is slightly larger than the maximum value of DNL; as shown in Fig. 11(b), the INL is caused by its own nonlinearity, and there will not be a large difference between the INL and the maximum value of DNL. The INL calibration method required for this model is more complicated and the required area is too large; the INL waveform shown in Fig. 11(c) indicates that the INL is caused by its own nonlinearity, and

the INL value may significantly exceed the maximum value of DNL. The area required by the INL calibration method is small.

The 16-bit ADC in this work is limited by the area, so we only calibrate the INL shown in Fig. 11(c). If the remaining two INL models appear, the INL calibration will not be performed. After normalizing the INL curve shown in Fig. 7(c), its maximum INL offset point is at 1/2 range, and the INL value of its first and last points is 0. The overall INL curve can be equivalent to a second-order parabola. This paper proposes a new INL calibration scheme. The capacitor array shown in Fig. 9 is regarded as the main capacitor array, and an additional independent INL calibration sub-capacitor array is added. The final SAR type capacitor array is shown in Fig. 12.

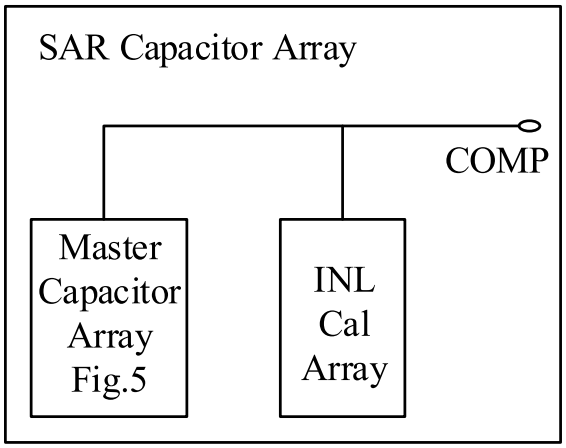

FIGURE 12. Schematic diagram of SAR capacitor array with INL calibration array..

The COMP terminal is the input port of the comparator. The main function of INL-Cal-Array is to make the INL calibration circuit shown in Fig. 13(a) generate a nonlinear voltage through a certain digital algorithm. This nonlinear voltage is also a parabola, and its peak voltage is the same as that in Fig. 11(c), but the opening direction is opposite to it. The theoretical model of this voltage is shown in Fig. 13(b).

From the analysis in Fig. 9, we can see that the corresponding capacitance value of 1LSB should be 1C/1024. Therefore, in order to meet the requirement of 16-bit conversion accuracy, the minimum trimming step of INL is set to 1LSB in this work. The trimming steps of the INL-Cal-Array calibration array are 1LSB, 2LSB, 3LSB, and 4LSB respectively; so the corresponding capacitances are 1C/1024, 2C/1024, 3C/1024, and 4C/1024, respectively.

The working principle of the INL-Cal-Array unit is that when the calibration starts, the weight switches S1∼S4 of the unit are grounded. At this time, the voltage generated by the INL-Cal-Array at the COMP terminal is a DC voltage of 0V. Fig. 13(b) is the second-order parabola, and the abscissa X represents the input codeword (range 0∼65535). The ordinate Y indicates the value of INL, and the highest value is 5LSB.

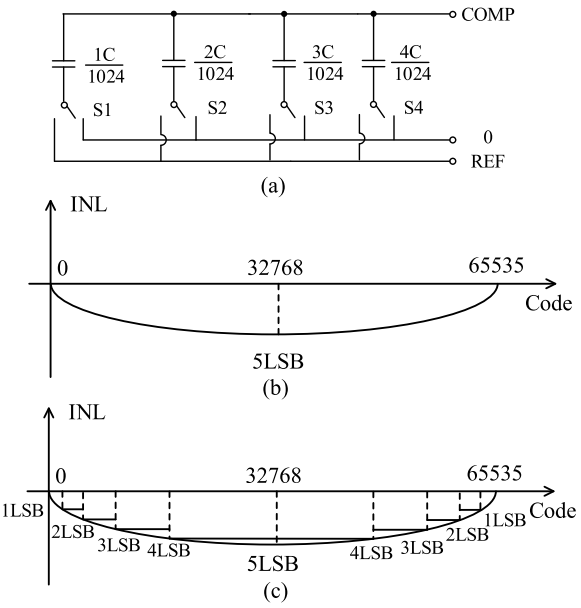

FIGURE 13. (a)Schematic of INL-Cal-Array. (b)The voltage generated by INL-Cal-Array at the COMP terminal. (c)The actual waveform generated by the INL-Cal-Array.

The parabolic formula shown in Fig. 13(b) is:

$$Y = (X - 32768)^2 \times 5/32768^2 - 5 \tag{18}$$

When Y = 1, Y = 2, Y = 3, Y = 4, the values of X are: $32768 \pm 32768 \times 0.8^{0.5}$ (represented as $32768 \pm X_1$), $32768 \pm 32768 \times 0.6^{0.5}$ (represented as $32768 \pm X_2$), $32768 \pm 32768 \times 0.4^{0.5}$ (represented as $32768 \pm X_3$), $32768 \pm 32768 \times 0.2^{0.5}$ (represented as $32768 \pm X_4$).

When $0 \le X \le 32768 - X_1$ or $65535 \ge X \ge 32768 + X_1$, the switches S1, S2, S3, and S4 are all connected to 0V, and the COMP terminal will generate a voltage of 0 LSB.

When $32768 - X_1 \le X \le 32768 - X_2$ or $32768 + X_1 \ge X \ge 32768 + X_2$, the switch S1 is connected to REF, and the switches S2, S3, S4 are all connected to 0V, and the COMP terminal will generate a voltage of 1 LSB.

When $32768 - X_2 \le X \le 32768 - X_3$ or $32768 + X_2 \ge X \ge 32768 + X_3$, the switch S2 is connected to REF, and the switches S1, S3, S4 are all connected to 0V, and the COMP terminal will generate a voltage of 2 LSB.

When $32768 - X_3 \le X \le 32768 - X_4$ or $32768 + X_3 \ge X \ge 32768 + X_4$, the switch S3 is connected to REF, and the switches S1, S2, S4 are all connected to 0V, and the COMP terminal will generate a voltage of 3 LSB.

When $32768 - X_4 \le X \le 32768$ or $32768 + X_4 \ge X \ge 32768$, the switch S4 is connected to REF, and the switches S1, S2, S3 are all connected to 0V, and the COMP terminal will generate a voltage of 4 LSB.

Therefore, the actual waveform generated by the INL-Cal-Array at the COMP terminal is shown in Fig. 13(c). In summary, the SAR capacitor array shown in Fig. 12 is used in this work. By performing DNL and INL calibration on the final circuit, the conversion accuracy of the final circuit

can meet the requirements of 16-bit applications. Ideally, the DNL for all of the codes are 0LSB. After INL calibration, codes $32768 \pm X_1$, $32768 \pm X_2$, $32768 \pm X_3$ and $32768 \pm X_4$ will have DNL error. Considering a certain code $32768 - X$, its analog counterpart is $V_{32768-X}$, V_{LSB} represents one LSB voltage. The DNL error for the code $32768 - X_1$ is $V_{32768-X_1+1} - V_{32768-X_1} - 1$, similarly, the DNL error for code $32768 + X_1$ is $V_{32768+X_1+1} - V_{32768+X_1} - 1$. Without the INL calibration, $V_{32768-X_1+1} - V_{32768-X_1} - 1 = 0$, $V_{32768+X_1+1} - V_{32768+X_1} - 1 = 0$. After the INL calibration, the analog voltage for the code $32768 - X_1$ is still $V_{32768-X_1}$, while the analog voltage for the code $32768 - X_1 + 1$ becomes $V_{32768-X_1+1} - V_{LSB}$, as a result, DNL for the code $32768 - X_1$ is: $(V_{32768-X_1+1} - V_{LSB}) - V_{32768-X_1} - 1 = -V_{LSB} = -1$LSB, the same is true for codes $32768 - X_2$, $32768 - X_3$ and $32768 - X_4$, whose DNL error become -1LSB after INL calibration. On the other hand, DNL error for codes $32768 + X_1$, $32768 + X_2$, $32768 + X_3$ and $32768 + X_4$ change to 1LSB after INL calibration. In a conclusion, the INL calibration range is limited within 5 LSB, which degrades the DNL for about 1 LSB.

III. CIRCUIT SIMULATION

In order to verify the performance of SAR capacitor arrays of IC foundries, it is necessary to perform mismatch simulation on the absolute size of all capacitors in the SAR capacitor array. In this work, the ADC is manufactured using the $0.6\mu m$ standard CMOS process, so the maximum size of the capacitor is set to $0.6\mu m$. Although the mismatch is small, it is known through theoretical analysis that SNR will not show a large deviation. However, there will be significant differences of the DNL values of BIT(6), BIT(10), BIT(11), and BIT(16). Therefore, in the simulation, we will focus on comparing the DNL parameters.

Cadence software is used for the main performance simulation. The simulation conditions are set to VDD = 12V, VSS = −12V, VLL = 5V, VREF = 2.5V, VIN = −5V ∼ 5V, and the sampling frequency is 250kHz. The VDD is the analog power supply, while the VLL is the digital power supply. This SAR ADC proposed in this work is a commercial product, which is designed to satisfy many consumers. Some consumers demand ±5V input while other consumers need ±10V input, therefore we use ±12V supply to enhance the flexibility. The block diagram of the 16-bit SAR ADC is shown in Fig. 14(a).

The comparator unit COMP in Fig. 14(a) uses a three-level output offset storage structure. The schematic diagram of each output offset storage unit is shown in Fig. 14(b). The simulation results of the comparator show that: offset error < 5μV, minimum resolution ≤ 5μV, propagation delay ≤ $100nS$.

The circuit diagram of the sampling capacitor and capacitor array is shown in Fig. 14(c). VIN is the input port of the analog signal, and the sample/hold capacitance is 16C, while the conversion capacitors is 64C, corresponding to the 2.5V reference voltage and 10V analog range.

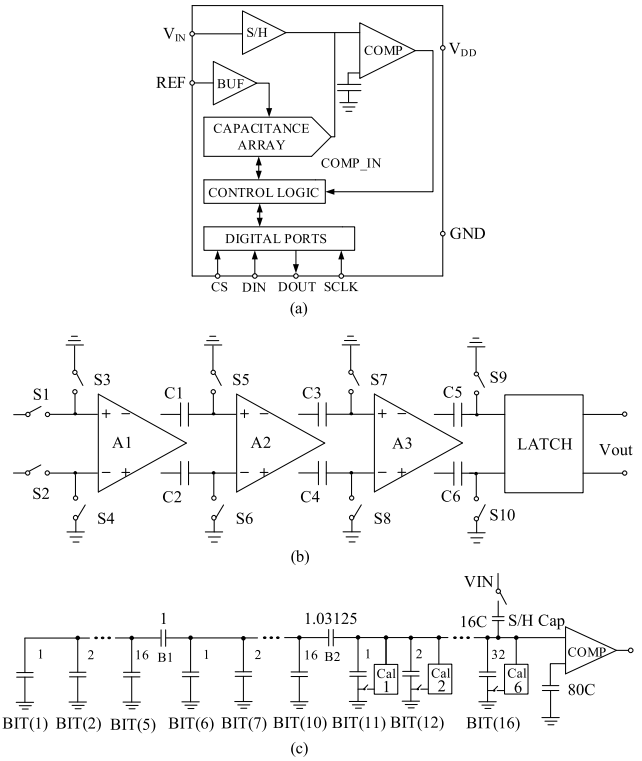

FIGURE 14. (a)The block diagram of the 16-bit SAR ADC. (b)The block diagram of the comparator. (c)The core diagram of the ADC.

The design document of the 0.6μm standard COMS process used in this work shows that the relationship between the matching accuracy of the linear capacitor and the capacitor area is

$$\sigma(\Delta C/C) = 1.28/(W \times L)^{0.5} \tag{19}$$

In order to ensure that the matching accuracy of the capacitor array is higher than 10 bit, it is necessary to satisfy $\sigma(\Delta C/C)/100 \leq 1/2^{10}$, so the minimum area of the unit capacitor is

$$W \times L \geq 171.8\mu m^2 \tag{20}$$

The maximum input range of the 16bit ADC in this work is VIN = −5V ∼ 5V, so the minimum resolution voltage is $10V/2^{16} = 0.000152$V. In order to meet the minimum resolution requirement, the thermal noise of the sampling capacitor must be less than the minimum resolution.

$$(kT/16C)^{0.5} \leq 0.000152V \tag{21}$$

$$C \geq 8 \times 10^{-15}F = 8fF \tag{22}$$

The square capacitance of the process used in the technology is $1fF/\mu m^2$. According to Equation (6) and Equation (8), when the minimum area of the unit capacitor is $171.8\mu m^2$, the thermal noise will be much smaller than the minimum resolution of the 16bit ADC. In order to further improve the matching performance of the capacitor array, the size of the unit capacitor is finally determined to be $20\mu m \times 20\mu m$.

During simulation verification, add a mismatch to the weight capacitor, and then perform DNL calibration through the calibration network to verify the linearity calibration function.

For BIT(11)∼BIT(16), the method for judging whether there is a deviation in the weight is (for the convenience of description, take BIT(11) as an example): When the output has no missing codes, the average input voltage of output code 1024 is V_1, the average input voltage of output code 1023 is V_2, and the voltage of 1LSB is V_{LSB}. If the weight of BIT(11) is smaller than the ideal value, the weight error is $((V_1 - V_2)/V_{LSB} - 1)/1024$. Assuming BIT (11) is larger than the ideal value, for example, the ideal weight of BIT (11) is 1024, while the real weight is 1030, the summation of all of the bits lower than BIT(11) is only 1023. As a result, the DNL is 6LSB.

If there is a missing code near the output code 1023, and the largest code less than 1023 is X. Assuming BIT (11) is smaller than the ideal value, and its weight error is $(1023 - X)/1024$. For example, the ideal weight of BIT (11) is 1024, while the real weight is 1013, which corresponds to 01111110101 $(1 + 4 + 16 + 32 + 64 + 128 + 256 + 512 = 1013)$. As a result, the DNL is $2 + 8 = 10$LSB.

A. SIMULATION OF THE CONVENTIONAL 5 + 5 + 6 BITS CAPACITOR ARRAY

The conventional 5 + 5 + 6 bits capacitor array is shown in Fig. 3. The size of the unit capacitor is $20\mu m \times 20\mu m$, and the size of the bridge capacitors B1 and B2 is $20\mu m \times 20.65\mu m$. The simulation results show that the SNR of the conventional 5 + 5 + 6 bits capacitor array is 88.02dB, and the SFDR is 94.16dB. The SFDR simulation result is shown in Fig. 15, and the DNL simulation results of BIT(6), BIT(10), BIT(11) and BIT(16) are shown in Table 1. One of the limiting factors for the dynamic performance possibly come from the nonlinearity of the switch. Because this is a high-voltage design. The switch is a high-voltage device, whose length is about $6\mu m$, as a result, big parasitics and on-resistance of the switch introduce the nonlinearity. The

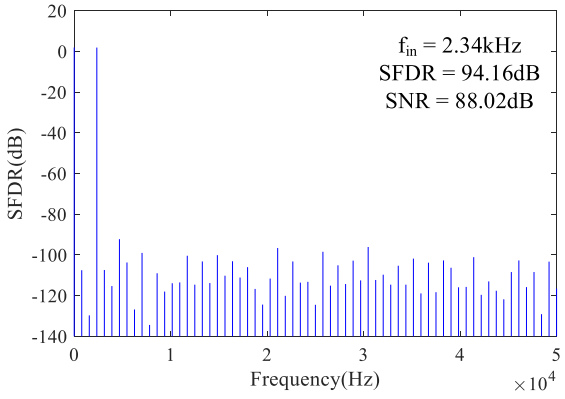

FIGURE 15. The SFDR simulation result of conventional 5 + 5 + 6 bits capacitor array.

TABLE 1. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) in the conventional 5 + 5 + 6 bits capacitor array.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0 LSB	0 LSB	0 LSB	0 LSB

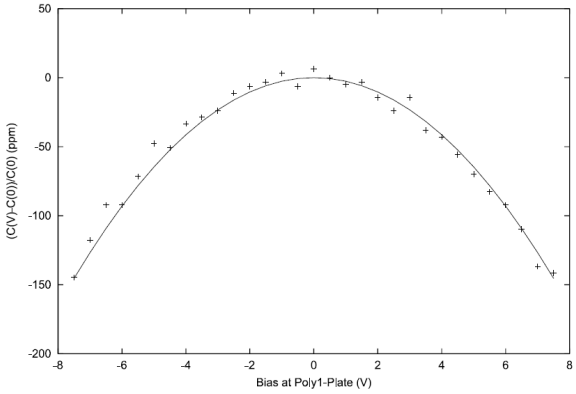

FIGURE 16. The voltage coefficient of poly-to-poly capacitor .

poly-to-poly capacitors have been used in this design. The absolute value of unit capacitor is 400 fF. The voltage coefficient of poly-to-poly capacitor is shown in Fig. 16. Therefore, the maximum voltage coefficient is about 100 ppm (1/10000), corresponding to 14 bits resolution, which does not reach 16 bits resolution (1/65536), as a result, the limitation of voltage coefficient of capacitors is one of the reasons for not good enough performance. Finally, the resolution of comparator and the bottom plate capacitor parasitics also deteriorate the dynamic performance.

B. SIMULATION OF THE CONVENTIONAL 5 + 5 + 6 BITS CAPACITOR ARRAY WITH MISMATCH

Then we set the size of all unit capacitors to $20\mu m \times 19.4\mu m$ (the deviation is $0.6\mu m$), and the sizes of the bridge capacitors B1 and B2 remain unchanged. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) are shown in Table 2.

TABLE 2. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) in the conventional 5+5+6 bits capacitor array with a deviation.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0.75 LSB	0.75 LSB	30.25 LSB	30.25 LSB

It can be seen from Table 2 that in the conventional 5 + 5 + 6 bits segmented capacitor array, if there is deviation in the size of the unit capacitor, the DNL of BIT(6)∼BIT(16) will have obvious errors.

C. SIMULATION OF THE OPTIMIZED 5 + 5 + 6 BITS CAPACITOR ARRAY

The optimized 5 + 5 + 6 bits capacitor array is shown in Fig. 4, in which the size of all unit capacitors and the bridge capacitor B1 is $20\mu m \times 20\mu m$. The size of the bridge capacitor B2 is $20\mu m \times 20.65\mu m$. Simulation results show

that the optimized 5 + 5 + 6 bits capacitor array has an SNR of 88.71dB and an SFDR of 94.55dB. The SFDR simulation result is shown in Fig. 17, and the DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) are shown in Table 3.

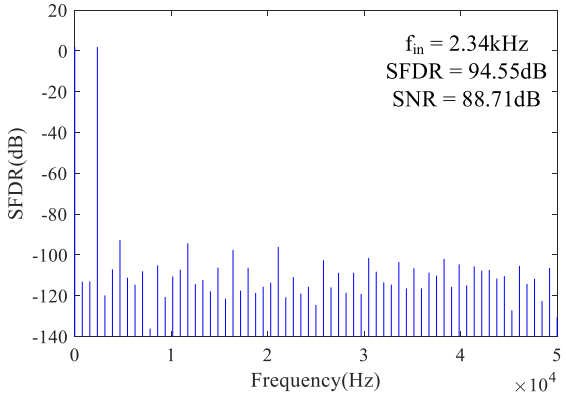

FIGURE 17. The SFDR simulation result of the optimized 5 + 5 + 6 bits capacitor array.

TABLE 3. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) in the optimized 5 + 5 + 6 bits capacitor array.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0 LSB	0 LSB	0 LSB	0 LSB

D. SIMULATION OF THE OPTIMIZED 5 + 5 + 6 BITS CAPACITOR ARRAY WITH MISMATCH

Then we set the size of all unit capacitors and bridge capacitor B1 to $20\mu m \times 19.4\mu m$ (the deviation is $0.6\mu m$), and the sizes of the bridge capacitor B2 remain unchanged. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) are shown in Table 4.

TABLE 4. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) in the optimized 5+5+6 bits capacitor array with mismatch.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0 LSB	0 LSB	29.75 LSB	29.75 LSB

It can be seen from Table 4 that in the optimized 5 + 5 + 6 bits segmented capacitor array, if there is a deviation in the size of the unit capacitor, the DNL values of BIT(6)∼BIT(10) will not change significantly, only BIT(11)∼BIT(16) will have obvious errors.

E. SIMULATION OF LINEAR ERROR CALIBRATION

As shown in Fig. 9, in the SAR capacitor array, only the bridge capacitor B2 is a non-unit capacitor. The process will introduce a large size deviation to the capacitor B2. Therefore, the calibration function can be simulated by giving a deviation to capacitor B2 and performing linear error calibration.

The size of all unit capacitors and bridge capacitor B1 is set to 20μm $\times$ 20μm, and the size of the bridge capacitor B2 is 20μm $\times$ 20.85μm(the deviation is 0.2μm). When the bridge capacitor B2 has mismatch, the SNR is 74.76dB and the SFDR is 84.08dB. The SFDR simulation result is shown in Fig. 18, and the DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) are shown in Table 5.

It can be seen from Fig. 18 and Table 5 that when there is a size offset (+ $0.2\mu m$) of the bridge capacitor B2, the SNR, SFDR, and DNL will have obvious errors. The DNL error will only appear at BIT(11)∼ BIT(16), and will not affect BIT(1)∼BIT(10). Then, calibrate BIT(11)∼BIT(16). After calibration, the SNR is 86.78dB and the SFDR is 92.10dB. The SFDR simulation result is shown in Fig. 19. Table 6 shows the DNL value of BIT(6), BIT(10), BIT(11) and BIT(16). As mentioned above, the minimum trimming step of Cal1 unit is 0.5 LSB. Therefore, 0 LSB in Table 6 means the error is limited to 0.5 LSB actually.

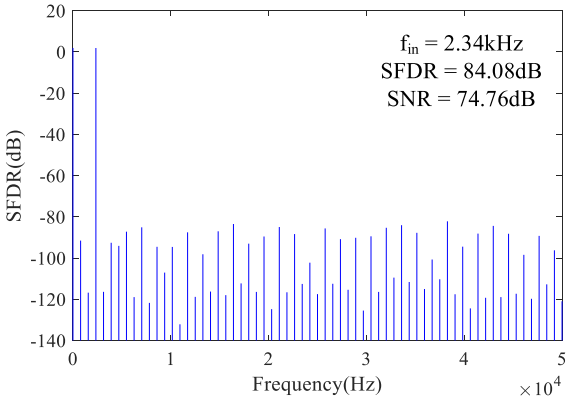

FIGURE 18. The SFDR simulation result when there is a size offset of the bridge capacitor B2.

TABLE 5. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) when there is mismatch of the bridge capacitor B2.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0 LSB	0 LSB	9.50 LSB	9.50 LSB

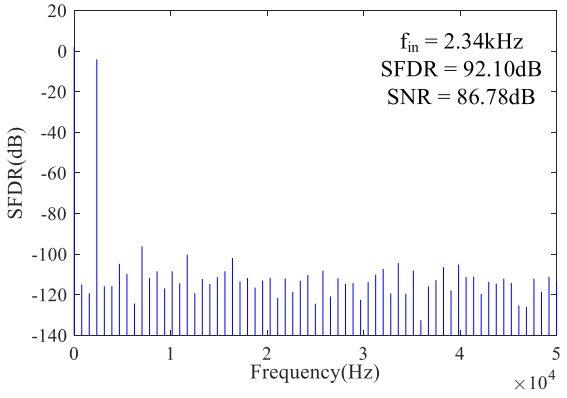

FIGURE 19. The SFDR simulation result after calibration.

TABLE 6. The DNL values of BIT(6), BIT(10), BIT(11) and BIT(16) after calibration.

	BIT(6)	BIT(10)	BIT(11)	BIT(16)
DNL	0 LSB	0 LSB	0 LSB	0 LSB

F. ANALYSIS OF SIMULATION RESULTS

By comparing the simulation results of Subsection A and Subsection C, it can be concluded that the main performance of the optimized SAR capacitor array used in this work is basically the same as the conventional structure.

By comparing the simulation results of Subsection A and Subsection B, we can see that when there is a large deviation in the conventional capacitor array, the DNL values of BIT(6)∼BIT(16) have obvious errors, which results in a large area of DNL calibration unit.

By comparing the simulation results of Subsection C and Subsection D, which shows that when there is a large mismatch in the optimized capacitor array, the DNL values of BIT(6)∼BIT(10) are almost unchanged, only BIT(11)∼BIT(16) have large errors. It can be seen from Section E that this situation is basically the same as the DNL error caused by the mismatch of the bridge capacitor B2, so DNL calibration can be performed to calibrate this DNL error by the Cal-unit of BIT(11)∼BIT(16).

In summary, the mismatch of the overall capacitor array and the bridge capacitor B2 just affect the DNL of BIT(11)∼BIT(16) but not the DNL of the lower 10 bits. It can be seen from Subection E that the DNL error of BIT(11)∼BIT(16) can be calibrated by the Cal-unit of the corresponding bit.

IV. LAYOUT DESIGN

The 16-bit 6-channel SAR ADC is manufactured using the standard $0.6\mu m$ COMS process. The chip photo of the 16-bit 6-channel SAR ADC is shown in Fig. 20. The total 6-channel ADC area including pads is 6.6mm × 6.6mm. As for single channel SAR ADC, the area is 0.9mm × 2.0mm. The poly-to-poly capacitors have been used in this design. The absolute value of unit capacitor is 400 fF. Two important measures have been adopted to deal with the parasitics of the floating bottom plate of the bridge capacitor. Firstly, the 400 fF unit capacitor is large enough to overcome the bottom parasitics of capacitor B1. Secondly, custom designed layout is an effective method to mitigate the bottom parasitics. The area of the top plate of the unit capacitor is 20μm × 20μm, while the area of the bottom plate is 26μm × 26μm, larger bottom plate can shield the parasitics between the top bottom and the ground. However, the parasitics between the bottom plate and the ground will become larger, sacrificing the sampling rate.

V. CHIP MEASUREMENT

Because the ADC is a low-speed product, its main application environment is measurement and control. In order to verify the conversion accuracy more easily, the main test specifications are DNL and INL. In order to ensure the testing accuracy, we use Teradyne J750 high-precision platform for parameter testing.

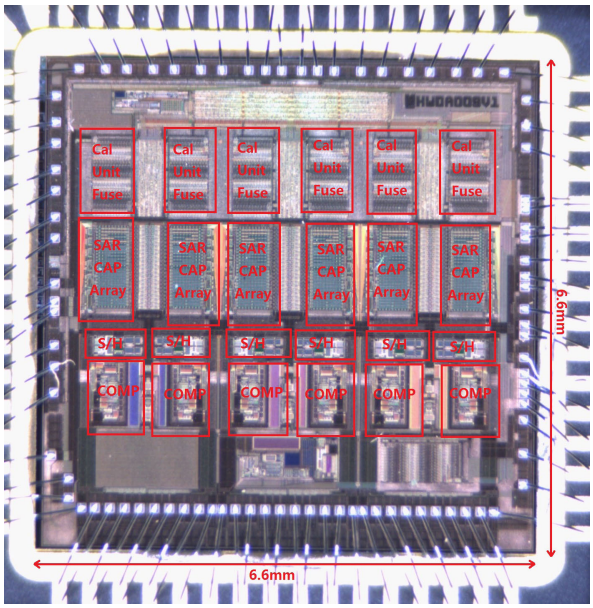

FIGURE 20. The chip photo of the 16-bit SAR ADC.

As well known, if the maximum value of DNL and INL is Y LSB ($Y = 2^N$), then the effective accuracy is $16 - N$ bits.

A. CHIP MEASUREMENT WITHOUT DNL CALIBRATION

The measurement results of the 16-bit ADC without DNL calibration are shown in Fig. 21 and Fig. 22. Fig. 21 shows the DNL measurement results over the full range, and Fig. 22 shows the INL measurement results over the full range. Theoretically, the error in Fig. 21 starts from the second bridge capacitor B2, which means Bit (11) ∼ Bit (16) lead to big DNL error, the error begins from code 1024, and abrupt jumps of DNL occur every 1024 interval. In a conclusion, theoretically, high DNL error appear at codes 1024, 2048, 3072, 4096, …64512.

The DNL and INL measurement results of the lower 10-bit without DNL calibration is shown in Fig. 23 and Fig. 24.

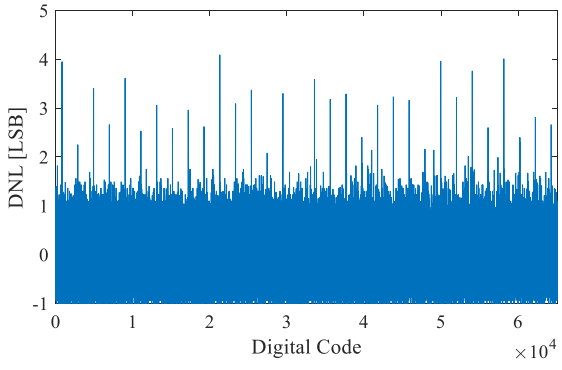

FIGURE 21. The DNL measurement result of the 16-bit ADC without DNL calibration.

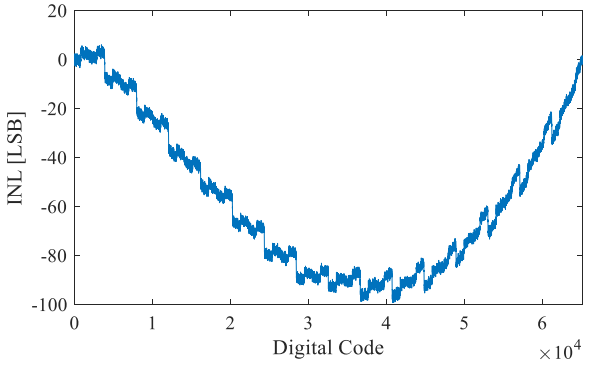

FIGURE 22. The INL measurement result of the 16-bit ADC without DNL calibration.

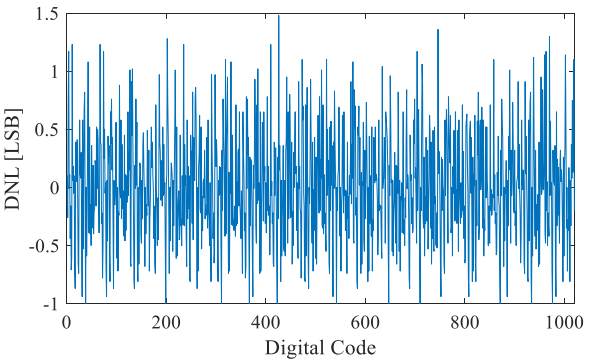

FIGURE 23. The DNL measurement result of the lower 10-bit without DNL calibration.

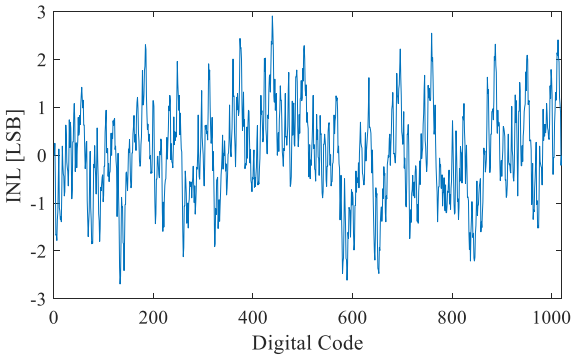

FIGURE 24. The INL measurement result of the lower 10-bit without DNL calibration.

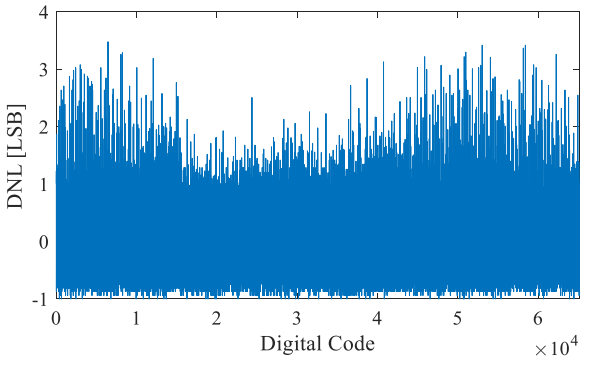

FIGURE 25. The DNL measurement result of the 16-bit ADC after DNL calibration.

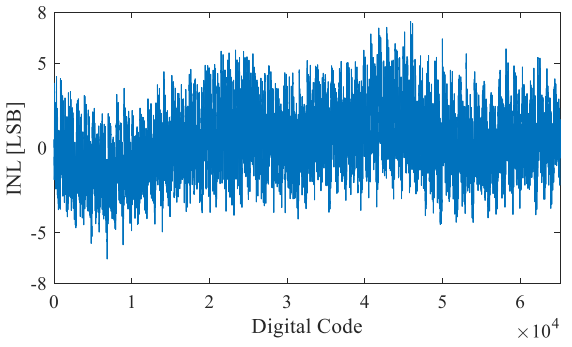

FIGURE 26. The INL measurement result of the 16-bit ADC after INL calibration.

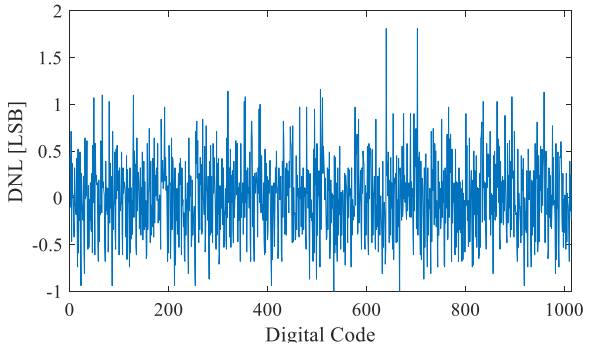

FIGURE 27. The DNL measurement result of the lower 10-bit after DNL calibration.

It can be seen from Fig. 21 to Fig. 24 that before the calibration, the lower 10-bit capacitor array of the ADC did not show a significant mismatch. The ADC has a DNL value of 4.09LSB and an INL value of -97.83LSB over the full range. Therefore, the effective conversion accuracy of the ADC before calibration is about 10 bits, which is consistent with the conclusions of theoretical analysis and simulation.

B. CHIP MEASUREMENT AFTER DNL CALIBRATION

According to the measurement data, the DNL error of the 16-bit ADC in this paper is mainly introduced by the capacitors of BIT(11)∼BIT(16). After all calibrations are completed, the main measurement data is shown in Fig. 25, Fig. 26, Fig. 27, and Fig. 28. Fig. 25 is the DNL measurement result after DNL calibration. Fig. 27 is the DNL measurement result of the lower 10-bit after DNL calibration. The DNL is larger than 1 LSB demonstrates that there are indeed missing codes. Since we think the lower 10 bits satisfy the matching demands, the linearity error perhaps due to the lack of comparator resolution because the DNL error is basically evenly distributed throughout the whole interval. Fig. 26 is the INL measurement result after INL calibration. Fig. 28 is the INL measurement result of the lower 10-bit after DNL calibration.

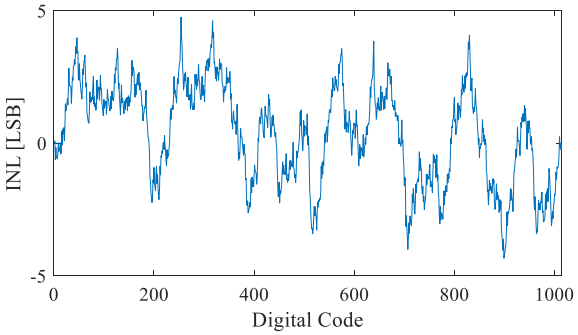

FIGURE 28. The INL measurement result of the lower 10-bit after DNL calibration.

It can be seen from Fig. 25 to Fig. 28 that the DNL calibration of the ADC will hardly affect the linearity of the lower 10 bits, but the DNL error of BIT(11)∼BIT(16) bits will be significantly improved. Within the full input range of the 16-bit ADC, the DNL is 3.51LSB and the INL is 7.36LSB after calibration. Therefore, the effective conversion accuracy of the 16-bit ADC is greater than 13 bits after calibration, which is consistent with the theoretical analysis and simulation.

C. CHIP MEASUREMENT AFTER INL CALIBRATION

As shown in Fig. 26, the shape of the INL is consistent with the model in Fig. 11(a). As mentioned above, for the two INL models of Fig. 11(a) and Fig. 11(b), INL calibration will not be performed. However, in order to verify the INL calibration function proposed in this paper, INL calibration is still performed, and the measurement result after INL calibration is shown in Fig. 29.

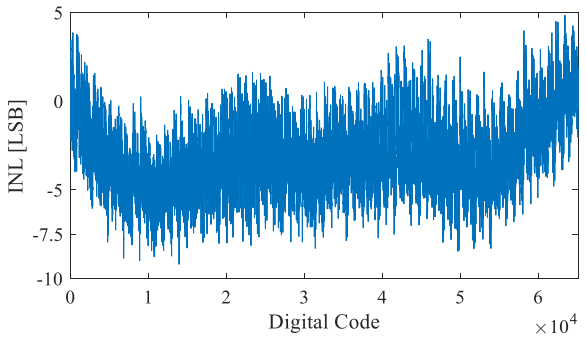

FIGURE 29. The INL measurement result of the 16-bit ADC after INL calibration.

Comparing Fig. 26 with Fig. 29, we can see that the INL calibration method used in this paper can indeed change the overall shape of the INL, thus affecting the final INL value. However, since the INL in Fig. 26 is already the most optimized INL, the final circuit does not require INL calibration.

D. MEASUREMENT OF MAIN PERFORMANCE

In order to verify the batch-to-batch consistency, the main performances of 5 final chips have been measured, and the measurement results of the final chips are shown in Table 7. It can be seen from Table 7 that the 16-bit SAR ADC proposed in this work has an effective conversion accuracy of about 13 bits after calibration, which is consistent with the theoretical analysis.

TABLE 7. Main performances of 5 final chips.

	1	2	3	4	5
DNL (LSB)	3.2	3.6	2.9	2.8	3.6
INL (LSB)	7.3	7.9	6.9	7.2	8.0
SNR (dB)	85	85	86	86	84
I_{VDD} (mA)	0.53	0.52	0.53	0.51	0.52
I_{VSS} (mA)	-0.53	-0.52	-0.53	-0.51	-0.52

TABLE 8. Performance comparison with the state-of-the-art works .

	This work	[14]	[15]	[16]
Resolution	16	14	16	16
Technology[μm]	0.6	0.6	0.25	0.18
Speed[kS/s]	250	400	1000	1000
ENOB [bits]	13	11.89	14.49	14.01
FOM[pJ/conv.-step]	48	59.41	4.56	0.41
Calibration	on-chip	on-chip	off-chip	off-chip

Table 8 concludes the performance comparison with the state-of-the-art works. The chip in this work is a high-voltage commercial product, therefore, advanced technology may not be applicable. Table 8 also demonstrates that the on-chip calibration will not benefit FOM, but it is of great value for the practical application.

VI. CONCLUSION

The 16-bit SAR ADC proposed in this work is manufactured by a 0.6μm standard COMS process. The measurement results show that the effective conversion accuracy of the SAR ADC reaches 13 bits by using novel DNL and INL calibration methods. Within the full input range of the 16-bit ADC, the DNL is 3.51LSB and the INL is 7.36LSB after calibration.

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