Feed-Forward Control Method for Digital Power Factor Correction in Parallel Connected Buck-Boost Converter (CCM Mode)

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***Abstract*—Amongst power converters, rectifiers are needed by many devices that are connected at the distribution end of AC electrical power networks. When large capacitors are used to reduce the voltage ripple at the dc output, the line current becomes non-sinusoidal. Such non-sinusoidal line currents increase the total harmonic distortion, resulting in significant power losses within the power network. The power factor correction converter or PFC converter is a well-known alternative to generate a flat dc voltage while shaping the input current to the input ac grid voltage, emulating a resistive behavior. As the parallel connection of PFC converters is a promising way to achieve a higher power rating, questions arise on balancing the current and power over these connected converters. In this paper, based on the differential equations of a buck-boost converter, a method is obtained to compute the duty cycles of the semiconductor devices aimed at obtaining the unity power factor while balancing the current. Feed-forward algorithms are used to tune the model parameters in order to strongly reduce the input current harmonics. The proposed scheme is simulated in MATLAB and results are given showing that the proposed algorithms result in a good power factor correction.**

Keywords—Power factor correction, Parallel connected buck-boost converter, Feed-forward control algorithm.

I. INTRODUCTION

Power supply modules can be connected in parallel or series in order to build up a power system. Connecting many converters is more beneficial compared to a single larger power unit in terms of component stresses, modular implementation, flexible power requirements, and design variations. All of above benefits can be achieved as long as the load current is distributed between the converters in a controllable manner. Parallel connection of power supply modules is, despite being an effective method, a method that requires a good current balancing algorithm to distribute the input current distortion and current stresses over the different modules.

Power can be shared between parallel connected converters to achieve the most cost effective design. Power converters were arranged before in parallel designs for inverter uninterruptible power systems (UPS) [1] for improving reliability and capacity of the power system. The maintenance and the protection depends upon the configuration of the system, while keeping the modules identical. Concerning the failure of converter modules, analysis on the basis of system reliability, performance and ripple reduction are performed in [2], [3]. Ensuring maximum power delivery was proposed before in [4].

For DC/DC converters, different techniques have been presented in [5]– [7] to control the way the load current is shared. Among these controllers, [5], [6] is the most effective and easy to implement because it is convenient in controller design and it has good performance. Details about constructing controllers for current sharing in parallel modules are reported in [5], [8]**.** Concerning the reliability and capacity of power systems, a parallel connection of AC/DC converter modules may provide better results in terms of design variations and flexible power requirements. These setups are helpful in eliminating harmonics in the input line current as well as to provide a power factor correction at the input. A rectifier connected in parallel provided with a controller to share the current is presented in [9]**.**

With the development of Digital Signal Processors, or DSPs, and other digital chips, more complex and advanced algorithms can be included in the control system. To implement current control, the Average Inductor Current Mode Control or AICMC technique is often used in digital control [10]. In terms of PFC implementation, comparing digital control with analog, existing methods cannot take full benefit of digital control techniques because switching frequency is related to the speed of DSP. So high switching system requires DSP with high speed that is subjected to high cost problem.

So considering this fact, feed-forward control technique is proposed for digital PFC implementation. Digital feed-forward control for buck-boost converters connected in parallel, shown in fig. 1, is presented in this paper. This feed-forward control will help in the calculation of the duty cycles responsible for bringing power factor to unity. This technique is based on feed-forward control, So a low cost DSP can be used to achieve power factor correction.

In this paper, section II is about problems in existing digital PFC control implementation. Digital buck-boost converter PFC feed-forward control is derived in section III of this paper. Feed-forward control algorithm for parallel connected buck-boost converter PFC is highlighted in section IV. Input voltage feed-forward implementation is considered in section V. Simulation results are made in section VI and conclusion is made in section VII of this paper.

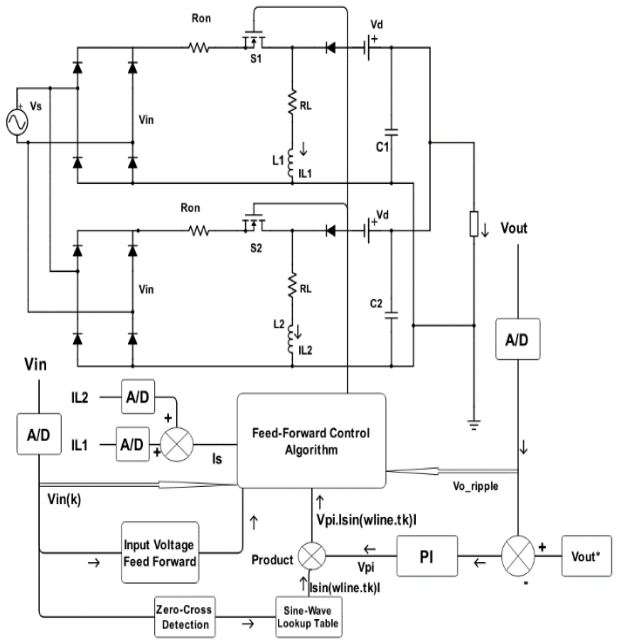

Figure 1. Two Parallel BBC PFCs with Digital Feed-Forward Algorithm.

II. EXISITNG DIGITAL CONTROL PFC IMPLEMENTATION PROBLEMS

Due to the processing time and sampling delay in digital control systems there is limitation on the switching frequency. As discussed above the AICMC is a technique used for analog control. This AICMC technique is also used for digital control in [10]**.** In AICMC technique, i_L and i_{ref} are used as feedback currents in controller and from their difference, the duty cycles for switch are calculated by DSP for each and every switching cycle T_s [11] and the inductor current i_L is multiplied by the rectified input voltage and then it is pushed to follow reference current $i_{ref.}$ The whole process of AICMC contains plenty of processes to perform PFC and all these processes are running simultaneously in each cycle so in each t_{on} time all these process should be completed to achieve power factor correction. So in analog implementation there is no limitation on it but in digital control it is related to the DSP speed where switching frequency is limited. So this is the main disadvantage of digital control. To overcome this problem, duty cycle calculation per switching cycle is minimized in [12] to increase the switching cycle and minimizing the time for calculation by using dead beat control method. But due to this harmonics are generated in system which results in low PFC. Another method is presented in [13] with two control parallel loops. But the same problem of duty cycle calculation in each cycle was an issue. Feed-forward control is also used for power factor correction in [14] for removing the input current zero crossing distortion. Feed-forward control strategy for buck-boost PFC is used in this article, focusing mainly on Continuous Conduction Mode CCM, to achieve high power factor and less distortion in current with efficient current distribution amongst parallel connected converters.

III. FEED-FORWARD CONTROL ALGORITHM FOR BUCK-BOOST PFC

Fig. 2 shows the buck-boost Converter topology. Based on the switch operation, the buck-boost converter operation can be divided into two main states .i.e. on-state and off-state (shown in fig. 3).

The feedforward controller for the buck-boost PFC converter is discussed under the assumption that the converter operates in Continuous Conduction Mode. Furthermore input voltage V_{in} can be well approximated by holding the sampled voltage during each sample period as the sampling frequency is larger than line frequency.

Keeping the assumptions in account, the inductor current is given by;

$$L.\frac{di_L}{dt} = V_{in} \qquad for \qquad t_k \le t < t_k + d_k.T_s \tag{1}$$

$$L.\frac{di_L}{dt} = V_{out} \quad for \quad t_k + d_k.T_s \le t < t_{k+1} \tag{2}$$

Equation (1) and (2) represents the inductor current for on-state and off-state of the switch respectively.

According to the assumptions made, the $(K+1)^{th}$ cycle inductor current is given by

$$i_L(t_{k+1}) = i_L(t_k) - \frac{V_{in}.d_k.T_s}{L} + \frac{V_{out}.(1-d_k).T_s}{L} \tag{3}$$

The inductor current is forced to follow the reference current i_{ref} as shown in fig. 4. In voltage loop, the output voltage is forced to follow the reference voltage, so we can do the below given replacements i.e.

$$V_{out} = V_{ref} \tag{4}$$

$$i_L(t_{k+1}) = i_{ref}(k+1) \tag{5}$$

$$t_k = k \tag{6}$$

By putting these values in (3), the value of duty cycle is obtained for switching period k

$$d(k) = \frac{(i_{ref}(k+1) - i_{ref}(k))\left(\frac{L}{T_s}\right)}{V_{in}(k) - V_{ref}} - \frac{V_{ref}}{V_{in}(k) - V_{ref}} \tag{7}$$

Equation (7) shows the feed-forward algorithm for Buck-Boost PFC that can be used to calculate duty cycle values. To improve performance in calculating duty cycle values, detailed topology of buck-boost converter is shown in fig. 5. The switching resistance R_{on}, the inductor resistance R_L, the diode voltage drop V_d and ripple at the output voltage v_{o_ripple} are considered in calculations. So referring to the most accurate model in fig. 5, duty cycle calculation is given by

$$d_k = \frac{(i_{ref}(k+1) - i_L(k))\left(\frac{L}{T_s}\right)}{v_{in}(k) - (V_{ref} + v_{o\_ripple}(k) + V_d) + R_{on}.i_{ref}(k)} + \frac{(V_{ref} + v_{o\_ripple}(k) + V_d) + R_L.i_{ref}(k)}{v_{in}(k) - (V_{ref} + v_{o\_ripple}(k) + V_d) + R_{on}.i_{ref}(k)} \tag{8}$$

Equation (8) is the required feed-forward control for buck-boost PFC.

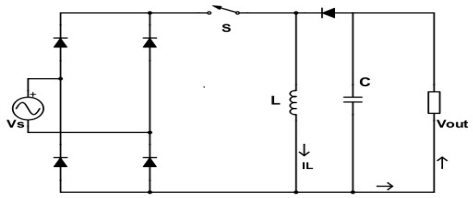

Figure 2. Buck-Boost Converter Topology.

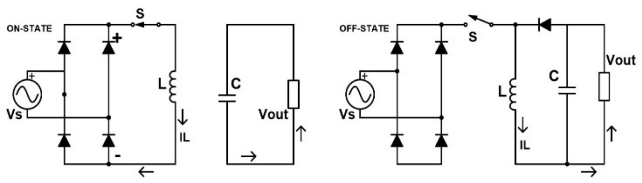

Figure 3. Buck–Boost Converter topology when switch is ON(Left) and OFF(Right).

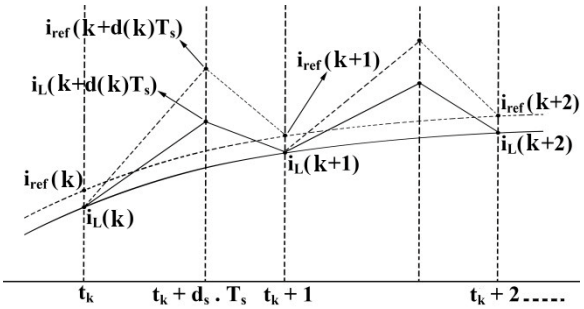

Figure 4. Inductor current and Reference current waveforms.

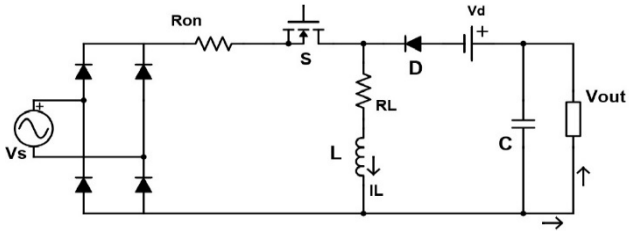

Figure 5. Detailed Diagram of Buck-Boost PFC.

IV. FEED-FORWARD ALGORITHM FOR PARALLEL CONNECTED BUCK-BOOST PFCS

For the purpose of Power Factor Correction, the inductance is needed. For this, increasing the inductor value for high power rating will also increase the size and the current stress. To eliminate this stress, parallel connection of PFCs are used to share the stress between them. The load current is shared between each PFC depending upon the converter capacity and their distance from the load. Parallel connection is also advantageous in doubling the energy storing capacity of the system which helps in estimating output power capabilities. PFCs connected in parallel provides the same level of the output power using low inductor values as compared with conventional single PFC.

The feed-forward control for parallel connected buck-boost PFCs is shown in fig. 1 (without considering the part of input feed-forward voltage).

Taking the assumption in to account that $L_1+L_2=L$, summing both the inductor current will results in source current $I_s(k)$ i.e.

$$I_s(k) = I_{L1}(k) + I_{L2}(k) \tag{9}$$

Replacing $i_L(k)$ in (7) by $I_s(k)$ will results in the feedforward algorithm for parallel connected buck-boost converters shown in fig. 1.

$$d(k) = \frac{K_{pi}|\sin(\omega_{line}.t_k)| - I_s(k)}{2K_c} + \frac{V_{ref}}{V_{in}(k) - V_{ref}} \tag{10}$$

Where K_c is given by

$$K_c = \frac{T_s(V_{in}(k) - V_{ref})}{L} \tag{11}$$

This technique helps in finding the duty cycle in particular switching instant and it also eliminates the errors from the system that occurs in the previous switching cycle.

Outer voltage loop of feed-forward control is responsible for determining output voltage with the help of PI controller. The reference current $i_{ref}(k)$ is obtained from voltage PI controller. The amplitude of this reference current is dependent on PI voltage controller output while its shape and phase is determined by the input voltage peak value and zero cross signal detection.

V. IMPLEMENTING INPUT VOLTAGE FEED FORWARD COMPENSATION

For steadiness of the output voltage referring to the line voltage deviations, input voltage feed-forward is introduced in to the feed-forward control loop. It permits output voltage to be less sensitive to the input voltage deviations. This also helps in duty cycles compensation for opposing distortion in input current and ensuring less THD rate even though there is distortion in the line voltage. $V_{in}(k)$ in (7) represents peak value of the input voltage which is purely sinusoidal. But in case of a distortion in the line voltage, the instantaneous input voltage is taken for adjusting the duty cycle values which are calculated in advance. Equation (7) comprises of two main components i.e.

$$d(k) = d_1(k) + d_2(k) \tag{12}$$

Where

$$d_1(k) = \frac{\left(i_{ref}(k+1) - i_L(k)\right)\left(\frac{L}{T_s}\right)}{v_{in}(k) - V_{ref}} \tag{13}$$

Equation (13) shows that $d_1(k)$ is a current forcing component because it contains difference between the inductor current and the reference current which is obtained from outer/voltage loop. So it will responsible for the output voltage regulations and also for providing sinusoidal line current. Furthermore the second component of (12) is given by

$$d_2(k) = \frac{V_{ref}}{v_{in}(k) - V_{ref}} \tag{14}$$

Here $d_2(k)$ is referred as voltage equilibrium component.

Now considering the compensation of input voltage feed forward, updated duty cycle is

$$d_{update}(k) = d(k) + \Delta d(k) \tag{15}$$

The value of $d(k)$ is taken from (7), while $\Delta d(k)$ is the compensated duty cycle given by

$$\Delta d(k) = \frac{V_{ref}}{\Delta v_{in}(k)} \tag{16}$$

Where

$$\Delta v_{in}(k) = V_{in}(k) - v_{in}(k) \tag{17}$$

Here $\Delta v_{in}(k)$ shows variations in input voltage while $v_{in}(k)$ is instantaneous input voltage. In case of harmonics,

$$v_{in}(k) = |V_1.\sin(\omega_{line}.t_k) + \sum_{i=3,5,..}^{\infty} V_i.\sin(\omega_{line}.t_k)| \tag{18}$$

So (17) becomes

$$\Delta v_{in}(k) = |V_1.\sin(\omega_{line}.t_k)| - |V_1.\sin(\omega_{line}.t_k) + \sum_{i=3,5,..}^{\infty} V_i.\sin(\omega_{line}.t_k)| \tag{19}$$

Considering (19) in (16), we get

$$\Delta d(k) = \left[\frac{V_{ref}}{(|V_1.\sin(\omega_{line}.t_k)| - |V_1.\sin(\omega_{line}.t_k) + \sum_{i=3,5,..}^{\infty} V_i.\sin(\omega_{line}.t_k)|)}\right] \tag{20}$$

Putting this value of $\Delta d(k)$ in (15) we obtained updated duty cycle value in terms of compensation of the input feed-forward voltage and is given by

$$d_{update}(k) = \left[\frac{\left(i_{ref}(k+1) - i_L(k)\right)\left(\frac{L}{T_s}\right)}{v_{in}(k) + V_{ref}} + \frac{V_{ref}}{v_{in}(k) + V_{ref}}\right] + \left[\frac{V_{ref}}{(|V_1.\sin(\omega_{line}.t_k)| - |V_1.\sin(\omega_{line}.t_k) + \sum_{i=3,5,..}^{\infty} V_i.\sin(\omega_{line}.t_k)|)}\right] \tag{21}$$

In case of the two parallel connected buck-boost converters, (21) can be rewrite as

$$d_{update}(k) = \left[\frac{K_{pi}|\sin(\omega_{line}.t_k)| - I_s(k)}{2K_c} + \frac{V_{ref}}{v_{in}(k)+V_{ref}}\right] + \left[\frac{V_{ref}}{(|V_1.\sin(\omega_{line}.t_k)| - |V_1.\sin(\omega_{line}.t_k) + \sum_{i=3,5,..}^{\infty} V_i.\sin(\omega_{line}.t_k)|)}\right] \quad (22)$$

This equation provides feed-forward control for parallel connected buck-boost PFCs while taking the input voltage feed-forward compensation in account, shown in fig. 1. The input voltage sine wave look up table only contains peak value $V_{in}(k)$ when there is no distortion in the input voltage . But in case of input voltage feed forward compensation, it contains both peak value $V_{in}(k)$ and instantaneous value $v_{in}(k)$. Input feed forward voltage compensation helps in stabilizing and dynamic performance improvement of the system with high power factor and less distortion in the line current because of the fact that distortion in the input voltage drops down on diode.

Worth of our control scheme is that it will calculate the duty cycle values that bring power factor to one. A low cost DSP can be used to carry out the operation even at very intense frequency. Using the low cost DSP or microprocessor, it can accomplish some other role which includes observing and communication with the main controller. From fig 6, it is obvious that three main steps are required by DSP to perform, amongst them, A/D conversion and PI voltage regulation of the output voltage are the first two operations. The third and the important step is to perform our proposed algorithm calculation for duty cycle which will be performed in iterative way to get all the duty cycle values which takes most of the computational time as compare to first two steps.

VI. SIMULATIONS AND RESULTS

The proposed scheme is verified in MATLAB SIMULINK. Two buck-boost converters are used in parallel. THD of the input current is taken as an objective function for obtaining the unity power factor. Simulations are performed for the inductors L1=0.5mH and L2=5mH and switching frequency is used 10kHz and line frequency is kept at 50Hz. The simulations are done for variable input voltages to verify our proposed scheme and to achieve objective function, shown in table 1. Results reflect that the harmonics in the current waveforms are reduced. Results are shown in fig. 7-13.

From results, fig. 7 shows that input voltage and current are sinusoidal. THD of line current is calculated and shown in results i.e. 5.20%. With this THD, power factor of the system is 0.998, shown in Table 1. The relation of THD and power factor is shown in below equations. THD of line current increases with increasing input voltage which means that power factor has inverse relation with input voltage shown in fig. 11.

*Power factor = Displacement factor*Distortion Factor* (23)

Where as

$$Distortion\ Factor = \frac{1}{\sqrt{1 + (THD)^2}} \quad (24)$$

Table 1. THD and Power Factor Analysis.

Voltage (V)		Current (A)		Power (W)		Power Factor	THD (%)
Input	Output	Input	Output	Input	Output		
90	398.5	18.7	7.21	1688	2877	0.998	5.20
110	399.6	18.4	7.37	2024	2945	0.996	8.67
150	400.5	16.6	6.94	2487	2770	0.987	15.92
170	399.8	16.9	7.03	2870	2801	0.98	20.17

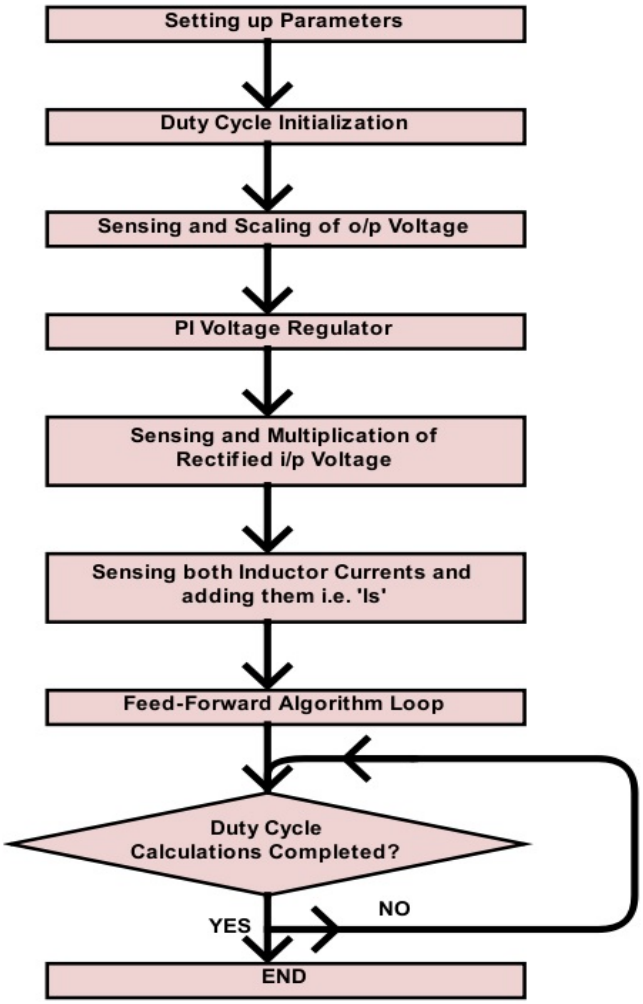

Figure 6. Feed-Forward Algorithm Flow chart Diagram.

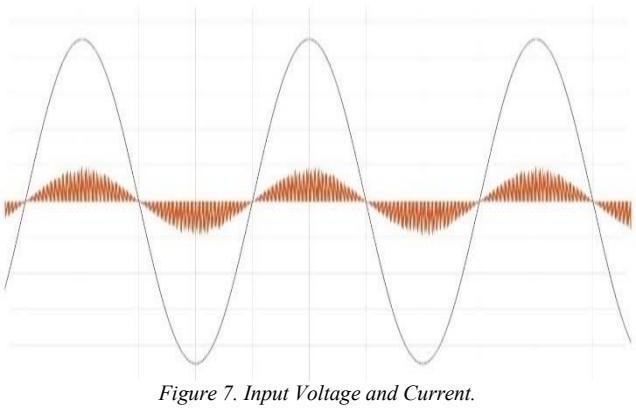

Figure 7. Input Voltage and Current.

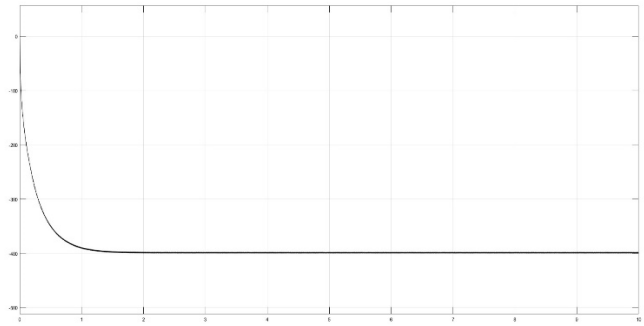

Figure 8. Output Voltage.

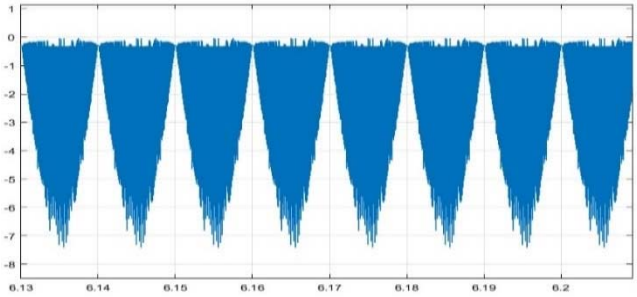

Figure 9. Output Current profile.

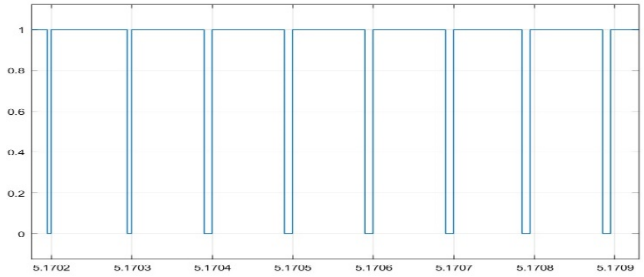

Figure 10. Gate Signals for Switches.

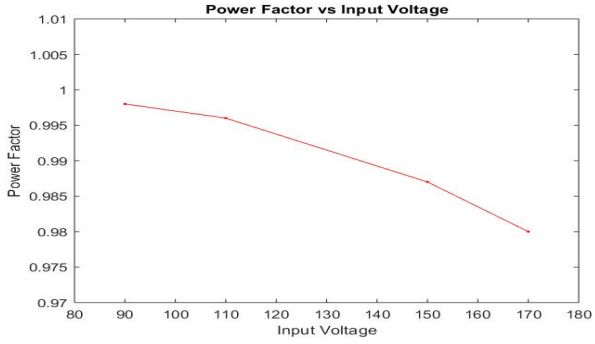

Figure 11. Power Factor Profile.

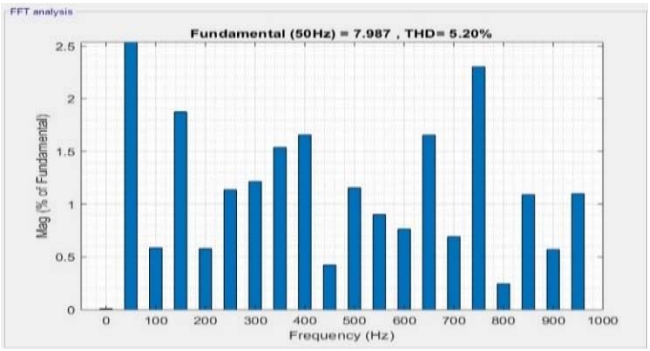

Figure 12. Total Harmonic Distortion THD.

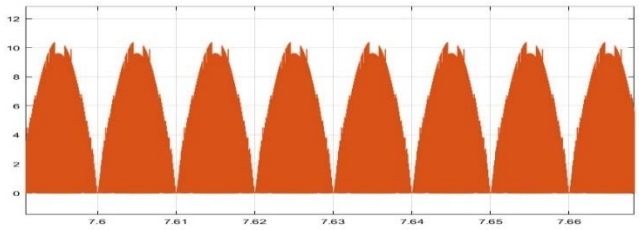

Figure 13. Inductor Current Profile.

VII. CONCLUSION

Digital feed-forward control for parallel connected PFCs, operating in CCM, is proposed in this paper. Buck-boost converter equations are used to derive the feed-forward algorithm in detail. The load current sharing and the voltage regulation performed by the feed-forward control method is verified by simulations. Duty cycles for the unity power factor are generated efficiently by the proposed scheme. Harmonics in the current are eliminated, making it in phase with the line voltage. Power factor is improved to unity.
Simulation results shows that the current is in phase with the input voltage. Proposed scheme performs better in both steady and transient state and can bring unity power factor of the system.

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