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50 GBd PAM4 transmitter with a 55nm SiGe BiCMOS driver and silicon photonic segmented MZM

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Abstract: We demonstrate an optical transmitter consisting of a limiting SiGe BiCMOS driver co-designed and co-packaged with a silicon photonic segmented traveling-wave Mach-Zehnder modulator (MZM). The MZM is split into two traveling-wave segments to increase the bandwidth and to allow a 2-bit DAC functionality. Two limiting driver channels are used to drive these segments, allowing both NRZ and PAM4 signal generation in the optical domain. The voltage swing as well as the peaking of the driver output are tunable, hence the PAM4 signal levels can be tuned and possible bandwidth limitations of the MZM segments can be partially alleviated. Generation of 50 Gbaud and 53 Gbaud PAM4 yields a TDECQ of 2.8 and 3.8 dB with a power efficiency of 3.9 and 3.6 pJ/bit, respectively; this is the best reported efficiency for co-packaged silicon transmitters for short-reach datacenter interconnects at these data rates. With this work, we show the potential of limiting drivers and segmented traveling-wave modulators in 400G capable short-reach optical interconnects.

1. Introduction

The ever-rising growth of the internet and its associated applications have pushed datacenters to deploy optical transceivers with continuously increasing performance. Recently, 200 Gb/s and 400 Gb/s standards were approved, requiring line rates of 26.5625 Gbaud PAM4 over 0.5, 2 or 10 km SMF and 53.125 Gbaud PAM4 up to 0.5 km SMF [1]. Standards employing 53.125 Gbaud PAM4 up to 2 and 10 km SMF are being developed [2]. Designing transceivers at 53 Gbaud proves to be a challenging task: low power, small footprint and manufacturability are key factors in the design. Transmitters based on silicon photonic modulators are very attractive since they offer low cost, high volume and high yield manufacturability of devices. Several silicon photonic PAM4 transmitters have already been shown [3–5]. While microring modulators and electro-absorption modulators may offer smaller footprints and a lower power consumption [3,4] compared to Mach-Zehnder modulators (MZMs), both have a limited optical bandwidth and introduce chirp which limits the fiber reach. Furthermore, ring modulators typically need additional control circuitry. Silicon photonic coherent transceivers (requiring MZMs) are already being deployed by industry [6].

Recent examples of MZM-based silicon photonic transmitters with integrated drivers can be found in [7–10]. In [7], a two channel open-drain CMOS driver integrated with a silicon IQ traveling-wave (TW) MZM capable of 40 Gbaud PAM4 and 28 Gbaud QPSK is presented. The

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authors of [8] use a 16-segment silicon lumped MZM with monolithically integrated driver, resulting in 25 Gbaud PAM4. With a 6-segment silicon lumped MZM driven by a BiCMOS driver, 60 Gb/s NRZ is obtained in [9], however optical-domain equalization was required. The authors of [10] demonstrate 34 Gbaud DP-16QAM with a silicon IQ TW MZM. From these papers, it becomes apparent that silicon transmitters employing TW MZMs generally have a higher bandwidth compared to their lumped segmented counterparts. However, their bandwidth is typically limited due to the electrical losses on the electrodes.

By splitting the long TW modulator into two shorter TW segments, the total loss on the segment electrodes can be decreased [11]. Hence the bandwidth of each segment is higher than the bandwidth of the initial long TW MZM. Compared to driving a single TW MZM (of length L) with a PAM4 signal, higher datarates can now be achieved by driving both segments (with a combined length L) using two binary signals. This technique also avoids a linear modulator driver for the long TW modulator. A linear driver consumes more power for the same voltage swing at the same datarate, while also requiring additional equalization to counteract the lower bandwidth of the longer modulator. In [11], 50 and 84 Gbaud PAM4 is generated using a TW MZM with two segments driven by binary signals. However, no dedicated modulator driver is integrated and digital signal processing is used to reach 84 Gbaud. The authors of [12] generate 28 Gbaud PAM4 with a two segment TW MZM monolithically integrated with CMOS drivers, the reported efficiency is 4.8 pJ/bit.

In this work, we generate ≥56 Gb/s NRZ and ≥50 Gbaud PAM4 using a two segment traveling-wave silicon photonic MZM co-packaged with a limiting SiGe BiCMOS driver. The power efficiency of the transmitter (driver & MZM) is 3.7, 3.9 pJ/bit and 3.6 pJ/bit for 56 Gb/s NRZ, 50 Gbaud PAM4 and 53 Gbaud PAM4 respectively. To the best of our knowledge, the reported power efficiency at 50 Gbaud and 53 Gbaud is the best reported efficiency for co-packaged silicon transmitters employing MZMs for short-reach datacenter interconnects.

This paper is organized as follows: Section 2 describes the four channel driver, while Section 3 encompasses the design and characterization of the MZM. The experiment setup and results are discussed in Sections 4 and 5.

2. SiGe BiCMOS modulator driver

The driver consists of four parallel channels capable of 60 Gb/s operation. As shown in Fig. 1(a), each channel contains an input stage followed by a line equalizer with tunable peaking (up to 10 dB), a limiting predriver and a limiting output stage with adjustable output swing and peaking. The tunable peaking at the input helps to alleviate bandwidth limitations of the cables, connectors and PCB traces leading to the driver. The adjustable output swing is used to optimize the PAM4 signal levels while the tunable peaking at the output stage can help compensating the possible bandwidth limitation of the modulator. By DC-coupling the modulator to the driver, the high-speed path can be made as short as possible and does not have to include any additional bulky external components (e.g. capacitors) that can degrade the performance.

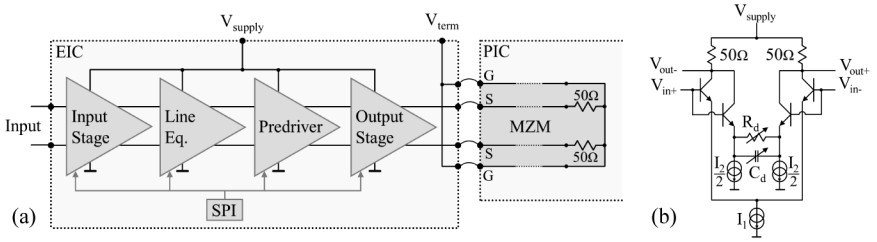

Fig. 1. (a) Simplified schematic of a single driver channel and the traveling-wave modulator DC-coupled to the channel. (b) Simplified schematic of the output stage.

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A simplified schematic of the output stage is shown in Fig. 1(b). The output stage consists of two parallel differential pairs: each pair has its own current source and one differential pair has additional emitter degeneration to introduce peaking in the frequency response. By tuning the current sources together (such that $I_1 = I_2$), the output swing can be tuned. By increasing I_2 and decreasing I_1, the peaked differential pair will become dominant leading to a more peaked response. By decreasing I_2 and increasing I_1, the peaked differential pair will become less dominant and the output stage will exhibit less peaking. Additionally, the emitter degeneration itself can be tuned to further increase or decrease the peaking. Remark that the amount of peaking not only depends on the settings, but also on the load impedance. Depending on the settings and load, it is possible to generate up to a few 100 mV of overshoot in the 2 $V_{pp,diff}$ NRZ eye.

If an NRZ input signal of 350 $mV_{pp,diff}$ is applied to the input, the output has a peak swing of 2 $V_{pp,diff}$ for a 100 Ω differential load. The differential in- and output impedance are both 100 Ω to minimize any reflections and to maximize the power transfer. The driver is designed for a 100 Ω differential load consisting of two 50 Ω loads that are connected to V_{term} through the driver, see Fig. 1. Typically, V_{term} is externally connected to V_{supply}. However if required, V_{term} can be chosen independently of V_{supply}. This allows tuning of the voltage at the driver's output stage, which in turn allows controlling the performance (speed versus available headroom) of the output stage's transistors. The peaking at the in- and output, and the currents in the output stage can be configured per channel using a serial digital (SPI) interface. The driver has a nominal supply voltage of 2.5 V. At the default settings, each channel consumes 180 mW. This increases to 200 mW at a supply voltage of 2.75 V. The driver hosting 4 channels is designed and fabricated in a 55 nm SiGe BiCMOS technology and measures 1.2 by 2.5 mm^2, the channel pitch is 375 μm.

3. Segmented traveling-wave MZM

3.1. Design of the MZM

The segmented MZM is designed on imec's iSiPP50G platform [13]. It consists of two parallel child MZMs where each modulator branch comprises two traveling-wave segments, see Fig. 2(a). One child MZM is not used and therefore biased at minimum transmission. The long and short segments are respectively used to generate the MSB and LSB of the PAM4 modulation. The cross-section in Fig. 2(b) shows that a coplanar stripline structure is used for the electrodes. The PN phase modulators are placed in series between the signal lines. In the center, a narrow inductive line is added to bias the PN junctions [14]. This allows to separate the high-speed path from the biasing, such that the high-speed operation can be optimized. We used the technology's standard dimensions and doping levels for PN phase modulators, however the electrodes are designed to work with our driver- and biasing-architecture. The width and spacing of the electrodes are chosen to obtain a differential characteristic impedance as close as possible to 100 Ω, the simulated characteristic impedance is around 75 Ω, depending on the PN bias voltage. The electrical diagram of a segment is shown in Fig. 2(c). The GSSG configuration and biasing are designed to be compatible with the driver (see Fig. 1).

Each signal line is terminated with an on-chip n-doped 50 Ω resistor (100 Ω termination in total). Thermo-optic heaters are used to bias the MZMs. Optical coupling is done through fiber grating couplers (FGCs) with around 5 dB insertion loss at 1550 nm and a 1 dB optical bandwidth of 35 nm. The complete structure (including the unused part) measures 1.3 by 2.5 mm^2. While the MZMs here are designed for C-band, conversion to O-band on imec's platform is straigthforward. The C-band PN phase shifters and O-band phase shifters have almost identical electrical characteristics, thus the electrical part is unaffected. The loss is very similar and the O-band phase shifter has a slightly lower V_π. The C-band and O-band grating couplers have similar insertion loss [13]. The unused child MZM is identical to the one that has just been described. Together, they could be used for 16QAM generation.

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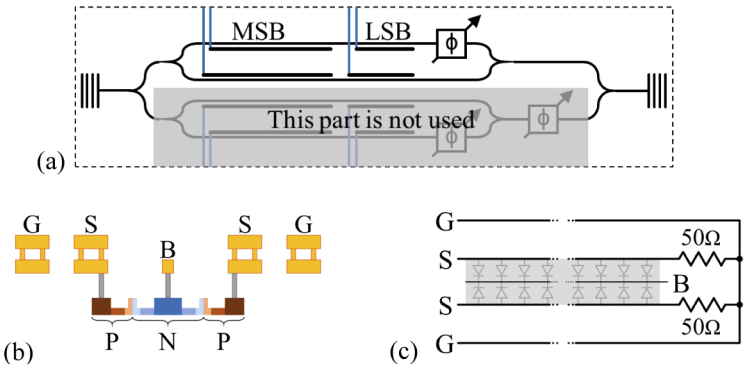

Fig. 2. (a) optical connection diagram of the full MZM, (b) cross section of a single segment, (c) electrical diagram of a single segment.

3.2. *Measured MZM characteristics*

The small and large segments are 1.2 and 2.25 mm long. All measurements are conducted at a wavelength of 1550 nm. The measured $V_\pi L_\pi$ (at DC) and optical attenuation for a reverse bias of 1, 2 and 3 V over the PN junction is 19.2, 22.1 and 23.5 Vmm and 1.77, 1.69 and 1.61 dB/mm respectively. The V_π and attenuation of the small and large segment at a reverse bias of 2 V are respectively 18.4 V and 2 dB and 9.8 V and 3.8 dB, resulting in a total V_π of 6.4 V and 5.8 dB attenuation. The magnitude of the measured input impedance and normalized electro-optic responses of the MSB and LSB segments are given in Fig. 3. As expected, the input impedance shows significant variation due to the mismatch between the characteristic impedance of the transmission line and the termination. For a 100 Ohm port impedance, the reflection coefficient is below than −10 dB over the full range. The periodicity of the ripple is smaller for the MSB segment as it is longer than the LSB segment. At low frequencies, the impedance is around 100 Ohm, thus the DC operation of the driver will not be affected. The impedance variations will

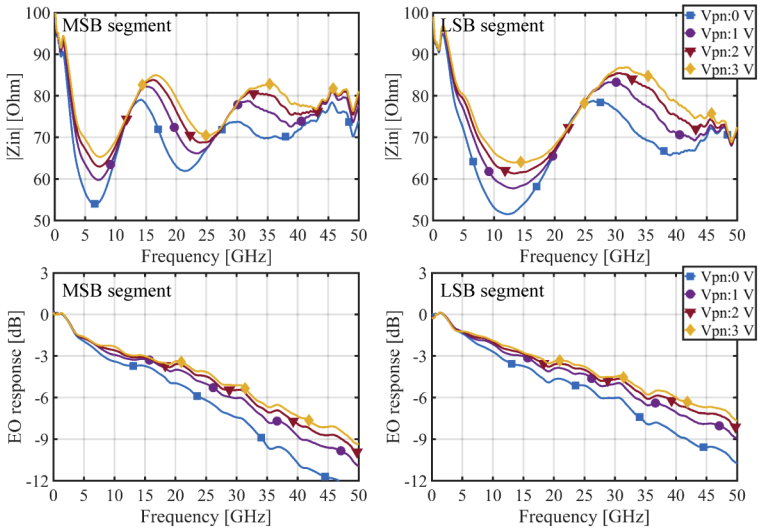

Fig. 3. Magnitude of the measured input impedance and normalized electro-optic response of the long segment (MSB) and short segment (LSB) for various PN reverse biasing voltages.

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affect the high-frequency response. Looking to the normalized electro-optic responses of the MSB and LSB segments, for a reverse bias voltage between 1 and 3 V, the 3dB electro-optic bandwidth of the large segment is 11-15 GHz and 15-17 GHz for the small segment. A higher biasing voltage decreases the PN junction capacitance resulting in an increased modulation bandwidth, but at the cost of an increased $V_\pi L_\pi$. The 1-2 dB drop in the low GHz-range is caused by the mismatched termination impedance of the modulator, an effect that is also illustrated in [15]. Lowering the termination resistor to 75 Ω will result in a flatter input impedance and will lower the drop in the EO response at low frequencies. On it's turn, this will enhance the bandwidth significantly. Remark that in an assembly the bandwidth can be increased due to peaking introduced by the driver, the inductive peaking from the bondwires and the interaction between the driver and the frequency dependence of the modulator input impedance.

4. Experiment setup

The EIC and PIC are glued on a custom PCB and wirebonded together, as illustrated in Figs. 4(b) and (c). The inputs of the EIC are wirebonded to high-speed transmission lines. The length of the wirebonds is approximately 250 μm. High-speed connections to the PCB are done through miniSMP connectors, see Fig. 4(b). The decision to DC-couple the modulator to the driver and to separate the PN junction biasing from the high-speed signal path, simplifies the assembly significantly. The high-speed path contains a minimal amount of parasitics that can deteriorate the performance and only some additional DC-traces are required for the power supply of the EIC, the digital control of the EIC and the biasing of the modulator. As described earlier, the full structure consists of two parallel segmented MZMs. Only one is used for the experiments in this work.

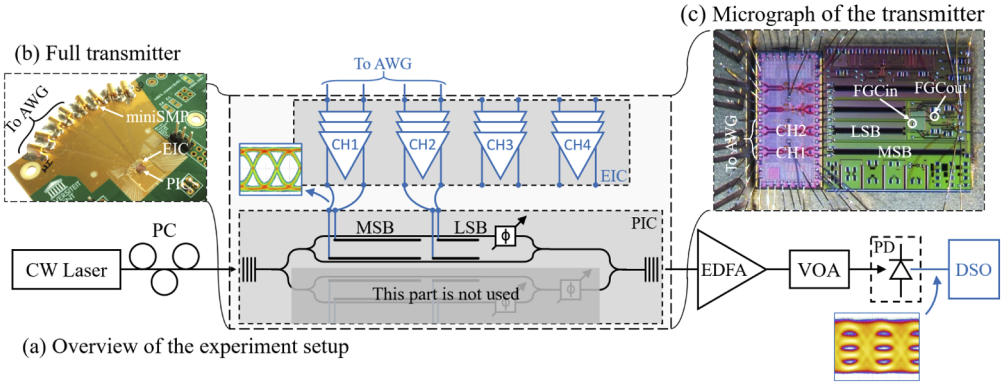

Fig. 4. (a) Experiment setup: CW laser set to 1550 nm, PC: polarization controller, AWG: arbitrary waveform generator, EDFA: erbium doped fiber amplifier, VOA: variable optical attenuator, PD: DC-coupled 70 GHz photodiode, DSO: 70 GHz digital sampling oscilloscope. (b) Picture of the full transmitter. (c) Micrograph of the wirebonded EIC and PIC on a custom PCB.

The full experiment setup is shown in Fig. 4(a). A CW laser is set to 1550 nm and 13 dBm output power. As the FGCs of the PIC are polarization dependent, a polarization controller is added before the fiber probe. The output of the PIC goes to an EDFA and VOA that amplifies the optical signal to an average power of 8 to 9 dBm, and is then coupled into the DC-coupled 70 GHz photodiode. The total insertion loss of the PIC is around 24.8 dB with a reverse bias of 2 V on the PN junctions, of which 2x5 dB from the FGCs, 2x3 dB because one child MZM is not used, 3 dB because the active MZM is biased at the quadrature point and 5.8 dB attenuation from the PN junctions reverse biased at 2 V. Note that by using more efficient edge couplers (typ. 2

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dB loss [13]) and by omitting the unused child MZM, the insertion loss can be improved by 12 dB. With the given laser output power of 13 dBm, this would result in a launch power of 0.2 dBm, which is compliant with both the IEEE 802.3bs 400-GBase DR-4 standard [1] (launch power between −2.9 and 4.2 dBm) and the MSA 400G-FR4 standard [2] (launch power between −3.3 and 3.5 dBm). The 70 GHz photodiode used in the setup is internally matched to 50 Ω and connected to a 70 GHz digital sampling oscilloscope (DSO). The 92 GS/s arbitrary waveform generator (AWG) generates two identical PRBS15 streams with a Gaussian pulse shape. We have selected the PRBS15 sequence as this is the longest sequence that still fits in the AWG memory. The AWG is set to an output voltage of 400 $mV_{pp,diff}$.

5. Results

To assess the effect of the integration and the loading of the modulators on the driver channels, the measured large-signal S-parameters of the driver were combined with the EO-response measurements of the modulators. The interconnecting bondwires were assumed to be 250 pH. As such, the whole cascade could be simulated using measured data for the driver and modulators. The results can be found in Fig. 5. For the driver measurements, the default driver settings were used and the driver power supply was set to 2.5 V. It is observed that by increasing the input power from −10 dBm to −4 dBm, the gain drops from 16.8 dB to 12.0 dB but the bandwidth increases from 36.3 GHz to 43.8 GHz. In Fig. 5(b), the cascade of the driver response from Fig. 5(a) with the MSB segment is shown. The bondwires between the driver and the segment were assumed to be 250 pH. At −4 dBm input power to the driver, the bandwidth is between 11.2 and 13 GHz for a reverse bias between 1 and 3 V over the PN junction. However, the roll-off is very slow: at 25 GHz, the response dropped between 3.8 and 4.7 dB with respect to DC. Thus by configuring the driver to introduce around 1-2 dB of peaking at 25 GHz, the 3dB-bandwidth of the cascade can be increased to 25 GHz. The results of the cascade of the driver with the LSB segment interconnected using 250 pH bondwires show a similar trend: the 3 dB bandwidth is between 14.8 and 16.8 GHz. But at 25 GHz, the response dropped only between 3.8 and 4.3 dB with respect to DC, thus 1-1.5 dB of peaking introduced by the driver at 25 GHz is sufficient to obtain a bandwidth of 25 GHz for the full cascade.

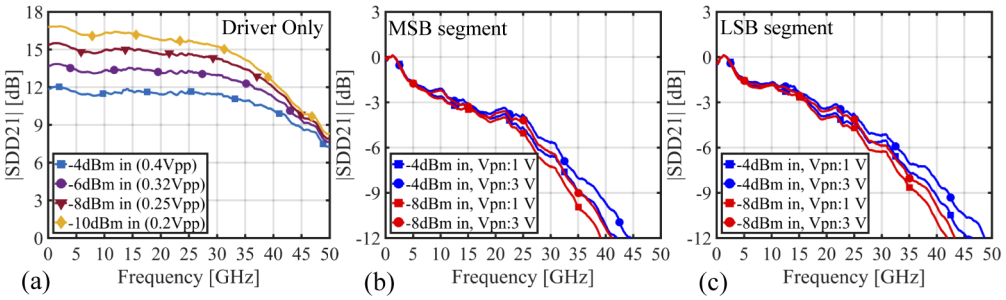

Fig. 5. (a) Large-signal differential S-parameters (S_{DD}) of the driver for input powers between −10 and −4 dBm, (b) and (c) cascade of the large-signal differential S-parameters of the driver and the EO-response of the MSB and LSB with 250 pH bondwires as interconnection between the driver and MZM, normalized at 1 GHz.

For the data experiments, the transmitter was first tested by generating 50, 56 and 60 Gb/s NRZ using only one driver channel and the MSB segment (length 2.25 mm). The adjustable input peaking of the driver is used to compensate for the RF attenuation of the cables, connectors and PCB traces. The eye diagrams can be found in Fig. 6. The average optical input power to the PD is 8 dBm. For 50, 56 and 60 Gb/s, V_{term} and V_{supply} are 2.75 V. The PN junction was biased around 1 V for 50 and 56 Gb/s to maximize the extinction ratio (ER) by keeping $V_\pi L_\pi$ as low as

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possible. As the low reverse bias voltage of 1 V decreases the EO-bandwidth of the modulator, the driver is configured to introduce some peaking at its output. However, it is also expected that the driver-modulator interface introduces some additional peaking due to the presence of the inductive bondwires and because the modulator input impedance varies with frequency. As the driver is nonlinear, it is very difficult to quantify this effect. At 60 Gb/s, the driver cannot introduce sufficient peaking, so we increase the reverse bias of the PN junction to 2 V in order to raise the modulator bandwidth (see Fig. 3). The power consumption of the active driver channel and MZM is 205 mW for 50 and 56 Gb/s, resulting in a power efficiency of 4.1 and 3.7 pJ/bit respectively. At 60 Gb/s, the power efficiency improves to 3.5 pJ/bit.

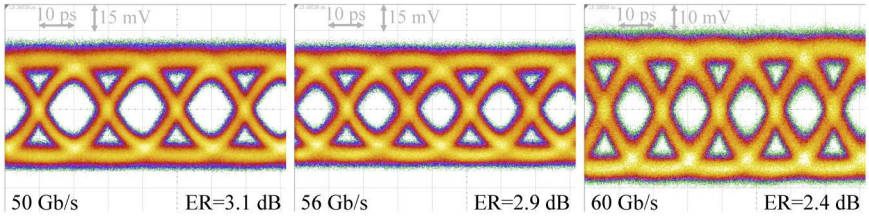

Fig. 6. Eye diagrams of NRZ generation using the MSB only.

In the next step, both the MSB and LSB segments are driven by the same PRBS15 sequence. The delay between the MSB and LSB is sufficient to decorrelate both NRZ streams for the PAM4 signal. Some skew is added between the signals to align the edges of the LSB bitstream with the MSB bitstream. In our experiment, this skew was tuned using the AWG, however, delay cells could be added to the driver input to align the edges [16]. In a transceiver, additional control loops will be required to tune both the gain and delay of the MSB. A system similar as used in [17] could be used. A monitor photodiode can be added to the modulator, the output of this photodiode is typically used to keep the modulator biased at it's correct operating point. But it can also be used to align the MSB and LSB and even to calibrate the MSB and LSB signal swing. To quantify the quality of the generated PAM4 signal, TDECQ is used [1]. This is a measure of the vertical eye closure of an optical transmitter when the signal is sent through a worst-case optical channel and is measured through an optical to electrical (O/E) converter. It can be shown that TDECQ is roughly proportional to the receiver power penalty [1]. An in-depth discussion about TDECQ can also be found in [18]. The IEEE 802.3bs 400-GBase DR-4 standard and the MSA 400G-FR4 standard require a TDECQ below 3.4 dB [1,2], the target symbol error rate for minimizing the TDECQ was 4.8×10^{-4}. The complete procedure of determining the TDECQ is done automatically in the Keysight DCA-X 86100D. The eye diagrams at 40 Gbaud before and after the TDECQ processing are shown in Fig. 7. During the measurements, no detrimental impact from crosstalk between the MSB and LSB was observed.

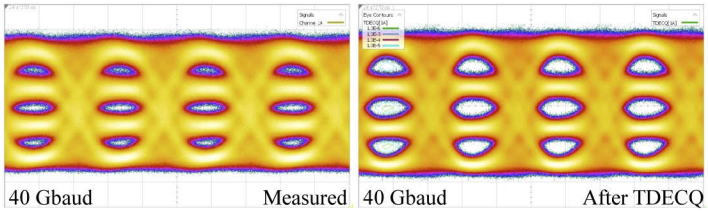

Fig. 7. 40 Gbaud PAM4 before and after the 4th order Bessel filter and 5-taps FFE for TDECQ measurements. The ER before processing is around 4.5 dB.

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The eye diagrams at 40 Gbaud before and after the TDECQ processing are shown in Fig. 7. The significant improvement can be explained by the slow roll-off of the electro-optic response of the modulator (Fig. 3), which can be readily compensated with the 5-taps FFE. This FFE is part of the TDECQ measurement procedure applied by the measurement equipment.

The eye diagrams at 40, 50 and 53 Gbaud after TDECQ analysis are shown in Fig. 8. Again, V_{supply} was 2.75 V, but V_{term} and the reverse bias of the PN junction were set to 3.1 V and 3.5 V respectively to maximize the transmitter bandwidth. Compared to a reverse bias of 3 V, this led to a rather modest improvement of 0.1-0.2 dB in TDECQ, leading us to the conclusion that the changes in V_π, loss and bandwidth are very small. Remark that the output swing of the LSB driver channel was optimized to obtain equally-spaced PAM4 levels, this results in an relative level mismatch (RLM) higher than 0.92 for all cases. The ER was in all cases around 4.5 dB, compliant with both IEEE 802.3bs 400-GBase DR-4 standard [1] and the MSA 400G-FR4 standard [2], both require and ER of at least 3.5 dB. The average optical power on the PD was 8 dBm for 40 and 50 Gbaud and 9 dBm for 53 Gbaud. At 40 and 50 Gbaud, the TDECQ is 1.54 dB and 2.78 dB with a total power consumption of 374 and 386 mW. At 40 Gbaud, the MSB and LSB driver channels are consuming 199 mW and 175 mW respectively. While at 50 Gbaud, the MSB and LSB driver channels are consuming 201 mW and 184 mW. The LSB channel is consuming less power as the swing has been slightly decreased to tune the PAM4 levels and peaking is decreased since the LSB modulator has a higher bandwidth. This results in a power efficiency of 4.7 pJ/bit and 3.9 pJ/bit at 40 and 50 Gbaud. The measurement at 50 Gbaud was redone with TDECQ threshold optimization for the PAM4 levels. The thresholds were allowed to deviate from their ideal levels over a range equal to 1% of the outer OMA. This improves the TDECQ from 2.78 dB to 2.52 dB. For 53 Gbaud, with threshold optimization, a TDECQ of 3.78 dB was measured, the power efficiency is 3.6 pJ/bit. The driver uses the same settings at 50 and 53 Gbaud, thus the power consumption is identical. Both the IEEE 802.3bs 400-GBase DR-4 standard [1] and the MSA 400G-FR4 standard [2] require a TDECQ below 3.4 dB. While the 40 Gbaud and 50 Gbaud PAM4 comply, the TDECQ at 53 Gbaud is 0.4 dB too high. However, by redesigning the MZM as explained in Section 3 and 4, the bandwidth can be enhanced and the insertion loss can be decreased. It is expected that the changes will have a very limited effect on the power efficiency. On one hand, the power consumption decreases as the driver needs to introduce less peaking and V_{term} can be lowered to keep the collector voltage of the output stage constant. On the other hand, the lower load impedance causes the voltage swing to drop. This will have to be compensated by increasing the output stage current and hence the power consumption. We expect that these effects will cancel each other out almost completely. Improving the insertion loss does not affect the driver performance, but enhances the noise performance of the link. These changes should enhance both the OMA at the output of the transmitter as well as the TDECQ such that OMA, TDECQ and OMA-TDECQ specification of the referred standards are all met.

A benchmark comparison to several implementations of optical transmitters employing integrated MZMs co-packaged with drivers is presented in Table 1. As can be observed, the transmitter presented in this paper features the best power efficiency for the given datarate. In [19], a full transceiver is demonstrated at 28 Gbaud PAM4 using the same BiCMOS technology, only the power of the output stage was taken into account to calculate the efficiency here. The authors of [7] show a very good power efficiency, but reach only up to 40 Gbaud using a linear driver in a 65 nm CMOS technology. However, an open-drain output stage is used. While saving on power consumption, the driver is much more sensitive to interconnection parasitics and variations in the load impedance. A linear driver without modulator is presented in [20]. The driver achieves a similar datarate and swing as our architecture, but at a much higher power consumption. A large-swing linear driver capable of 64 Gbaud PAM4 and 56 Gbaud PAM8 is demonstrated in [21]. However, no experiments with integrated MZMs are shown. While a better power

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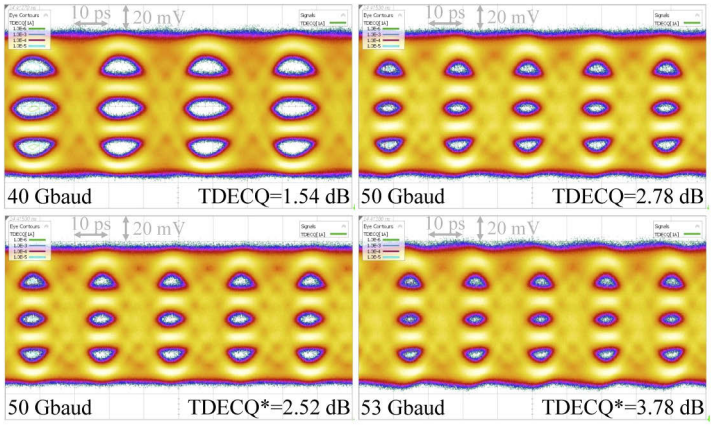

Fig. 8. Eye diagrams and TDECQ of 40, 50 and 53 Gbaud. TDECQ* means the PAM4 threshold were optimized for minimal TDECQ.

efficiency for a higher datarate is obtained for the coherent transmitter in [22], the transmitter has around 3 dB peaking in its EO response, and quite some equalization will be required to flatten this response and avoid degradation in the PAM4 eye. In the case of [22], this equalization is provided by the digital signal processing required for the coherent experiments. This is undesired for short-reach datacenter interconnects employing PAM4, as additional equalization increases the total link power consumption and the link latency. No transmission experiments without additional DSP are shown in [22], prohibiting a correct comparison. Comparing the presented transmitter to the other references, we can show the best power efficiency at 50 and 53 Gbaud thanks to the use of the limiting driver coupled to a segmented traveling-wave modulator and thorough co-design of the driver and modulator.

Table 1. Comparison between PAM4 transmitters using integrated Mach-Zehnder modulator and drivers.

Ref.	Implementation Details	Datarate [Gbaud]	Output [$V_{pp,diff}$]	Efficiency [pJ/bit]	Driver Technology
[19]	3 seg. Si TW MZM, flipchipped driver	28	-	5.2	55 nm BiCMOS
[12]	2 seg. Si TW MZM, monolithic integrated driver	28	2.2	4.8	90 nm CMOS
[23]	2 seg. lumped Si MZM, flipchipped driver	28	1	1.59	28 nm CMOS
[7]	Single Si TW MZM, wirebonded linear driver	40	2	2.25	65 nm CMOS
[20]	Linear driver only	56	1.8	7.5	0.25 um InP DHBT
[21]	Linear driver only (PAM4/PAM8)	64/56	4.8/3.8	6.4/4.9	55 nm BiCMOS
[22]	InP TW MZM, wirebonded linear driver	64	2	1.4	65 nm CMOS
This work	2 seg. Si TW MZM, wirebonded driver	50	2	3.9	55 nm BiCMOS
		53	2	3.6	

6. Conclusion

We demonstrate a transmitter consisting of a segmented traveling-wave silicon MZM wirebonded to a custom designed SiGe BiCMOS driver chip. The MZM is split into a long and a short traveling-wave segment to enhance the bandwidth and to eliminate the use of power hungry linear modulator drivers. The driver and modulator are co-designed in order optimize the high-speed operation as much as possible and to minimize the complexity of the assembly. Using only the long segment, we demonstrate 56 Gb/s NRZ with an ER of 2.9 dB and a power efficiency

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of 3.7 pJ/bit and 60 Gb/s NRZ with an ER of 2.4 dB and a power efficiency of 3.5 pJ/bit. By using both segments, 50 Gbaud PAM4 and 53 Gbaud PAM4 can be obtained with an ER of around 4.5 dB with a TDECQ of 2.78 dB and 3.78 dB. The power efficiency is 3.9 pJ/bit and 3.6 pJ/bit respectively. The ER at 50 and 53 Gbaud is compliant with both the IEEE 802.3bs 400-GBase DR-4 standard [1] and the MSA 400G-FR4 standard [2]. The obtained power efficiency is the best at 50 and 53 Gbaud PAM4 for silicon photonic transmitters using MZMs for short-reach datacenter interconnects. With this work, we have shown the potential of silicon optical transmitters using limiting drivers and segmented traveling-wave modulators for 400G capable short-reach optical interconnects employing PAM4.

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Disclosures

The authors declare that there are no conflicts of interest related to this article.

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