Analog I/Q FIR Filter in 55nm SiGe BiCMOS for 16-QAM Optical Communications at 112 Gb/s

M. Verplaetse, J. Lambrecht, M. Vanhoecke, L. Breyne, H. Ramon, P. Demeester and G. Torfs

***Abstract*—We propose a novel implementation of a complex analog equalization filter for the compensation of frequency dependent variations in coherent optical links. The analog compensation filter can be used in coherent-lite optical communication links where digital signal processing (DSP) is removed to limit the complexity and power consumption. In these links, the filter can compensate electrical bandwidth limitations and distortion introduced by chromatic dispersion in the fiber. The complex filter is implemented by combining 4 distributed analog finite impulse response (FIR) filters to obtain the necessary response. The filter delays are implemented using active delay cell structures to create a compact solution. The analog filter is implemented in a 55nm BiCMOS technology and consumes 185 mW core power for 5 complex filter taps. Performance is evaluated using S-parameter measurements, noise and linearity measurements and real-time system experiments using 112 Gb/s 16-QAM modulated signals.**

***Index Terms*—Analog Equalization, Coherent, Data center, Dispersion, MIMO, EDC**

I. Introduction

COHERENT communication schemes both in electrical and optical links are one of the most important and well-known techniques to increase spectral efficiency, receiver sensitivity and frequency selectivity. Extra, for optical communication links, it provides a method for linear detection to enable efficient channel compensation mechanisms. Due to the introduction of digital signal processing (DSP), the throughput of coherent links has increased significantly in the past decades. In today's long-haul optical transceivers, it is impossible to imagine coherent links without DSP as even a small sensitivity improvement may increase the reach substantially [1]. However, the introduction of DSP inevitably leads to a high power consumption scaling with the baudrate (DSP consumes approximately 50% of the total power in long-haul links [2]) and increases the latency over the link.

In today's optical intra- (0-10 km) and inter (10-80 km) datacenter links and passive optical networks (PON), design challenges are different compared to long-haul interconnects. Cost, latency, compactness and power consumption are more important, which cause intensity modulation and direct detection (IM/DD) to be favored over coherent transmission schemes if possible. To answer the demand for higher bit rates per wavelength needed for future 400 Gb/s connections, higher order pulse amplitude modulation formats (PAM) will have to be adopted in IM/DD. This increased complexity causes reduced power budgets and increased sensitivity to bandwidth limitations in the link. The question arises today whether IM/DD can still be scaled towards future 800 Gb/s and even 1.6 Tb/s interconnects. One of the possible solutions would be to use coherent communication. To replace today's IM/DD links with coherent schemes, the problem of increased latency and power consumption due to DSP should be resolved. Conventional DSP solutions require accurate high speed ADCs. State-of-the art reported ADC designs are presented in [3] and [4] consuming respectively 0.95 and 0.7 W. To avoid these consuming ADCs, several solutions are introduced in [1], [5]–[7] and [8] to create 'Coherent-lite' transceivers. These systems try to take advantage of a limited amount of channel impairments to either reduce/simplify the amount of DSP [8] or remove it [1][6] by moving crucial signal processing steps to the analog domain. A similar shift in processing from the digital to the analog domain is successfully proposed in recent 60 GHz wireless links [9]–[11].

Signal processing that provides electronic compensation of dispersion (EDC) and other linear bandwidth limiting effects is important to increase the reach in coherent links. This equalization step is ideally suited to be shifted to the analog domain by the introduction of analog I/Q (complex) finite-impulse response filters. Reported designs of complex analog finite impulse response (FIR) filters today are limited to lower baudrates (e.g. 5 Gbaud with 384 taps [11]) or have a limited amount of taps (e.g. 25 Gbaud with 2 taps [6]) due to the increased complexity compared to state-of-the-art real valued analog FIR filters (e.g. [12], [13]). In this work, we implement an analog FIR filter with both the capability to handle high baudrates (28 Gbaud) and to compensate longer channel responses by employing 5 complex FIR taps. This is possible by using compact active delay cell circuits in combination with a distributed FIR filter topology.

In Section II, we introduce analog coherent transmission systems in general together with the necessary analog equalization filter. In Section III, the actual filter architecture and circuit implementation in a 55nm BiCMOS technology is discussed. Section IV focuses on the characterization of the designed circuit and the performance in system experiments.

II. Analog coherent transmission system

The system overview of a conventional (dual polarization) optical coherent link can be found in Fig. 1. Transmission

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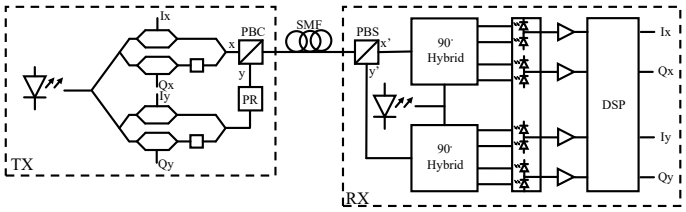


Fig. 1. System overview of a dual polarization coherent link.

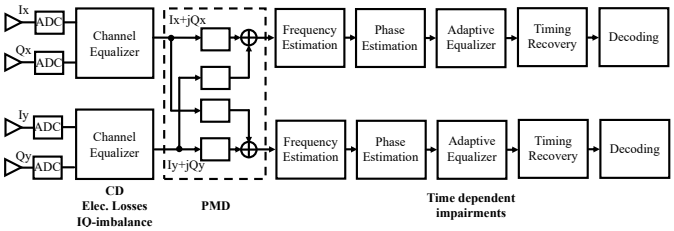


Fig. 2. Example DSP architecture for coherent optical dual polarization links [14]. Polarization mode dispersion (PMD).

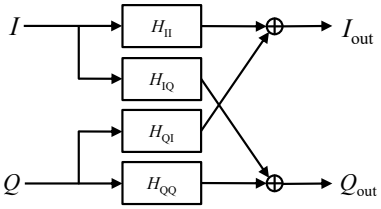


Fig. 3. Filter implementation of a complex channel equalizer.

in this system makes use of four degrees of freedom in the optical fiber, two phases of the electric field (I and Q) and two polarizations (x and y polarization). At the transmitter (TX), a low linewidth laser generates the optical carrier on which the data will be modulated. Throughout the paper, it is assumed that the laser emits wavelengths in the C-band (1530 – 1565 nm) as this transmission band yields the lowest fiber losses and a wide variety of optical components are available at this band. In the dual polarization IQ modulator, the laser light is first split and sent through single IQ modulators. After modulation, one of the signals is send through a polarization rotator (PR) to create the x and y polarization. Next, both optical signals are combined with a polarization beam combiner (PBC) and sent through a single mode optical fiber (SMF). At the receiver (RX), the light is split into its 2 polarizations. Each polarization is split into its I and Q components by using a 90° hybrid, balanced photodiodes (PD) and a laser source. After detection, 4 electrical signals are obtained, commonly processed further by DSP to compensate the link and demodulate the signal.

An example of the DSP steps in today's dual polarization (optical) coherent receiver are found in Fig. 2 [14]. In [1], [6] and [8], several solutions are proposed to create complete analog links avoiding all the steps in the DSP of Fig. 2. In this paper, we provide a solution to shift the channel equalization (and adaptive equalization) of Fig. 2 in front of the ADC. This analog channel equalizer could be used as an addition to proposed DSP-free links to increase the operating range as no channel compensation is considered in these references. However, it could also be used in combination with systems still using limited DSP where the channel equalization is removed from the DSP. This will yield a reduction in latency, power reduction in the DSP and requires a smaller dynamic range and resolution in the used ADCs [15]–[17]. From this point on, a single polarization link is assumed in the discussion and hence only a single channel equalizer is considered. Using coherent-lite links, the extension towards dual-polarization links can be done assuming two channel equalizer filters. This is possible as polarization rotation becomes the sole polarization dependent impairment that needs to be compensated [1]. This compensation could for example be done by using low-speed optical polarization controller circuits as proposed in [1] and [8].

A. Channel equalizer

The channel equalizer can be used to compensate frequency dependent variations. The most important frequency dependent mechanism which limits the transmission distance is the chromatic dispersion (CD) of the fiber. Based on the propagation equation of a pulse in a single-mode fiber [18], the frequency response of the fiber in the presence of CD can be calculated. The chromatic dispersion in the fiber is modeled by the dispersion coefficient D_{smf} and its small variation over wavelength by the dispersion slope S_{smf} which is neglected in this discussion. Doing so, the CD frequency response in function of the fiber length L is given in Eq. (1) with λ the center wavelength and c the speed of light.

$$H_{\mathrm{CD}}(\omega, L) = \exp(-j\frac{D_{\mathrm{smf}}\lambda^2\omega^2 L}{4\pi c}) \tag{1}$$

In this paper, transmission at a wavelength of 1550 nm (C-band) is used as an example for a chromatic dispersive channel. At this wavelength, the value of the dispersion coefficient D_{smf} is approximately equal to $16\frac{\mathrm{ps}}{\mathrm{nm\ km}}$. The complex transfer function in Eq. (1) introduces a frequency dependent phase rotation which should be compensated by the complex channel equalizer at the receiver to allow correct demodulation. A complex equalizer filter defined as $H_{\mathrm{Re}} + jH_{\mathrm{Im}}$ must operate on a complex input signal defined as $I + jQ$ which leads to 2 real valued input signals I and Q. Now, filtering can be implemented by a combination of 4 different subfilters, which are independent linear real valued filters (H_{II},H_{IQ},H_{QI},H_{QQ}) connected as in Fig. 3 and yielding the filter equations in Eq. (2) ($*$ = convolution):

$$\begin{aligned} I_{\mathrm{out}}(t) &= H_{\mathrm{II}}(t) * I(t) + H_{\mathrm{QI}}(t) * Q(t) \\ Q_{\mathrm{out}}(t) &= H_{\mathrm{QQ}}(t) * Q(t) + H_{\mathrm{IQ}}(t) * I(t) \end{aligned} \tag{2}$$

If the transfer function of $H_{\mathrm{IQ}} = -H_{\mathrm{QI}} = H_{\mathrm{Im}}$ and $H_{\mathrm{II}} = H_{\mathrm{QQ}} = H_{\mathrm{Re}}$, the filter in Eq. (2) behaves as a linear complex filter. In today's DSP design, this complex filter is either implemented as a time-domain finite impulse response (FIR) filter or implemented in the frequency domain.

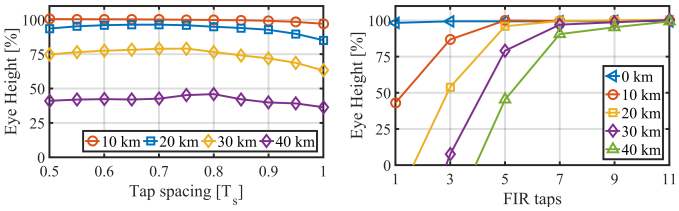


Fig. 4. Vertical eye height at the output of the FIR filter for different lengths of fiber in function of the tap-to-tap spacing when 5 taps are used (a) and the different number of used taps (with tap-to-tap spacing= $3/4$ T_s) (b) using QPSK modulation at 28 Gbaud (Raised-cosine pulse, $\alpha = 0.5$).

B. Time-domain FIR-filter specifications

To design an analog time-domain FIR filter, the amount of (complex valued) taps and the tap spacing are important parameters as they will limit the theoretical performance. As stated in [19], equalization performance drops quickly if the tap spacing increases beyond the symbol period, as it becomes more difficult to provide sufficient spectral control around and above the Nyquist frequency of the data in the link. Depending on the used pulse shape, the communication link becomes more and more susceptible to variations in the spectral content above the Nyquist frequency. To have increased control over these frequencies, the tap-to-tap delay should be reduced. On the other hand, one intends to keep the tap spacing as large as possible such that a longer physical impulse response can be obtained with the same number of taps. To support this reasoning, an optical link simulation in C-band at a baudrate of 28 Gbaud is performed where the tap spacing is varied for different fiber lengths. In Fig. 4a, the vertical eye opening on either the I or Q output of the optimized filter when using QPSK modulation are shown for an example number of 5 taps (dispersion coefficient $D_{\mathrm{smf}} = 16\frac{\mathrm{ps}}{\mathrm{nm\ km}}$ at 1550 nm, Raised-Cosine pulse, $\alpha = 0.5$). The eye height in Fig. 4a shows a limited variation in function of the tap spacing. For the shorter fiber spans, the optimal delay lies more towards a tap-to-tap spacing of $1/2$ T_s because the filters are sufficiently long and extra frequency control can be used to increase the eye height. However, for longer fiber spans requiring longer filter responses, the optimum range shifts towards $3/4$ T_s. To optimize performance for the longest fiber lengths, a delay value around $3/4$ T_s appears to be a reasonable choice. With this value, the performance in function of the number of taps is simulated in Fig. 4b. In the case of 28 Gbaud communication, the filter can compensate the CD in a 20 km fiber (in C-band) with only a limited penalty. If longer transmission distances are required, a FIR filter with more taps will be necessary. Additionally, the limited variation in function of the tap spacing in Fig. 4a gives an indication that small variations in the tap spacing, for example due to PVT variations, will have a limited influence on the performance.

III. System Architecture and Circuits

In the past, several analog FIR filter architectures have been reported in literature. Most of them are single input single output FIR filters used in wired and direct detection optical links. Two main FIR architectures are used in previous designs, respectively direct and distributed FIR implementations. Recent direct FIR implementations can be found in [9], [11], [12] and [19]. The main limiting structure in direct FIR filters is the summation node for all filter taps. The bandwidth reduces when increasing the number of taps which limits the maximal baudrate. To solve the scalability, distributed FIR filters are introduced (e.g. in [20], [21]), providing a distributed summation. As we intend to implement a complex FIR filter, complexity increases even more and directs us to the use of a distributed filter.

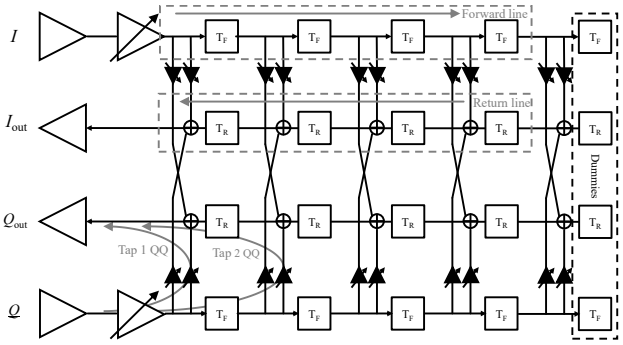


Fig. 5. Detailed single-ended equivalent block diagram of the IQ equalizer with the filter VGAs marked in black.

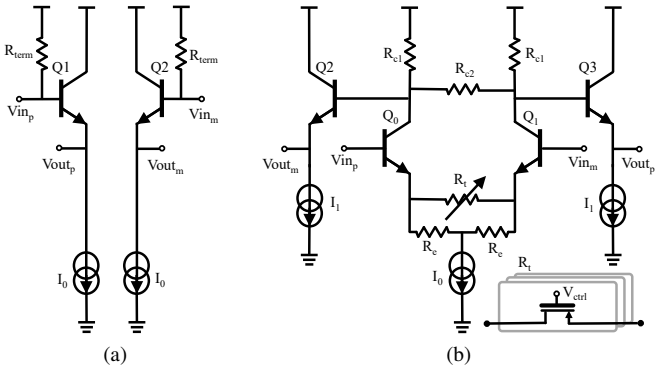


Fig. 6. Schematic of the 100 Ω differential input interface and emitter follower (a) followed by the variable gain stage (b).

The proposed distributed 5-tap FIR architecture can be found in Fig. 5. It shows two input stages (I and Q) followed by a variable gain stage, the analog filter itself and two 50 Ω output drivers (outputs I_{out} and Q_{out}). For clarity, Fig. 5 shows a single-ended circuit, in reality a fully differential implementation is used. Subfilters H_{II} and H_{IQ} (H_{QQ} and H_{QI}) share the same delay line at the input, addressed further as the 'forward' delay line with a delay value of T_{F}. Subfilters H_{II} and H_{QI} (H_{QQ} and H_{IQ}) share the same delay line at the output of the filter, addressed as the 'return' delay line with a delay value of T_{R}. The FIR filter tap-to-tap delay is determined by $T_{\mathrm{F}} + T_{\mathrm{R}}$. In Fig. 5, dummy cells are visible which make sure that every tap has the same load. In a future design, these dummies can be replaced by passive variants.

A. Input stage

To capture both the I and Q signals on the chip, an input stage implementing a 100 Ω differential input impedance is required. In Fig. 6a, an emitter follower (EF) is used to buffer the incoming signal on chip. The differential termination resistance of 100 Ω is obtained by placing a termination resistor $\mathrm{R_{term}} = 50\ \Omega$ between the separate input lines and the supply. In this way, both the differential mode and common mode are terminated correctly. The bases of the EF transistors Q1 and Q2 are biased through the 50 Ω termination resistors to the supply voltage. Hence, with this input stage design, we assume external AC-coupling of the differential input signals. The biasing current $\mathrm{I_0}$ is equal to 2 mA and a supply voltage of 2.5 V is used. To allow an approximately fixed signal swing incident on the filter core under different input power levels, a variable gain stage is added after the input stages. The schematic of this variable gain stage is found in Fig. 6b. To provide the variable gain, a differential pair (Q0-Q1) with partially fixed ($\mathrm{R_e}$) and partially variable ($\mathrm{R_t}$) emitter degeneration is used. The variable emitter resistance $\mathrm{R_t}$ can be changed by digital control signals by switching NMOS transistors in triode on/off. The output of the amplifier stage is buffered using the EFs Q2 and Q3 to be able to drive the equalizer core. The collector load resistors are formed by the resistors $\mathrm{R_{c1}}$ and $\mathrm{R_{c2}}$. The differential $\mathrm{R_{c2}}$ is used to lower the net differential impedance at the collectors ($\mathrm{R_{c1}}//(\mathrm{R_{c2}}/2)$) while the DC collector voltage is only determined by $\mathrm{R_{c1}}$. Hence, the DC output level can be controlled to obtain the correct levels to interface with the filter core. The biasing currents $\mathrm{I_0}$ and $\mathrm{I_1}$ are both equal to 2 mA. The resistors $\mathrm{R_e}$, $\mathrm{R_{c1}}$ and $\mathrm{R_{c2}}$ are respectively equal to 125 Ω, 400 Ω and 320 Ω leading to a DC output common mode of 1.25 V. The nominal gain of the variable gain stage is tunable between -1.2 dB and 5 dB.

B. Output stage

To interface the filtered signal towards a 100 Ω AC-coupled differential load, a dedicated output driver is necessary. The schematic of the implemented output driver is shown in Fig. 7. The EF transistors Q0-Q1 are used to drive the cascoded output driver differential pair Q2-Q3 (cascodes Q4-Q5). The cascodes are placed to limit the collector emitter voltage to avoid breakdown and to avoid multiplication of the Miller capacitance (bias voltage $\mathrm{V_{casc}}$=2.25 V). To obtain a matched load, $\mathrm{R_{term}}$ is chosen to be equal to 50 Ω. The EF biasing $\mathrm{I_0}$ is equal to 2 mA. The output stage bias current $\mathrm{I_1}$ is equal to 11.5 mA to allow sufficient swing in the output load resistors. The emitter degeneration $\mathrm{R_e}$ is equal to 8 Ω. Using these values, the output stage has a nominal gain of 3 dB. The combination of the bondpad and ESD parasitic capacitances and the output bondwires of 600 µm, limit the bandwidth to 27 GHz in simulation.

C. Variable gain tap amplifiers

The variable gain amplifiers (VGAs) in Fig. 5 marked in black are needed to create arbitrary filter responses. The amplitude and sign of the VGAs' gain are chosen to be digitally programmable. The schematic of two identical but independently tunable transconductance VGAs used to capture the same input signal is given in Fig. 8. The output currents are converted back to a voltage in the summation nodes of Fig. 5 which are incorporated in the design of the return delay line discussed in section III-D. The gain of the VGA (in principle a Gilbert cell multiplier) is tuned by choosing the value of the difference current 'a'. By using this biasing scheme, both the gain and the sign can be tuned in the VGA. The DC current through the VGA is independent from the gain setting. To control the biasing currents of a single VGA on chip, a 7 bit complementary current DAC with 2 outputs (6 bit + 1 sign bit) is used to generate the $\mathrm{I_0}+$a and $\mathrm{I_0}-$a currents. To increase the linearity of the VGAs, emitter degeneration is added in Fig. 8. The VGA is designed assuming an input common mode of 1.25 V, making it possible to add a cascode transistor on top of the VGA to shield the summation nodes when a supply voltage of 2.5 V is used. The biasing current $\mathrm{I_0}$ is equal to 0.320 mA. The maximum simulated voltage gain of the VGA is around 5 dB when the VGA is connected to the summation node which is implemented as a summation resistor with a value of 300 Ω.

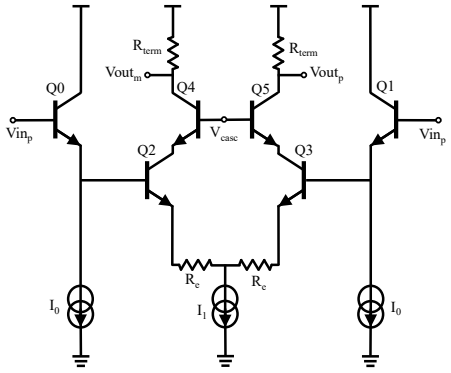


Fig. 7. Schematic of the 100 Ω differential output interface.

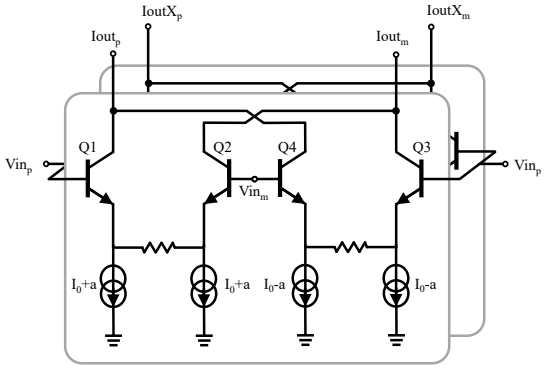


Fig. 8. Schematic of the transconductance VGA pair.

D. Delay elements

The delay elements with a delay of $\mathrm{T_F}$ and $\mathrm{T_R}$ in Fig. 5 can be implemented in different ways. In literature both active (e.g. [9], [11], [12], [19]), passive (e.g. [21], [22]) or hybrid (e.g. [20]) solutions are presented in analog FIR filters. Passive

solutions provide the most promising performance in terms of bandwidth, especially if on-chip transmission lines are used, but they require a large chip area. If the needed area for the delay cells is too large, the different tap nodes in the filter will likely be placed physically far apart and will complicate the summation. Active delay solutions, although suffering from limited bandwidth and linearity, are much more compact and simplify the physical layout of a complex equalizer. For this reason, for both the $\mathrm{T_F}$ and $\mathrm{T_R}$, active delay implementations are used in the design.

1) Return Delay elements: The delay cells of the return line should be co-designed with the summation nodes in Fig. 5. The summation of the VGA outputs (g_m stages) is done in a resistor, shielded by a cascode to maximize the bandwidth at the summation node. This means that ideally, the return stage itself acts as a g_m stage such that it can be directly connected to the same summation node.

In Fig. 9, the proposed return cell circuit can be found. Transistors Q3-Q4 are summation cascodes to which the VGAs are connected. The actual delay cell is formed by the transistors Q1-Q2-Q5-Q6. These transistors form a linearized cross-quad differential pair. The cross-quad circuit acts as a single g_m stage such that it can easily be summed together with the VGA currents. The DC transconductance of the cross-quad, assuming all transistors are equal and matched, is given in Eq. (3) [23]:

$$g_{m,\mathrm{return}} = -\frac{1}{R_e} \tag{3}$$

Due to the positive feedback in transistors Q5-Q6, the sign of the transconductance is inverted with respect to a normal differential pair. The choice for a linearized cross-quad over a simple emitter peaked differential pair is strengthened by several advantages. First, due to the cross-coupled pair and under the assumption of adequate matching between Q1-Q2 and Q5-Q6, the nonlinearities of the Q1-Q2 pair are compensated, creating a very linear g_m stage, even in large signal regime [23]. Secondly, due to the sign inversion of the gain, the Miller effect is removed if the cell is assumed to have unity gain. Third, the negative resistance created by the cross-coupled pair and the parasitic capacitance at nodes A and A' will create a right half plane zero. Compared to emitter peaking, which increases bandwidth but lowers the delay, this circuit increases bandwidth while increasing the delay. A drawback of this delay implementation is that the amount of delay is directly linked to the peaking. Therefore, the delay cannot be designed for a desired value but is merely the product of the bandwidth of the circuit, determined by the parasitics. This is however not a problem when the net delay of the return cell is lower than the total desired delay. The residual delay should then be implemented by a topology with a more controllable delay.

In Fig. 9, the DC-offset cancellation circuit is also shown. The offset can be sensed at the summation resistor and compensated by tuning one of the two current sources added under the summation cascodes. The compensation currents also lower the amount of DC current through the collector resistances and hence increase the output common mode. The circuit is designed for a supply voltage of 2.5 V and an input

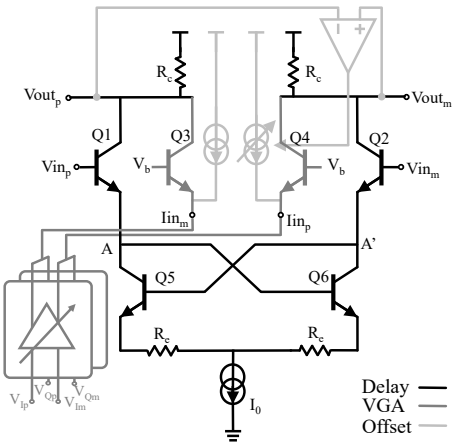


Fig. 9. Schematic of the return delay cell together with the VGAs and summation node.

(and output) common mode of 2.1 V. The bias current $\mathrm{I_0}$ is equal to 1 mA. The collector resistance $\mathrm{R_c}$ and emitter resistance $\mathrm{R_e}$ were designed to be approximately 300 Ω. The offset current sources have a nominal value of 0.4 mA. The simulated amplitude and group delay response of the return cell can be found in Fig. 11, showing a 3dB bandwidth of 44 GHz, 14 ps delay at 1 GHz, a nominal gain of 0 dB and a linear input range of 600 mVpp.

2) Forward Delay elements: The forward cell should implement the residual delay $\mathrm{T_F}$ via a more controllable active delay cell circuit with enough bandwidth. Designs based on single g_m stages can be found in [6] and [20]. These designs depend on the delay of single gain stages where the delay is inversely proportional to the bandwidth of the cell if no extra broad banding techniques are used. The return cell from Fig. 9 can also be placed in this category. More efficiently, one may use an all-pass filter built with g_m stages which approximates the ideal $e^{-s\tau}$ transfer function. A widely used approximation is the first order all-pass filter in Eq. (4), used in [12], [19] and [24].

$$H(s) = \frac{1 - s\tau}{1 + s\tau} \tag{4}$$

The frequency dependent group delay response τ_g of the filter in Eq. (4) is given by Eq. (5) [19]:

$$\tau_g(f) = \frac{2\tau}{1 + (2\pi f\tau)^2} \tag{5}$$

The all-pass transfer function has a delay of 2τ and no inherent bandwidth limitation, promising better performance than single g_m stages. The group delay rolls off for higher frequencies, possibly limiting the performance of the FIR filter. The impact on the analog FIR performance of this group delay roll-off is analyzed in [19], where it was concluded that the equalization capabilities are not compromised. It can even help the performance as the roll-off can provide peaking for frequencies above the Nyquist frequency determined by the low frequency delay of the filter.

One can obtain the transfer function in Eq. (4) by combining two filters as in Eq. (6). A slow path formed by a single pole

low-pass filter with a gain of 2 and a fast path consisting of an inverted unfiltered version of the input.

$$H(s) = \frac{2}{1+s\tau} - 1 = \frac{1-s\tau}{1+s\tau} \tag{6}$$

In Fig. 10, the proposed schematic for the differential implementation of Eq. (6) can be found. The fast path between the input and the output is formed by transistors Q1-Q5 (Q2-Q6), the slow path is formed by transistors Q3-Q7 (Q4-Q8). To form a controlled single pole in the slow path, which does not effect the fast path, the cascode transistors Q7 (Q8) and the tunable capacitor C_0 are introduced. The capacitor creates a pole with $\tau = \frac{2C_0}{g_{m7,8}}$ in the slow path. To implement the tunable capacitor (bank), the gate capacitance of parallel PMOS transistors are switched on or off. The gain and sign difference between both paths is implemented by scaling the number of parallel input transistors (2 vs 1) and cross connecting the collectors of the cascodes in both paths. The emitter followers Q9 and Q10 are added to shift the DC output common mode down such that the input and output common mode of the delay cell are equal. In this way, the cells can be cascaded without DC blocking capacitors. The emitter followers are also needed to shield the large load of the delay cell (consisting of 1 delay cell and 2 VGAs) from the bandwidth limiting summation in the R_c resistors. The emitter resistance R_e is added to increase the input linearity of the cell while lowering the g_m of the net total input transistor to $g_{m,eff} = \frac{g_m}{1+g_m R_e/2}$. Bandwidth peaking is provided through the net emitter capacitance C_e formed by the capacitance from the current sources which provide peaking in $g_{m,\text{eff}}$.

The circuit is designed for a supply voltage of 2.5 V and an input common mode of 1.25 V. The bias current I_0 is equal to 1.4 mA and I_1 is equal to 0.65 mA. The collector resistance R_c was designed to be 340 Ω, the emitter degeneration R_e has a value of 165 Ω. In the circuit of Fig. 10, offset compensation is added which makes sure that the DC offset caused by mismatches in the chip is compensated in every delay cell. The offset compensation is implemented via a variable current mirror (nominal 0.1 mA) under the slow path cascode. This location is ideal for the compensation mirrors for two reasons. First, as any capacitance on these nodes will only contribute to the delay of the filter and not to the 3dB bandwidth of the delay cell. Secondly, the compensation causes to decrease the $g_{m7,8}$ of the slow path cascode slightly, but again this change will only contribute to the delay of the filter and not to the 3dB bandwidth. The simulated amplitude and group delay response of the cell can be found in Fig. 11, showing a 3dB bandwidth of 31 GHz and a nominal gain of 0 dB. In the simulation of Fig. 11, the tunable capacitor C_0 is set as such that a net tap-to-tap delay of 27 ps ($3/4$ T_s at 28 Gbaud) is obtained at 1 GHz, needing a delay of approximately 13 ps in the forward cell.

3) Simulation results: Besides the transfer functions of the forward and return delay cell in Fig. 11a, two extra responses are simulated. First the response of the second tap (path indicated in Fig. 5, from input filter core to the output of the filter core) is simulated at maximum gain. This results in a net bandwidth of 21.6 GHz which is sufficient for 28 Gbaud

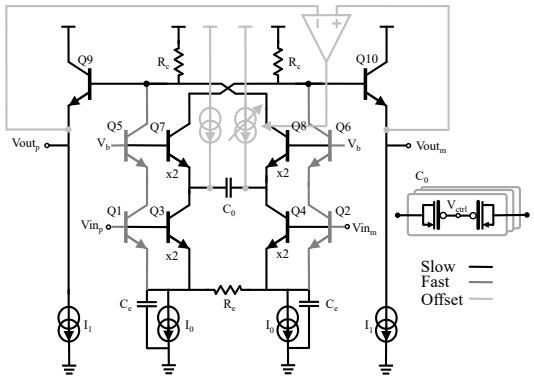


Fig. 10. Schematic of the forward delay cell.

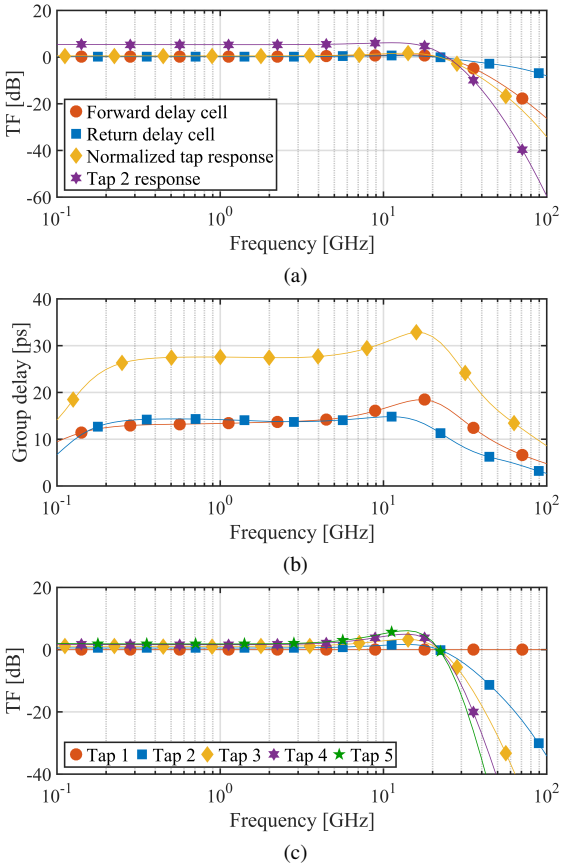
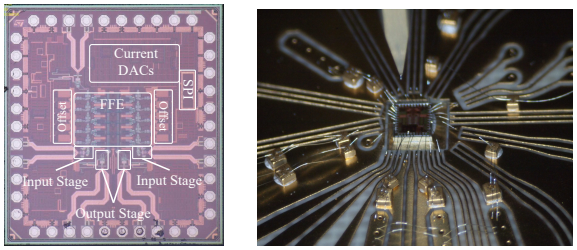


Fig. 11. Simulated transfer functions for the key circuits in the equalizer. (a) Shows the amplitude responses, (b) shows the group delay responses of the separate delay cells and their combination (same legend from figure (a) applies). The different simulated tap responses through the II path of the chip normalized to the first tap are found in (c).

communication. The normalized tap response is obtained by dividing the second tap response by the first tap response. In this way, all common losses to the filter taps are canceled resulting in the combination of the forward and return delay cell transfer function. This combination has a bandwidth of 28 GHz. Looking at the group delay responses in Fig. 11b, the total tap delay is divided equally between the forward and return cell at the aimed delay of 27 ps. However, by tuning C_0, the delay of the forward cell can be slightly increased/lowered. In simulation, the delay was designed to be tunable from



(a) (b)

Fig. 12. Die microphotograph (1220 µm x 1310 µm) with annotated functional blocks (a) and the chip wire bonded to the PCB (b).

25 ps to 50 ps. However, the on-capacitance of the PMOS gates was overestimated as a quasi-static transistor model was used in combination with large transistor channel lengths (up to 6 µm) during the design. To obtain reliable capacitors, the non-quasi static model must be used in simulation together with minimum length transistors. The combined group delay response shows some peaking which will cause the filter to deviate more from the ideal analog FIR equivalent. As long as the maximum group delay value is lower than the symbol period, the performance penalty will be limited as can be expected from the simulations in Fig. 4a. The roll-off at lower frequencies can be attributed to the self-heating effect of the bipolar transistors. To conclude, the simulated (normalized) transfer functions for the different taps are provided in Fig. 11c showing a gradually decreasing bandwidth from 28 GHz for the second tap to 23 GHz for the last tap.

IV. Experimental Results

The complex equalizer chip is fabricated in a 55nm SiGe BiCMOS technology. A microphotograph is found in Fig. 12a with annotated important functional blocks. Total die area including bondpads is 1.6mm^2. The analog FFE core including the 4x5 filter VGAs and 4x5 delay cells has an approximated area of 0.160 mm^2. The chip has been wire bonded to a PCB as shown in Fig. 12b. The lengths of the bondwires to the input and output bondpads vary between 400 µm and 800 µm. The different gain elements are controlled via on chip registers, configurable through an SPI interface. These digital settings are used to control the 7 bit complementary current DACs. In total, the chip consumes 150 mA (including dummies) from a 2.5 V supply and uses an extra 1 V supply for the SPI logic. A breakdown of the power consumption is provided in Table I. The dummy delay cells in the design could be removed or replaced by passive dummy loads without major impact on performance. The power including the dummies is therefore reported separately. The reported unit element power includes the power consumed by the last current mirror biasing the high-speed circuits. The biasing power consists of the power lost in the remaining distribution of reference currents (derived from a single 0.1 mA input current) throughout the chip. The core power is defined as the sum of the delay cells and VGAs power consumption. The reported measurements are performed at room temperature on a single die.

TABLE I
Power consumption breakdown

Block	#	Unit Element Power [mW]	Total Power [mW]
Input stage	2	29	58
Forward cell (a)	8 (+ 2 dummies)	11.8	94.4 (118)
Return cell (b)	8 (+ 2 dummies)	2.6	20.8 (26)
VGA (c)	20	3.5	70
Output stage	2	39	78
Biasing			22
Core (a+b+c)			**185 (218)**
Full Chip			**343 (376)**

A. Small signal characterization

Using a four port vector network analyzer (VNA), the small signal behavior of the equalizer chip was analyzed. In Fig. 13, the different responses of the individual taps are given. The responses were measured by setting the digital gain control of the tap under test at maximum (corresponding to $\mathrm{a} = \mathrm{I}_0$ in Fig. 8) and placing all other gains to 0 (corresponding to $\mathrm{a} = 0$ in Fig. 8). The measurements in Fig. 13a include connector, PCB and bondwire losses. The tap-to-tap delay is estimated from the S-parameters and set to be in the range of 27 ps corresponding to $3/4\ \mathrm{T_s}$, with $\mathrm{T_s}$ = 36 ps, the symbol period for 28 Gbaud signaling. The bandwidth of the first tap for the various filters varies between 16 and 18 GHz, mainly limited by the input and output bondwires. There is no noticeable difference between the through filter (e.g. II) and the cross filter (e.g. IQ). The DC gain of each tap is approximately 5.5 dB, which is a combination of the loss in the input stage, gain in the output stage and the VGA gain. To observe the penalty introduced by the delay lines in the filters, the S-parameters in Fig. 13a and Fig. 13b are normalized with respect to the first tap response, similar to the response in Fig. 11a. These results are found in Fig. 13c and Fig. 13d. The measured 3dB bandwidth of the normalized responses for the different filters are shown in Fig. 14. As expected, for increasing tap numbers, the bandwidth drops, mainly due to the limited bandwidth of the forward delay lines. The bandwidth of the second taps in the filters varies slightly around 28 GHz, which is comparable to the simulated values in Fig. 11a. The bandwidth of the later taps are lower compared to the simulation. Ideally, all the tap bandwidths are desired to be $> \frac{2}{3\mathrm{T_s}}$ (assuming a tap-to-tap spacing = $3/4\ \mathrm{T_s}$) to cover the full spectrum controlled by the ideal filter response. The last tap has a minimum measured bandwidth of 13 GHz, which is lower than the 18.7 GHz limit assuming a 28 Gbaud link. However, simulations show that the unavoidable penalty caused by this limited bandwidth is reasonably low in our case. The gain of a single tap is measured in function of the digital setting of the 7 bit complementary current DAC. The result in Fig. 14b shows a nonlinearity resulting from the emitter degeneration in the VGAs. This nonlinearity is not a problem if gradient based update loops are used to optimize the filter.

Next, the S-parameters of the compensation filters can be measured when they are programmed to the settings used to compensate a certain amount of CD in fiber and electrical bandwidth limitation. These optimal settings are obtained via

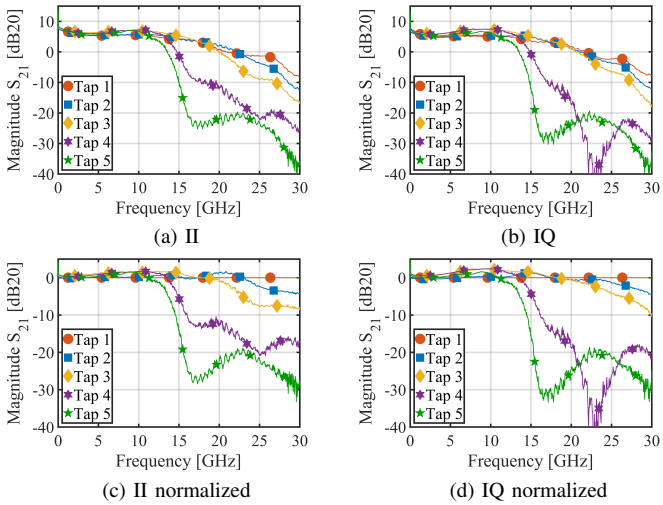


Fig. 13. S-parameter measurements for the different taps on the II (a) and IQ (b) filters, and normalized responses w.r.t the first tap for II (c) and IQ (d).

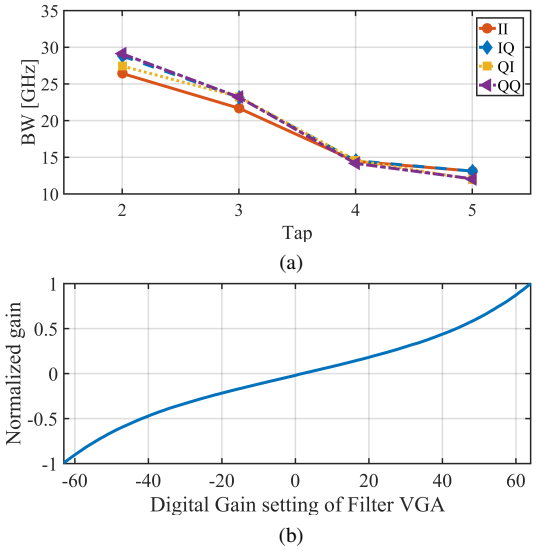


Fig. 14. Measured bandwidth (a) of the different normalized equalizer taps. (b) Measured gain of a single filter VGA in function of the digital gain setting.

the least mean squares (LMS) optimization in the system experiments of Section IV-C. The measured S-parameters for different filter settings for the II and IQ filters can be found in Fig. 15. The S-parameters are normalized w.r.t the first tap (similar as in Fig. 13). To observe how good the equalizer behaves as an ideal analog equivalent of a FIR filter, the measured S-parameters can be compared with the filter responses that are generated if the digital gain settings (with compensation of the nonlinearity in Fig. 14b) of the chip are used to create a digital FIR filter. Using these tap values in an ideal FIR filter and a fixed tap spacing of 27 ps, the estimated filter frequency responses in Fig. 15 are obtained. For all cases, a good correspondence at lower frequencies between the ideal FIR and the analog FIR filter are obtained. At higher frequencies, both start to deviate but still the same trends are visible (for example the second pass-band in Fig. 15b). The deviations at higher frequencies are caused by the reduced bandwidth of the last taps in the filter as visible in Fig. 14a.

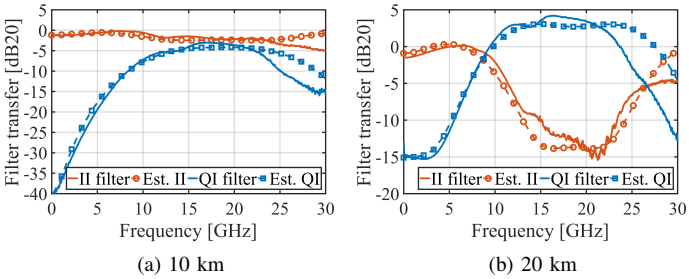


Fig. 15. Measured normalized filter transfer functions and idealized digital (= estimated) filter response of the chip for different fiber lengths.

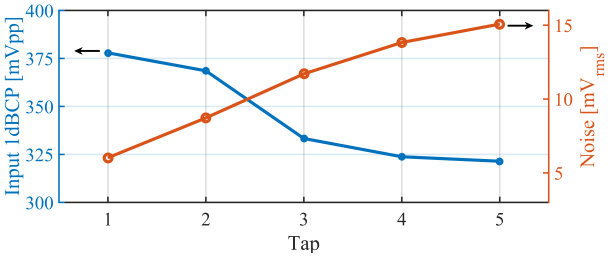


Fig. 16. Output noise level and input 1dBCP voltage at 1 GHz of the equalizer for the different taps in the II filter.

Other deviations can be accounted for by deviations in the tap-to-tap spacing in the filter itself, the frequency dependent group delay variations and slight gain offsets between the amplifiers in the filters. From this comparison, it can be concluded that the designed analog FIR filter behaves well within the band of interest.

B. Noise and linearity

For the characterization of the noise, a sampling scope with 50 GHz bandwidth is used to capture the output noise signal. To measure the noise of a subfilter in the equalizer, no input to the I or Q input of the chip is applied and all taps are first set to a digital gain of 0 except one which is set to the maximum gain to observe the noise at the output. The resulting noise levels for the different taps in the II filter are found in Fig. 16. Assuming an all-pass filter response using only the third tap (V_{rms} =11.07 mV) and an output swing of 250 mV, a symbol error rate of 1e-4 can be expected for 16-QAM communication (using the Personick Q [25]) which is low enough to be compensated by commonly used forward error correcting codes (FEC) (e.g. KP4 FEC [26]).

The linearity of the filter is verified by a 1dBCP measurement at 1 GHz. Setting the input stages to minimal gain (which is also used in later system experiments), the linearity results of Fig. 16 are obtained. For all taps, the 1dBCP is $\geq$ 300 mVpp. Simulations show that the linearity is mainly limited by the forward delay line. From the measured 1dBCP it can be concluded that input signals up to 300mVpp can be safely processed by the input delay line.

C. System experiment

To verify the equalization capabilities of the chip, the system experiment from Fig. 17 is used. Via VPI^{TM} TransmissionMaker, a coherent link is simulated, based on the system in

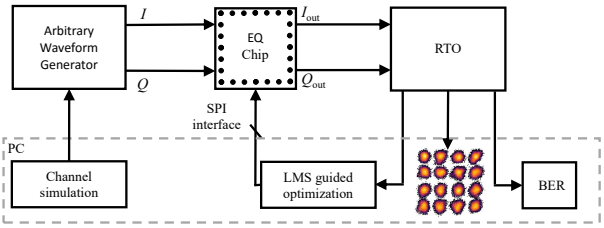
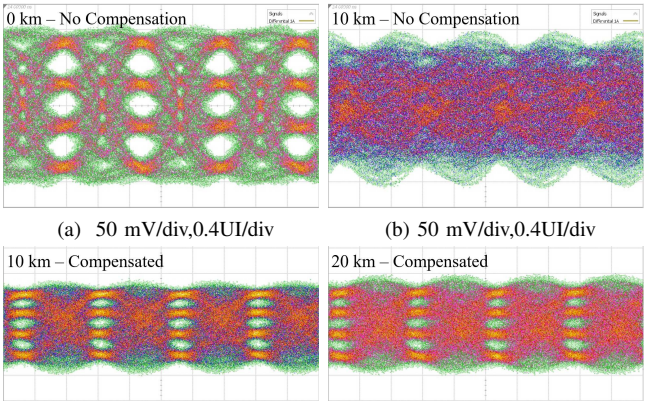


Fig. 17. Measurement setup used for the system experiments.



(a) 50 mV/div,0.4UI/div (b) 50 mV/div,0.4UI/div

(c) 100 mV/div,0.4UI/div (d) 100 mV/div,0.4UI/div

Fig. 18. Eye diagrams from the I channel for 16-QAM - 28Gbaud communication at the output of the AWG in the B2B case (a) and 10 km of fiber (b) and after the IQ filter for 10 km (c) and 20 km (d) of fiber. Eye diagrams are captured with a 50 GHz digital sampling oscilloscope.

Fig. 1 but with a single polarization. The chromatic dispersion is modeled with a dispersion coefficient of $D_{\text{smf}} = 16\frac{\text{ps}}{\text{nm km}}$ at 1550 nm (C-band). Throughout the simulations, a root-raised cosine transmit pulse with $\alpha = 0.5$ and a pseudo-random bit pattern with a length of $2^9 - 1$ is used. Other non-idealities in the link such as carrier offset, IQ-mismatch, nonlinearities in the TX/RX etc. are not simulated to isolate performance with respect to the CD compensation. The simulated I and Q outputs of the link are then loaded in a 92 GS/s Arbitrary-Waveform-Generator (AWG) to be sent to the equalizer chip. Eye-diagrams for the I channel at the output of the AWG for different 16-QAM communication links are found in Fig. 18. The swing of the AWG is set to 250 mVpp, corresponding to an output level which can be expected from linear TIA's which should precede the equalizer filter [27]. After sending the signal through the chip, the two differential output signals are captured by a real-time oscilloscope (RTO) to observe the waveforms. The waveforms are analyzed in software to calculate updates for the equalizer taps such that they are iteratively updated to the optimal (LMS) settings. In the future, continuous time adaptation systems for the equalizer taps can be implemented on chip to perform iterative updates. In [6], a possible implementation using a constant modulus algorithm is proposed and tested in [7] to obtain an 8 Gb/s analog coherent link. Updates can also be guided by using binary information coming from extra data slicers in the decoder as mentioned in [11].

The system is tested at 28 Gbaud 16-QAM for various fiber lengths, hence for increasing amount of chromatic dispersion. Fig. 18c and Fig. 18d show optimized eye diagrams at the output of the filter. Fig. 19a and Fig. 19b provide the corresponding constellation diagrams. The bit-error-ratio (BER) for different distances is given in Fig. 19c. The BER increases over distance as for the longer fiber spans a penalty is expected due to the limited number of taps (ref. the penalties for QPSK in Fig. 4b). For the back-to-back experiment (B2B), the equalizer chip only compensates the electrical impairments introduced by the chip itself and by the bondwires. However, no error-free operation is achieved in this case as the noise of the equalizer chip lowers the SNR. This increased BER is not a problem as long as the BER is below the FEC limit of the application. Two commonly used FEC limits for error-free operation (7% OH-HD FEC = 3.8e-3 and KP4-FEC = 2.4e-4) in data center applications (where coherent-lite systems may be used in the future) are annotated in Fig. 19c showing that performance up to 20 km can be achieved.

Table II compares our designed FIR filter with the results of state-of-the art fabricated analog filter designs. Compared to the single FFE equalizers, we report a similar performance in terms of bandwidth and delay values with respect to previously reported full active delay solutions [12], [19]. Passive solutions like [13] and [20] show increased bandwidth but are not area efficient. Compared to the most recent state-of-the-art complex FFE (CFFE) in [11] several performance differences can be observed. As [11] uses sample and hold techniques at low baudrates, very compact and low power high delay implementations can be obtained with a large amount of taps. However, with respect to [11], we scaled the processing baudrate with more than a factor of 5.

Implementing an ADC based receiver instead of the analog filter would require at least two ADCs. Using the state-of-the-art 56 GS/s ADCs in [4] requires 1.4 W. Compared to our total power consumption of 343 mW, analog filtering shows to be a promising solution when a limited amount of signal processing is necessary. However, the introduced noise should be lowered in later designs to make a fair comparison with ADC based receivers with an ENOB of approximately 6 bits.

V. Conclusion

In this work, a five tap complex analog FIR filter is presented. The filter can be used to compensate frequency dependent variations in coherent (optical) links. It is capable to compensate distortion introduced by chromatic dispersion in optical fibers. The filter is designed using a distributed FIR filter architecture with two types of custom designed analog delay circuits and Gilbert cell multipliers to control the filter transfer function. The chip is fabricated in a 55nm BiCMOS technology with a core power consumption of 185 mW from a 2.5 V supply. The chip functionality is verified via S-parameter measurements and system experiments using 28 Gbaud 16-QAM modulation. This works shows an increased baudrate with respect to state of the art complex analog FIR filters and shows the possibility to be a viable low complexity alternative for digital signal processing filtering in the future.

TABLE II
COMPARISON WITH FABRICATED ANALOG (COMPLEX) FFE EQUALIZERS IN LITERATURE

	[19]	[12]	[20]	[13]	[9]	[11]	**This Work**
Technology	28nm CMOS	28nm CMOS	65nm CMOS	55nm BiCMOS	65nm LP CMOS	28nm CMOS	**55nm BiCMOS**
Architecture	FFE	FFE	FFE	FFE	CFFE+CDFE	CFFE + CDFE	**CFFE**
FFE Topology	Tapped delay FIR	Tapped delay FIR	Distributed FIR	Distributed FIR	Tapped delay CFIR	Tapped delay CFIR	**Distributed CFIR**
# of Coef.	7	4	7	6	16x4	96x4	**5x4**
Delay impl.	Active delay	Active delay	Active/Passive	Passive	S/H	S/H	**Active/Active**
Tap Delay [ps]	30	25	12.5	8.5	250 (4 Gbaud)	250 (4 Gbaud)	**27**
Delay BW [GHz]	24.4	18	41 (active)	-	-	-	**28**
Modulation	NRZ	NRZ/PAM4	NRZ	NRZ/DB	QPSK	DP 16-QAM	**16-QAM**
Datarate [Gb/s]	25	25	40	100	8	40	**112**
Power [mW] *	90	25	65	263	30	82***	**185 (343)**
Efficiency (pJ/bit)	3.6	1	2	2.63	3.75	2.05	**1.6 (3)**
Core Area [mm^2]	0.086	0.068	0.75	3.8**	4.25**	4.32**	**0.16 / 1.6****

* Only FFE power is considered
** Total chip area (including extra functionality)
*** Est. comparing power with/without usage of FFE

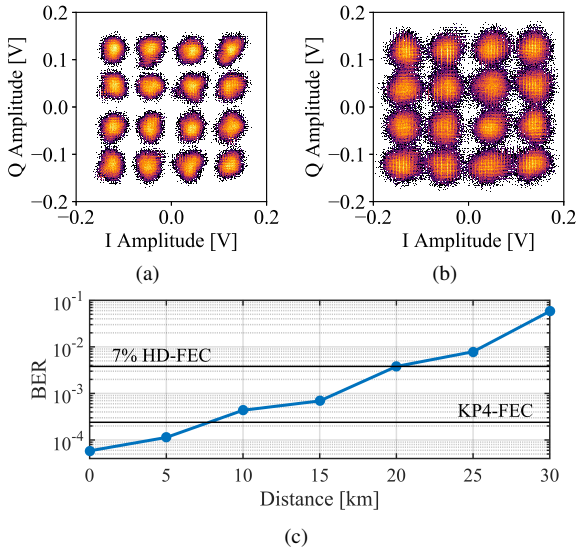


Fig. 19. Constellation diagrams for (a) no dispersion and (b) 20 km of fiber at 28 Gbaud 16-QAM ($2.8\text{x}10^5$ points). (c) Measured BER for different lengths.

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