ANALOG TO DIGITAL CONVERTOR STUDIES

by

JAMES ALAN HEISE

BSEE, Kansas State University, 1986

A MASTER'S THESIS

submitted in partial fulfillment
of the requirements for the degree

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

KANSAS STATE UNIVERSITY
Manhattan, Kansas

1988

Approved by:

Donald A Gorham
Major Professor

PATENT CAUTION

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TABLE OF CONTENTS

LIST OF FIGURES AND TABLES

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1.0 Introduction

In today's modern world people are using computers to even greater extents to monitor, control, and test the environment around them. As these people try to interface the computer's digital environment with the analog environment that surrounds it there arises tremendous needs for methods to convert analog signals to their digital equivalent. Also with advancing technology the areas which are applying computers or digital data systems are rapid expanding. These changes are placing even greater demands on analog–to–digital (A/D) conversion methods. This thesis will look at two particular applications of A/Ds that were done for Sandia National Laboratories and shows some of the diversity and variety in A/D systems.

The research done on both systems starts very similarly, although the details and specifications of each system are quite different. The first system, discussed in Chapter 2, is a 32–channel 12–bit analog–to–digital conversion board which is one part of a larger system that Sandia is developing. The second system, discussed in Chapter 3, is a 500 MHz 8–bit analog–to–digital convertor with a 16K byte circulating memory to continuously accept the A/D's output. This system is needed to obtain a very high resolution digital representation of incoming signals. The major similarity of the research done on these projects was the desire for them to be produced from commercially available components. This desire was satisfied on the first project, but due to the extreme speed requirements of the second project, there were no commercial devices of that nature available. Therefore, the work on the second project turned into an

investigation of companies involved in high speed A/D research to see if such a device was possible and if so, which company could best produce such a device with a custom design. This fact then made for the major difference between the two projects. The design of the 32–channel 12–bit A/D involved the choice and integration of commercially available devices. The researching of the 500 MHz 8–bit A/D–memory system was a more paper–oriented project involving contacting companies and studying research papers in the area of high speed A/Ds and memories.

Some of the main characteristics of data acquisition systems will be defined and explained for future reference. The defining of terminology and characteristics of these systems will start at the front of the system and work through to the end. One of the first considerations of any A/D system deals with the characteristics of the signal to be converted to see if a sample–and–hold (S&H) must be placed in front of the A/D. The purpose of a S&H is to reduce the aperture time of an A/D system by "freezing" the analog input at some instance so a conversion can be done on it. The reduced aperture time is needed because A/Ds can require sample pulse widths of hundreds of microseconds, where a S&H is on the order of tens of nanoseconds. Generally, a S&H is used whenever the input signal changes by more than one–half of the least significant bit (LSB) of the A/D during the A/D's conversion time. This criterion can be checked by looking at the maximum rate of change, slew rate, of the input signal.

The following S&H parameters are very important when designing a data acquisition system: acquisition time, aperture time, aperture jitter, droop rate, and hold time. Acquisition time is the length of time between

the sample command and the moment the output is tracking the input to within a specified accuracy. It is dependent on the time constant necessary to charge the hold capacitor and the slew rate of the operation amplifier in the S&H circuit. The acquisition time of a S&H is usually specified for a full–scale or half–scale voltage change at the device's input. The aperture time is the time between the initiation of the hold command and the beginning of the hold mode. This time delay can often be compensated for by advancing the control timing an equivalent amount. In addition to the aperture time there is the aperture jitter (or uncertainty time) due to the non–repeatability of the aperture time. The jitter is caused by the uncertainty of the switch. The sum of the three parameters discussed so far is the major limiting factor for how fast successive samples of a signal can be taken.

Once the input signal has been sampled, the other two parameters mentioned above determine how long the signal can be held. The hold time is a parameter not mentioned in a device's specifications but rather a parameter created by the requirements and other components' parameters of the system. The hold time is the length of time which a sample value can be maintained on the hold capacitor without its value decaying more than one–half LSB of the A/D. The rate at which the hold capacitor decays is called the droop rate. The droop rate is due mainly to leakage currents through the switch, operation amplifier bias currents, and the value of the hold capacitor. Herein lies the major difficulty of S&H designs, the larger the capacitor value the lower the droop rate; however, it also slows the charge time and thus the acquisition time. Therefore, by increasing the size

of hold capacitor the output stability increases as device speed decreases. For more details on S&H parameters and errors, a list of references is given in Appendix B.

The other major component of a data acquisition system is the A/D. There are many different architectures for A/D convertors and the choice of which is best often depends on its application and environment. A brief discussion of three basic architectures will now be given. The first to be discussed is the parallel or flash architecture. This is probably the best known and most popular type of A/D for higher speed applications. It consists of 2^N-1 comparators for an N–bit A/D, where each comparator compares the unknown input to different known voltage levels. This approach is commonly used without a S&H circuit, because the comparators can be strobed to provide the sampling function. Due to the use of many comparators these A/Ds are inherently very fast; however, their resolution is usually limited to 6 or 8 bits because of the number of comparators required.

The next approach is a feedback architecture. The most common A/D of this type is the series feedback or successive approximation A/D. This approach uses a single comparator and requires one clock cycle per bit plus one or more additional cycles for a S&H which is almost always used with this architecture. Since this architecture is rather simple, there are few sources of error, and it is used for A/Ds ranging from 4 to 16 bits. The need for several clock cycles per conversion limits the maximum conversion rate considerably compared to flash A/Ds. However, the conversion rate can be increased by using more than one comparator to determine more than

one bit per clock cycle. In such a series–parallel feedback architecture the complexity is increased, which also increases error possibilities.

The final approach to discuss is called a feed–forward or pipeline architecture. This approach consists of successive blocks, where each block quantizes part of the input signal and subtracts that amount from the input, then the residue is passed on to the next block. Each block can determine one or more bits of the final result, which is collected in an output register. A S&H, or other means of analog delay, is included in each stage to allow all stages to simultaneously determine their output. The implementations which use more than one bit per block are called series–parallel feed–forward architectures.

There are more A/D architectures than have been discussed here, but these are the ones often used for higher speed applications. With all of these architectures the more devices that are introduced to any method just create more places for inconsistencies and errors to arise which makes the overall system less accurate.

2.0 32–Channel 12–Bit A/D Board

The first system that will be discussed is the design of the 32–channel 12–bit A/D board. To understand the design criteria and decisions made on this system, a brief explanation of where the inputs originate would be helpful. The 32 analog signals are output from an array of infrared sensors mounted vertically on a platform which rotates at a constant angular velocity of 1/2 Hz (2 seconds per revolution). These sensor outputs are then filtered, amplified and routed to the input of the A/D board. The A/D board is then supposed to digitize all 32 analog signals 2^{14} times per revolution of the platform in a repeatable manner. Repeatable means every 2^{14} conversion of the array must be at the same absolute rotational orientation. However, the conversion of the 32–channel array does not have to be simultaneous; a time skew can exist between channels. Each signal to be converted has a full scale range of Ov to 5v and can have a full scale change between conversions. The following list restates the initial design limits that are used to develop the 32–channel 12–bit A/D:

- Vertical array of 32 sensors on a rotating platform at 1/2 Hz.
- 12–bit conversion of each sensor output 2^{14} times per revolution
- Ov – 5v sensor output (input to board)
- Possible full scale sensor change between conversions
- Time skew on array elements conversions allowed
- The 2^{14} array conversions must be repeatable
- Available power supply ±15v and +5v
- Keep power consumption below 20 watts.

In addition to the 12–bit digital output for each analog input, the following status bits or lines are desired.

- Bad Cell (high)
- Bad Cell (low)
- Bad Set
- Run–on or Repeated Set
- A/D Failure

The bad cell bits are to be activated if any of the analog inputs are thought to be in error. These two status bits could be accomplished by comparing the analog signal about to be converted to the upper and lower limit of the full scale range, because the signals are amplified such that normal infrared sensors still should not produce analog output signals near either rail. One characteristic of the infrared sensors is that when they fail they produce a rail output. The bad set bit is to be flagged if the 32 conversions have not been done by the time the next array of 32 is to begin. In the same manner the run–on or repeat bit is to be flagged if the 32 conversions are completed too quickly and the next series of conversion starts before it should. The final flag is to tell the health of the A/D convertor(s). Once all limits and parameters have been established, the design methods can begin to take form.

2.1 System Considerations and Methods

One of the first things that needs to be considered in designing the 32–channel A/D is the method of synchronizing the conversions so they happen at the same place on every revolution. A clocking method would be needed, not as much to maintain an absolutely exact clock frequency but to clock through the channels at an appropriate rate to maintain repeatability

between revolution. In order to do this a signal is needed to synchronize the rotation of the platform with the conversion of the input signals. This synchronizing signal can be obtained from the shaft encoder on the platform. The signal from the shaft encoder is a 2^{16} Hz square wave, that when divided by 8 would produce a 2^{13} Hz signal corresponding to what is needed to tell when to start converting each array of 32 signals. By referencing the start of an array conversion signal to the shaft encoder, the timing would reflect any change or fluctuations in rotation velocity so the most accurate repeatability would be achieved.

To begin the design process, some of the system parameters are considered to get ideas on possible solutions. The main parameter of the system is time. To convert 2^{14} arrays of input during a 2 second revolution, which is 2^{13} arrays per second, means there is 122.07μs ($1/2^{13}$) to convert the 32–channel array. If this is broken down more, it gives 122.07μs/32 inputs or 3.815μs to convert each signal to its 12–bit equivalent. Additionally, since all of the digital outputs must be transmitted over the same data bus, they must be multiplexed together somewhere through the process. And lastly, due to the input signals' ability to have a full scale change between conversions, a sample and hold (S&H) must be used on the analog input before conversion can be done. To summarize, the neccesary components of this system are a sample and hold, an analog–to–digital convertor, multiplexing of data, and controlling circuitry to sequence through these operations and produce the status bits which were explained earlier. The different strategies were conceived on the basis of where the multiplexing of data is done and are shown in Figure 1.

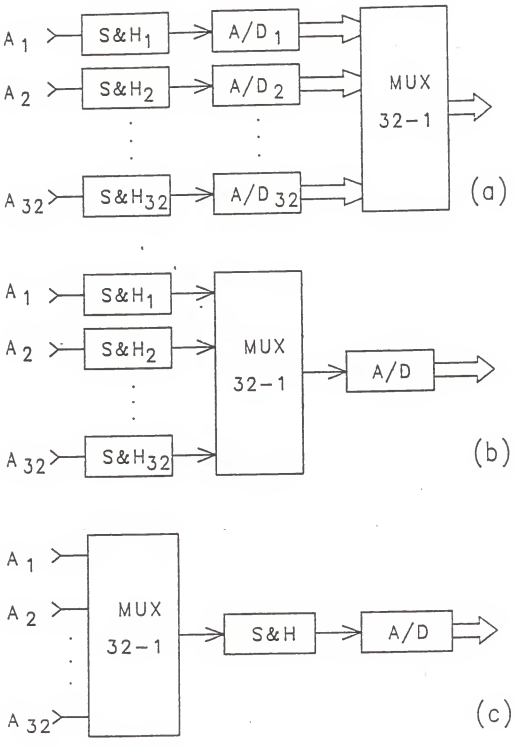


Figure 1. Possible System Strategies.

A discussion of each of the strategies will be given, relating their advantages and disadvantages to this project. In the first strategy, Figure 1a., the data is multiplexed at the output of the A/Ds. The advantage of this method is that there is 122μs for the S&H, A/D, and multiplexing of data for each channel so the components used can be slower which often aids accuracy and lowers the cost of each component. Also, all 32 channels can be converted at the same time so there would be no time skew between channels of the vertical array. However, there are some major disadvantages to this method. To start with, 32 A/Ds and S&Hs would be needed, and the 384 lines of digital output produced would need to be multiplexed into 12. This would require 2 levels of digital multiplexers (MUXs), since 32–channel digital multiplexers do not exist commercially. Even though time requirements allow getting less expensive and lower power chips, the power consumption and cost of the system would still be extremely high due to the quantity of chips. Another disadvantage to this method is the amount of board space such a design would require. Due to these significant disadvantages and the fact that simultaneous conversion of all 32 channels is not needed, this method was quickly dismissed.

The second design strategy, Figure 1b., places the multiplexers between the S&Hs and A/Ds. This method still allowed simultaneous sampling of all 32 channels, then switching each channel through and converting it. Since there was only one acquisition and hold delay needed for all 32 channels, the majority of the 122μs could be used to sequence through and convert the channels. The advantage to this strategy is that it eliminates 31 A/D

convertors over the previous design. Also the multiplexers are now analog so there are fewer of them required as well. This reduces size and power consumption requirements as well as inaccuracies caused by inconsistencies between similar A/D convertors. By converting all 32 channels with the same A/D, each channel will then contain the same A/D offset and nonlinearity errors. If these errors are consistent through all channels they can be more easily compensated for or even ignored. The disadvantages of this strategy center around the S&Hs and MUX. First of all there is nearly as large a chip count as in the previous strategy. Secondly, switching all 32 held outputs through one A/D creates new problems related to the hold time and droop rate of the S&H circuits. These parameters will determine how much time is available for the conversion of the 32 channels, because all 32 channels must be converted before the signal on the last S&H has been able to droop more than the accuracy of the A/D. Inaccuracies will also develop between channels because each successive channel will have had more time to droop than the previous channel. This problem could be gotten around by having S&H's with progressively larger hold capacitors, but such a set of S&H hold circuits would have to be custom designed, and this would add greatly to the complexity of the system.

The third strategy, Figure 1c., places analog multiplexers in front of a single S&H and A/D. This reduces the chip count, board space, and power consumption to a minimum, but it greatly reduces the amount of time allowed for each component in the design to complete its function. Another advantage to this strategy is that any inaccuracies in the S&H or A/D are

consistent across all 32 channels. The only disadvantage to this strategy is the time constraint, because the signal must be switched, sampled, and held while allowing the signal to settle in each stage, then converted, all in 3.815μs. This means that each step must take less than 1μs. In comparing the advantages and disadvantages of this strategy with the other, this strategy was considered the best if the proper components could be found.

2.2 Implementation of Strategy

After these three design strategies were developed, a component search was done to find existing commercial devices that would best implement the third strategy discussed in the previous section. The component search yielded a few A/D and S&H devices that met the time requirements for the third strategy, but they had slightly differing abilities and specifications. Since there were a small number of devices found, each device was looked at individually, and a design was developed that would best utilize that device's characteristics. The basis of all of these device dependent designs is the same. It is to multiplex all 32 channels into one S&H and A/D. Therefore, each design has many components that are common to all the other versions.

The first common component is the analog multiplexer. The multiplexers must be able to switch each input channel into the S&H within the aforementioned time allotment while still maintaining the accuracy of A/D. The main parameter of concern for the multiplexer is of output settling time once a particular channel is selected. However, crosstalk between channels and non-uniform channel characteristics are also of

concern. The 74HC405X series of high speed CMOS analog multiplexers was found to satisfy all these parameters, and is a common component in each design.

The next similarity between designs has to do with the timing and control of the conversions. The 2^{16} Hz signal from the shaft encoder will be used to synchronize the beginning of each array conversion, but there is still another signal needed to clock the circuitry used to control the sequencing through and conversion of the 32–channel array. This signal needs to have a frequency of about 1 MHz and was to come from an on board oscillator circuit; however, this signal is to be generated elsewhere in the system and will be another input to the A/D board. Also common in the control logic of each design will be the generation of the status lines for a bad cell either high or low and the detection of bad set. The bad set detection will be activated only when the signal to start an array conversion comes before the last array conversion has been completed. The reason for this is because the control logic for each design will stop converting the input channels once all 32 have been converted and wait for the start signal before it begins converting another array. In this manner, erroneous output will not be produced which needs the repeat status line.

The differences in the resulting designs are primarily due to the characteristics of the two A/Ds that were found to do a 12–bit conversion at 1 MHz. The first design, shown in Figure 2., is the most ideal of all the possibilities. This design uses a CSC5212 A/D which has a S&H circuit on the A/D chip. This device can hold the analog signal and convert it in

one microsecond. Since a separate S&H circuit is not needed, the overall process of converting a channel has now been made into a two step process. The reduction of complexity has several benefits. First it allows for the use of a slower internal clock frequency because the 3.8μs available only has to be split between the MUX settling time and A/D conversion time. Secondly the control logic consists of only a 6-bit counter to sequence through the 32 channels with the LSB of the counter controlling the A/D. And lastly, due to the simple design there are fewer chips, so less space and power are required. However, there is one major problem that did not allow this design to be used, which is the fact that the CSC5212 had not yet been released on the market.

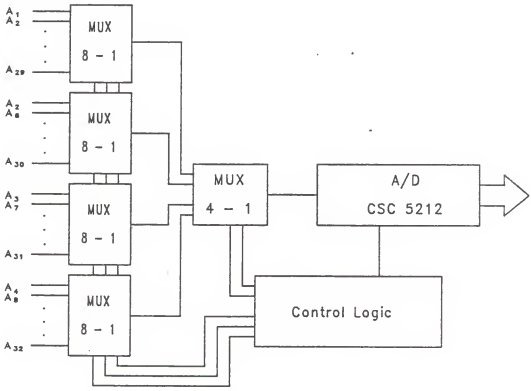


Figure 2. System Design with A/D Containing on Chip S&H.

Since the most desired possibility was not yet available, the next best solution would be to use an individual S&H and A/D chip as shown in Figure 3. This design is very similar in function to the previous design except separate commands must be sent to the S&H and A/D. This adds complexity to the design in two ways. First the control logic no longer goes in a natural binary sequence, instead two separate counters must be used. The first counter causes the 32 inputs to be sequenced through, and a second counter pulses the MUX counter then the S&H then the A/D. The other added complexity is that now only one-third of the 3.8μs per channel can be used to multiplex the 32 channels, and that is pushing the time limit of these devices. The reason for this is because

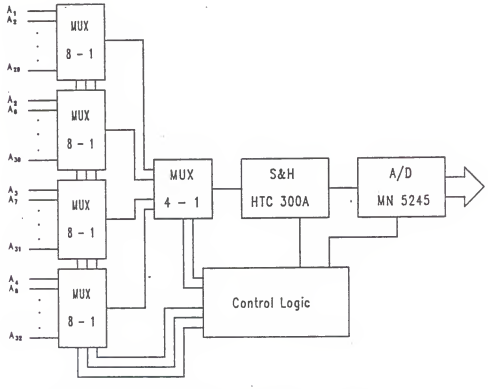


Figure 3. System Design with Separate S&H and A/D.

multiplexing of 32 channels has to be done in two levels, since a 32–to–1 analog MUX does not exist commercially, and 2 levels of settling on the 74HC405X series of multiplexers is about 1.2μs. These two levels of multiplexing cause the 3.8μs per channel to actually be divided into 4 parts.

However, in the search for S&Hs, the CSC31412, a 4 channel track and hold was found that would fit the design requirements. The benefit of such a device is that it combines the second level of multiplexing inputs with the S&H, so the 3.8μs per channel can be divided into 3 segments with each segment having ample time. The design implementing this device is shown in Figure 4. Since the A/D with an on chip S&H was not yet on the market, and due to the benefits of the CSC31412 four channel track and

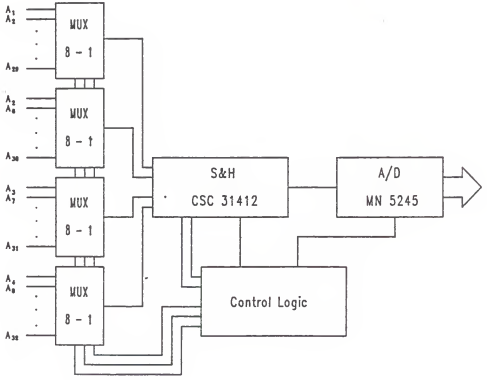


Figure 4. System Design with Four Channel Track & Hold

hold (4CT&H), the later mentioned design was chosen to be implemented and will be discussed in detail in the next section.

2.3 Four Channel Track & Hold Design

The design using the four channel track and hold (4CT&H), introduced in the previous section, was decided upon as the best solution for the problem at hand. At this time the 4CT&H design will be analyzed in more detail to include the overall system operations, design of the control logic, timing diagrams, and explanation of special inputs and outputs.

2.3.1 System Operation

The first thing to be looked at is the overall operation of the 32–channel 12–bit A/D system. The 32 analog inputs are multiplexed into the 4CT&H with four 8–to–1 multiplexers, then the output of the 4CT&H is fed to the A/D. A schematic of the complete system including the control logic and output latches can be seen in Figure 5. Also a list of the chips used in this design is given with their power requirements in Section 2.3.7. Since the 4CT&H does a simultaneous hold of all four analog inputs a little more time is saved, but a slightly more complex controlling circuitry is required. The sequence of the control logic is as follows: 1) allow for the multiplexers to settle after being switched, 2) hold the inputs of 4CT&H and allow outputs to settle, 3) switch through and convert each of the four held signals, 4) switch in a new set of four signals and allow them to settle as in step one. This sequence needs to be executed eight times to allow all 32 channels to be converted, and after the eighth sequence is done, the control logic needs to shut itself off.

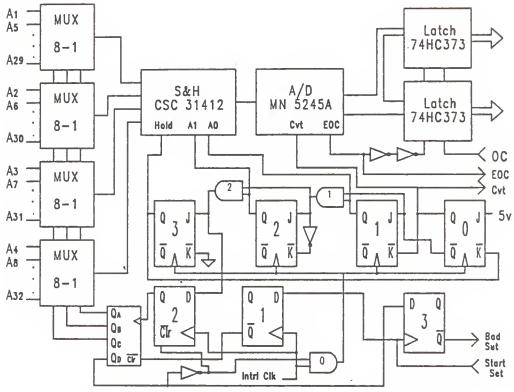


Figure 5. Four Channel Track & Hold Schematic

2.3.2 Control Logic Design

To achieve the proper control of the system a special purpose counter was designed using JK flip-flops. The first of the eight sequences is shown in Table 1. Steps 2 through 10 of the table are repeated seven more times to get all 32 channels converted. The switching of the MUX's is initiated in step 9, because an additional clock pulse is needed for the signal to propogate the D flip-flop in front of the counter clock. This flip-flop is present to eliminate any glitches that might occur in the counter circuit from clocking the counter at the wrong time. As shown in the timing diagram in Figure 6., the counter circuit can produce glitches if the outputs of the JK flip-flops do not change at the same time. This glitch could then pass through the AND gates to the input of the D flip-flop; however,

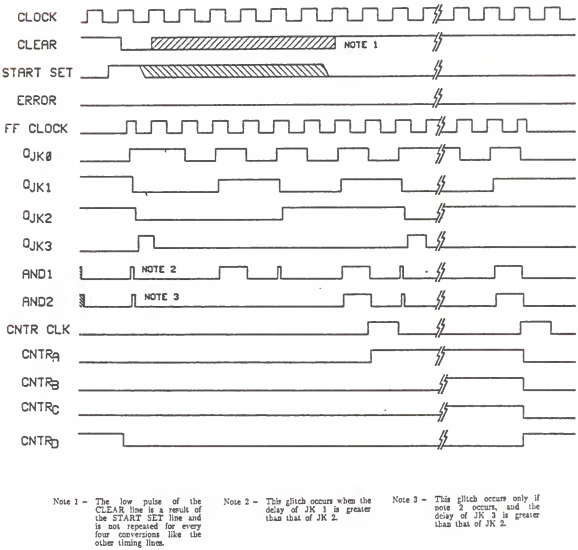
Table 1. Sequence of Special Counter

	MUX			4CT&H			A/D
	Q_2	Q_1	Q_0	Hold	A_1	A_0	Cnvrt
1)	0	0	0	0	1	1	0
2)	0	0	0	1	0	0	1
3)	0	0	0	0	0	0	1
4)	0	0	0	0	0	0	0
5)	0	0	0	0	0	1	1
6)	0	0	0	0	0	1	0
7)	0	0	0	0	1	0	1
8)	0	0	0	0	1	0	0
9)	0	0	0	0	1	1	1
10)	0	0	1	0	1	1	0
11)	0	0	1	1	0	0	1

since these glitches are much smaller in duration than the clock period, they will not get past the D flip–flop.

A D flip–flop was also placed between the start set signal and the asynchronous clear of the counter to synchronize the control logic's sequencing with the internal clock signal. Otherwise the start set signal could cause a short clock period that would not allow enough time for the 4CT&H to accurately sample the input signal. The necessary time delays can be seen in the first clock period of the timing diagram.

The last major function of the control logic is to shut itself off after the 32 conversion has been completed. This is accomplished by using the most significant bit of the MUX counter. This counter output is inverted and ANDed with internal clock, so when the counter is clocked the 33rd time the internal clock will be shut off, causing the system to stop in the power–up state. Then when the MUX counter is cleared asynchronously, system operation will start again.



Note 1 – The low pulse of the CLEAR line is a result of the START SET line and is not repeated for every four conversions like the other timing lines.

Note 2 – This glitch occurs when the delay of JK 3 is greater than that of JK 2.

Note 3 – This glitch occurs only if note 2 occurs, and the delay of JK 3 is greater than that of JK 2.

Figure 6. Timing Diagram for 4CT&H Design.

2.3.3 Internal Clock

The operating frequency range for the internal clock was found through the following manner. From the timing diagram, Figure 6., it can be seen that the maximum frequency must allow for delays through a D flip–flop (t_1), the asynchronous clear of the counter (t_4), an inverter, an AND gate (t_5), and the acquisition time of the 4CT&H, which all occur in the first clock period of each array. This value equals 1.13μs, so the maximum frequency is 885.0 KHz. At this clock frequency an array conversion which requires 72 clock periods should be done in 81.4μs which is 66.65% of the total allowed time. The delay through the J$\overline{K}$ flip–flop of the counter can be ignored, because it also occurs in every conversion, so it acts as a time skew. The minimum frequency is that which would still allow all the conversions to be performed within the 122.07μs allowed. For all 32 conversions to occur, 72 clock periods must be sequenced, so that would allow a maximum clock period of 1.695μs or a minimum frequency of 589.82 KHz. Therefore, the range of the internal clock frequency is 885.0 KHz to 589.82 KHz.

2.3.4 Start Set Signal

The start set signal is an external input which synchronizes the conversion of a 32–channel array with the system's rotational orientation. In order for the system to meet its initial requirements this signal must be at a frequency of 2^{13} Hz, so a rising edge would occur every 122.07μs. This signal should be normally at a logic low level then pulse high. The above specifications for the range of internal clock frequency would require the pulse to be greater than 1.7μs and less than 6.9μs. The reason for this

pulse width is because the signal must be logic high for greater than one internal clock period and less than seven internal clock periods. The reason for its length requirements is so the pulse is long enough to guarantee it is seen as a data input to the D flip–flop and short enough that when the MUX counter needs to switch in the next four inputs, the clear signal is gone from the counter so a count can occur. If the start set is a negative logic signal the clear to the counter should be taken from the non–inverting output of the D flip–flop. If the start set signal is to be generated from the 2^{16} Hz shaft encoder then a circuit will need to be designed that will divide the frequency by eight and generate a pulse of the required width. But this was to be done elsewhere in the system.

2.3.5 Power–Up

All of the controller chips have the capability of being set or cleared at power–up by holding the appropriate pin low with a resistor–capacitor power–up circuit. The counter and each flip–flop are set to the following state at power up: D flip–flops (1) and (3) and $J\overline{K}$ flip–flops (0) and (3) are set low, D flip–flop (2) and $J\overline{K}$ flip–flops (1) and (2) are set high, and the counter outputs Q_D Q_C Q_B Q_A are loaded with the values 1000, respectively. By powering up to this state the first four input signals are already being tracked at the input of the 4CT&H, so they are ready to be held and the conversions to begin. Also the most significant bit output from the counter is a one, so the clock to the special purpose counter is off so this system will not generate any erroneous output.

2.3.6 Outputs

The outputs of the current design include the 12–bit data value, end of conversion (EOC), and error. The EOC output is from the A/D to tell when the latches contain valid data. This signal is needed because of the somewhat asynchronous nature of the 32 twelve–bit outputs. After the start set arrives it is approximately three internal clock periods before the first 12–bit conversion is valid on the output latches. At that time each of the first four outputs are latched every two internal clock periods, then there is another delay for three internal clock periods before four more outputs are latched at two internal clock period intervals. This continues until all 32 channels have been converted, then the last channel to be converted is held valid until the next array conversion begins. The timing details of when the output is valid are as follows: during a conversion of the A/D (when convert line is low) the output is not valid but becomes valid on the falling edge of the EOC line and remains valid until 40ns after the EOC line goes high. This means valid data will be at the output of the latches from the previous conversion while the convert line is high, waiting for its analog input to settle.

The other error line tells if the last array of 32 channels was done before the start set signal arrived. If the last set was completed the error line remains low, or goes low if it was high prior to the start set signal. However, if the last set was not completed when the start set signal arrives, then the error line goes high, or remains high if it was previously so, until the next start set signal arrives. The start set signal is a positive edge transition.

The bad cell high and low have not been built into this circuit but could be easily done by comparing the output of the 4CT&H to 5v and Ov, respectively. In this manner, if a signal appeared which was out of that range, then the proper comparator would have a logic high output signaling a bad cell. Also this circuit does not contain a status line to relay the health of the A/D, or a Repeat line. The reason for not giving a Repeat line is because after the circuit converts the last of the 32 channels, it stops itself instead of starting over again. The A/D health line was not implemented, because there is no way of knowing that information without running a special test on known data which is not accessible from system control.

2.3.7 Power Requirements

This system requires ±15v and +5v power supplies. The only chip which requires the ±15v is the A/D. The other chips are powered at Ov and 5v. The power dissipation of each chip listed below is a maximum for that chip as given by manufacturers data sheets.

Table 2. Power Requirement for 4CT&H Design

MN5245A		2.63 W
CSC31412		.5 W
74HC4051	4 @ .5W each	2.0 W
74HC161		.5 W
74HC109	2 @ .5W each	1.0 W
74HC74	2 @ .5W each	1.0 W
74HC08		.5 W
74HC04		.5 W
	Total power dissipation	8.63 W

2.3.8 Calibration

The only part of this circuit that can be calibrated to changing conditions is the 4CT&H. It has an auto-calibration capability which reduces internal errors to $\pm 700\mu v$ ($\pm 1/2$ LSB for 12 bits over a 6v range). The calibration cycle takes 3.5 ms and is required to be done at power-up. It is also recommended by the manufacturer to calibrate the device occasionally (once a day under normal operating conditions). Without this occasional calibration the device can drift with temperature to a maximum constant offset of about 6 mv. Also there is an approximate linear relationship between the voltage offset and operating temperature of about $30\mu v/^{o}C$, and for temperatures above the $70^{o}C$ the relationship is slightly greater. However, since all four channels are identically designed the voltage offsets should be identical over all four channels.

3.0 500 MHz 8–bit A/D Memory System

This chapter investigates possible sources for a 500 MHz analog–to–digital (A/D) converter and a 16 K byte random access memory (RAM) in Gallium Arsenide (GaAs). The designs made in this chapter are based on information gathered at this time, and due to the rapid advancements that are being made in this area, these could change at later dates. Also any opinions and conclusions drawn in this chapter are those of the author and may not be held against Kansas State University or Sandia National Laboratories. Some of the characteristics of this A/D memory system are:

A/D – · 8–bit @ 500 mega samples per second
· analog bandwidth ~ 250 MHz
· input range > 100 mV
· power dissipation< 1 Watt

Memory – · 16 K x 8 bit of RAM
· circulating architecture
· power dissipation 1 – 2 Watts

System – · continuous running
· radiation hardness – total dose 10^6 Rad/si
– single event upset not critical

Time Frame – · Bread board in 1989
· Functional A/D in 1991
· Space Qualified in 1992

This chapter summarizes the information I have gathered to date on current technologies to solve this problem, and who in industry is

working on these technologies.

The A/D system desired is of very high speed and extremely high accuracy for that speed, especially compared to existing devices. However, there are several semiconductor technologies that industry is trying to take to these speeds. They are:

silicon:

1) emitter-coupled logic (ECL)
2) bipolar

gallium arsenide:

1) enhancement/depletion mode metal semiconductor field effect transistor (E/D MESFET)
2) high electron mobility transistor (HEMT), or modulation-doped field effect transistor (MOD-FET), or selectively doped heterostructure transistor (SDHT)
3) heterojunction bipolar transistor (HBT).

Each of these types of GaAs semiconductors will be explained more in later sections. Most of the research for this device has been done in the GaAs technologies, but silicon was also considered briefly.

Research on GaAs started about the same time as Si; however, because silicon was more readily available and less expensive, GaAs was not worked with as much. However, now due to the need for faster, lower power, and more radiation resistant devices, GaAs is getting much more attention. Gallium arsenide is currently and probably always will be used for a limited market. This market is one which is looking for extreme speed, low power and/or high radiation tolerance.

The designers and manufacturers are very specialized and only work in some small segment of the market. Current research with GaAs has achieved the medium to large scale of integration (MSI → LSI), and production lines are turning out wafers with moderate to good yields. The improvement of production yield will come with time as the process is further studied and refined. Also, as the fabrication process is making its evolutionary improvements, GaAs devices are becoming more reliable and easier to design into a system. As of now there are very few commercially available GaAs chips or devices "on the shelf", but there are many devices being developed, most of which are for military uses or for high speed test equipment.

From our finding, a 500 MHz, 8-bit A/D with 16 K bytes of circulating memory is possible in the time frame desired but not within the power budget. However, it probably won't be able to be done by a single source, because developers of GaAs devices are still very specialized. That is, those who have done much A/D work have not tried to develop memory and vice-versa. But I have found leaders in each area, and they are:

A/D	Memory
1. TRW	1. Honeywell
2. Rockwell	1. Rockwell
3. Hughes-TI	2. McDonnell-Douglas

From our investigation I feel that TRW is most able to produce an 8-bit A/D in GaAs to meet the prescribed requirements. However, for a GaAs memory system, Honeywell and Rockwell are very evenly matched.

Therefore, I feel that the best device would come from a joint effort of TRW and whichever of Honeywell and Rockwell whose process is most compatible with TRW's.

As this project proceeds, there are several aspects which need to be considered and monitored throughout the devices' development. One of them is methods of controlling these devices and making them function as a system. Along with current developments of A/Ds and memory, much work has also been put in gate arrays, which could be used to make these devices function together [11]. Logic levels also need to be considered to make GaAs devices function together. Due to the newness of GaAs, there are no standard logic levels or power supplies which are used in existing designs. This may seem trivial, but some devices or designs depend highly on these parameters and possibly could not be redesigned or modified to different levels. Another consideration is that due to the current state of technology, getting this entire device on one chip is impossible, and with multiple chip design comes an enormous job of interconnecting. Due to the speed of these devices, every trace becomes a transmission line which needs to be the proper length with the proper shielding and matched impedances [5]. Last, and possibly most crucial, is that of testing. Extensive testing needs to be done before, during and after production. One characteristic GaAs has experienced is the difficulty in producing truly identical transistors. Even for transistors which have been through the same production process side-by-side on the same wafer, they can and have exhibited strikingly different fundamental

characteristics [13].

Given the requirements of the above mentioned A/D memory system this paper summarizes a search conducted to see what companies, if any, could develop and design such a system. The next section discusses the companies that were contacted and their involvements and accomplishments in GaAs. After that is an overview of what was found out about GaAs in general. It will discuss the most common GaAs technologies being used and some of the advantages and disadvantages of GaAs versus silicon.

3.1 Company Comparison

To begin the search for a company that could build a device to meet the specifications, an extensive literature search was conducted to get material pertaining to very high speed memory and A/Ds. From this material I first tried to gain a good working knowledge of the problems and characteristics inherent in producing an 8-bit, 500 MHz A/D and a SRAM with sub-two nanosecond cycle times. This material also gave us many companies doing work in these areas and the person to contact within the company. A questionnaire was then drawn up which contained pertinent topics to be asked of each of the companies on what that company had achieved and what it had planned for development in the near future. Table 1 gives a brief summary of these company findings. A list of all the companies' contacts with their addresses and telephone numbers is given in Appendix A.

Table 3. Overview of Company Surveys

Company	Contact	Achievements	Ability
TRW	Ken de Graaf	Delivered 6-bit A/D 16 M byte system @ 330 Msps	A/D – good
Rockwell International	Jim Donovan	Have 4-bit HHT quantizer and 1 K SRAM	A/D, Memory – good
Honeywell	Wayne Walters	1 K SRAM; t_c < 1 ns	Memory – good
Hughes	Paul Greiling	Testing 4-bit A/D @ 500 M – 1 GHz	Memory – good
TI Central Research Center	Bill Wisseman	HHT process line for DARPA A/D's	A/D – fair
McDonnell-Douglas	Rainer Zuleeg	1G K x 1 SRAM 90% operational	Memory – good
Gigabit Logic	Mike Pawaik	Marketing 256 x 4 SRAM access time; t_a = 2.5 ns	Memory – fair
Vitesse Electronics	Tom Ducan	Marketing 256 x 4 SRAM; t_c = 3 ns	Memory – fair
Gain Electronics	Mike Logan	1 K x 4 SRAM in March; t_a = 3, 4, and 5 ns	Memory – fair
Ford Micro Electronics	Rich Griffith	1 K SRAM; t_a = 2 – 2.4 ns	Memory – fair
A T & T	Howard Kirsh	256 x 1 this year; t_a ~ 2 ns	Memory – fair
ITT GaAs Technology Center	Edward Griffin	Working toward 8-bit A/D and 1 K SRAM @ 1 GHz	Memory – fair
TI Defense Systems & Electronics	Larry Housey	1 K SRAM; $t_c \geq 2$ ns	Memory – fair
Microwave Semiconductors	Jim Dilorenzo	Testing 5-bit A/D @ 500 MHz	A/D – fair
Anadigics	Michael Gagnon	Marketing sample & hold; 8 ns acquisition time	Poor
Harris Microwave	Kim Thomas	Just starting digital work	Poor
Pacific Monolithics	Alan Podell	Some comparator work	Poor
Tri Quint	Tom Reeder	Good foundry, but no custom design	Excellent foundry
Adams-Russell Electronics	Michael Smith	Not digital	Not applicable
Bipolar Integrated Technology	Bruce Miller	Does Si work	Not applicable
GE	Mosshi Namordi	Has done A/D's but not interested	Good
Hewlett-Packard	John Corcoran	Uses GaAs but doesn't do custom work	Not applicable
Mayo Clinic	Barry Gilbert	Does direct DOE and DOD research	Not applicable
Micrel	Ray Zinn	Does Si work	Not applicable
RCA Advanced Technology Center	Jerry Richards	GaAs work on hold	Poor

The following is a brief discussion of each of the relevant companies. The discussion about each company will first contain the information I obtained from that company about their current activities with GaAs. Most of this information was obtained during phone conversations or sent as a result of these conversations. After the discussion will be an assessment of what I feel are that company's capabilities relative to the development of an A/D–memory system or some part of the system. The latter part will contain ideas by that company about the system and our opinions about credibility of their ideas.

Each of the companies in the above table will now be described in more detail. As with the table, these companies will be discussed in descending order of achievement to date, thus rating them with respect to whom I feel could best develop an 8–bit, 500 MHz A/D and 16 K x 8 SRAM within the specifications given us.

TRW

A/D

TRW has several A/D memory systems they are designing and/or testing at or above 500 MHz in both E/D MESFET and HBT technology.

1) They have an 8–bit 1 GHz A/D in the final layout which has been developed through a DARPA contract with Naval Research Laboratories (NRL). The A/D does a conversion one bit at a time with a serial feed forward architecture. This A/D is being made with a Honeywell E/D MESFET Process. The NRL contract monitor is Dr. Ken Sleger at phone number (202) 767–3894 in Washington, D.C. This development project currently is on hold, however.

2) They are also developing another A/D with 8-bit accuracy at greater than 500 MHz sampling rates. This A/D is series parallel feed forward architecture that is in the late layout stage. They have the first wafers now and expect to see a chip in the near future which they will be testing through January, 1988. This is with TRW HBT technology. This work is being done for SDI with the Army at Huntsville through Dynetics. The contract monitor is Bob Cashion at phone number (205) 837-9230 in Huntsville.

3) They have delivered a 6-bit A/D with 16 M bytes of memory that had a sample rate of 300 M samples per second to the Air Force. The person to contact is Chern Huang at Wright Patterson AFB, phone number (513) 255-7142.

Memory

TRW has not developed any GaAs memory. Some of the above mentioned A/D systems have also included memory compatible with them. However, the way in which TRW develops its memory systems is to demultiplex the output of the A/D into a wide memory buffer between the A/D and memory. This way they slow the data rate into memory enough to use available CMOS memories. Their system design strategy is to develop custom GaAs until they can use available GaAs then down to CMOS.

Assessment

I have found no other company that has developed A/D devices as close to what I are looking for than TRW.

TRW has developed and has been testing the highest precision A/Ds in the 500 MHz to 1 GHz range that I could find. For this reason I feel that they are most capable of developing an 8-bit, 500 MHz A/D that could place its output into memory. Also, since TRW has developed complete A/D memory systems, they should already know the communication and interconnection problems that must be worked out at these speeds. However, since they have not done any development on high speed memory, I feel there are other companies better able to achieve that goal. The CMOS memory used may not be able to withstand the radiation hardness criteria placed on this project.

Rockwell International

A/D

Rockwell has several A/Ds that are being worked on.

1) 6-bit 1 GHz A/D in HEMT technology. This A/D has a flash architecture with a sample and hold in front of it. It has been tested on signals up to 400 MHz. They do not feel that a HEMT A/D could be made to get 8 bits of precision.

2) They have also developed 4-bit quantizers in HBT technology and are working on 6-bit quantizers. One question they are working on with these quantizers is the need for sample and holds in front of them. Due to the characteristics of HBT and their design approach, they feel a sample and hold might not be needed for sampling rates less than about 1 GHz.

Memory

Rockwell has built fully functional 1 K static random access memories (SRAMs) for the Office of Naval Research (ONR). These SRAMs have access times of .5 to .6 ns and dissipate 200 mW of power. The contract monitor at ONR is Max Yoder, phone number (202) 696-4218. This memory chip was made in HEMT technology because HEMT tends to have a lower power consumption. They now have a 4 K x 1 SRAM about 70% functional. This 4 K device has had access times from .6 ns to 1.6 ns, cycle times of at least 5 ns, and dissipates 700 mW. They feel the reason for the failures is because these devices are being made in the research and development lab. Masks are being made to move these devices to a cleaner production environment; then they expect fully functional 4 K devices.

Assessment

Rockwell was found to be second best in A/D development, and their memory work equals the best found. Rockwell International has done development of both A/Ds and memories, so they would have a good knowledge of what would be needed to develop an A/D memory system. However, they have not yet produced an A/D or memory of the size desired. This is what places them in second place. To achieve an 8-bit A/D, they would place 4 of the 6-bit quantizers together to get the 256 comparators needed for 8-bit flash. They had much reservation about the power requirement on the 16 K x 8 memory. From their experience, they felt that a continuous running system would require at least 10 W of power, even with lower power HEMT memory.

Honeywell

A/D

Honeywell is currently working toward 8-bit and is testing 4-bit.

1) Honeywell is testing a 4-bit 1 GHz A/D that is in MESFET technology. When tested at 1 Gsps this A/D demonstrated 6-bit linearity with an analog bandwidth of ≈ 600 MHz and dissipated 500 mW. More power would produce more speed, 2W at 2 Gsps. However, they do not plan to extend MESFET technology to 8 bits.

2) Honeywell has tested a comparator in MODFET (HEMT) technology that is accurate to 2 nV at 1 GHz. Currently, they have a 4-bit A/D using this comparator design in process. They expect to extend this design to 8 bits.

Memory

Honeywell has current memory projects in Self Aligned Gate (SAG) MESFET.

1) Honeywell had a contract to develop a 4 K RAM on the Subnanosecond Memory/Logic Development program funded by USAF Aeronautical Systems Division of A. F. Wright Aeronautical Laboratories (AFWAL), Contract No. F33615-85-C-1807. The contract monitor was Ron Bobb, phone number (513) 255-8645. AFWAL funding problems caused the program to end early, but it still resulted in 256 x 1 and 256 x 4 bit devices which were tested to have access times of 1 ns with 300 mW power dissipation on the 256 x 1 devices. This program was continued on corporate funding and resulted in 1 K x 1 chips with 1.2 ns access times at 500 mW. The next step in this process is to organize a 4 K device into 16 256 x 1 blocks. This strategy is to reduce power, because all except the active block would be at a reduced (standby) power level.

2) Another project is a 16 K, 8 ns, 1 W device funded by NRL. This is Contract No. N00014-85-C-2584, monitored by Ingam Mack, phone number (202) 767-1019. So far they have demonstrated a 1 K with 3.8 ns access times at 800 mW. The next pass will be a 4 K chip with different drive electronics to significantly reduce the standby row and column power dissipation.

3) Honeywell has done some initial research with other GaAs technologies that show great promise. Honeywell GaAs complimentary heterostructure technology can be used to achieve SRAM with performances of 1 ns access times with about 20 mW per 1 K bits. They also have shown 256-bit MODFET (HEMT) SRAMs with access times of .7 ns.

Assessment

Honeywell has done much development in both A/Ds and memories. They have also developed a sample and hold in MODFET that should greatly reduce the aperture jitter. However, their A/D development does not seem to be as far as that of TRW or Rockwell. But in the area of GaAs memory Honeywell appears to be among the best. Since the A/D-memory system will be doing a sequential fill of memory, a block architecture of memory would work well and reduce total continuous power. Honeywell has worked on a segmented reduced power memory architecture before and is planning to use it in future GaAs memory designs.

Hughes

A/D

1) Hughes has conducted tests on a 4-bit MESFET A/D in the 500 MHz to 1 GHz range. They do not yet have results on which to draw conclusions. This project has been stopped for lack of funds.

2) They have just received a joint DARPA contract with TI. Hughes' part is to do the circuit design and layout of these A/Ds: 8-bits @ 1.5 GHz, 5-bits @ 2.5 GHz and 14-bits @ 10 MHz. These A/Ds are to be in HBT technology. Contract details are given in the TI section.

Memory

Hughes has done no memory development.

Assessment

Hughes proposes that the A/D-memory system should be done in HBT technology, and this would work nicely with their existing DARPA contract. However, I question their ability in reference to the time frame. The DARPA contract is a three-year project which was just awarded in September, and at last account was still being finalized. "General industry feeling is that HBT is still too researchy."

Texas Instruments – Central Research Laboratory

A/D

TI has just been awarded a joint DARPA contract with Hughes from ONR. It is the GaAs Heterojunction Device Based A/D Converter Program, Contract No. N00014–87–C–0314, and the contract monitor is Max Yoder, phone number (202) 696–4218. TI's part in the contract is to develop the processing and fabrication of the HBT A/Ds listed prior. This is to be a planned process.

Memory

TI has done no memory development.

Assessment

As discussed with respect to Hughes, the main factor is the time frame. When talking with TI, they expressed no interest in custom design of other devices yet and also expressed concern about manpower availability. Their interest would be with the A/D only.

McDonnell–Douglas

A/D

McDonnell–Douglas has no A/D program.

Memory

They have a 4 K bit SRAM chip with 4 ns access time that is one year old. Also, they have a 16 K x 1 SRAM. The second lot had two functional devices. The process uses DCFL for the peripheral portion of the memory and complementary FETS for the memory. It is on a single chip with access times of 10 ns. They are also working on an AOSP contract with DARPA for 10 Mbytes of GaAs storage with 10 W of power. The speed requirement is uncertain. The contract monitor is Sven Roosild at phone number (202) 694–3145 in Arlington, Vermont.

Assessment

McDonnell–Douglas has worked on several memory projects. However, most of their work has been at access times from 4 ns to 10 ns. Getting the cycle time under 2 ns has proven to be very difficult for other companies. Even though McDonnell–Douglas has developed larger memories with moderate power consumption, the fact that they have not achieved lower cycle times places them below the companies mentioned above. Also, their capabilities would be limited to that of memory.

GigaBit Logic

All their work has been in D and E/D MESFET.

A/D

They are currently working on a contract for a 4-bit A/D to run at about 1 Gsps. This design is being done using the common cell library used in their foundary.

Memory

They are marketing a 256 x 4 SRAM that uses a D-mode MESFET process. This chip has a fully pipelined architecture with access times of 2.5 ns and power consumption of 2.5 W. The architecture design allows the chip to be internally clocked and generate its own read and write signals. The core memory of this chip would have access times of about 1 ns by itself with an external clock. This would also greatly reduce its power consumption. They are about to start testing on a 4 K SRAM chip that is a core type memory in E/D MESFET. It should have access times near 1 ns and power consumption of about 2.5 W.

Assessment

GigaBit Logic has capabilities of producing an A/D-memory system, but they are not as capable as the companies discussed above. For the A/D-memory system they felt they could extend their current 4-bit MESFET A/D to 8 bits. To go with the A/D they have existing memory capable of the speeds needed, but it needs to be expanded to larger sizes and refined to reduce power consumption. The only factor holding back GigaBit is that other companies have produced devices closer to our needs.

Vitesse Electronics

All their GaAs work has been in E/D MESFET.

A/D

They have been contacted by Sandia previously to submit ideas for an 8-bit 1 GHz A/D. At that time they proposed a system which had a GaAs sample and hold in front of 4 silicon quantizers. However, nothing materialized from the proposal. This proposal is the only work they have done with A/Ds or sample and holds. All of their work is concentrated on purely digital systems.

Memory

Currently, they are marketing the AMD 2900 series microprocessor bit-slice family in GaAs. These chips use a MESFET technology and the memory chip AMD 2902, a 256 x 4 SRAM, and have cycle times around 3 ns. They are working on

a 4 K (1 K x 4) SRAM to use with the bit-slice family, but it is not quite ready for market yet. The AMD 2902 has been tested to be radiation hard to 100 Mrads. Some of these radiation tests have been done by Sandia.

Assessment

Along with the bit-slice family, Vitesse also produces 1500 and 4500 count gate arrays in GaAs. All of these devices are produced in their foundry, of which they offer high quality foundary services. They are now doing more custom design of devices to be produced in their foundry. Also, they are doing research with other device technologies, but none of them are at a stage to be implemented yet. In reference to the A/D-memory system, Vitesse's capability would be with gate array controllers or memory, but their memory work is not as advanced as other companies already discussed.

Gain Electronics

A/D

Gain Electronics has not done any A/D work previously, but they gave an initial proposal of how they would progress to achieve an 8-bit A/D. They proposed to develop an A/D in SDHT (HEMT) technology with a flash design approach. First, they would design a comparator with 8-bit precision and implement it with a 6-bit A/D design. Then from the results of the 6-bit testing, they would make any necessary modifications to fabricate an 8-bit design.

Memory

They have developed 1 K and 4 K memory chips on a gate array design basis. There are to be discrete samples of these chips available in March of 1988. The memory chips are to be in 3, 4, and 5 ns versions. All of these timing versions are with no self-timing included.

Assessment

I believe Gain Electronics would be able to provide an A/D memory system to meet the desired specifications, but not in the time frame set out. The reason for this belief is because to develop such a device they would probably need to use their SDHT technology, but they have not developed many devices in SDHT and no A/Ds in any technology. So there would be much analog characterizing that would need to be done in the development of a comparator to base an A/D on.

Ford Micro Electronics

They use an E/D mode Self-Aligned Gate FET technology (E/D SAGFET).

A/D

To date Ford has not produced an entire A/D in GaAs. However, they have been fabricating A/D components on SRAM wafers, then testing the components. These tests have then helped them characterize both their E/D SAGFET technology and their A/D component design. Some of the components they have tested include: comparator trials, custom logic, and gate arrays. Also through this process they have produced a 4-bit D/A.

Memory

They are currently working on a 1 K SRAM in E/D SAGFET. From their preliminary tests, they are getting access times from 2 ns to 2.4 ns in the best cases. This device is not totally functioning yet, because to get all of the bits to function, the power supplies have to be adjusted slightly on a bit-by-bit basis.

Assessment

Ford Micro Electronics is at about the same stage as Gain Electronics. They have the capability, given enough time. However, I don't believe they could produce an 8-bit A/D and 16 K x 8 SRAM by mid 1992.

A T & T

A/D

Currently they are setting up an SDHT process line, from which they plan to produce GaAs A/Ds, but they have no contracts or internal plans to design an A/D currently. The pilot line should be set up by April.

Memory

They have a DARPA contract to develop memory for the MIPS microprocessor that McDonnell-Douglas is developing. The memory will have cycle times of at least 2.5 ns, because that is the speed that the processor is to operate at. However, A T & T would like to have its time under 1 ns, because that would make a more desired device in industry. The architecture of the memory is not definite either, because that also depends somewhat on the processor. Currently it is a non-pipelined architecture. They plan to have a 256 bit sometime this year, 1 K in the middle of 1988, and a 4 K sometime in 1989. Currently the power consumption is about 200 μW/bit, but that is a function of the process. As the process gets more refined, the power requirements should decrease.

Assessment

A T & T is also in the same state as Gain Electronics and Ford Micro Electronics, in that they are developing a good process, but they are not ready to handle an 8-bit A/D with 16 K bytes of memory at sub 2 ns. They are still testing their SDHT technology and finding out what its characteristics are. They are seeing how much they can reduce the power consumption, without causing problems like single event upset.

ITT GaAs Technology Center

They use a Self-Aligned Gate direct couple FET technology (SAGFET) all on IR & D money.

A/D

They made a 4-bit A/D as a fabrication test vehicle. When it underwent testing, it achieved 3-bits of resolution. The problems were traced to error algorithms of the device. Currently, they are in the final layout of a 5-bit A/D, which they hope to have in fabrication by the end of the year.

Memory

They are currently working on memory systems much like our device would need. They are demultiplexing the data into a wide enough word, so it can be handled by CMOS memory. However, this would not have the radiation hardness, which is needed. They are also developing GaAs memories, currently working on a 256-bit memory.

Assessment

The goal that ITT is working toward is an 8-bit A/D and 1 K x 8 SRAM that operate at or above 1 GHz. This developmental process is currently being funded from internal research and development funds. The first phase of this goal is due to produce a 5-bit A/D and 256-bit memory by the end of 1988. They seem to be well on their way to meeting this goal, but once again, there are other companies which may deliver such a device sooner.

TI Defense Systems and Electronics

A/D

They have not done any A/D work.

Memory

They have developed a 1 K SRAM with access times from 2 ns – 4 ns, but the development of a 4 K has been placed on hold. The development stopped, because the contract ran out of money, and internal funds could not be acquired.

Assessment

TI Defense Systems and Electronics has done development on strictly digital GaAs devices. Their current work is on a DARPA contract to build a RISC processor and compatible co-processor and memory mapper. Larry Housey from TI DSE gave a presentation on their work to Sandia on May 23, 1987. Since their work has been with processors, and they stopped their memory development, I believe other companies are better qualified to develop the A/D-memory system.

Microwave Semiconductors

A/D

Microwave Semiconductors is currently testing a 5-bit A/D at a sampling rate of 500 MHz. Details about this and any other devices could not be obtained on any of several attempts.

Anadigics

Anadigics has not done much work with digital circuits.

A/D Related

They have not developed any A/Ds or memories. However, they have worked on some small devices related to A/Ds. The first is a hysteresis free comparator. This comparator operates from ± 5 V power supplies and has a 1 ns propagation delay with a + 30 mV input offset voltage. This device is accomplished in D MESFET with a proprietary hysteresis-killing circuitry. Another related device is that of sample and holds. They have developed a GaAs sample and hold with 8 ns acquisition time and a droop rate of 30 mV/μs. This device also operates at ± 5 V power supplies over the commercial temperature range and consumes .5 W – 1 W of power.

Assessment

Anadigics had been developing mainly monolithic microwave integrated circuits (MMIC), but now they are starting to work into analog-to-digital conversion. At this time I do not feel they are capable of developing an A/D-memory system, due to their lack of work in that area.

Harris Microwaves

Assessment

Harris Microwaves has produced many MMIC devices on a 1 μm FET technology and is now starting to look into the digital market. They have just begun a program to develop a 6-bit A/D. However, there has been very little work done on this device to date. This work is being done due to corporate initiative to get involved with A/Ds.

Pacific Monolithics

Assessment

Pacific Monolithics also works mainly with MMIC devices. They have done a little work with comparators but no A/D development. To develop a device to operate at or above 500 MHz would be no problem. However, to reach an accuracy of 8-bit would push their limit.

Tri Quint

Assessment

Tri Quint has a very high quality foundry service, but they are just starting to do custom design of devices. They have produced RAM devices and an 8-bit D/A. However, for the A/D-memory system desired, they are not experienced with space qualified parts, and 8-bits would be a major problem. For our device they would use either a 2-stage flash or a 4-6 bit quantizer architecture. Also, this device would need a sample and hold on the front end. They feel that HBT technology characteristics would be best, but that technology is still "too researchy" for the time frame of this project.

The following companies were also contacted about their use of GaAs devices and development of the technology. However, due to the work of these companies they are not interested in development of an A/D-memory system. These companies are: Adams-Russell Electronics, Bipolar Integrated Technology (BIT), General Electric-Electronics Laboratory, Hewlett-Packard, Mayo Clinic, Micrel, Microwave Associates and RCA Advanced Technology Center. Each of these companies will now

be discussed briefly. Adams-Russell Electronics does analog design only, mainly MMIC devices. BIT and Micrel deal with high speed silicon devices. They were contacted to see if their silicon devices would be adequate for this project. General Electric does only design work in GaAs, and it is going to be down-scaled some next year, because GaAs does not apply to a large market. For the same reason, RCA has put their GaAs development on hold for a while to see how the industry is going to react to GaAs advances. Mayo has done research in GaAs on a direct DOD or DOE basis. However, because of their non-profit status, they do not get involved in contract projects. And, finally, Hewlett-Packard has used some GaAs devices in their instruments, mainly sample-and-holds and D/As, but they are developing some A/Ds also. However, they do not plan to market any of the state-of-the-art GaAs discrete devices used in their instruments.

3.2 Technical Overview

The development of GaAs technologies is a result of the many favorable properties that are characteristic to GaAs. The most important of these properties are high speed, wide temperature range, low parasitic capacitances, low power, and high radiation tolerances. However, with these favorable traits there are problems that need to be overcome. The major problems that are encountered are production or fabrication related, such as count density and yield. Another problem is the lack of uniformity between similar transistors. Also, at these speeds communication between and within

chips becomes a large consideration. The following paragraphs will discuss these favorable traits and problems in an evaluation of the current state of the GaAs IC industry.

In comparing GaAs and silicon bipolar technologies for high speed devices, GaAs has several advantages. All the development that has been done with silicon has allowed it to achieve speeds of 100 – 200 MHz for digitally related circuits, memories, gate arrays and A/Ds. This corresponds to propagation delays as low as 5 ns for some ECL memories and gate arrays and conversion times of 10 – 15 ns with bipolar A/Ds. These speeds were attained mainly by reducing the voltage swing of the transistors which then allow the gate widths to be reduced. However, a limit is being approached for the voltage swings not to be affected by noise and other problems. One of the other major problems silicon has is the effect of radiation on its performance. Radiation hardening can be done by special designing of the system that will keep it from latching up when exposed to radiation. Unfortunately, these methods to stop latch up involve limiting carrier movement, and this slows the device. These are the main reasons why development of GaAs has gotten a resurgence.

Some of the reasons for GaAs higher speeds are larger mean free path, near zero momentum crystal–lattice structure and low density free electrons. The mean free path of GaAs is about 1000 Angstroms compared to silicon's of about 100 Angstroms. The advantage of this is that the size of transistors is nearing .1 μm = 1000 Å, and as the transistors approach the mean free path of a compound, the speeds increase because there are fewer carrier collisions. Another reason is due to the characteristics of its

conduction band. In GaAs the minimum velocity point of the conduction band is near the zero–point of the crystal–lattice momentum, so electrons will jump into the conduction at very low velocities [4]. However, for silicon the zero–point of the crystal–lattice is near the maximum velocity point of the conduction band, so very high velocities are required to make the jump. A third characteristic of GaAs, closely related to this, is that the effective mass of its free electrons is only about seven percent that of silicon. Therefore, much less energy is needed to produce the momentum for the electron to jump into the conduction band.

The structure of GaAs also gives it a property of semi–insulating, rather than semi–conducting. This semi–insulating property greatly reduces the parasitic capacitance of the transistor's substrate. Also, it allows for devices to be placed close together on a wafer without any insulating process during fabrication. Other GaAs advantages due to its semi–insulating nature are an increased normal operating temperature range of – 200 $^{\circ}$C to 200 $^{\circ}$C with possibilities of reaching 300 $^{\circ}$C or 400 $^{\circ}$C, and its radiation hardness is typically 10^7 to 10^8 RADs. All of these advantages make GaAs a very good choice for military and space applications.

As mentioned at the beginning of the paper, GaAs has been applied to several different transistor technologies which include E/D–MESFET, HEMT (or MODFET or SDHT), and HBT. Now each of these technologies will be discussed in more detail. The first GaAs devices were made in D–MESFET, mainly because they could be fabricated with much the same process as silicon. D–MESFET fabrication was done by implanting ions directly into a GaAs semi–insulating substrate. The substrate then provides electrical

insulation between devices. Gate widths of approximately one micrometer give D–MESFETs a large voltage swing, which allows good control of pinch–off voltages. Also, a thick channel region makes low source–gate resistances. The combination of these properties gives D–MESFET high speed performance (switching times $\approx$ 50 picoseconds) and large noise margins. However, the threshold voltages are negative, and level shifting is required between transistors. This level shifting circuitry causes D–MESFET circuits to have a higher power dissipation.

E–MESFET is another planar (or horizontal) technology like D–MESFET, but it uses a single power supply and makes simpler logic gates without the need of level shifting, so it requires less power. This is accomplished by having an extremely thin lightly doped channel. However, this thin channel has a smaller voltage swing, so the transistor does not have as much noise immunity. Other difficulties which arise from this type channel is that the transistor is harder to control and is highly resistive. Also, the channel is extremely surface sensitive. Due to these problem areas, E–MESFET requires much more precision and control in fabricating. One of the most severe problems in fabrication of E–MESFETs is to reduce the channel resistance. One method of doing this is to use a self–aligned gate fabrication method similar to that used for NMOS. Another solution is to use a recessed gate method. By placing the gate below the channel surface, it reduces resistivity, and the threshold voltage becomes a function of the gate depth. Also, this reduces the surface sensitivity of the channel–region.

Currently, much of GaAs work is being done in E/D–MESFET, which combines both E–MESFET and D–MESFET technologies. E/D–MESFET takes advantage of D–MESFET's large voltage swing and higher noise margin, but with the incorporation of E–MESFET's simpler logic gate design and lower power. However, E/D–MESFET is more difficult to fabricate, although with current fabrication process improvements, E/D–MESFET circuits are reaching LSI levels with yields greater than 90%. D–, E–, and E/D–MESFET technologies have many similarities to existing silicon processes, so many of the silicon breakthroughs that are being made can be adapted to GaAs.

However, all of the planar processes above still encounter surface scattering of electrons, which slows response times. Also, the widths of transistor gates are controlled and improved by making a cleaner and higher resolution photolithography process. These horizontal dimensions cannot be controlled as accurately as vertical dimensions. The HEMT technology is still limited by horizontal dimensions, but it does get around the problem of surface scattering by burying its channel in the substrate [21]. But most of its speed advantage is because this buried channel is pure GaAs. Doping GaAs reduces its electron mobility because the donors share space with the electrons and cause electron–scattering. Switching speeds near 10 ps have been achieved at room temperatures. HEMT also has the advantages of lower power consumption and potentially simple fabrication methods. However, it may not have as much radiation hardness as MESFET, because radiation generates charge in AlGaAs [17].

A technology that also eliminates the gate width problem is HBT, because it is a vertical technology. A vertical technology is one in which its critical parameters are adjusted by vertical dimensions, like the thickness of the base region which controls the transistor's gain. These heterojunction bipolar transistors are formed by initially placing an extremely thin layer of AlGaAs on the GaAs substrate, so there has to be some way to separate the transistors; usually ion implantation is used. Due to the large bandgap of AlGaAs and GaAs, it can have high base doping without losing any current gain. This way a very thin base region can be used to give a high gain bandwidth. The threshold voltage of HBT is also determined by these bandgaps, rather than being a process parameter like the channel doping and/or gate widths and thicknesses. Proposed switching speeds of HBT are near 1 ps, although they have not yet been reached. However, GaAs HBT will suffer from charge–storage effects when operating in current saturation, just as it does in silicon. There has not been as much work done with HBT until the last few years, because fabrication processes were being developed and improved. Molecular Beam Epitaxy is often used to place the thin layers of AlGaAs. Ion implantation and photo lithography are also used, but not with the resolution needed in HEMT or MESFET.

Both HEMT and HBT technologies make use of super–lattice structures. A super–lattice is a structure formed by depositing alternating layers of different group III and V compound semiconductors (or insulators). In this case these compounds are GaAs and AlGaAs. These layers are from 10 to 100 Angstroms thick, which is only a few times larger than a unit cell and thus higher electron mobilities. The performance of these

super–lattices depends on the ability to place uniform layers of these materials a few atoms thick. Two methods used to do this are Molecular Beam Epitaxy (MBE) and laser annealing. As these techniques are improved, they produce layers which are more uniform in thickness as well as molecular orientation, thus giving higher switching speeds.

All of the before mentioned GaAs technologies show promise for highly integrated ICs, because of their high load drivability and low power dissipation properties. However, designing circuits in any technology for speeds of 500 MHz and above requires special considerations for signal propagation and communication. The propagation of signals through conductors can cause large delays relative to the signal period. For digital systems near 500 MHz the package needs to be less than one inch across due to I/O time delay considerations [16]. When the signals begin to go off chip, more problems arise. Multiple chip designs sharply degrade performance of high speed devices, so the partitioning of functions across chip boundaries must be done very carefully. Another consideration in high speed device design is that these speeds have been reached by reducing the voltage swing on the transistors, so noise margins have also been reduced.

Another problem found with GaAs transistors is that of adjacent non–uniformity on a wafer. Recently Dr. M.S.P. Lucas worked with TRW, Redondo Beach, CA, on the development of a semi–automatic test station for the on–wafer measurement of GaAs transistor parameters. The purpose of the system was to select the lowest noise devices by making noise measurements on the wafer. The noise measurements were made at 8, 10, and 12 GHz. It was noted adjacent transistors could have quite different

characteristics. The noise measurements were repeatable on several consecutive passes. Special high frequency probes were required to test the devices [13].

Dr. D.H. Lenhert and Dr. M.S.P. Lucas have both observed that industrial vendors of analog–to–digital convertors have inadequate or non–existent production test procedures. Their experience has been that only static tests are performed, and that these tests are performed only on a sampling basis. The more important dynamic tests are usually ignored. For the A/D–memory system desired, testing would require extremely high speed and quality systems to produce reliable signals on which tests could be run and monitored.

4.0 CONCLUSION AND RECOMMENDATIONS

The A/D systems discussed in this thesis represent implementations of the many technical advances that have been reached in the area of micro–electronics. The manner in which this technology is applied to any problem can vary widely depending on the specifications and environment of that particular problem. The specification of interest in the discussion for first project is time. In particular, the indifference of a time skew between channels of the array in the design of the 32–channel 12–bit A/D system. In the A/D–memory system the requirement of space qualification of such a high speed device made the use of gallium arsenide a near necessity. Also the type of A/D architecture used for the A/D–memory system depends on the semiconductor technology in which the system is fabricated, because some semiconductor technologies inherently implement particular architectures with more ease.

A wire–wrapped version of the 32–channel 12–bit A/D system was built and tested to perform as designed and is being used at Sandia National Laboratories in the prototyping of a larger system. It is the authors recommendation that the control circuitry in the 4CT&H be replaced with a programmable logic array (PLA). This idea was initiated at Kansas State University but time requirements at Sandia did not allow its completion. The 500 MHz A/D–memory system is being looked at further at Kansas State University to find methods by which it could be tested and evaluated at some future date if and/or when such a device is produced.

Appendix A. List of Companies Contacted

1.	Adams–Russell Electronics 80 Cambridge St. Burlington, MA 01803	Michael Smith (617) 273–3333
2.	A T & T Bell Laboratories 2525 N. 12th Redding, PA 19612	Howard Kirsh (215) 939–6984
3.	Anadigics 35 Technology Dr. Warren, NJ 07060	Michael Gagnon (201) 668–5000
4.	Bipolar Integrated Technology 1050 N.W. Compton Dr. Beaverton, OR 97006	Bruce Miller (503) 629–5490
5.	Ford Micro Electronics 10340 State Highway 83 North Colorado Springs, CO 80908–3698	Rich Griffith (303) 528–7868
6.	Gain Electronics 22 Chub Way Summerville, NJ 08876	Mike Logan (201) 526–7111
7.	G.E. – Electronic Laboratory P.O. Box 4840–EP3 Syracuse, NY 13221	Mosshi Namordi (315) 456–2491
8.	Gigabit Logic 1908 Oak Terrace Lane Newbury Park, CA 91320	Mike Pawaik (805) 499–0610
9.	Harris Microwave 1530 McCarthy Boulevard Milpitus, CA 95035	Kim Thomas (408) 433–2222

10.	Hewlett Packard Building 28C 1651 Page Mill Rd. Palo Alto, CA 94304	John Corcoran (415) 857–3178
11.	Honeywell – Physical Science Center 10701 Lyndale Ave. 5 Bloomington, MN 55420	Wayne Walters (612) 887–4090
12.	Hughes Research Lab MS–RL61 3011 Malibu Canyon Rd. Malibu, CA 90265	Paul Greiling (213) 456–6411
13.	ITT GaAs Technology Center 7670 Enon Drive Roanoke, VA 24019–1088	Edward Griffin (703) 563–8600
14.	Mayo Clinic Medical Sciences Building 201 Street S.W. Rochester, MN 55905	Barry Gilbert (507) 284–4056
15.	McDonnell–Douglas 5301 Bolsa Ave. Huntington Beach, CA 92647	Rainer Zuleeg (714) 896–1937
16.	Micrel 1235 Midas Way Sunnyvale, CA 94086	Ray Zinn (408) 245–2500
17.	Microwave Associates (M/A COM) 100 Chelmsford St. Lowell, MA 01851	Ron Cavalari (617) 937–2800
18.	Microwave Semiconductors 100 School House Rd. Somerset, NJ 08873	Jim Dilorenzo (201) 563–6210
19.	Pacific Monolithics 245 Santa Ana Court Sunnyvale, CA 94086	Alan Podell (408) 732–8000

20.	RCA Advanced Technology Center Mail Station 145–3 Moorestown, NJ 08057	Jerry Richards (609) 866–6514
21.	Rockwell International Mail Code: BD08 3370 Niraloma Ave. Anaheim, CA 92803	Jim Donovan (714) 762–1686
22.	TRW 1 Space Park Dr. M5–1464 Redondo Beach, CA 90278	Ken de Graaf (213) 535–1912
23.	TI – Central Research P.O. Box 655936 Mail Station 134 Dallas, TX 75265	Bill Wisseman (214) 995–2451
24.	TI Defense Systems and Electronics P.O. Box 660246 Dallas, TX 75266	Larry Housey (214) 995–7828
25.	Tri Quint Semiconductors Group 700, P.O. Box 4935 Beaverton, OR 97076	Tom Reeder (503) 629–3100
26.	Vitesse Electronics 741 Calle Plano Camarillo, CA 93010	Tom Ducan (805) 388–3700

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ANALOG TO DIGITAL CONVERTOR STUDIES

by

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BSEE, Kansas State University, 1986

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ABSTRACT

This paper contains the discussion of two high speed A/D systems. The first discussion is about the design of a 32-channel 12-bit A/D board. The discussion contains the possible system approaches, then details the design of the system that was chosen. The system designed multiplexed the 32 analog inputs into a single S&H and A/D to minimize chip count, board space, power requirements, and errors due to inconsistencies between like devices. The second section is an investigation to find a source for a 500 MHz 8-bit A/D with a 16K x 8 SRAM circulating memory that can continually accept the A/D's output. Each company talked to is presented on an individual basis telling its capabilities and goals. Current GaAs technologies are compared with each other and silicon for producibility and for which would be best suited for space qualified devices. A list of companies contacted and their addresses is also included.