Characterization and TCAD Modeling of Mixed-Mode Stress Induced by Impact Ionization in Scaled SiGe HBTs

Nicolò Zagni, *Student Member, IEEE*, Francesco Maria Puglisi, *Member, IEEE*, Giovanni Verzellesi, *Senior Member, IEEE*, and Paolo Pavan, *Senior Member, IEEE*

***Abstract*—We investigate the reliability of state-of-the-art SiGe HBTs in 55-nm technology under mixed-mode stress. We perform electrical characterization and implement a TCAD model calibrated on the measurement data to describe the increased base current degradation at different collector-base voltages. We introduce a simple and self-consistent simulation methodology that links the observed degradation trend to interface traps generation at the emitter/base spacer oxide ascribed to hot holes generated by impact ionization in the collector/base depletion region. This effectively circumvents the limitations of commercial TCAD tools that do not allow impact ionization to be the driving force of the degradation. The approach accounts for self-heating and electric fields distribution allowing to reproduce measurement data including the deviation from the power-law behavior.**

***Index Terms*—SiGe HBT, Impact Ionization, Reliability, Degradation, TCAD Modeling.**

I. Introduction

SILICON Germanium (SiGe) Heterojunction Bipolar Transitors (HBTs) are currently the leading technology option for amplifiers for 5G networks and THz industrial sensors [1]–[3]. In addition, they are employed for a large variety of applications in healthcare, material science, security, industrial automation, communications, and space exploration. Despite the high performance and cost effectiveness, several aspects related to the reliability of these devices need to be addressed to further improve the technology and its pervasiveness [1]. Since HBTs are frequently driven close to the Safe-Operating-Area (SOA) limits, they are prone to self-heating (SH) and degradation issues. Specifically, prolonged operation leads to degradation of the low-frequency gain β due to base current increase, which is conventionally attributed to surface states generation at the emitter-base (E-B) spacer oxide due to impinging hot carriers generated by impact ionization (II) [4]–[7]. In earlier technologies such as the 0.13 μm process from IHP [4] and the first generation of the 55 nm process from STM [8], the base current degradation was reported to empirically follow a power-law. However, deviations occurred at some point in time (typically after several hours), depending on the specific stress conditions, which is thought to be related to the combined effect of SH and of II dynamics [4]. Nevertheless, in the literature the physics of this mechanism was either only partially analyzed [5], [7], or explained by empirical [4] or approximated analysis [6] that are better suited for aging compact models to be used in circuit simulations than for TCAD aging models to be exploited for degradation-aware device optimization. This calls for more comprehensive modeling efforts, especially with further device scaling.

In this paper, we perform electrical characterization of mixed-mode (MM) stress reliability of state-of-the-art scaled 2nd-generation SiGe HBT technology from STM under different collector-base stress voltages. We implement a TCAD model of the HBT device and calibrate it to reproduce the behavior of fresh devices. A self-consistent simulation methodology that considers SH and the effect of 2D electric field distribution is then introduced that allows correctly reproducing mixed-mode stress data by ascribing the degradation to hot holes generated by II at the collector/base junction that drift towards the E-B spacer oxide. The developed model gives a direct empirical connection between trap generation rate and II rate in contrast to earlier reports that either: *i*) computed the generation rate from hot carriers models [5] or from the energy distribution function of carriers [7]; or *ii*) derived an approximated analytical solution for the generated trap density with generation rates used as fitting parameters [6].

II. Devices and Experiments

The devices analyzed in this study are state-of-the-art SiGe HBTs fabricated in 55-nm BiCMOS technology by STM [9]. With respect to the 1st-generation of the technology, device dimensions have been scaled in the vertical direction (e.g., base width W_B) and doping profiles were accordingly re-defined, especially at base-collector junction. Each device is composed of two parallel HBT structures in the CBEBC configuration

This work has received funding from the European Commission's Horizon 2020 TARANTO Project, grant agreement n° 737454.

N. Zagni, F. M. Puglisi, and P. Pavan are with the Dipartimento di Ingegneria "Enzo Ferrari", Università di Modena e Reggio Emilia, 41125, Modena, Italy. (corresponding author e-mail: nicolo.zagni@unimore.it).

G. Verzellesi, is with the Dipartimento di Scienze e Metodi dell'Ingegneria (DISMI) and with EN&TECH, Università di Modena e Reggio Emilia, 42122, Reggio Emilia, Italy.

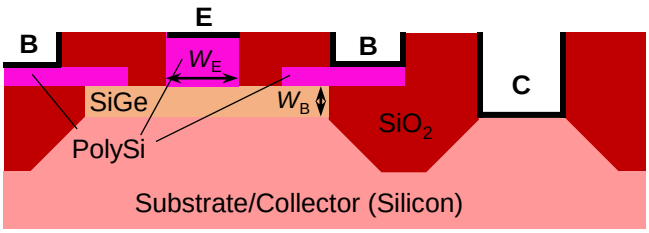

Fig. 1. Cross-section of the simulated SiGe HBT. Important device dimensions are highlighted: emitter width (W_E) and base width (W_B).

with 3 emitter fingers, with an emitter width and length of W_E = 0.20 µm and L_E = 5.56 µm (in the 3rd dimension), respectively. The Gummel curves at V_{CE} = 1.2 V and output curves at different V_{BE} values (in the range 0.75 V – 0.9 V) collected on fresh devices are shown in Fig. 2(a) and Fig. 2(b), respectively, with the latter showing the signature of a modest device self-heating only at V_{BE} = 0.9 V. The device dimensions and most relevant figures of merit are reported in Tab. I, benchmarked with IHP SG13S technology [10] (used for comparison also in the degradation analysis). To assess the reliability of the devices under study, we performed MM stress by forcing an emitter current density, $J_{E,STR}$, of 1 mA/µm^2, which corresponds to a V_{BE} of ≈0.8 V. The base terminal is kept grounded while the voltage at the collector-base junction, $V_{CB,STR}$, is set to different values ranging from 1.5 V to 2.1 V. These values are chosen as a reasonable trade-off between keeping stress conditions close to the operating ones and getting a non-negligible degradation in a reasonable amount of time, with the total stress time set to 10^4 s. Indeed, in typical circuits for high-frequency applications such as power amplifiers, V_{CB} ranges from 0 V to 1.5 V [2], whereas J_E (or equivalently J_C) varies in the range where the f_T peaks – typically tenths to tens of mA/µm^2 [1], [4]. The stress sequence was interrupted every 100 s to measure Gummel curves at V_{CE} = 1.2 V, as shown in Fig. 4(a), which allows extracting the relative increase (as compared to the fresh device) of I_B at different $V_{CB,STR}$ as an indicator of the devices reliability. I_B is evaluated at V_{BE} = 0.7 V to directly compare the results reported here with the outcomes of MM stress experiments performed on a previous technology (0.13 µm) and reported in the literature [4]. All measurements are performed at room temperature.

III. TCAD Model and Calibration

The sketch of the SiGe HBT device cross-section implemented in the simulator is shown in Fig. 1. The TCAD simulation tool is the commercial software SDevice™ by Synopsys, Inc. [11]. The device structure was derived by refining an existing model in SDevice™ for the HBT device, and the mesh was revised to optimize the trade-off among computation time, simulation accuracy, and reproducibility. Comparison of measurement data and calibrated TCAD simulations is shown in Fig. 2, in terms of Gummel plot, Fig. 2a), and output characteristics, Fig. 2b). Because the DC MM stress conditions represent an upper limit to HBT degradation under RF operating conditions, here we discuss only the calibration of the device DC characteristics. Analysis of dynamic characteristics (to estimate f_T and f_{max}, for instance) and comparison between measurements and simulations will be

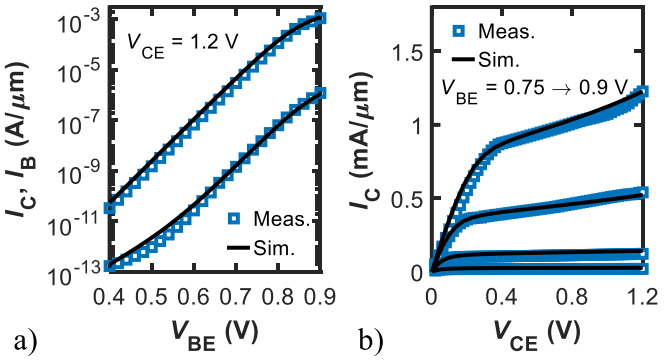

Fig. 2. Calibration of simulated (solid black lines) against measurements (blue squares) a) I_C, I_B-V_{BE} characteristics and b) a) I_C-V_{CE} characteristics.

TABLE I
Comparison of Technology Parameters and Dimensions

	STM B55 [9]	IHP SG13S [10]
A_E (µm^2)	0.2 × 5.56	0.16 × 0.52
f_T (GHz)	320	250
f_{MAX} (GHz)	370	300
BV_{CEO}, BV_{CBO} (V)	1.45, 5.2	1.7, 5.0

subject of future work.

The Ge mole fraction (x) profile in the $Si_{1-x}Ge_x$ varies from 0 to 0.28 from the emitter to the collector junction. The base width was set to 26 nm (W_B in Fig. 1). In agreement with results in the literature, the doping profile in the emitter is assumed flat, while a Gaussian doping profile is assumed in the base [1]. The doping profile in the collector/sub-collector and, in general, the overall doping profile is in agreement with that suggested by a TCAD-based roadmap for SiGe HBT devices developed in the DOTSEVEN project [1]. Hydrodynamic simulations were carried out to correctly reproduce the currents in all regimes of operation [12]. The lattice, electron, and hole temperatures are self-consistently calculated in TCAD, which accounts for the effects of self-heating. Models for carriers' recombination (and doping-dependent Shockley-Read-Hall), II (Okuto model), and field-, material-, and doping-dependent mobility [12]–[14] were also included. Calibrating such models for SiGe required only a slight tuning of few parameters in agreement with earlier literature reports [8], [14]. To consolidate the soundness of the calibration procedure, default values for Si and polysilicon were used. Series resistances and thermal resistances were also included at all contacts, and their values were calibrated to capture the behavior of the output curves in the saturation region and in the active region, respectively, as confirmed by the good agreement between experimental and simulated output curves at different V_{CE}, Fig. 2(b). Specifically, the good agreement at high V_{CE} – when SH effects start to be visible – was obtained by tuning the thermal resistance at the emitter, base, and collector contacts (which strongly depend on the structure of the overlying back-end of line). Conversely, to strengthen the dependability of the calibration procedure, the substrate thermal resistance was set in agreement with previous reports in the literature [14]–[16]. In addition, finite carriers' recombination velocity at the emitter was included [13]. Auger recombination and band-to-band tunneling were also included, as they are known to affect the excess base current at low bias. Finally, defects at the emitter-base (E-B) spacer interface

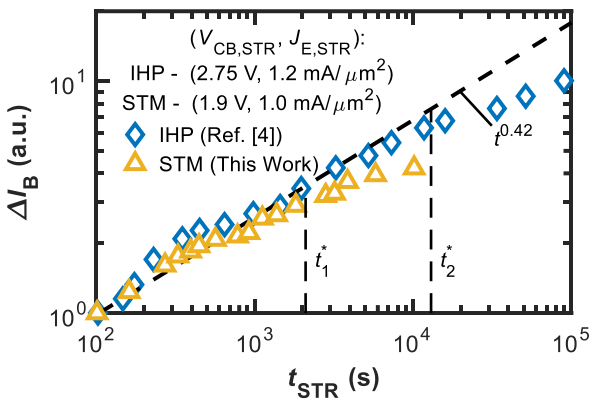

Fig. 3. ΔI_B (a.u. – normalized to ΔI_B @ 100 s) vs t_{str} (symbols) for different SiGe HBT technologies (see legend). The black dashed line follows a power-law and serves as a guide to the eye to show the deviation of data from it, which occurs at $t_1^* \approx 2 \times 10^3$ s and $t_2^* \approx 1.5 \times 10^4$ s for the STM and IHP technology, respectively. This deviation calls for a more precise modeling strategy of degradation phenomena.

TABLE II
SIMULATION PARAMETERS

Parameter	Value
Emitter Doping Peak ($N_{E,ACC}^{max}$)	1.9×10^{20} cm^{-3}
Base Doping Peak ($N_{B,DON}^{max}$)	1.0×10^{20} cm^{-3}
Collector Doping Min/Max ($N_{C,ACC}^{min/max}$)	$3\times10^{17}/1.9\times10^{20}$ cm^{-3}
Peak $Si_{1-x}Ge_x$ (x)	0.28
Interface Trap Density Peak (D_{IT})	1.0×10^{11} cm^{-2}eV^{-1}
Emitter Thermal Res. ($R_{E,TH}$)	0.2 cm^2.mK/W
Base Thermal Res. ($R_{B,TH}$)	0.05 cm^2.mK/W
Collector Thermal Res. ($R_{C,TH}$)	0.2 cm^2.mK/W
Substrate Thermal Res. ($R_{SUB,TH}$)	3.5 cm^2.mK/W†

†Taken from [14].

located at 0.5±0.035 eV from the valence band with a peak density of 10^{11} cm^{-2}eV^{-1} were included.

Note that although the simulated structure is a simplified version of the fabricated devices, a very good agreement between simulations and measurements could be achieved as shown in Fig. 2. The most relevant simulation parameters (electrical and thermal resistance at contacts, maximum doping levels) are collected in Tab. II.

IV. DEGRADATION DURING MIXED-MODE STRESS

Typically, the base current degradation resulting from MM stress in SiGe HBT devices is attributed to the generation of interface states at the E-B spacer interface [1], [4], [8], [14], [17]. The latter is supposed to stem from the carriers generated by II in the collector-base depletion region, that travel toward the E-B spacer interface under the action of the vertical field and de-passivate Si-H bonds at the Si/SiGe interface. Results reported in the literature for the 0.13 µm IHP technology [4] are consistent with this hypothesis and show that the resulting I_B degradation approximately follows a power-law ($\sim at^b$) with a slope b ≈ 0.5, although showing deviations starting from ~10 h of stress [18]. Actually, the picture is more complex, and b is found to be less than 0.5 even at low stress times (i.e., few minutes) for higher stress current densities [18]. In Fig. 3, we report a comparison of the relative trends of I_B degradation (normalized to ΔI_B @ t_{STR} = 100 s) for the IHP technology investigated in [4], [18] and the STM technology used in this work. We compare ΔI_B for the same $J_{E,STR} \approx 1$ mA/µm^2. Note

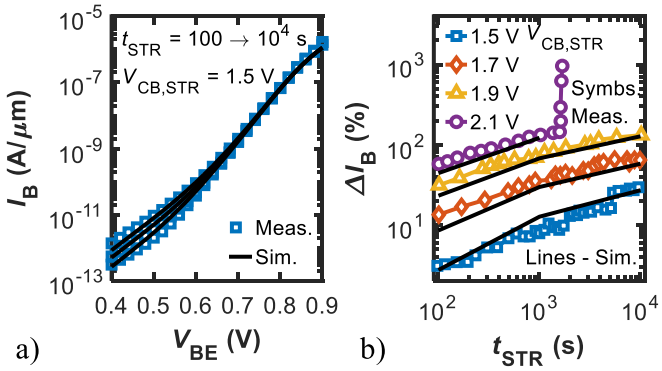

Fig. 4. Comparison between simulations and measurements of the evolution of base current with stress time (t_{str}). a) I_B-V_{BE} curve for $V_{CB,STR}$ = 1.5 V at different t_{str}. b) ΔI_B (%) vs t_{str} for different $V_{CB,STR}$ (see legend). Good agreement between simulations and measurements is obtained under all conditions.

that we have used a slightly lower exponent than 0.5 (in light of the considerations in [18]), b = 0.42 that better fits the IHP data. Interestingly, we find that STM ΔI_B data deviates from the power-law behavior at t_1^* (≈ 2×10^3 s), prior than IHP data ($t_2^* \approx 1.5\times10^4$ s), indicating an earlier onset of traps passivation mechanism.

In the following, we exploit TCAD simulations to refine our understanding of I_B degradation (and its deviation from the single power law-behavior) by linking it to the effects of device geometry and II rate, and to check whether additional mechanisms must be considered in the description of the degradation. To this extent, the calibrated simulation deck is used to reproduce measured degradation data. Analogous conditions to those used during the stress tests (described in Section II) were adopted in the simulations. The constant emitter current density ($J_{E,STR}$ = 1 mA/µm^2) was set by applying a negative voltage to the emitter contact with the base grounded. This was done for numerical reasons as this solution guaranteed convergence for all stress conditions with different $V_{CB,STR}$. Stress was simulated for $t_{STR} = 10^2$, 10^3, 10^4 s, after which the I_B-V_{BE} curves were recorded. The device aging in terms of interface traps generation (at the emitter/base access region – the SiGe/SiO_2 interface, see Fig. 1) was reproduced by adapting the reaction-diffusion (R-D) model available in SDevice™ [11]. The evolution of interface trap concentration (N_{IT}) reads:

$$\frac{dN_{IT}}{dt} = \nu(N - N_{IT}) - \gamma N_{IT} \qquad (1)$$

where ν (γ) is the de-passivation (passivation) rate. $\gamma = \gamma_0 N_H / N_H^0$ where γ_0 is obtained by imposing the equilibrium condition at $t = 0$, i.e., $\gamma_0 = \nu_0(N - N_{IT}^0)/N_{IT}^0$ (N_{IT}^0 is the concentration of defects at $t = 0$, ν_0, and γ_0 are the de-passivation/passivation constants, respectively). N_H (N_H^0) is the (equilibrium) hydrogen concentration at the interface (in the oxide). In this work we assume degradation to be mostly limited by reaction, thus $N_H/N_H^0 = 1$. The approach followed in [19], that considered similar de-passivation rates but passivation rates depending on hydrogen concentration (and thus on the diffusion rate), reached similar conclusions regarding the deviation from the single 'power-law' behavior (due to partial annealing of defects). The dependence of ν on the activation energy (E_A^0) and on the electric field is written as [11], [20]:

TABLE III
PARAMETERS USED IN THE DEGRADATION MODEL

Parameter	Value
De-Passivation Constant (ν_0)	1.0×10^{-8} s^{-1}
Passivation Temperature (T_0)	300 K
Lattice Temperature (T)	{313.8; 314.6; 316.2; 318.6} K
Activation Energy (E_A^0)	{0.8; 1.6; 2.3; 2.6} eV
Bond Concentration (N)	1.0×10^{14} cm^{-2}
Initial Trap Concentration (N_{IT}^0)	8.8×10^{9} cm^{-2}
Power Exponent Coefficient (β)	0.5
Passivation Constant (γ_0)	1.14×10^{-4} s^{-1}

$$\nu = \nu_0 \exp\left(\frac{E_A^0}{kT_0} - \frac{E_A^0 + \Delta E_A}{E_T}\right) \quad (2)$$

where $\Delta E_A = -E(\mathcal{E}_\perp) + (1+\beta)E_T \ln(N_{IT}/N_{IT}^0)$ is the change in E_A^0 due to stretching of Si-H bonds by the perpendicular electric field and by chemical potential variation (first and second term, respectively). $E_T = kT + E(\mathcal{E}_\parallel)$ is energy of hydrogen in Si-H bonds (T is the lattice temperature) that depends on the electric field parallel to the interface. However, this model as is cannot be successfully used to verify the role of II in the degradation dynamics since the de-passivation rate does not depend directly on the hot carrier current, see Eq. (2). This comes from the fact that ν does not depend on the excess carrier generation due to II. Thus, for reproducing the measurements in Fig. 4 we varied E_A^0 (see Tab. III) to equivalently take into account the effect of increased $V_{CB,STR}$ in the R-D model. This allowed to self-consistently consider the effect of lattice temperature and both parallel and vertical electric field on the degradation process. It is important to observe that E_A^0 is varied only to mimic the ν variation with $V_{CB,STR}$ in the simulator without altering the model implementation itself (as done for example in [5]). The actual physical mechanism that causes ν variation is in fact II, and not a change in E_A^0. The set of parameters that allows reproducing the measured data is reported in Tab. III. Specifically, the lattice temperature at different stress conditions was directly extracted from the TCAD by averaging the temperature profile along the E-B spacer interface. The resulting N_{IT} vs t_{STR} profile under the four different stress conditions obtained from these simulations are reported as symbols in Fig. 5a).

The connection between ν and hot carriers (generated by II) is then estimated by re-writing the de-passivation rate change at each $V_{CB,STR}$ in terms of an empirical factor k_{HC} as follows:

$$\nu = \nu_0 k_{HC}. \quad (3)$$

k_{HC} in Eq. (3) can be assumed to be a power-law function of hot carrier current [11] or II rate α_n as follows:

$$k_{HC} = 1 + \delta_{HC}(\alpha_n/\alpha_0)^{\rho_{HC}} \quad (4)$$

where δ_{HC} and ρ_{HC} are fitting parameters ($\alpha_0 = 1\ \mathrm{cm}^{-1}$ is a normalization factor). To verify the validity of the proposed model and to determine the fitting parameters δ_{HC} and ρ_{HC} we evaluated the relation between ν/ν_0 and the II coefficient α_n as obtained from simulations. This is shown in Fig. 5b), where the power-law trend is evidenced. The resulting fitting parameters are also shown in Fig. 5b). Moreover, we compared the N_{IT} vs t_{STR} profiles obtained by using Eqs. (1), (2) by varying E_A^0 [symbols in Fig. 5a)] with the ones obtained by using Eqs. (1), (3), (4) [black solid lines in Fig. 5a)] obtaining an excellent

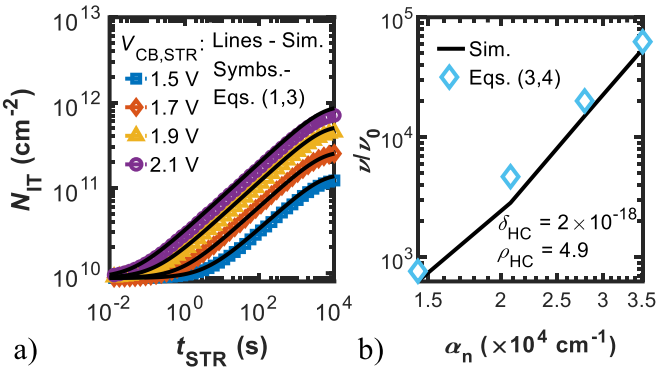

Fig. 5. a) Comparison of simulated (black lines) and calculated (colored symbols) N_{IT} vs t_{STR} for different $V_{CB,STR}$ (see legend). The calculation is achieved by combination of Eqs. (1),(3). Panel b) shows the comparison between simulated ν/ν_0 vs α_n (II coefficient) and ν/ν_0 obtained from Eqs. (3),(4). The comparison shows how to effectively translate N_{IT} degradation as obtained from simulations with Eqs. (1),(3) [panel a)] to II coefficient variation by fitting simulation data inserting the power-law model of Eq. (4) in Eq. (3).

agreement. Note that, while α_n accounts for the likelihood of hot holes generation, the parameter α_0 could be used to account for the probability of the generated hot holes to recombine or scatter while drifting toward the E-B spacer interface, which determines the generation rate of interface states. Therefore, in principle, α_0 could be taken to be dependent on $J_{E,STR}$, which regulates the scattering chance. Still, analyzing this dependence is out of the scope of this paper and will be addressed in future works.

As shown in Fig. 4, the model allows reproducing the base current degradation at different stress times and conditions. The experimental and simulated I_B-V_{BE} curves at $V_{CB,STR}$ = 1.5 V for different t_{STR} in Fig. 4a) show excellent agreement. Fig. 4b) shows the experimental and simulated relative I_B variation ($\Delta I_B = (I_B^{t_{str}} - I_B^0)/I_B^0$) at a fixed V_{BE} = 0.7 V (conventionally used to estimate the device lifetime [17]) for the four $V_{CB,STR}$ [see legend in Fig. 4b)] under investigation in this work. Notably, also the curvature of the degradation trend in Fig. 4b) is well captured (i.e., the deviation from the power-law approximation). The sudden base current increase occurring for $V_{CB,STR}$ = 2.1 V at $t_{STR} \approx$ 2000 s is likely due to collector-base junction breakdown (as confirmed by the concurrent collector current increase, not shown for brevity). This behavior could not be captured with simulations possibly due to the simplified simulated structure (see Fig. 1) that could lead to an underestimation of electric field peaks possibly present in the real device. However, since the goal in this work was to capture the base current degradation due to EB spacer interface trap generation (that does not cause breakdown) the validity of the present analysis is not affected by this discrepancy.

The overall good agreement between measurements and simulations confirms the validity of the proposed approach and highlights that:

1. Even in scaled devices, the main source of MM stress degradation is the generation of hot holes due to II drifting towards the E-B spacer interface where de-passivation of Si-H bond may happen.
2. In scaled devices, the power-law approximation of the base current degradation leads to strong deviations from the actual trend even at fairly short stress times

(≈ 2000 s).

V. Conclusion

We investigated the reliability of state-of-the-art SiGe HBTs in 55-nm technology under MM stress. Experimental results were successfully reproduced by using a TCAD model calibrated on fresh devices. We developed a self-consistent simulation methodology that connects the observed degradation trend to interface traps generation (ascribed to II-generated hot holes) at the E-B spacer oxide. This approach circumvents the limitations of commercial TCAD tools that do not allow II to be the driving force of the degradation. In addition, it: *i*) accounts for self-heating and electric fields distribution; *ii)* directly links the II coefficient (α_n) to the generation of traps; and *iii*) allows reproducing measurement data including the deviation from the power-law behavior observed at relatively short stress times.

References

[1] M. Schroter, T. Rosenbaum, P. Chevalier, B. Heinemann, S. P. Voinigescu, E. Preisler, J. Bock, and A. Mukherjee, "SiGe HBT technology: Future trends and TCAD-based roadmap," *Proc. IEEE*, vol. 105, no. 6, pp. 1068–1086, Jun. 2017. DOI: 10.1109/JPROC.2015.2500024.

[2] B. Heinemann, R. Barth, D. Bolze, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, M. Lisker, S. Marschmeyer, H. Rücker, D. Schmidt, J. Schmidt, M. A. Schubert, B. Tillack, C. Wipf, D. Wolansky, and Y. Yamamoto, "SiGe HBT technology with fT/fmax of 300GHz/500GHz and 2.0 ps CML gate delay," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2010. DOI: 10.1109/IEDM.2010.5703452.

[3] P. Chevalier, T. F. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, and A. Chantre, "Towards THz SiGe HBTs," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2011, pp. 57–65. DOI: 10.1109/BCTM.2011.6082749.

[4] G. G. Fischer and G. Sasso, "Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions," *Microelectron. Reliab.*, vol. 55, no. 3–4, pp. 498–507, 2015. DOI: 10.1016/j.microrel.2014.12.014.

[5] K. A. Moen, P. S. Chakraborty, U. S. Raghunathan, J. D. Cressler, and H. Yasuda, "Predictive physics-based TCAD modeling of the mixed-mode degradation mechanism in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 2895–2901, 2012. DOI: 10.1109/TED.2012.2210898.

[6] C. Mukherjee, T. Jacquet, G. G. Fischer, T. Zimmer, and C. Maneux, "Hot-Carrier Degradation in SiGe HBTs: A Physical and Versatile Aging Compact Model," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 4861–4867, Dec. 2017. DOI: 10.1109/TED.2017.2766457.

[7] H. Kamrani, D. Jabs, V. D'Alessandro, N. Rinaldi, T. Jacquet, C. Maneux, T. Zimmer, K. Aufinger, and C. Jungemann, "Microscopic hot-carrier degradation modeling of SiGe HBTs under stress conditions close to the SOA limit," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 923–929, Mar. 2017. DOI: 10.1109/TED.2017.2653197.

[8] F. M. Puglisi, L. Larcher, and P. Pavan, "Mixed-Mode Stress in Silicon-Germanium Heterostructure Bipolar Transistors: Insights from Experiments and Simulations," *IEEE Trans. Device Mater. Reliab.*, vol. 19, no. 2, pp. 275–282, 2019. DOI: 10.1109/TDMR.2019.2912853.

[9] A. Gauthier, J. Borrel, P. Chevalier, G. Avenier, A. Montagne, M. Juhel, R. Duru, L. R. Clement, C. Borowiak, M. Buczko, and C. Gaquiere, "450 GHz f-T SiGe:C HBT Featuring an Implanted Collector in a 55-nm CMOS Node," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium, BCICTS 2018*, Nov. 2018, pp. 72–75. DOI: 10.1109/BCICTS.2018.8551057.

[10] H. Rücker, B. Heinemann, W. Winkler, R. Barth, J. Borngräber, J. Drews, G. G. Fischer, A. Fox, T. Grabolla, U. Haak, D. Knoll, F. Korndörfer, A. Mai, S. Marschmeyer, P. Schley, D. Schmidt, J. Schmidt, M. A. Schubert, K. Schulz, B. Tillack, D. Wolansky, and Y. Yamamoto, "A 0.13 µm SiGe BiCMOS technology featuring fT/fmax of 240/330 GHz and gate delays below 3 ps," in *IEEE Journal of Solid-State Circuits*, Sep. 2010, vol. 45, no. 9, pp. 1678–1686. DOI: 10.1109/JSSC.2010.2051475.

[11] Synopsys, "Sentaurus SDevice Manual (O-2018.06)." 2018.

[12] G. Wedel and M. Schröter, "Hydrodynamic simulations for advanced SiGe HBTs," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2010, pp. 237–244. DOI: 10.1109/BIPOL.2010.5667955.

[13] Z. Yu, R. W. Dutton, and B. Ricco, "A Comprehensive Analytical and Numerical Model of Polysilicon Emitter Contacts in Bipolar Transistors," *IEEE Trans. Electron Devices*, vol. 31, no. 6, pp. 773–784, 1984. DOI: 10.1109/T-ED.1984.21606.

[14] V.-T. Vu, "Exploration and evaluation of a novel Si/SiGe heterojunction bipolar transistor architecture for next BiCMOS generation," 2016. [Online]. Available: https://www.theses.fr/2016BORD0304.pdf.

[15] S. Balanethiram, R. D'Esposito, A. Chakravorty, S. Fregonese, and T. Zimmer, "Extraction of BEOL Contributions for Thermal Resistance in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1380–1384, Mar. 2017. DOI: 10.1109/TED.2016.2645615.

[16] S. Balanethiram, R. D'Esposito, S. Fregonese, T. Zimmer, J. Berkner, and D. Celi, "Extracting the temperature dependence of thermal resistance from temperature-controlled DC measurements of sige HBTs," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Nov. 2017, vol. 2017-October, pp. 94–97. DOI: 10.1109/BCTM.2017.8112919.

[17] P. Cheng, C. M. Grens, A. Appaswamy, P. S. Chakraborty, and J. D. Cressler, "Modeling mixed-mode DC and RF stress in SiGe HBT power amplifiers," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2008, pp. 133–136. DOI: 10.1109/BIPOL.2008.4662730.

[18] G. G. Fischer, "Analysis and modeling of the long-term ageing rate of SiGe HBTs under mixed-mode stress," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Nov. 2016, vol. 2016, pp. 106–109. DOI: 10.1109/BCTM.2016.7738958.

[19] M. Couret, M. Jaoul, F. Marc, C. Mukherjee, D. Céli, T. Zimmer, and C. Maneux, "Scalable compact modeling of trap generation near the EB spacer oxide interface in SiGe HBTs," *Solid. State. Electron.*, vol. 169, p. 107819, Jul. 2020. DOI: 10.1016/j.sse.2020.107819.

[20] O. Penzin, A. Haggag, W. McMahon, E. Lyumkis, and K. Hess, "MOSFET degradation kinetics and its simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1445–1450, 2003. DOI: 10.1109/TED.2003.813333.