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PHYSICS-BASED COMPACT MODEL OF HEMTs FOR CIRCUIT SIMULATION

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Department of Electronic, Electrical and Automation Engineering

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Statement of Supervision

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I state that the present study, entitled "Physics-Based Compact Modeling of HEMTs for Circuit Simulation ", presented by Fetene M. Yigletu for the degree of Doctor has been carried out under my supervision at the Department of Electronic, Electrical and Automation Engineering of this university and that it fulfils all the requirements to be eligibile for the European Doctorate.

Tarragona (Spain), July 4th, 2014

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Declaration

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I state that the dissertation is my original work and that I have not received outside assistance. Only the sources sited have been used in this draft. Parts that are direct quotes or paraphrases are identified as such.

Tarragona (Spain), July 4th, 2014

Fetene Mulugeta Yigletu,

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Above all let *The Holy Trinity* and *Virgin Mary* be praised season in and out.

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Nomenclature

Symbol	*Description*
q	*Charge of an electron*
$\hbar$	*Reduced Planck's constant*
m_l	*Longitudinal effective mass*
D	*Two-dimensional density of states*
E_n	*Quantized energy of the* n^{th} *sub-band*
F	*Electric field*
eV	*Electron volt*
ϵ	*Dielectric permittivity*
N_A	*Ionized acceptors density*
E_C	*Conduction band energy*
E_V	*Valence band energy*
E_{f0}	*Fermi-level position in neutral state*
E_f	*Fermi-level position in non-equilibrium state*
δ_1	*Conduction band and Fermi-level difference*
δ_1	*Conduction band and Fermi-level difference*
ΔE_C	*Conduction band discontinuity*
d_1	*Depletion region in the small band-gap semiconductor*
d_2	*Depletion region in the large band-gap semiconductor*
d_s	*Spacer layer width*
d	*Thickness of barrier layer*
V_{20}	*Conduction band bending in neutral state*
V_2	*Conduction band bending in non-equilibrium state*
ϕ_M	*Metal Schottky-barrier height*
V_g	*Applied gate voltage*
V_d	*Applied drain voltage*

Symbol	*Description*
V_s	*Applied source voltage*
V_{sat}	*Saturation voltage*
E_0	*First sub-band energy level*
E_1	*Second sub-band energy level*
V_{th}	*Thermal Voltage*
n_s	*Sheet carrier concentration in the 2DEG*
μ_0	*Low-field mobility*
μ	*Saturation mobility*
V_{off}	*Cut-off voltage*
W	*Device width*
L	*Device length*
λ	*Channel length modulation parameter*
SCE	*Short channel effect parameter*
R_{TH}	*Thermal resistance*
I_{ds}	*Drain-source current*
Q_g	*Total gate charge*
C_g	*Gate capacitance*
l_2	*Virtual gate length*
λ_0	*Characteristics length of saturation region*
V_{VG}	*Virtual gate voltage*
JFM	*Johnson's figure of merit*
KFM	*Keyes' figure of merit*
BFOM	Baliga's figure of meri

List of Contributions

F. Yigletu and B. Iñiguez, "A model for the current collapse effect in AlGaN/GaN HEMTs suitable for circuit simulations," Revised version submitted to *IEEE Transactions on Electron Devices.*

F. Yigletu, B. Iñiguez, S. Khandelwal, and T. Fjeldly, "Compact Charge-Based Physical Models for Current and Capacitances in AlGaN/GaN HEMTs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 11, pp. 268-271, Nov 2013.

F. Yigletu, B. Iñiguez, S. Khandelwal, and T. Fjeldly, "Compact physical models for gate charge and gate capacitances of AlGaN/GaN HEMTs," in Simulation of Semiconductor Processes and Devices (SISPAD), 2013 IEEE, Sep 2013, pp. 268-271, Glasgow, UK.

S. Khandelwal, **F. Yigletu**, B. Iñiguez, and T. Fjeldly, "A charge-based capacitance model for AlGaAs/GaAs HEMTs," *Solid-State Electron.*, vol. 82, pp. 38-40, Feb 2013.

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F. Yigletu, R. Ritzenthaler, and B. Iñiguez, "A small signal HEMT model including current collapse for microwave simulations," in European Solid-State Device Conference (ESSDERC), 2011 IEEE, Sep 2011, Helsinki, Finland.

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Contents

Chapter 1

Introduction

III-V compound semiconductor based devices are one of the pillars of the semiconductor electronics industry. FET devices based on the hetero-junction at the interface of III-V compound material systems have showed superior performance, specially in high frequency and power electronics applications, as compared to their silicon counterpart owing to their desirable material properties such as wide band-gap, high breakdown voltage and high electron mobility. After showing excellent performance in RF and power applications, they have received a considerable attention and their use and development have been in progress for the last four and half decades. Today, III-V hetero-junction based devices are ubiquitous components in most communication systems, high frequency and high power applications and a lot more.

Compact modeling of III-V devices has also been equally important in the field of circuit design and simulation to realize Integrated Circuits (IC). Device modeling for circuit simulation have come a long way improving with the improving device technology. The modeling of III-V heterostructure field effect transistors (HFETs) generally shares common aspects with the rest of FET family and it also has its own unique features to consider. The common features in the general modeling of FETs have improved considerably, in most cases, with the cost of increased complexity. The special cases of III-V modeling are obviously due to some of the unique characteristics of the constituent materials and the resulting hetero-structure system. The operating conditions and application areas can also disrupt the normal operation of the device and give rise to the need to consider these effects in the device model.

Both empirical and physics-based approaches are being used to model special device characteristics. Most of the device models in commercial circuit simulators that have empirical roots continued incorporating empirical models of additional effects. This is one of the factors that is continuously increasing complexity and number of model parameters. Physics-based modeling of special physical effects is an attractive alternative. They guarantee high accuracy and stability with a minimum set of parameters which, in most cases, possess physical significance and can easily be extracted from measurements.

Independent physics-based models that are developed for a certain physical effect exhibited by a device can be incorporated to core empirical or physics-based models. The integration in physics-based core current models is, indeed, more natural and maximizes accuracy and robustness. The integration in empirical models is also valuable and improves model performance considerably. Here, the former modeling activity, development of physics-based core as well as non-idea effect models, is exercised to come up with a set of compact models for HEMT devices.

1.1 History

At the early stages of the emergence of III-V hetero-junction based devices, various investigations and comparisons with silicon based devices in terms of important material

Table 1.1: Electrical Properties of some important semiconductor materials for power electronics application.

Material	$E_g(eV)$	ε	$\mu(cm^2/Vs)$	$E_C(MV/cm)$
Si	1.12	11.8	1350	0.3
GaAs	1.4	13.1	8500	0.4
GaN	3.4	9.5	1500	2
4H-SiC	3.26	10	720	2
6H-SiC	2.86	9.7	370	2.4

E_g : Band gap, ε : Dielectric constant, μ : Electron mobility, E_C : Critical electric field

Table 1.2: Figures of Merit for RF application normalized to Silicon

Material	JFM	KFM	$BFOM$
Si	1	1	1
GaAs	11	0.45	28
GaN	790	1.8	910
4H-SiC	410	5.1	290
6H-SiC	260	5.1	90

JFM : Johnson's figure of merit, KFM : Keyes' figure of merit, $BFOM$: Baliga figure of merit

properties were performed [1]. Such studies are of great importance in the selection of materials for different applications. Table 1.1 shows the basic semiconductor properties of silicon and some important compound semiconductor materials [2, 3]. The III-V material systems such as GaAs and GaN have got much wider band gaps and are capable of handling very high maximum electric fields. In particular, GaAs have showed very high electron mobility which indicates its suitability for high speed applications.

Silicon has continued to be the main component in many high power electronic circuits, power MOSFETs, even after III-V based devices have came into picture. This was because of its low cost production and its processing technology which was way advanced as compared to the new comers. However, through time, the processing technology of III-V based devices has also advanced considerably and they have outperformed those using silicon in RF and power applications.

Various figures of merit have been devised that can be used to evaluate the suitability of different materials for a specific application. Table 1.2 shows the list of materials and the value of some of the critical power application figures of merit, Johnson's figure of merit (JFM), Keyes' figure of merit (KFM), and Baliga's figure of merit (BFOM) [4, 5].

JFM conveys the information about power application performance and the related operating frequency of a semiconductor material [6]. It is originally formulated as a product of the semiconductor breakdown field and the maximum carrier drift velocity. KFM relates the thermal performance of a semiconductor with its high frequency performance [7]. In terms of KFM, both 4H-SiC and 6H-SiC have showed more than five times superiority over silicon. This shows the good thermal stability of SiC in high frequency and high temperature applications. GaN has also showed an almost doubled performance superiority according to this figure of merit. BFOM, calculated using the low field mobility, the dielectric constant and the band gap of the material, is an important figure of merit for high power application [8]. It was derived with an assumption that in low frequency operation of a device the power loss is related to the on state resistance of the material. It does not take into account switching loses related to high frequency operation. Thus, for high frequency and high power performance evaluation switching loses due to the charging and discharging of the input capacitance should be considered. The modified BFOM that takes into account the operating frequency, Beliga's high frequency figure of merit (BHFFOM), can be used for such evaluation. GaN has a very high normalized BFOM, with that of silicon, which shows that it is one of the best materials for high power application.

Some GaAs FETs were in the forefront when the use of III-V hetero-junction devices has blossomed. In the last few years, however, GaN based power FETs have been given a considerable attention. They are one of the best candidates for high power and high frequency applications [9, 10, 11, 12, 13, 14]. Since the late 1990s and early 2000s, GaN

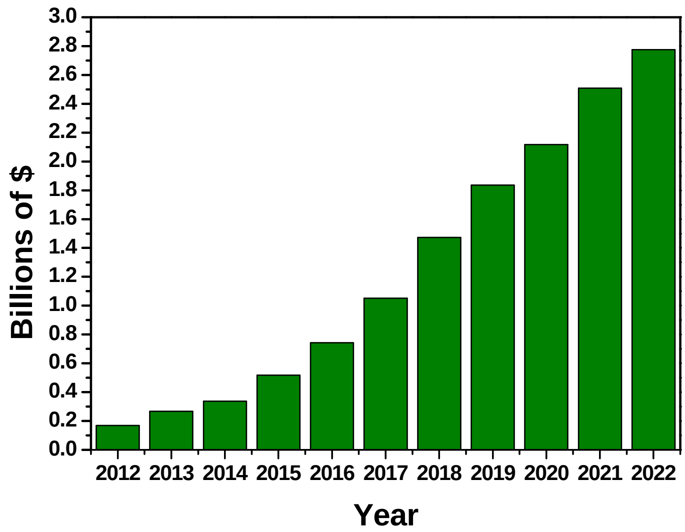

Figure 1.1.1: Market forecast for GaN and SiC based power devices. Source: I-Micronews

technology and development have progressed a lot. One reason for this progress was that it became possible to make high quality 4H-SiC reproducibly that can be used as substrates [15]. Most of the early progresses in GaN FET fabrication were made on sapphire substrates due to its availability and the high quality epitaxial layer that can be grown on it [16, 17, 18]. However, due to their poor thermal conductivity property, sapphire substrates could not be used to fabricate GaN transistors for high power applications. Then, silicon and SiC substrates have emerged as better alternatives for power applications. The high thermal conductivity of SiC allows the high power densities to be dissipated efficiently and avoids the high channel temperature that would result due to self-heating. State of the art power levels of GaN FETs were achieved using SiC substrates, $800W$ at $2.9GHz$ and $500W$ at $3.5GHz$ [19]. Silicon substrates also provide a good alternative specifically for low cost and large wafer diameter production. This can boost the availability of GaN on Si devices with competitive price in the market. This, however, could not be achieved easily because of the difficulties to grow GaN epitaxial layers on Si substrates due to the large lattice mismatch between the two materials. In

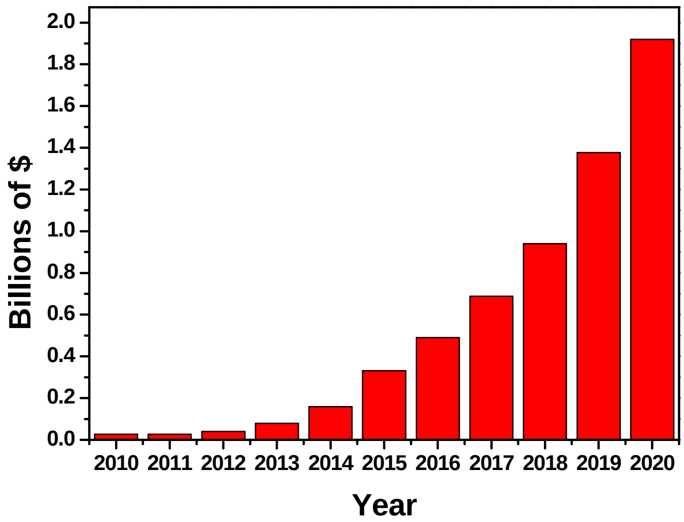

Figure 1.1.2: Market forecast for GaN and SiC based power devices. Source: IHS IMS research

addition, even if Si substrates have better thermal conductivity compared to Sapphire substrates, it is still not as good as SiC substrates. This sets a limit on the high power application of GaN on Si devices.

In spite of the existing issues yet to be solved, powered by the continuous improvement in epitaxial growth technology of GaN on Si and expected future improvements, some vendors are making moves for the mass production of GaN on Si devices for high power application. GaN on Sapphire is the main stream for LED applications. However, GaN on Si devices are expected to dominate the high power applications. High performance semiconductor manufacturers such as M/A-COM and GaN Systems have already started to make commercial GaN on Si power devices. Fig. 1.1.1 shows the market forecast for SiC and GaN power devices in total and Fig. 1.1.2 shows only that of GaN in the coming few years.

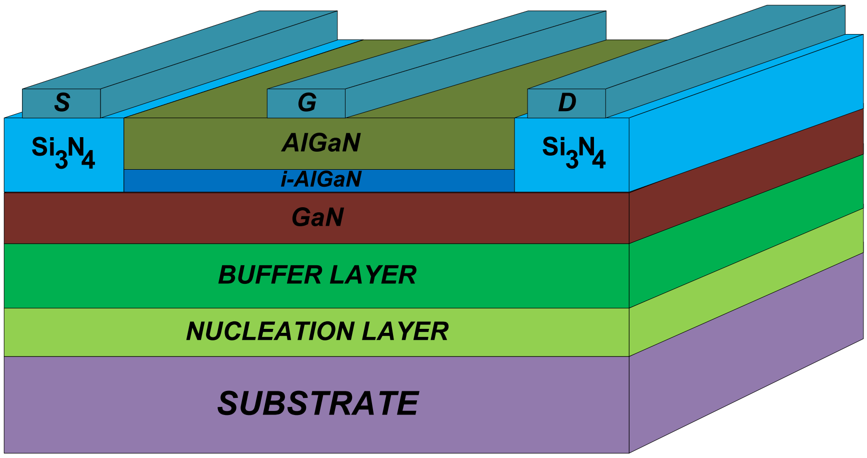

Figure 1.2.1: A source/drain recessed HEMT device structure.

1.2 Device State of the Art

A typical AlGaN/GaN high electron mobility transistor (HEMT) device structure, source-drain recessed structure, is shown in Fig. 1.2.1. Basically, HEMT structures are formed using two materials with different band gaps, in this case using AlGaN and GaN. The hetero-structure interface and the conduction band bending created when the two materials come in contact with each other is the key point of the principle of operation of such devices. This creates a potential well where free electrons from the wide band gap material (AlGaN) can be confined and form the so called *two dimensional electron gas* (2DEG) along the hetero-junction interface. Since these electrons are separated from the parent atoms and are confined in the potential well, they can move very fast as they do not experience any scattering from the ionized atoms as in the case of MOSFET operation. In fact, they experience coulombic scattering from the parent ionized atoms that are just at the surface of the hetero-junction [20]. This can be reduced by using a thin spacer layer, an undoped AlGaN layer. Gate, drain and source metallic schottky contacts are then formed at the top of the wide band gap material.

In AlGaN/GaN structure a 2DEG with sheet carrier concentration of more than $10^{13} cm^{-2}$ can be achieved at the hetero-junction interface without intentional doping [21, 22, 23, 24, 25, 26, 27, 28, 29]. This is well above that is achievable in other III-V material systems. This is mainly attributed to the high piezoelectric and spontaneous polarizations at the interfaces. In Wurtzite AlGaN/GaN hetero-structure the piezoelectric polarization of the strained top layer is more than five times larger than that of AlGaAs/GaAs structures [30, 31]. Moreover, it has been found that the spontaneous polarization is very high in Wurtzite group III nitride generally and specially in AlN it was found to be three to five times less than that of typical ferroelectric perovskites [32]. A very high number of electrons will be then accumulated and confined at the hetero-junction interface to compensate the polarization induced positive charge.

Surface states at the AlGaN surface are believed to be the sources of these free charge carriers [22]. In actual devices, however, the free charge carrier source could be a combination of other possible sources such as unintentional dopants, interface states at the AlGaN/GaN interface, deep-level defects. One important point to consider about the surface states being the sources of free charge carriers is the effect of surface passivation in improving device performance. Surface passivation is known to enhance device performance mainly by increasing the 2DEG concentration [33]. If it is assumed it does so by decreasing surface states, it would then be a contradiction with the assumption that the surface states are the sources of free charge carriers and thus if their concentration is decreased the 2DEG concentration should also decrease. One explanation that can probably pacify the contradiction between the two observations could be that surface passivation reduces the ionization energy of the surface states relative to the conduction band energy rather than eliminating the surface states [34].

1.3 Compact Modeling

It is a common practice to adapt some of the key features of a modeling technique used to model a previous group of devices, at least as an initial reference, whenever a new group of devices emerge that also requires to be modeled. It is obvious that the new group of devices will come with some new features that are unique to the group requiring a special treatment. The general modeling of III-V FET devices for circuit simulation is different in some aspects from that of silicon based devices. This, mainly, is due to the fundamental differences in material properties, the complex nature of the interface at the III-V hetero-junction and complex dependence of the drain current on the terminal voltages, additional effects such as frequency dispersion due to the surface traps and application areas [35]. III-V FETs have got applications in relatively high power applications such as in power amplifiers (PA). The design of these power amplifiers involves a difficult tradeoff between linearity and power added efficiency (PAE). The simulation of linearity and PAE require extensive modeling techniques. Linearity simulations require very robust and continues models capable of differentiating to higher orders. Similarly, PAE simulations require consideration of temperature effects due to power dissipation. One efficient modeling approach, therefore, would be to thoroughly consider device specific issues under a skeletal structures of previously well established modeling techniques.

Basically, there are two forms of compact device models, models for circuit simulation, table based and closed-form equation based. Table based device models, as the name indicates, are composed of set of tables that contain device measurement data. The device measurement data can be generated from 2D device simulations or from experimental measurements. Then the data can be inferred at a specific bias point when needed [36, 37, 38, 39]. This approach requires a considerable amount of measurement to be performed and a very big memory space to store it. It also requires the use of some interpolation functions for possible intermediate readings. If these interpolation algorithms are chosen to be very simple, the accuracy of the model can be affected. To make use of simpler interpolation algorithms and maintain good accuracy, the database should contain more closely spaced points requiring more memory space. Thus, memory and interpolation algorithm sophistication should be traded off [40].

The other group of compact models are closed form equation based models. They are basically sets of analytical equations that relate all the parameters of the model and express the physical relation between the terminal characteristics of the device. The model parameters are commonly extracted from measurements. Usually, procedural parameter extraction techniques are developed along with the models. The qualities of such models, in most cases, are evaluated from the point of model expressions simplicity, number of model parameters involved, ease of the parameter extraction techniques and the accuracy of the obtained results.

Physics-based compact models are closed form equation based models that are formulated based on device physics. Such models are relatively accurate as they are based on fundamental semiconductor equations such as current density and continuity equations. Since they are based on interdependent relations between physical semiconductor parameters, in their original formation these models may require iterative numerical calculations to get simulation results. This could result in fairly long simulation time. This has been one of the main reasons that kept them least ranked for circuit simulation applications. They can be used for circuit simulation applications when expressed in simplified analytical forms. It is important to make sure that accuracy of the models is sacrificed minimally while simplifying though. Moreover, in such forms they are very convenient to incorporate additional physical effects observed in different devices. There are indeed physics-based compact models for circuit simulation reported by different Authors [41, 42, 43]. However, majority of device models in commercial simulators are another forms of closed form equation based models, empirical curve fitting models.

Semi-empirical compact models available in most commercial circuit simulators are one of the essential entities in the integrated circuit designing and manufacturing industry. Such models normally go through regular and extensive revisions and improvements. Currently, there are a number of compact models in circuit simulators that can be used for general whole range device modeling as well as specialized circuit simulations. Models like EKV [44], Angelov [45], EEHEMT [46, 47], TOM3 [48] are some to mention out of many more available models. Most of these models, as mentioned earlier, are empirical, or curve fitting oriented, by their nature. However, they also incorporate considerable modifications based on device physics. In that regard they are not entirely empirical. Rather, they are semi-empirical.

1.4 Synopsis of this Thesis

In this thesis a physics-based compact modeling of HEMT, specifically AlGaN/GaN, devices for circuit simulation is presented. A complete modeling of drain current, gate charge and gate capacitances is discussed. The core drain current and gate charge models are derived using a simple charge control model derived from the solutions of Poisson's equation and Schrodinger's equation solved for the active operating area of the device. The models are simple continuous and applicable for the whole operating regime of the device. A separate model is also presented for the current collapse effect which is one of the serious issues both in the fabrication and modeling of AlGaN/GaN devices. The current collapse model is developed using the core current model as a background which resulted in a robust large signal model that can be used with and without the presence of current collapse. The models developed here are suited for circuit simulation application. They are implemented in a circuit simulator to carry out DC characteristics of AlGaN/GaN HEMT devices. The results of DC simulation carried out using the models are validated using experimental data where good agreement was found between the two. The details of model implementations and validations are also presented.

In *Chapter* 2 the development of the core charge control, drain current, gate charge and capacitance models is presented. The fundamental electrostatics analysis of the active region of the device is presented first that is used to formulate the basis of the physics-based models. The incorporation of non-ideal effects that are necessary to widen the application range of the model is discussed next. Moreover, the higher order derivatives of the model are also analyzed to investigate the continuity and stability of the model for further applications such as non-linearity studies. Model validations are then carried out through comparisons with experimental measurement data.

In *Chapter* 3 the analysis and modeling of current collapse effect that is observed during high power applications is presented. The reduction of 2DEG, and therefore the drain current, due to entrapment of charge carriers by surface states in the barrier layer is demonstrated using 2D device simulations. The compact modeling technique that is used to account for the observed phenomenon is explained. The current collapse model developed and its integration with the main drain current model are then discussed. Model implementation in a circuit simulator, the corresponding equivalent circuit model used and model validation using experimental data are then presented sequentially.

In *Chapter* 4 nonlinearity analysis and modeling of AlGaAs/GaAs pHEMT devices from RFMD is presented. The Volterra series analysis is used to perform intermodulation distortion simulations. The Volterra series coefficients are extracted using a methodology that involves linear and nonlinear harmonic measurements. All the measurements necessary for parameter extraction are described along with important issues that need to be considered during the measurements. The implementation of the nonlinear model in circuit simulators and Two-Tone intermodulation distortion simulations carried out using the model are presented. Then, the nonlinear model is verified using experimental measurement data.

Finally, a conclusion and a summary of the effort made in here to formulate complete compact models for circuit simulation of HEMT devices based on device physics is presented in *Chapter* 5. In addition, remaining modeling activities and possible future modeling paths that should be followed in order to boost the performance of the models presented here are also discussed.

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Chapter 2

Analytical Drain Current Gate Charge and Capacitances Modeling

This chapter discusses the development of physics-based compact models for the drain-source current, gate charge and gate capacitances of HEMT devices. The general electrostatic analysis of the hetero-junction region formed in III-V semiconductors is primarily presented. The main parameters that characterize this region have got a complex relationship between each other. This brings a challenge to develop simple analytical physics-based compact models. Using the inter-dependent relations between the hetero-junction main parameters and reasonable simplifying assumptions based on justified results a simple charge control model is developed first. This charge control model forms the basis for the development of analytical models of the terminal characteristics.

2.1 Carrier Concentration in the 2DEG

In the triangular approximation of the potential well if a quasi-constant electric field is assumed, the solution of the longitudinal quantized energy can be approximated as [1]

$$E_n(eV) \approx \left(\frac{\hbar^2}{2m_l}\right)^{1/3} \left(\frac{3}{2}\pi qF\right)^{2/3} \left(n + \frac{3}{4}\right)^{2/3} \tag{2.1.1}$$

where m_l is the longitudinal effective mass.

In GaAs material the first two sub-band energy levels are calculated to be

$$E_0(eV) \approx 1.83 * 10^{-6} F^{\frac{2}{3}} \quad and \quad E_1(eV) \approx 3.23 * 10^{-6} F^{\frac{2}{3}} \ . \tag{2.1.2}$$

The approximation of the energies of the sub-bands given in (2.1.2) over estimates the sub-band splitting. This is because the conduction band increases sublinearly. However, the 2/3 power relation between E_0, E_1 and F is reasonable [2]. A more accurate estimation of the band splitting can be done by improving the coefficients. This can be done by establishing a relationship between the electron sheet concentration and the interface electric field. Fig. 2.1.1 shows the band diagram of a hetero-junction consisted of an n-type large band-gap semiconductor and p-type semiconductor with a smaller band gap.

As the electric field in the smaller band gap material obeys Poisson's equation, we have [3]

$$\frac{dF_1}{dx} = -\frac{q\left[n\left(x\right) + N_{A1}\right]}{\varepsilon_1}. \tag{2.1.3}$$

The electric field is integrated within the limit of the depletion region. The boundary conditions for the electric field and the depletion width are:

⇒ F_1 from 0 at the end of the depletion region to F_{i1} at the hetero-junction interface

⇒ x from 0 at the hetero-junction interface to d_1 at the end of the depletion region

Thus, the integration of the Poisson's equation with these boundary conditions gives

$$\varepsilon_1 F_{i1} = qn_s + qN_{A1}d_1. \tag{2.1.4}$$

In most cases the smaller band gap material is doped very lightly or unintentionally doped to improve mobility of charge carriers in the region. In such cases the second term in the right side of (2.1.4) is very small. Thus, it can be written as

$$\varepsilon_1 F_{i1} = qn_s. \tag{2.1.5}$$

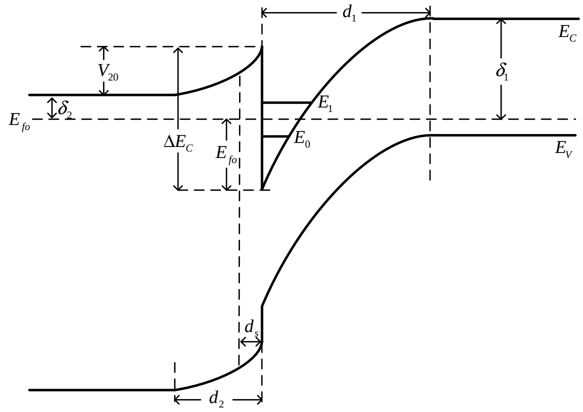

Figure 2.1.1: Band structure diagram at a hetero-junction formed by two semiconductors of different band gaps.

Equation (2.1.5) gives the approximated relationship between the electric field at the interface and the sheet carrier concentration. Substituting for the electric field from (2.1.5) into (2.1.2) gives

$$E_0 = \gamma_0 n_s^{2/3} \quad and \quad E_1 = \gamma_1 n_s^{2/3} \tag{2.1.6}$$

where

$$\gamma_0 = 1.83 * 10^{-6} \left(\frac{q}{\varepsilon_1}\right)^{2/3} \quad and \quad \gamma_1 = 3.23 * 10^{-6} \left(\frac{q}{\varepsilon_1}\right)^{2/3} . \tag{2.1.7}$$

For a GaAs material γ_0 and γ_1 are given as $\gamma_0 = 2.26 * 10^{-12}$ and $\gamma_1 = 4 * 10^{-12}$. γ_0 and γ_1 are adjustable parameters to meet measurement results.

The charge carrier concentration in the potential well at the hetero-junction interface can be calculated using the Fermi-Dirac distribution and the two dimensional density of states D. For a density of states D between E_0 and $E_1$and $2D$ for energy levels above E_1, the sheet charge concentration, n_s, is given as [1]

$$n_s = D\int_{E_0}^{E_1} \frac{de}{1+e^{\frac{(E-E_f)}{V_{th}}}} + 2D\int_{E_1}^{\infty} \frac{de}{1+e^{\frac{(E-E_f)}{V_{th}}}}. \tag{2.1.8}$$

After integrating (2.1.8), the charge carrier concentration is given as

$$n_s = DV_{th}ln\left[\left(1+e^{\frac{(E_f-E_0)}{V_{th}}}\right)+\left(1+e^{\frac{(E_f-E_1)}{V_{th}}}\right)\right]. \tag{2.1.9}$$

Equation (2.1.9) gives an important relation between the Fermi-level, E_f, the sheet charge carrier concentration, n_s, and the sub-band energy levels E_0 and E_1. However, it is not an explicit analytical relation between the parameters. The systematical developments of analytical relationships between the important parameters, for the development of compact analytical models, are described in the following consecutive sections.

2.2 Space Charge Region in Equillibrium

Before looking into the characteristics of the hetero-junction region while being manipulated by an additional schottky contact, in this section a hetero-junction in thermal equilibrium is investigated. The band diagram of the hetero-junction shown in Fig. 2.1.1 is in its equillibrium state. Assuming depletion approximation in the space charge region of the large band gap material, the potential and the electric field in the region obey the Poisson's equation [3]. Thus,

$$\frac{d^2V_2(x)}{dx^2} = -\frac{q}{\varepsilon_2}N_A(x) \tag{2.2.1}$$

and

$$\frac{dF_2}{dx} = -\frac{q}{\varepsilon_2}N_A(x). \tag{2.2.2}$$

The integration of the two Poisson's equations can be performed within the range of the space charge region. The boundary conditions can be defined, considering the fact that the donor density in the spacer layer is zero, as

$$\begin{aligned} N_A(x) &= 0 \qquad for - d_S < x < 0 \\ N_A(x) &= N_A \quad for - d_2 < x < -d_S. \end{aligned} \tag{2.2.3}$$

Thus, integration using these boundary conditions, shown in Appendix A, gives

$$V_{20} = \frac{qN_A}{2\varepsilon_2}(d_2^2 - d_S^2) \tag{2.2.4}$$

and

$$\varepsilon_2 F_{i2} = qN_A(d_2 - d_S). \tag{2.2.5}$$

V_{20}, the band bending, is the potential at $-d_2$ in the space charge region in the equilibrium state.

From (2.2.4) and (2.2.5) the product $\varepsilon_2 F_{i2}$ can be written as

$$\varepsilon_2 F_{i2} = \sqrt{2q\varepsilon_2 N_A V_{20} + q^2 N_A^2 d_S^2} - qN_A d_S. \tag{2.2.6}$$

By applying geometrical rules on Fig. 2.1.1, V_{20} can also be expressed as

$$V_{20} = \triangle E_C - \delta_2 - E_{F0}. \tag{2.2.7}$$

Equations (2.2.4) and (2.2.6) express the approximated values of the potential and the electric field at the hetero-structure in its equilibrium state. Note that the depletion length in the large band-gap material, d_2, is not necessarily the same as the total width

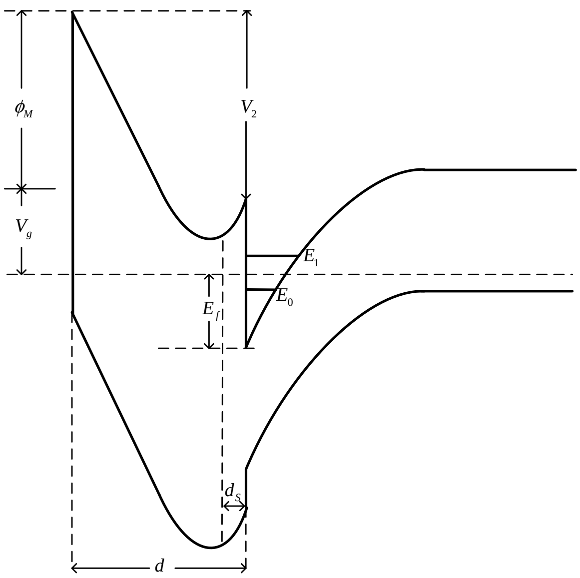

Figure 2.3.1: Band structure of a hetero-junction formed at the interface of two semiconductors with a different band-gap when a metallic material is placed in contact with the large band-gap semiconductor to form a schottky contact.

of the material and a complete depletion of the large band-gap material is not assumed in the calculations in this case.

2.3 Charge Control Mode

The band structure shown in Fig. 2.1.1 can be manipulated by placing a metallic contact with one of the semiconductors. Fig. 2.3.1 shows the band structure when a metallic material is attached to the large band-gap semiconductor to form a schottky contact.

Assuming that the region between the Schottky contact and the hetero-junction interface is fully depleted, the electrostatic potential in the region obeys Poisson's equation like that of the neutral state described in Section 2.2 [3, 4]. Therefore, (2.2.1) and (2.2.2) still hold in this region. A full depletion of the large band-gap semiconductor is assumed in this case. Thus, the second integration boundary in x is now extended to d, which is the total width of the large band-gap semiconductor. Hence, the electrostatic potential is given as

$$V_2 = \frac{qN_A}{2\varepsilon_2}(d - d_S)^2 - F_{i2}d. \tag{2.3.1}$$

From (2.3.1) one can easily obtain

$$\varepsilon_2 F_{i2} = \frac{\varepsilon_2}{d}(\frac{qN_A}{2\varepsilon_2}(d - d_s)^2 - V_2). \tag{2.3.2}$$

Similar to Fig. 2.1.1, applying basic geometry rules on Fig. 2.3.1 also gives

$$V_2 = \phi_M - V_G + E_f - \triangle E_C. \tag{2.3.3}$$

Substituting for V_2 from (2.3.3) into (2.3.2) gives

$$\varepsilon_2 F_{i2} = \frac{\varepsilon_2}{d}(\frac{qN_A}{2\varepsilon_2}(d - d_s)^2 - \phi_M + V_G - E_f + \triangle E_C). \tag{2.3.4}$$

If the interface states are neglected, the product of the dielectric constants and the electric fields at hetero-junction interface and the charge in the region can be related using Gauss law as

$$\varepsilon_1 F_{i1} = \varepsilon_2 F_{i2} = qn_s. \tag{2.3.5}$$

Therefore, the charge Q_S of the free charge carriers at the hetero-junction can be expressed as

$$Q_S = qn_s = \frac{\varepsilon_2}{d}(V_G - \phi_M - E_f + \triangle E_C + \frac{qN_A}{2\varepsilon_2}(d - d_S)^2). \tag{2.3.6}$$

In (2.3.6) the Fermi-level term, E_f, is very small as compared to the other terms, and the rest of the terms except V_g are summed and expressed as one single term, the so-called cut-off voltage, given as

$$V_{off} = \phi_M - \triangle E_C - \frac{qN_A}{2\varepsilon_2}(d - d_S)^2 \tag{2.3.7}$$

The cut-off voltage is a very important parameter as it defines the level of external voltage that is necessary to wipe out the charge carriers in the 2DEG. Thus, now Q_S can be written as

$$Q_S = qn_s = \frac{\varepsilon_2}{d}(V_G - V_{off} - E_f). \tag{2.3.8}$$

2.4 Threshold Voltage

In sections 2.2 and 2.3 the status of the hetero-structure region in equilibrium and non-equilibrium conditions have been investigated. What does really mark the transition between these two states? It is the threshold voltage that results in the transition from the neutral state to the charge control regime. This threshold voltage can be defined by equating the product $\varepsilon_2 F_{i2}$ calculated for each case [1]. By equating (2.2.6) and (2.3.4) one can easily find the threshold voltage to be

$$V_{threshold} = \phi_M - \delta_2 - \left(\sqrt{qN_2 d_2^2/2\varepsilon_2} - \sqrt{(\Delta E_C - \delta_2 - E_{f0}) + qN_2 e^2/2\varepsilon_2}\right)^2. \quad (2.4.1)$$

2.5 Simple Charge Control Model

The expressions given in (2.1.9) and (2.3.8) provide very important relations between the Fermi-level, the first two sub-bands, the charge carrier concentrations and the controlling gate voltage. However, these expressions are complicated and does not provide analytical relations between the parameters that can be used to build compact analytical models. In this section, using these relations and some simplifying assumptions, analytical expressions are developed that relate the controlling gate voltage and the charge carrier concentration.

The plots in Fig. 2.5.1 show the levels of the first two sub-bands and the Fermi-level calculated at a range of controlling gate voltage values. These levels are calculated numerically using (2.1.9) and (2.3.8) [5]. The plots show that the second energy level is higher than the first energy level and the Fermi-level of the full range of controlling gate voltage considered. While the first energy level is higher than the Fermi-level only up to a certain point and is lower for the rest of the voltage range. This shows that the contribution of the second energy level to the carrier concentration in the triangular potential well is negligible. Therefore, considering the contribution of only the first sub-band to the charge carrier concentration, (2.1.9) can be rewritten as

$$n_s = DV_{th} ln(e^{\frac{(E_f - E_0)}{V_{th}}} + 1). \quad (2.5.1)$$

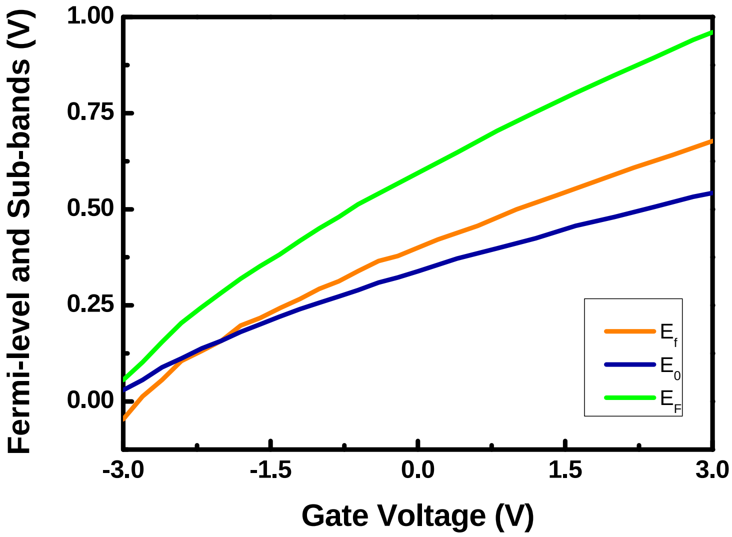

Figure 2.5.1: E_f, E_0 and E_1 calculated numerically using (2.1.9) and (2.3.8). Reproduced from [5].

Equation (2.5.1) gives the carrier concentration in AlGaN/GaN hetero-structure system where the contribution of only the first energy level is considered. After rearranging (2.5.1) and making use of (2.1.6) and (2.3.8), a simple charge control model is derived, given as

$$V_{g0} = \frac{qdn_s}{\varepsilon} + \gamma_0 n_s^{2/3} + V_{th} ln(\frac{n_s}{DV_{th}}). \tag{2.5.2}$$

The derivation of (2.5.2) is shown in Appendix B. It provides an explicit analytical relation between the controlling gate voltage and charge carrier concentration. This can be used to derive analytical expressions for terminal characteristics of a functional device based on such hetero-structure system. It, (2.5.2), can be extended to include the lateral potential V, considered as the local quasi-Fermi potential, at any point along the channel

[6]. Therefore,

$$V_{g0} - V = \frac{qdn_s}{\varepsilon} + \gamma_0 n_s^{2/3} + V_{th} ln(\frac{n_s}{DV_{th}}). \tag{2.5.3}$$

2.6 Drain-source Current Model

In this section and in the next consecutive sections, the developments of analytical models for terminal current and charges by making use of (2.5.3) are discussed.

An analytical drain-source current model can be formulated using the definition of the drain-source current along the channel written as [7]

$$I_{ds} = Wqn_s v \tag{2.6.1}$$

where v is the electron velocity in the channel. If a constant mobility, μ, of the electrons is assumed then, the relation between v and the electric field, F, at a certain point in the channel is given as

$$v = -\mu F = -\mu \frac{dV}{dx}. \tag{2.6.2}$$

Therefore,

$$I_{ds} = W\mu qn_s \frac{dV}{dx}. \tag{2.6.3}$$

After integrating along the total length of the channel from source to drain I_{ds} is expressed as

$$I_{ds} = \frac{W}{L} \int_{V_S}^{V_d} q n_s dV. \tag{2.6.4}$$

The integration variable can easily be changed to n_s, the carrier concentration, using the relation given in (2.5.3). Taking the derivative of both sides of (2.5.3) and rearranging gives

$$dV = -\left(\frac{qd}{\varepsilon} + \frac{2}{3}\gamma_0 n_s^{\frac{-1}{3}} + V_{th} n_s^{-1}\right) dn_s. \tag{2.6.5}$$

Substituting (2.6.5) in (2.6.4) for dV and integrating from the source to drain gives a simple analytical expression of the drain-source current that is written as

$$I_{ds} = -\frac{q\mu W}{L}\left[\frac{qd}{2\varepsilon}\left(n_D^2 - n_S^2\right) + \frac{2}{5}\gamma_0\left(n_D^{\frac{5}{3}} - n_S^{\frac{5}{3}}\right) + V_{th}\left(n_D - n_S\right)\right]. \tag{2.6.6}$$

In (2.6.6) n_S and n_D are the charge carrier concentrations, n_s, calculated at the source and at the drain terminals respectively. In principle, they can be calculated iteratively from (2.5.3). A more efficient way to calculate them, however, would be using an explicit expression of n_s which will make the model computationally faster [6].

2.7 Additional effects

The drain-source current model developed in the previous section is basically for an ideal long channel device where there are no other factors that affect the important parameters of the drain current such as the carrier charge concentration and the electron mobility. Thus, the expression in (2.6.6) forms the core current model. However, in real devices various physical phenomena have been identified that affect the final output current to a great extent. Some of these additional effects are being tackled as the device production technology advances and at the same time new undesirable effects are also being created while improving device performance, specially in relation with device size miniaturization. Application environment is also the other source of some of the non-ideal effects. Therefore, for the core current model to be used for a wide range of device types and sizes satisfactorily, the non-ideal effects should be included. Here, the most important non-ideal effects that have been incorporated with the core current model are discussed briefly.

2.7.1 Channel-length Modulation

After a saturation voltage has been reached, a high electric field is formed at the drain side of HEMT devices. A further increase in the drain voltage will then move the high field point towards the source. This effect is similar to shortening the channel length by an amount ΔL. This effect, the reduction of the effective length of the channel, is the so-called *channel length modulation* (CLM). The CLM can be accounted for using the CLM parameter, λ, that is used to modify the drain-source current as [7]

$$I_{ds,CLM} = I_{ds}(1 + \lambda V_d) \tag{2.7.1}$$

where $I_{ds,CLM}$ is the drain-source current model after the CLM modification.

2.7.2 Short-channel Related Effects

Reduction of the gate length will have an influence on the controlling capability of the gate. A shift in the threshold voltage of the device is observed with the reduction of the gate length. In addition, the shift in the threshold voltage depends on the drain-source bias. The total effects related with the short channel length can be incorporated as a threshold shift using the *short channel effect* parameter (SCE) as

$$V_{off,SCE} = V_{off} - \frac{V_d}{SCE} \tag{2.7.2}$$

where $V_{off,SCE}$ is the modified threshold voltage that contains the shift [7]. Long channel devices will have a high SCE value where the dependence of the threshold voltage on the applied drain voltage will be less while short channel devices have lower SCE parameter where the modification the threshold voltage by the drain voltage can be properly reproduced.

2.7.3 Self-heating Effects and Temperature Dependencies

Accounting for the effect of ambient temperature and device generated heating, *self-heating effect* (SHE), is critical specially for GaN-based HEMTs as they are the best candidates for high power applications [8, 9]. A considerable amount of heat could be generated during high power applications [10]. This could be worsened if the substrate is not a good heat sink. A reduced drain-source current and a negative conductance at high operating drain voltage are the main manifestations of the existence of SHE in a device [11, 12, 13]. The additional amount of temperature incurred due to SHE is given as

$$\Delta T = R_{TH} P_d \tag{2.7.3}$$

where $P_d = I_{ds}V_d$ is the dissipated power and R_{TH}, the thermal resistance, is the representative of the thermal behavior of the device [14, 15]. Therefore, the operating temperature of the device should be modified to account for the temperature increment, ΔT, as

$$T_{actual} = T_{ambient} + \Delta T \tag{2.7.4}$$

where $T_{ambient}$ is the ambient temperature and T_{actual} is the modified operating temperature. The thermal voltage, an important device parameter, and all the other temperature dependent parameters of the model should then be calculated using the modified operating temperature.

2.8 Derivatives of the Drain-source Current

The derivatives of a drain-source current model are one of the important figures of merit of a current model. They can be considered as the measures of the continuity of the current model and enable investigations of discontinuity anywhere in the operating regime of the model. The continuity of the current model is critical when it comes to applying the model for non-linearity studies which mainly involves the successive derivatives. The derivative of the drain-source model in terms of the gate voltage at a constant drain voltage, the transconductance, and the derivative in terms of the drain voltage at a constant gate voltage, the conductance, are the two main first derivatives of the current. These two parameters are defined as

$$g_m = \frac{\partial I_{ds}}{\partial V_g} \mid V_d \tag{2.8.1}$$

and

$$g_d = \frac{\partial I_{ds}}{\partial V_d} \mid V_g. \tag{2.8.2}$$

Once a drain-source current model is developed, obtaining the transconductance numerically from the calculated current is a common practice. Here, however, dedicated analytical expressions for the transconductance and conductance are developed. Having an independent transconductance expression will provide one an alternative to directly use the transconductance when it is not necessary to calculate the current for a certain application. The transconductance and conductance expressions are developed using the current model and the simple charge control model given in section 2.6 and section 2.5 respectively. The partial derivative of the current, (2.6.6), in terms of the gate voltage is

$$\begin{aligned}\frac{\partial I_{ds}}{\partial V_g} = g_m = -\frac{q\mu W}{L}\Bigg[\frac{qd}{2\varepsilon}\left(\frac{\partial n_D^2}{\partial V_g} - \frac{\partial n_S^2}{\partial V_g}\right) + \frac{2}{5}\gamma_0\left(\frac{\partial n_D^{5/3}}{\partial V_g} - \frac{\partial n_S^{5/3}}{\partial V_g}\right) \\ +V_{th}\left(\frac{\partial n_D}{\partial V_g} - \frac{\partial n_S}{\partial V_g}\right)\Bigg].\end{aligned} \tag{2.8.3}$$

From (2.8.3) a simplified expression of the transcondactance can be obtained as

$$g_m = -\frac{q\mu W}{L}\left[\left(\frac{qd}{\varepsilon}n_D + \frac{2}{5}\gamma_0 n_D^{2/3} + V_{th}\right)\frac{\partial n_D}{\partial V_g} - \left(\frac{qd}{\varepsilon}n_S + \frac{2}{5}\gamma_0 n_S^{2/3} + V_{th}\right)\frac{\partial n_S}{\partial V_g}\right] \tag{2.8.4}$$

where

$$\frac{\partial n_S}{\partial V_g} = \frac{1}{\frac{qd}{\varepsilon} + \frac{2}{3}\gamma_0 n_S^{-1/3} + V_{th} n_S^{-1}} \tag{2.8.5}$$

and

$$\frac{\partial n_D}{\partial V_g} = \frac{1}{\frac{qd}{\varepsilon} + \frac{2}{3}\gamma_0 n_D^{-1/3} + V_{th} n_D^{-1}} \tag{2.8.6}$$

are obtained from the differentiation of (2.5.3) at the source and at the drain respectively. Substituting each partial derivatives of the charge carrier concentrations at the source and drain given in (2.8.5) and (2.8.6) respectively in (2.8.4) and simplifying gives

$$g_m = -\frac{q\mu W}{L} \left[n_D - n_S \right]. \tag{2.8.7}$$

Equation (2.8.7) gives a very simplified analytical expression of the transconductance that is similar to previous transconductance expressions developed to MOSFET devices.

Similarly, the analytical expression of the conductance can be obtained by calculating the partial derivative of the current in terms of the drain voltage. Thus,

$$\begin{aligned}\frac{\partial I_{ds}}{\partial V_d} = g_d = -\frac{q\mu W}{L} \Bigg[\frac{qd}{2\varepsilon} \left(\frac{\partial n_D^2}{\partial V_d} - \frac{\partial n_S^2}{\partial V_d} \right) + \frac{2}{5}\gamma_0 \left(\frac{\partial n_D^{5/3}}{\partial V_d} - \frac{\partial n_S^{5/3}}{\partial V_d} \right) \\ + V_{th} \left(\frac{\partial n_D}{\partial V_d} - \frac{\partial n_S}{\partial V_d} \right) \Bigg].\end{aligned} \tag{2.8.8}$$

Since the charge carrier concentration at the source does not depend on the drain voltage, all the partial derivative terms of n_S in (2.8.8) result in zero. Therefore, the expression of the conductance can be written as

$$g_d = -\frac{q\mu W}{L}\left[\frac{qd}{\varepsilon}n_D + \frac{2}{3}\gamma_0 n_D^{2/3} + V_{th}\right]\frac{\partial n_D}{\partial V_d} \tag{2.8.9}$$

where

$$\frac{\partial n_D}{\partial V_d} = \frac{-1}{\frac{qd}{\varepsilon} + \frac{2}{3}\gamma_0 n_D^{-1/3} + V_{th} n_D^{-1}} \tag{2.8.10}$$

is obtained by the partial differentiation of (2.5.3) at the drain terminal. Thus, substituting (2.8.10) in (2.8.9) gives

$$g_d = \frac{q\mu W}{L} n_D. \tag{2.8.11}$$

2.9 Gate Charge Model

The total gate charge can be obtained by integrating the sheet charge carrier density along the channel over the total gate area [7]. Therefore,

$$Q_g = W\int_0^L q n_s(x)\, dx. \tag{2.9.1}$$

The integration variable in (2.9.1), dx, can be changed to dV using (2.6.3) as the expression of dV in terms of dn_s is already given in (2.6.5) and can once again be used to derive the gate charge expression in terms of charge carrier concentrations at the source and at the drain. Thus, using (2.6.3)

$$Q_g = \frac{W^2 q^2 \mu}{I_{ds}}\int_{vs}^{v_d} n_s^2 dV. \tag{2.9.2}$$

Again substituting for I_{ds} in (2.9.2) from (2.6.4) gives

$$Q_g = WLq\left(\frac{\int_{v_s}^{v_d} n_s^2 dV}{\int_{v_s}^{V_d} n_s dV}\right). \tag{2.9.3}$$

Let the two integrals at the numerator and denominator inside the brackets in (2.9.3) be represented as $f(n_s)$ and $g(n_s)$ respectively. Integrating the two separately after changing the integration variable from dV to dn_s using (2.6.5) gives

$$f\left(n_s\right) = \frac{qd}{3\varepsilon}\left(n_D^3 - n_S^3\right) + \frac{1}{4}\gamma_0\left(n_D^{\frac{8}{3}} - n_S^{\frac{8}{3}}\right) + \frac{1}{2}V_{th}\left(n_D^2 - n_S^2\right) \tag{2.9.4}$$

$$g\left(n_s\right) = \frac{qd}{2\varepsilon}\left(n_D^2 - n_S^2\right) + \frac{2}{5}\gamma_0\left(n_D^{\frac{5}{3}} - n_S^{\frac{5}{3}}\right) + V_{th}\left(n_D - n_S\right). \tag{2.9.5}$$

Thus, the complete gate charge expression becomes

$$Q_g = WLq\frac{f\left(n_s\right)}{g\left(n_s\right)} = WLq\left(\frac{\frac{qd}{3\varepsilon}\left(n_D^3 - n_S^3\right) + \frac{1}{4}\gamma_0\left(n_D^{\frac{8}{3}} - n_S^{\frac{8}{3}}\right) + \frac{1}{2}V_{th}\left(n_D^2 - n_S^2\right)}{\frac{qd}{2\varepsilon}\left(n_D^2 - n_S^2\right) + \frac{2}{5}\gamma_0\left(n_D^{\frac{5}{3}} - n_S^{\frac{5}{3}}\right) + V_{th}\left(n_D - n_S\right)}\right). \tag{2.9.6}$$

Equation (2.9.6) gives the total gate charge of the charge carriers in the whole channel region from source to drain [16].

2.10 Analytical Gate Capacitance Models

The two main intrinsic capacitances associated with the gate region, gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}, can be derived using the partial differentiations of the total gate charge with respect to the corresponding source and drain terminal voltages. To come up with simplified expressions of the gate capacitances, the two numerator and denominator functions of n_s given in (2.9.4) and (2.9.5) have been used. In addition, the letter x is also used to refer to a point along the channel so that one can determine the derivative of the gate charge not only at the source and drain but also at any point along the channel as long as the potential at that point is identified. Thus, the general gate capacitances are given as [16]

$$C_{gx} = WLq\left(\frac{\frac{\partial f(n_s)}{\partial V_x} g\left(n_s\right) - f\left(n_s\right)\frac{\partial g(n_s)}{\partial V_x}}{\left(g\left(n_s\right)\right)^2}\right) \tag{2.10.1}$$

where, for example, $V_x = V_s$ at the source terminal and $V_x = V_d$ at the drain terminal and similarly $C_{gx} = C_{gs}$ at the source and $C_{gx} = C_{gd}$ at the drain. To simplify the partial differentiations of $f\left(n_s\right)$ and $g\left(n_s\right)$, they can be written as the differences of two functions calculated at the source and the drain terminals as follows

$$f\left(n_s\right) = f_{main}\left(n_D\right) - f_{main}\left(n_S\right) \tag{2.10.2}$$

$$g\left(n_S\right) = g_{main}\left(n_D\right) - g_{main}\left(n_S\right) \tag{2.10.3}$$

where

$$f_{main}\left(n_x\right) = \frac{qd}{3\varepsilon}n_x^3 + \frac{1}{4}\gamma_0 n_x^{\frac{8}{3}} + \frac{1}{2}V_{th}n_x^2 \tag{2.10.4}$$

$$g_{main}\left(n_x\right) = \frac{qd}{2\varepsilon}n_x^2 + \frac{2}{5}\gamma_0 n_x^{\frac{5}{3}} + \frac{1}{2}V_{th}n_x \tag{2.10.5}$$

where $n_x = n_D$ at the drain and $n_x = n_S$ at the source. The main advantage of expressing $f\left(n_s\right)$ and $g\left(n_s\right)$ as given in (2.10.2) and (2.10.3) using the functions given in (2.10.4) and (2.10.5) is that the partial derivatives of $f\left(n_s\right)$ and $g\left(n_s\right)$ in V_s and V_d will be simplified into direct derivatives of $f_{main}\left(n_x\right)$ and $g_{main}\left(n_x\right)$ at the respective terminals as they can be calculated independently at each terminal. These derivatives of f_{main} and g_{main} are given as

$$\frac{df_{main(n_x)}}{dV_x} = \left(\frac{qd}{\varepsilon}n_x^2 + \frac{2}{3}\gamma_0 n_x^{\frac{5}{3}} + V_{th}n_x\right)\frac{dn_x}{dV_x} \tag{2.10.6}$$

and

$$\frac{dg_{main}\left(n_x\right)}{dV_x} = \left(\frac{qd}{\varepsilon}n_x + \frac{2}{3}\gamma_0 n_x^{\frac{2}{3}} + V_{th}\right)\frac{dn_x}{dV_x}. \tag{2.10.7}$$

Therefore, now the general gate capacitances expression in (2.10.1) can be written as

$$C_{Gx} = WLq\left(\frac{\frac{df_{main}(n_x)}{dV_x}g\left(n_S\right) - f\left(n_S\right)\frac{dg_{main}(n_x)}{dV_x}}{\left(g\left(n_S\right)\right)^2}\right). \tag{2.10.8}$$

The general gate capacitance term in (2.10.8) can now be used to calculate the gate capacitances, C_{gs} and C_{gd}. The calculation of these two capacitances using the expression given here are shown in section 2.11.5.

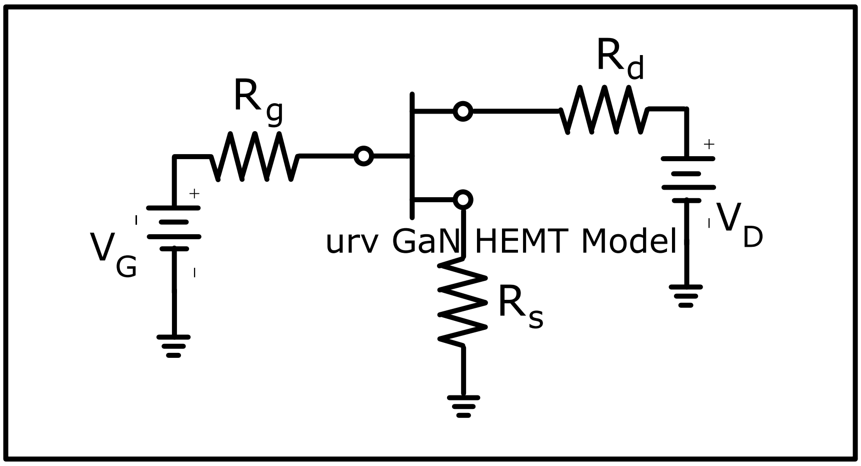

Figure 2.11.1: Basic test circuit set up used in ADS for model validation.

2.11 Results

The analytical current and charge models developed in previous sections have been implemented in Verilog-A, the industry-standard compact modeling language. The Advanced Design System (ADS) from Agilent© Technologies is then used to carry out standard set of simulations to test the performance of the models. Different sort of devices from various sources have been considered in order to verify the universal applicability of the models. Basically, the set of devices considered for the validation of the models are of two types: those that are obtained from commercially active semiconductor companies and those obtained from the world of research or literature. For the validation of the drain-source current model, the two main terminal characteristics, output and transfer, of the devices have been performed. In addition, the charge and capacitance models are verified through the modeling of the gate terminal capacitances. Fig. 2.11.1 shows the setup used in ADS for model validation.

Table 2.1: List of parameter values used to model a long channel device of $1\mu m$ gate length.

Parameter	Parameter description	Parameter value
$L(\mu m)$	Channel length	1
$V_{off}(V)$	Cut-off voltage	-2.85
$W(\mu m)$	Gate width	75
$d(nm)$	Thickness of barrier layer	25
$R_s(\Omega)$	Parasitic source resistance	0.6
$R_d(\Omega)$	Parasitic drain resistance	0.9
$v_{sat}(m/s)$	Saturation velocity	$1.19e5$
$\mu_0(m^2/Vs)$	Low field mobility	0.06

2.11.1 Core current model validation

The plots in Fig. 2.11.2 , (a) and (b), show the comparison between the drain-source current model and the $I-V$ characteristics of a long channel device with gate length of $1\mu m$ [17]. This mainly shows the validity of the core current model where most of the short channel and other additional effects do not play important roles. The model was able to reproduce both the output and transfer characteristics of the long channel device very well. Table 2.1 provides the list of the basic set of parameters used to reproduce the transfer and output characteristics of the long channel device shown in Fig. 2.11.2.

2.11.2 Output characteristics validation

The $I_d - V_d$ plots from Fig. 2.11.3 to Fig. 2.11.5 show the comparison between the modeled and measured output characteristics of devices with different gate lengths. Fig. 2.11.3 displays the $I_d - V_d$ curves of a device with gate length of $0.7\mu m$ [18]. A certain level of short channel effects have started to show up in the device even though not very significant. In addition, since the measurements are carried out only up to very low drain voltage values, no self-heating effect is observed as well. However, in Fig. 2.11.4 the output characteristics of a device with a gate length of $0.35\mu m$ are plotted up to

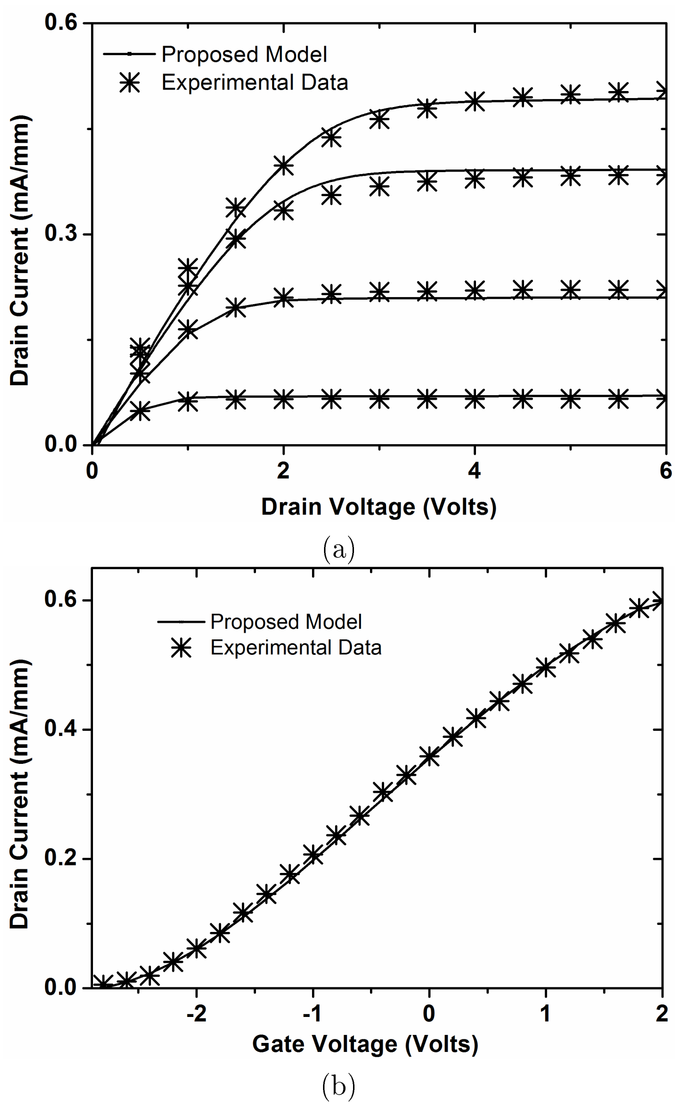

Figure 2.11.2: I-V characteristics of a $1\mu m$ device Modeled (solid lines) and Experimentally measured (symbols), (a) Output characteristics (b) Transfer characteristics, data taken from [17].

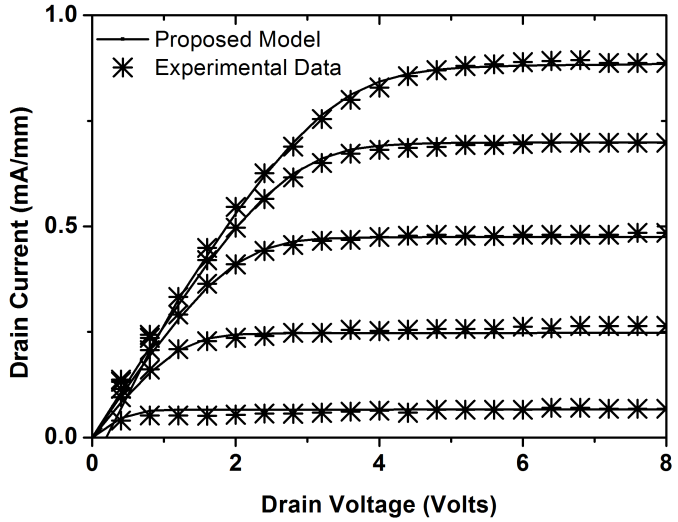

Figure 2.11.3: Output characteristics of a $0.7\mu m$ device Modeled (solid lines) and Experimentally measured (symbols), data taken from [18].

a relatively higher level of drain voltage [19]. At the higher drain voltage values the drain-source current have started to reduce, because of SHE. Since SHE is included in the model, it was possible to reproduce the current reduction at higher voltage that is caused by high power dissipation. The parameters used to model these two devices are given in Table 2.2. The output characteristics plotted in Fig. 2.11.5 are of a 9×100 GaN HEMT with a gate length of $0.125\mu m$ from Triquint©. The $I_d - V_d$ curves are measured under a controlled power compliance. Thus, no SHE is observed as the $I_d - V_d$ curves at higher gate voltage are measured only up to controlled levels of the drain voltage. Short channel effects are observed at the $I_d - V_d$ curves of low gate voltage values. In addition, at these low gate voltage values non-physical reduction of the current is observed near the knee region. The model has properly predicted the expected knee voltage behavior and the short channel behavior observed in the saturation region.

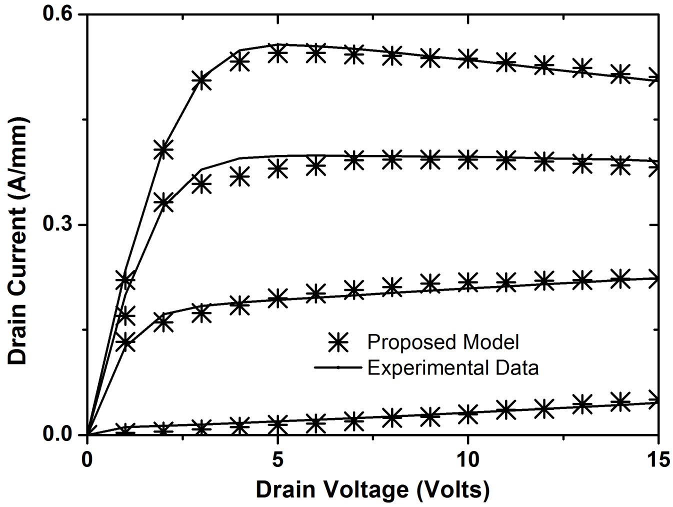

Figure 2.11.4: Output characteristics of a 0.35μm device Modeled (solid lines) and Experimentally measured (symbols), data taken from [19].

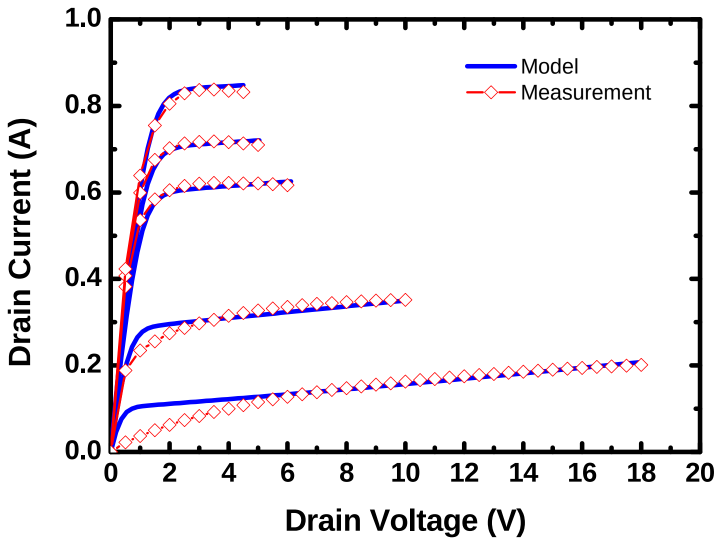

Figure 2.11.5: Measured (symbols plus lines) and modeled (solid lines) output Characteristics of a 9×100 device with a gate length of $0.125\mu m$. The gate Voltages are $0V$,$-0.6V$,$-1V$,$-2V$,$-2.6V$ from top to bottom.

Table 2.2: List of parameters used to model the $I-V$ characteristics of two devices with gate length of $0.7\mu m$ and $0.35\mu m$.

Parameter	Parameter description	$0.7\mu m$ Device	$0.35\mu m$ Device
$L(\mu m)$	Channel length	0.7	0.35
$V_{off}(V)$	Cut-off voltage	-3.8	-2.98
$W(\mu m)$	Gate width	25	250
$d(nm)$	Thickness of barrier layer	18	30
$R_s(\Omega)$	Parasitic source resistance	0.5	0.9
$R_d(\Omega)$	Parasitic drain resistance	1.6	2
$v_{sat}(m/s)$	Saturation velocity	$1.19e5$	$1.19e5$
$\mu_0(m^2/Vs)$	Low field mobility	0.04	0.05
$\lambda(V^{-1})$	CLM parameter	$1e-5$	$2e-4$
SCE	SCE parameter	$1e3$	31
$R_{th}(K/W)$	Thermal resistance	6.5	12

2.11.3 Transfer characteristics validation

The $I_d - V_g$ plots in Fig. 2.11.6 and Fig. 2.11.7 show the modeling of the transfer characteristics of the devices considered in section 2.11.2. The comparison between modeled and measured transfer characteristics of the device with the gate length of $0.7\mu m$ is shown at a single drain voltage of $5V$ in Fig 2.11.6. As shown in the output characteristics, see Fig. 2.11.3, a significant SCE is not exhibited by this device. Therefore, the transfer characteristics of this device are not expected to show any threshold voltage shift at different drain voltage values. Rather, Fig. 2.11.7, where the modeled and measured characteristics of the 9×10 GaN HEMT are displayed, show significant threshold shifts that occur for the different drain voltage values used. As mentioned earlier, the device has a gate length of $0.125\mu m$ which, to date, is a gate length in the lower limit of device gate length range. Therefore, the SCE is more pronounced in this device. Considering the SCE is of great importance in modeling device behavior at such gate lengths and below. An appropriate value of the SCE and the other model parameters are chosen so that the model can trace the threshold shifts properly. Table 2.3 summarizes the set of parameters used.

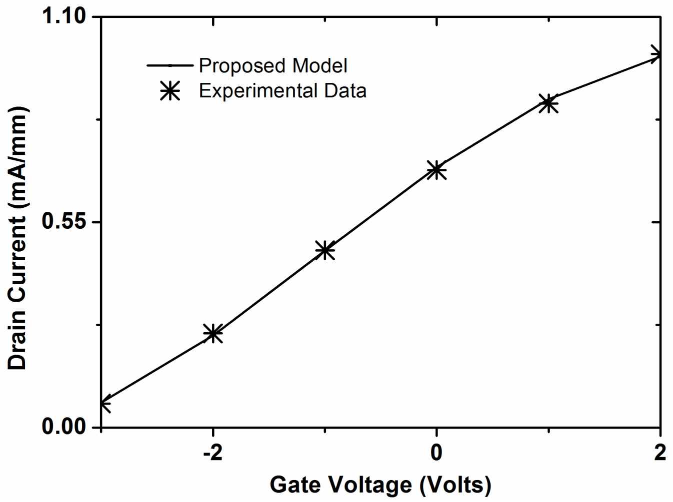

Figure 2.11.6: Measured (symbols plus lines) and modeled (solid lines) transfer Characteristics of a device with a gate length of $0.7\mu m$ at a drain Voltage of $5V$, data taken from [18].

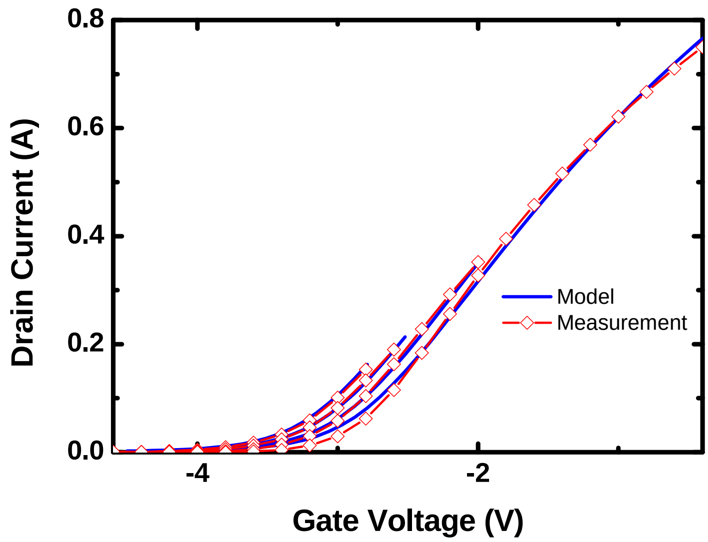

Figure 2.11.7: Measured (symbols plus lines) and modeled (solid lines) transfer Characteristics of a 9×100 device with a gate length of $0.125\mu m$. The drain Voltages are from $5V$ to $20V$ with a step of 5 from bottom to top.

Table 2.3: The set of parameters used to reproduce the $I-V$ characteristics of a 9×100 device with a gate length of $0.125\mu m$ from TriQuint© Semiconductor

Parameter	Parameter description	Parameter value
$L(\mu m)$	Channel length	0.125
$V_{off}(V)$	Cut-off voltage	-2.83
$W(\mu m)$	Gate width	900
$d(nm)$	Thickness of barrier layer	20
$v_{sat}(m/s)$	Saturation velocity	$1.19e5$
$\mu_0(m^2/Vs)$	Low field mobility	0.087
SCE	SCE parameter	47

2.11.4 Transconductance and conductance validation

Fig. 2.11.8 and Fig 2.11.9 present the derivatives of the drain-source current, the transconductance and the conductance. The first few derivatives of the drain-source current model, as mentioned earlier, are very important figures of merit. They are the measures of the continuity of the model in the whole operating regime and the continuity of the model is of interest specially in nonlinear modeling applications. Fig. 2.11.10 to Fig. 2.11.13 and Fig. 2.11.14 to Fig. 2.11.17 show the comparison between measured and modeled higher order derivatives of the transconductance and the conductance respectively. The good agreement shown between the model and the numerical derivatives of the experimentally measured current verify that the model is continuous in the whole operating regime of the device.

2.11.5 Gate charge and capacitance models validation

The $C-V$ characteristics, gate-source capacitances against the gate voltage and gate-drain capacitances against the drain voltage, of the device with $0.35\mu m$ gate length considered in the previous sections have been compared with the gate capacitance models given in section 2.10. Fig. 2.11.18 shows the modeled and measured gate-source

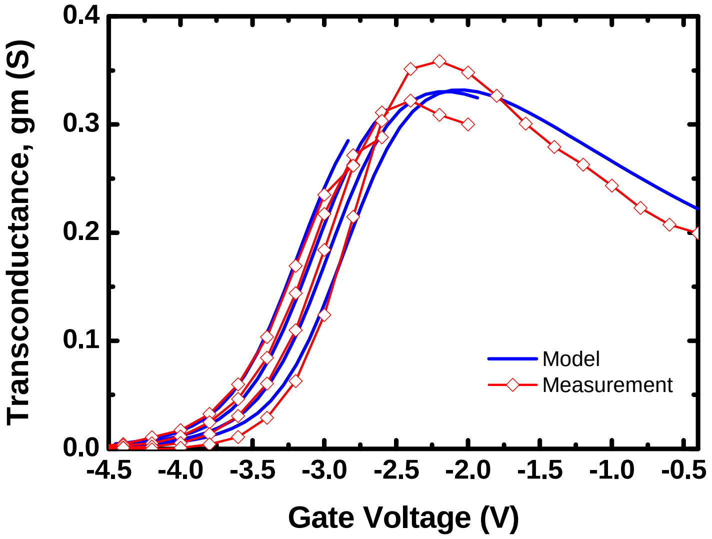

Figure 2.11.8: Measured (symbols plus lines) and modeled (solid lines) transconductance of a 9×100 device with a gate length of $0.125\mu m$. The drain Voltages are from $5V$ to $20V$ with a step of 5 from bottom to top.

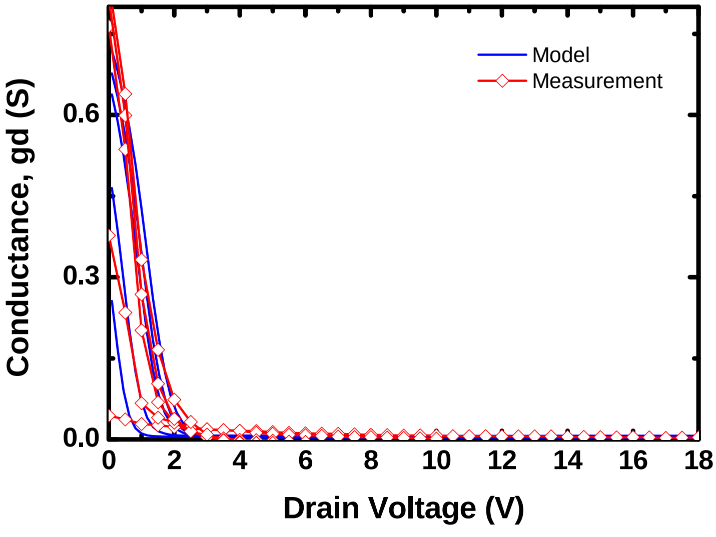

Figure 2.11.9: Measured (symbols plus lines) and modeled (solid lines) conductances of a 9×100 device with a gate length of $0.125\mu m$. The gate Voltages are $0V$,$-0.6V$,$-1V$,$-2V$,$-2.6V$ from top to bottom.

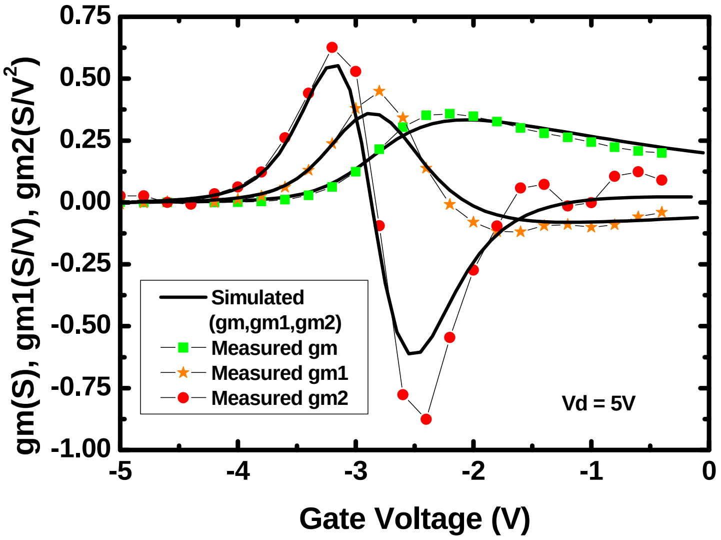

Figure 2.11.10: Transconductance, g_m, and its first two derivatives, g_{m1} and g_{m2} at a drain voltage of $5V$.

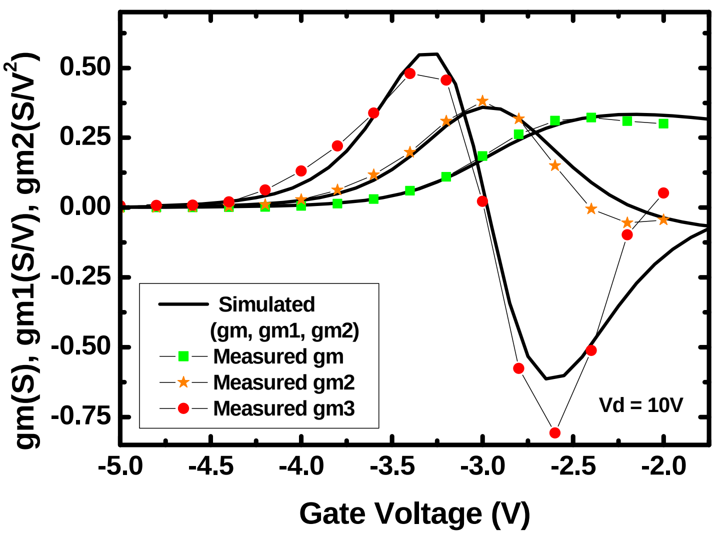

Figure 2.11.11: Transconductance, g_m, and its first two derivatives, g_{m1} and g_{m2} at a drain voltage of $10V$.

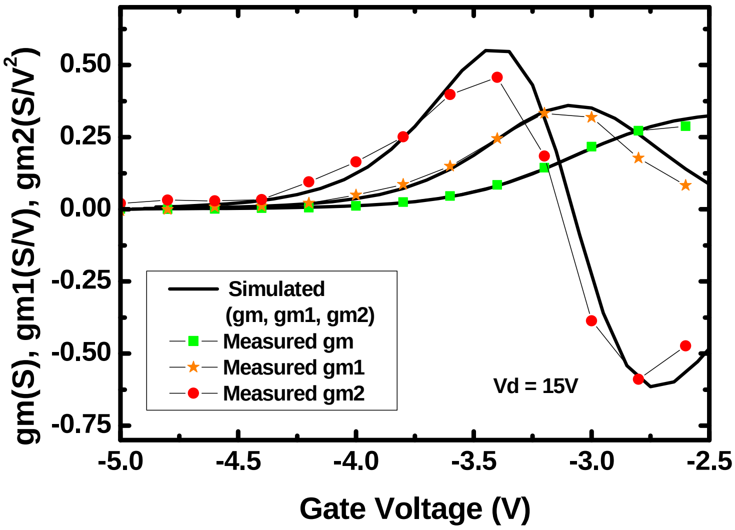

Figure 2.11.12: Transconductance, g_m, and its first two derivatives, g_{m1} and g_{m2} at a drain voltage of $15V$.

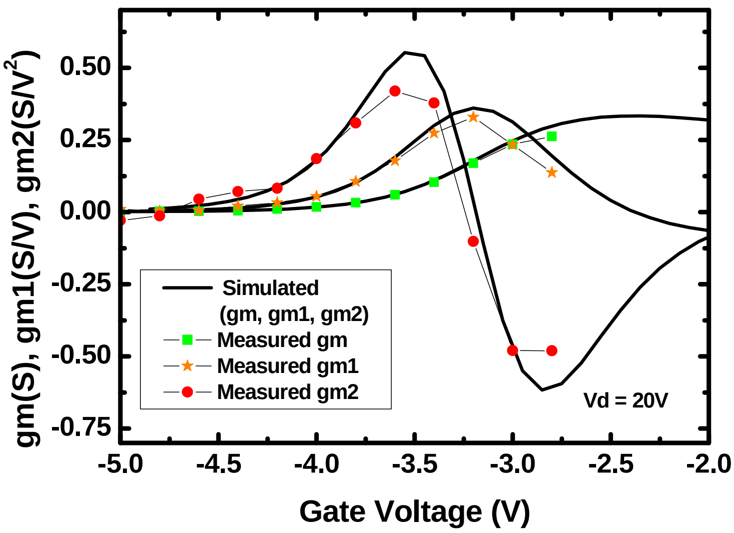

Figure 2.11.13: Transconductance, g_m, and its first two derivatives, g_{m1} and g_{m2} at a drain voltage of $20V$.

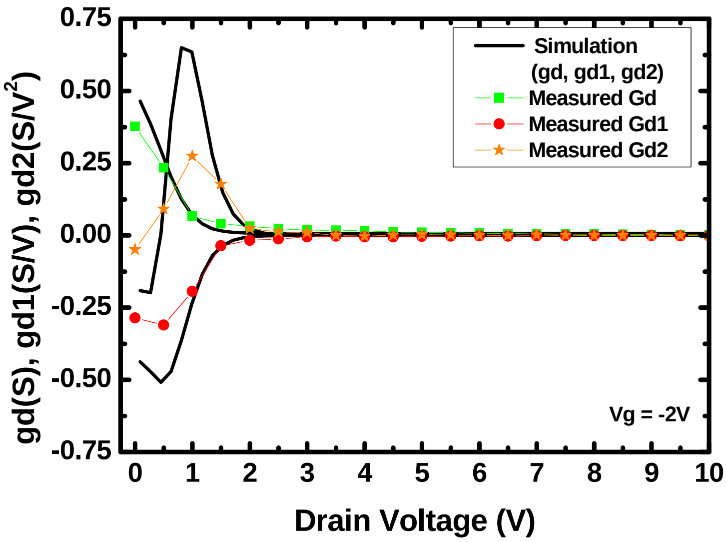

Figure 2.11.14: Conductance, g_d, and its first two derivatives, g_{d1} and g_{d2} at a gate voltage of $-2V$.

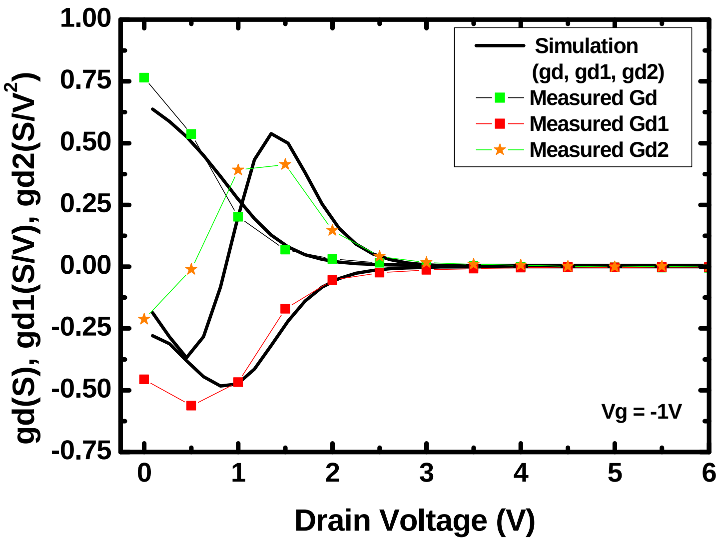

Figure 2.11.15: Conductance, g_d, and its first two derivatives, g_{d1} and g_{d2} at a gate voltage of $-1V$.

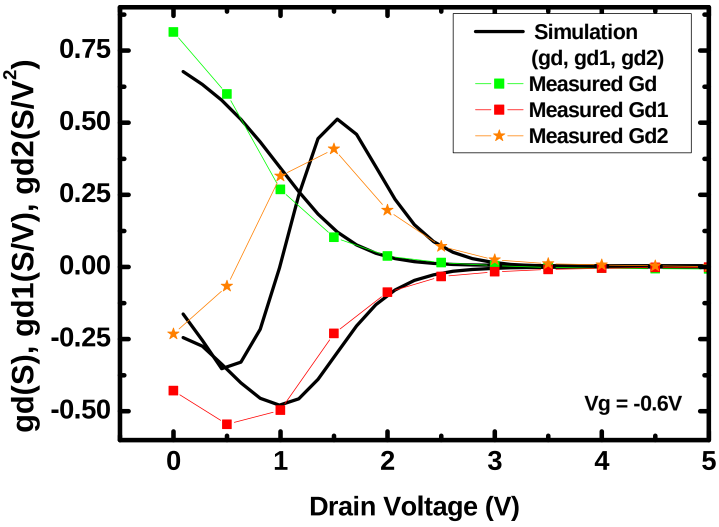

Figure 2.11.16: Conductance, g_d, and its first two derivatives, g_{d1} and g_{d2} at a gate voltage of $-0.6V$.

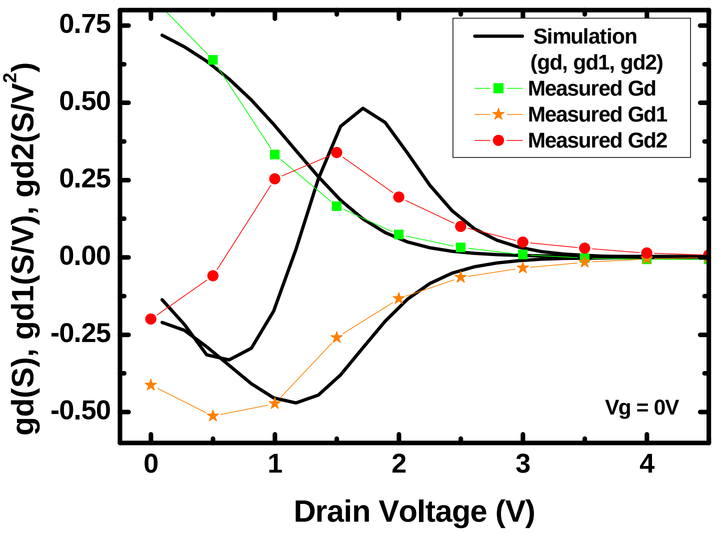

Figure 2.11.17: Conductance, g_d, and its first two derivatives, g_{d1} and g_{d2} at a gate voltage of $0V$.

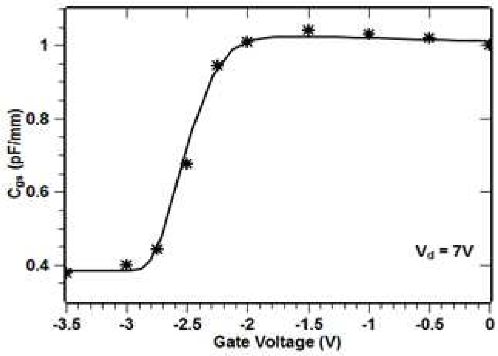

Figure 2.11.18: Measured (symbols) and modeled (solid lines) gate-source capacitance, C_{gs}, of a device with a gate length of $0.35\mu m$ at a drain voltage of $7V$, data taken from [19].

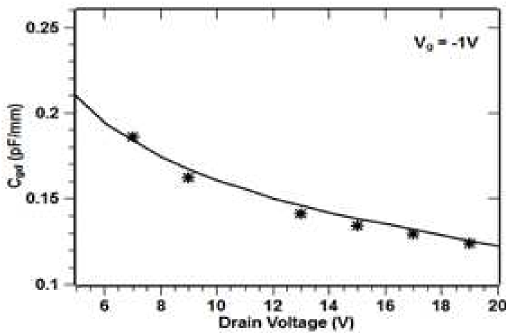

Figure 2.11.19: Measured (symbols) and modeled (solid lines) gate-drain capacitance, C_{gd}, of a device with a gate length of $0.35\mu m$ at a gate voltage of $-1V$, [19].

capacitances against the gate voltage where they showed a good agreement. The fringing capacitance of this device is about $0.37pF/mm$ and the measurements are obtained at a drain voltage of $7V$. The simulated and modeled gate-drain capacitances against the drain voltage are shown in Fig. 2.11.9. Measurement and model again show good agreement. The gate-drain capacitance values are measured at a gate voltage of $-1V$. The agreements between measured and modeled gate capacitances validates the total gate charge model expression given in section 2.9 in addition to the capacitance expressions that are derived from it using partial differentiations.

2.12 Conclusion

The chapter discussed a systematic development of physics-based compact models for circuit simulation based on the fundamental electrostatic consideration of the hetero-junction interface of general III-V devices. The models allow prediction of device performance based on device geometric structure and design features. The models have minimal set of parameters and does not require an extensive parameter extraction procedure.

In section 2.1 the derivative of the charge carrier concentration from the definitions of the Fermi-level and the first two energy sub-bands is presented. The relations between the energy levels and the electric field are obtained from the Schrodinger's equation solution of the longitudinal quantized energy assuming a quasi-constant electric field. Poisson's equation was applied on the electric field and solved which resulted in a simple relation between the electric field and the charge carrier concentration. The equilibrium state of the hetero-junction region assuming depletion approximation is analyzed in section 2.2. The band bending potential created in the large band-gap semiconductor is calculated after solving Poisson's equation for the potential and electric field in the region using the appropriate boundary conditions. The effect of an external potential applied through a schottky contact to disturb the equilibrium state is discussed in section 2.3. Using the Poisson's equation once again and considering the geometrical relations between the potentials from a non-equilibrium band-structure diagram, a relationship between the externally applied potential and the other hetero-junction parameters is established. The threshold voltage, the theoretical transition point that separates the two distinct states of the hetero-junction have been defined by equating the results obtained independently for the equilibrium and non-equilibrium cases.

The special case of AlGaN/GaN hetero-junction have been considered in section 2.5. The relative positions of the first two energy sub-bands and the Fermi-level have shown that the second energy level is significantly higher than the first energy level and the Fermi-level. Therefore, the contribution of the second energy level to the sheet charge concentration, 2DEG, has been neglected. Based on this simplifying assumption and the relations between the parameters of the hetero-junction region a simple charge control model has been derived. This charge control model is very useful as it gives analytical relation between the external voltage and the charge carrier concentration.

Using the charge control model, an analytical physics-based compact drain-source current model has been developed. The model basically depends on the calculation of charge carrier concentration at the source and drain of a device after which should be integrated based on the definition of drain-source current calculation. To enhance the robustness of the core current model, additional effects that directly affect the drain-source current have been included. These effects arise from different device operating conditions as well as from device technology. A standard set of modeling approaches, that are also used in the modeling of other FET devices, has been adapted here to model the non-ideal effects.

Analytical expressions of the transconductance and conductance were obtained through the derivation of the drain-source current model. The analytical transconductance expressions provide an alternative to calculate the derivatives directly which otherwise will be done by numerical differentiation after calculating the current.

A complete analytical expressions of the total gate charge has also been developed using the charge control model. The gate-source and gate-drain capacitance expression were then derived from the analytical gate charge model. The dedicated analytical expressions of the gate capacitances or the numerical derivatives of the calculated gate charge can be used in the equivalent circuit definition of a device in circuit simulator applications.

Different sets of test simulations have been carried out to demonstrate the validity of the current and charge models. The results of the models have been compared with real experimental measurement data of devices from the research as well as commercial areas. The performance of the models were presented in section 2.11. The models, in general, showed good agreement with measurement data taken from a wide range of devices in different operating conditions. The incorporation of additional effects to improve model performance has been demonstrated. The continuity of the model in the whole device operating regimes has been shown through the validation of the transconductance and conductance. This also automatically qualifies the model for non-linear applications. Moreover, the total gate charge model and the resulting gate capacitance models have also been verified by the good agreements shown between gate capacitance models and experimental data.

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Chapter 3

Modeling Drain Current Collapse in AlGaN/GaN HEMTs

AlGaN/GaN HFET devices show reduced RF power output due to the compression of the RF current swing as compared to the dc value [1, 2, 3]. In addition, they also show a reduced dc current in the knee region of their $I - V$ curves when a stress with a high drain voltage is applied continuously for hours [4, 5]. This RF power dispersion at higher frequencies, also know as current collapse, have put a great limitation on the application of these devices for high power and high frequency applications [6].

Much effort has been put into understanding and explaining of the root causes of the current reduction phenomena using detailed experimental work and theoretical models . For instance, operating at a frequency comparable with the carrier capture and emission frequency from deep centers [7] and charging of states due to charge transport delay [2] are a few to mention out of many other suggestions forwarded. The variety of explanations forwarded to explain the observed current collapse effects is useful to explore all the possible causes of this abnormality of such devices and finally to identify one or more universally acceptable mechanisms that are responsible for it [8, 9, 10]. A considerable research work is also being done to minimize the effects of current collapse [11, 12, 13]. In the mean time, the fundamental differences that exist in the understanding of the causes of current collapse make the formulation of physics-based compact models that incorporate the effect a challenging task.

The charging of surface traps in the gate-drain region is widely accepted as the main cause of the current collapse phenomenon and is used as a base of the current collapse modeling presented here [14, 15, 16, 17]. Earlier analytical drain current models that incorporate current collapse effects were developed with the assumption that the trapped region increases the drain and source access resistances and the effect of the field-dependent trapping is accounted as a modification of the access resistances [18, 19]. The trapped charge calculated as a fraction of the equilibrium electron concentration, by multiplying it with a field-dependent function, is used to calculate the value of the access region resistance modifier. An empirical field-dependent function with a fitting parameter is used that agrees with experimental data. However, here a somehow different perspective of the trapped charge region is used.

The modeling of permanent or semi-permanent current collapse effect observed in devices due to an applied stress is discussed. The modeling activity is consisted of combining the drain current model developed earlier in Chapter 2 with a virtual gate modeling technique that is going to be described shortly. A large signal equivalent circuit that is suitable for circuit simulation and the details of model implementation are presented.

3.1 The Virtual-gate Modeling Approach

Some of the acceptor-type surface states that are found in the gate-drain region, in the vicinity of the gate, are shown to be capable of trapping charge carriers [14]. The trapped carriers could originate from the hot electrons of the channel [20] or could be injected from the gate [21]. This creates an accumulated charge in the area that tends to deplete the 2DEG channel under it. This causes the reduction of carrier concentration which in turn results in a reduced drain current. This is, therefore, equivalent to applying a negative gate voltage via a secondary gate connected to the gate-drain region so as to deplete the 2DEG right under it, the virtual gate concept. Fig. 3.1.1 shows a layout of a device which had accumulated additional charge carriers in its gate-drain region. Fig. 3.1.2 shows a layout used for compact modeling where the charge accumulated in gate-drain region is represented by an equivalent virtual gate. The determination of the parameters of the virtual gate is very important to formulate a compact model. The potential of the virtual gate can be calculated by considering the electrostatics of the depletion region after stress. On the other hand a more robust way to consider the effect of the virtual gate would be to consider it as a fully functional very short channel virtual transistor connected with the main gate channel that saturates gradually similarly to the main gate. The techniques used to realize the virtual gate modeling will be described shortly in the following sections.

3.1.1 2D electron concentration distribution simulation

In order to demonstrate the assumption of an additional virtual gate in the gate-drain region, a 2D device simulation is presented here first. The simulation is carried out with and without surface trapped charge carriers in the gate-drain region so that the effect of the additional charge on the surface on the channel and the related key parameters can

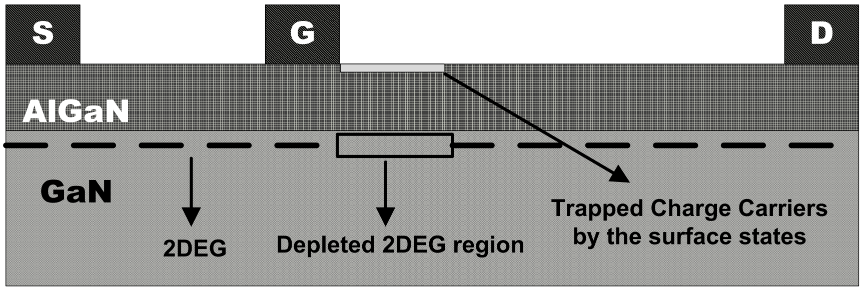


Figure 3.1.1: Entrapment of charge carriers by the surface states in the AlGaN barrier layer which causes the depletion of the 2DEG channel under it.

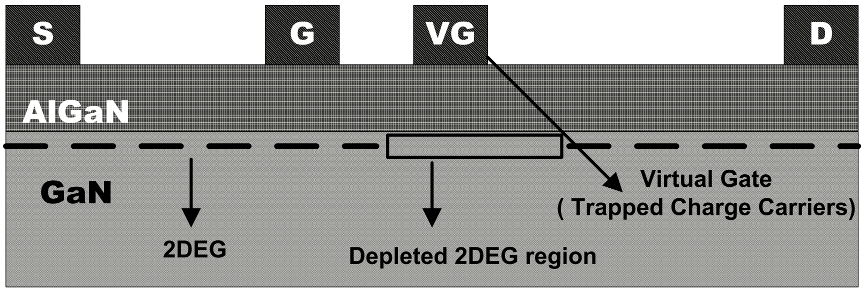


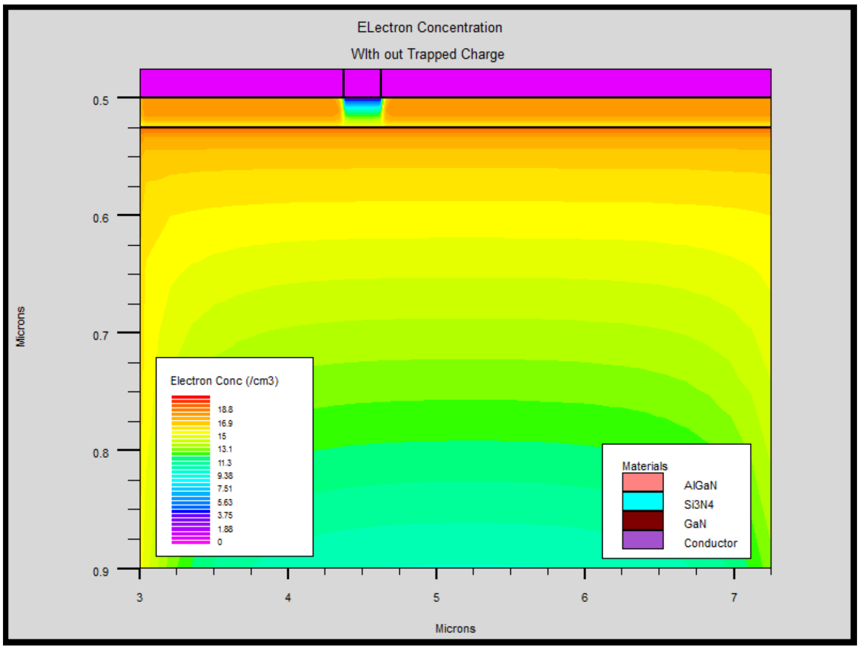
Figure 3.1.2: Application of a negative virtual gate voltage that is equivalent to the charge accumulated at the surface for the purpose of compact modeling.

be analyzed [22]. The physical device simulation is carried out using the ATLAS 2-D simulator of Silvaco.

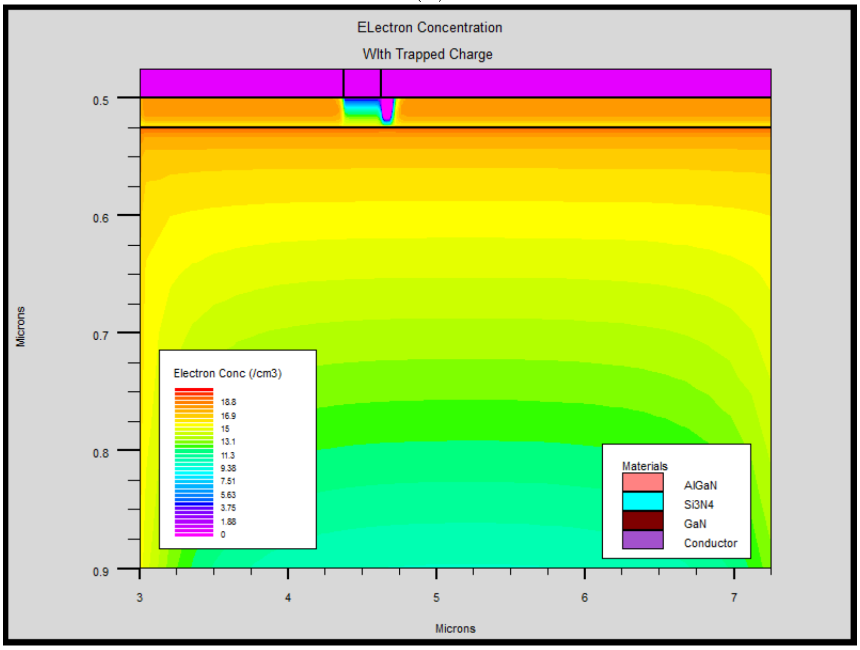
The simulated sample device has a gate length of $0.25\mu m$. A $25nm$ AlGaN barrier layer with 0.3 Al mole fraction and a $1.475\mu m$ GaN are used to form the hetero-junction. The total source-drain spacing is $4.5u\mu m$ with a gate-source spacing of $1.375\mu m$ and a gate-drain spacing of $2.875\mu m$. Polarization charges and uniform interface charges are defined at the hetero-junction and self-heating is also included. Finally, an additional charge has been added on the upper surface of the AlGaN barrier layer to model the charge carriers trapped by the surface states. The additional charge carriers defined are made to have fixed amount of concentration and length, -2×10^{13} and $75nm$ respectively, in this case.

The color contour plots from Fig. 3.1.3 to Fig. 3.1.6 show the electron concentration in the channel region before and after defining the charge carriers in the gate-drain region. The contour plots are shown for a $0V$, linear region and saturation region drain biases. In all cases, the additional charge carriers defined in the gate-drain region tend to deplete the 2DEG region under it.

To be able to compare the extent of 2DEG reduction caused by the trapped charge carriers, the electron concentration of the channel region before and after defining the additional charge carriers are plotted together, Fig. 3.1.7 to Fig. 3.1.10. One can see that defining additional charge carriers in the gate-drain region, indeed, resulted in a reduced electron concentration in the region under it. However, the effect is found to be more severe in the linear and knee regions as compared to those in the saturation region. This is in agreement with the experimental measurements where a higher drain current reduction is observed in the knee region as compared to the linear and saturation regions.

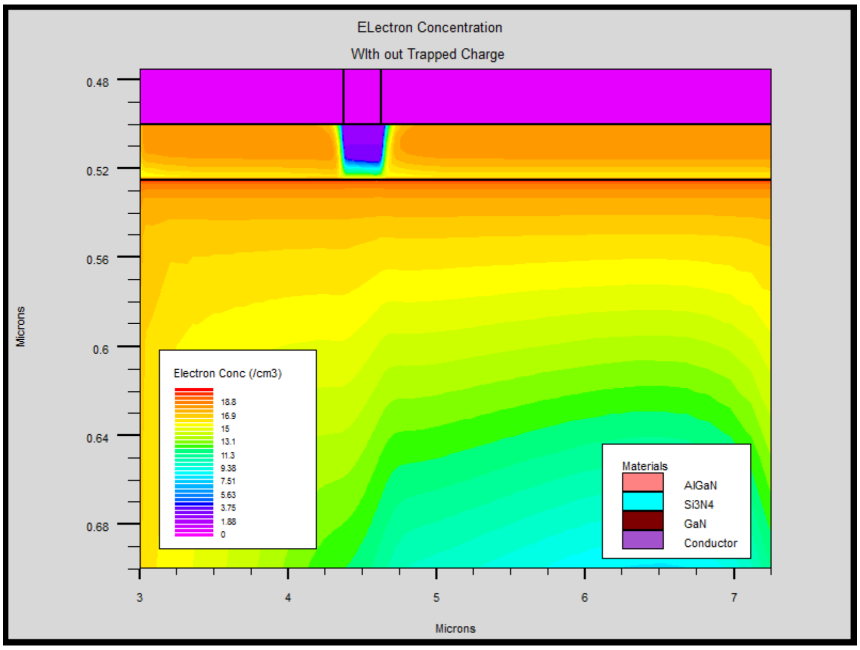


(a)

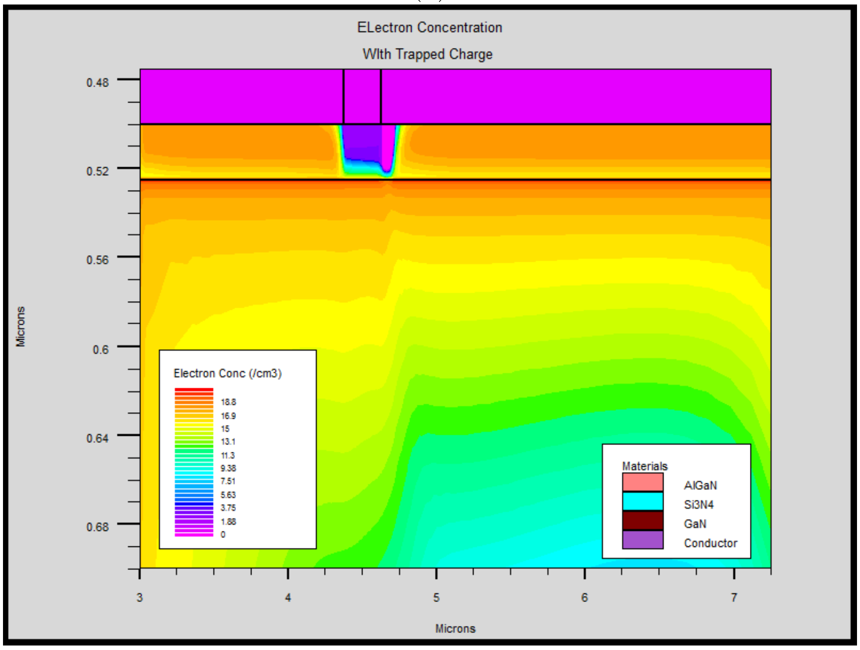


(b)

Figure 3.1.3: Electron concentration contour plot in the channel region at V_d=0V without (a) and with (b) additional charge carriers defined in the gate drain region.

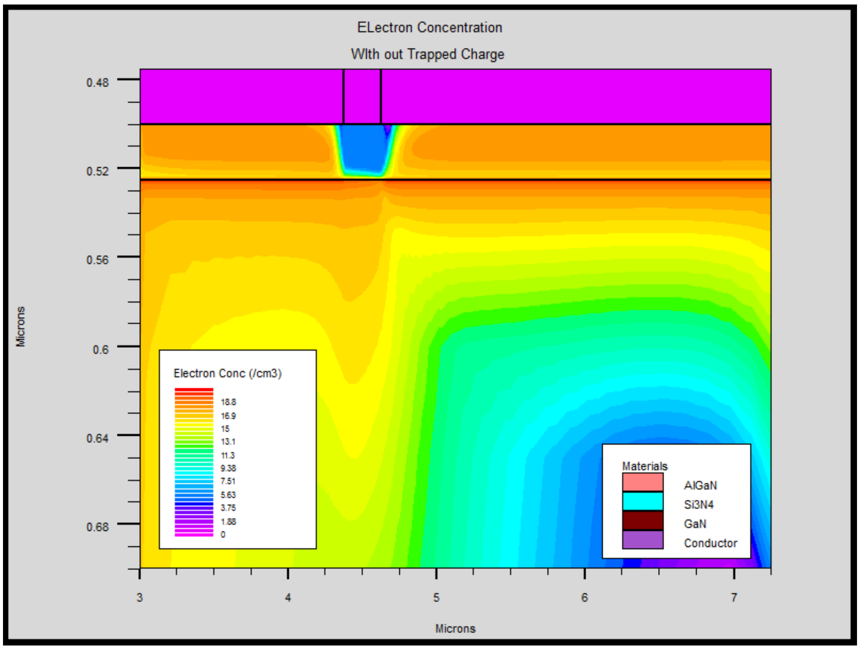


(a)

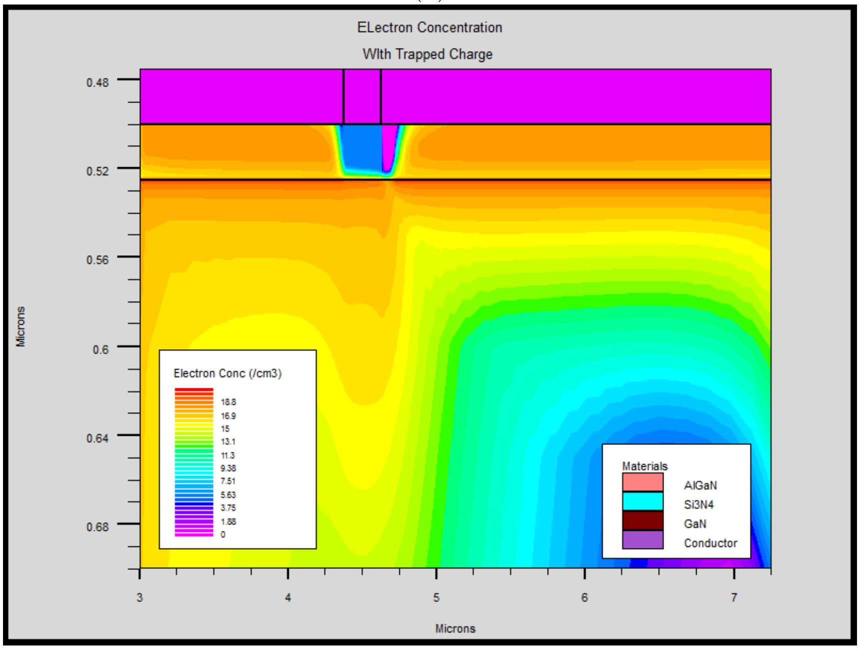


(b)

Figure 3.1.4: Electron concentration contour plot in the channel region at Vd=5V without (a) and with (b) additional charge carriers defined in the gate drain region.

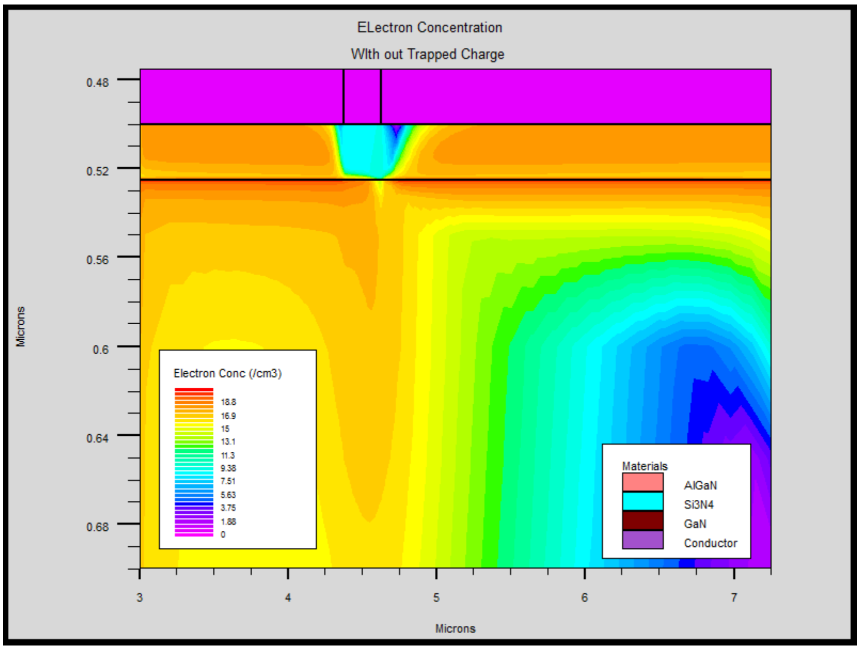


(a)

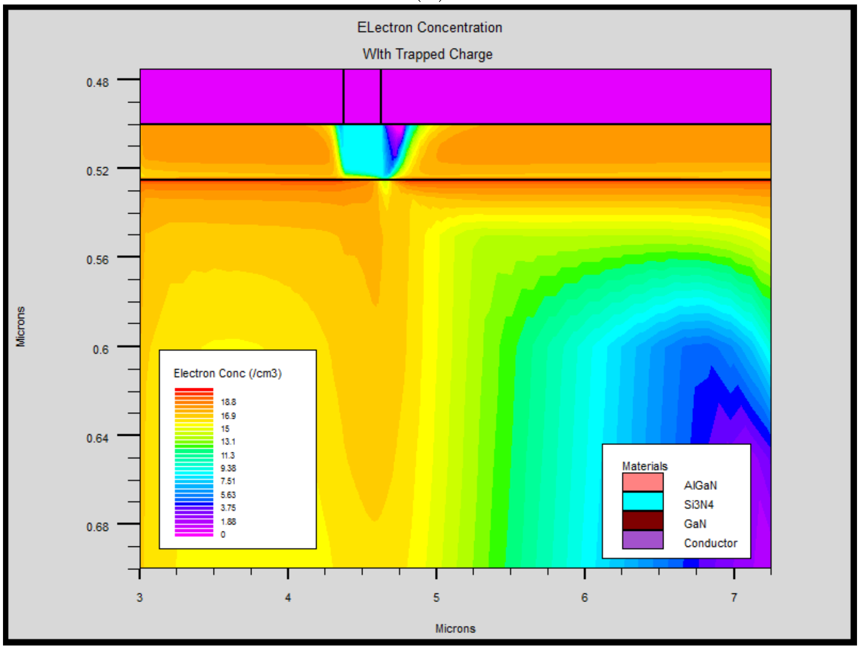


(b)

Figure 3.1.5: Electron concentration contour plot in the channel region at V_d=13V without (a) and with (b) additional charge carriers defined in the gate drain region.



(a)



(b)

Figure 3.1.6: Electron concentration contour plot in the channel region at $V_d = 25V$ without (a) and with (b) additional charge carriers defined in the gate drain region.

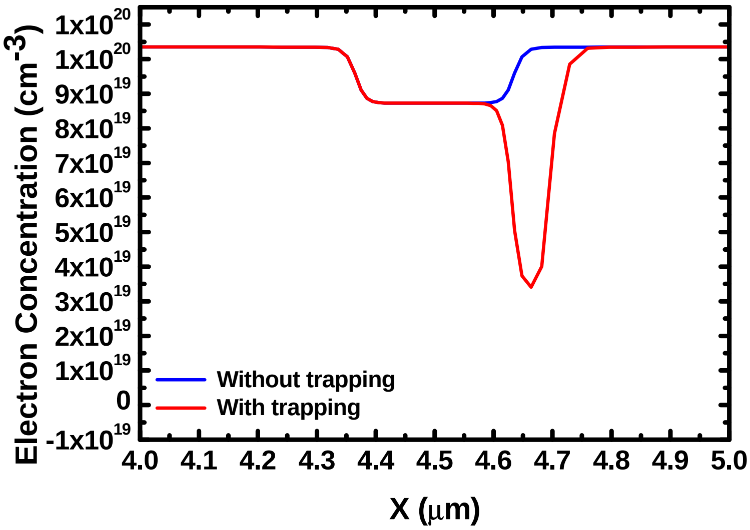


Figure 3.1.7: Electron concentration in the channel region at $0V$ with (Red) and without (Blue) trapped charge definition in the gate-drain region.

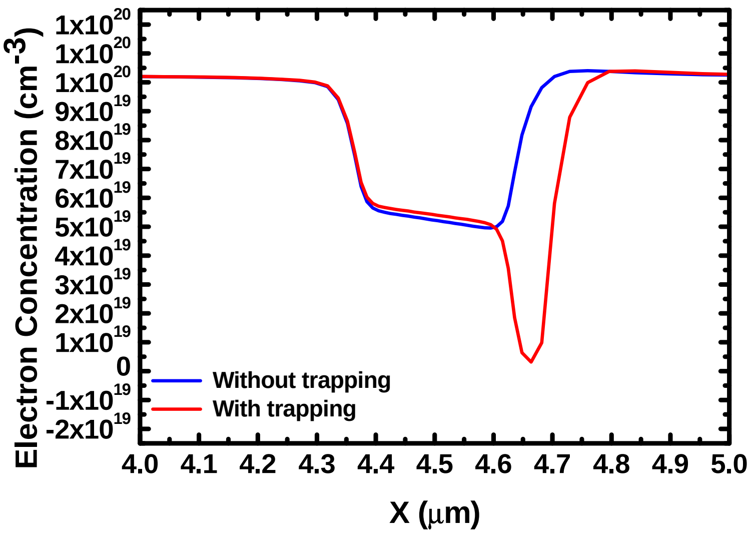


Figure 3.1.8: Electron concentration in the channel region at $5V$ with (Red) and without (Blue) trapped charge definition in the gate-drain region.

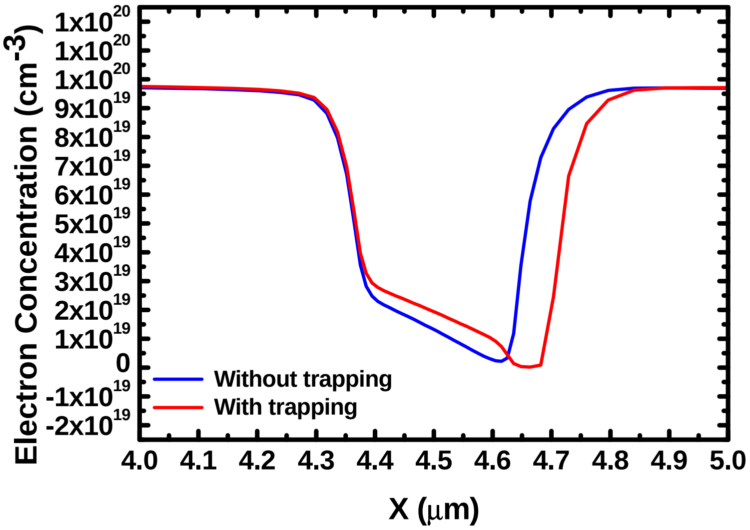


Figure 3.1.9: Electron concentration in the channel region at 13V with (Red) and without (Blue) trapped charge definition in the gate-drain region.

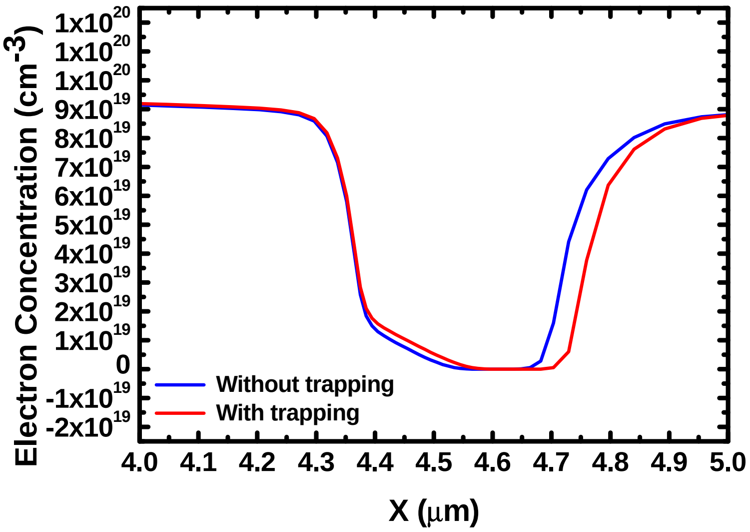


Figure 3.1.10: Electron concentration in the channel region at 25V with (Red) and without (Blue) trapped charge definition in the gate-drain region.

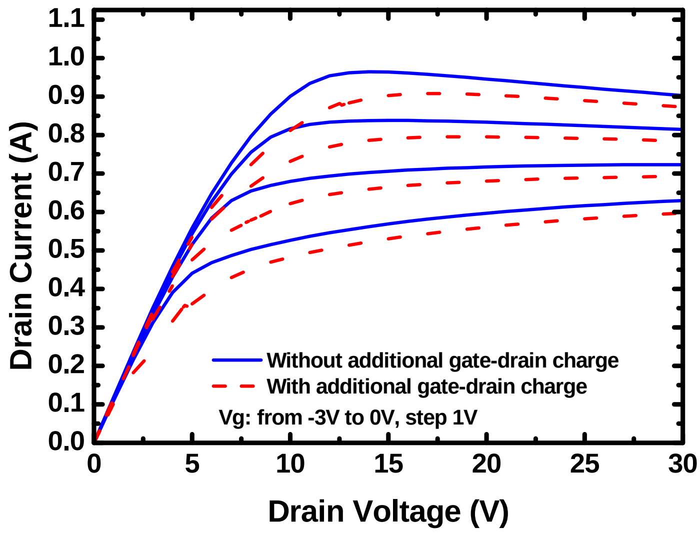


Figure 3.1.11: Output characteristics of the 2D simulated device with (broken lines) and without (solid lines) defining extra charge carriers in the gate-drain region on the surface of the barrier layer.

The output characteristics of the device are shown in Fig. 3.1.11. The solid lines show the output characteristics of the simulated device under normal working condition at different gate voltage values and the broken lines show output characteristics under the same biasing conditions after the fixed amount of charge is defined in the gate-drain region. It is interesting to see that the current collapse behavior shown in the 2D simulation is similar to that obtained from experimental measurements of real devices that have been put under stress. Note the higher current reduction at the knee region of the output characteristics.

3.1.2 Gradual Virtual and main gate saturation

In the gradual saturation of the virtual and main gate approach, it is assumed that a saturation of electron velocity is assumed to start at the drain of the virtual gate. With application of further drain voltage, the saturation point moves towards the drain of the main gate [23]. The current is assumed to be continuous under the main and the virtual gates. This is expressed as

$$I_{ds,main}(V_s, V_g, V_{int}) = I_{ds,Vir}(V_{int}, V_{VG}, V_d). \tag{3.1.1}$$

Equation (3.1.1) states that the current under the main gate that is a function of the voltage at the source, the voltage at the main gate and the voltage at the end of the main gate on the drain side should be the same as the current under the virtual gate which is a function of the voltage at the end of the main gate, as its source, the virtual gate voltage and the drain voltage applied to the device, as long as current continuity is assumed under each gate. In (3.1.1), the new internal node voltage, V_{int}, at the drain of the main gate, and at the source of the virtual gate, and the virtual gate voltage value, V_{VG}, are the two unknowns. In the simplest case, the virtual gate voltage is set in proportion with the amount of charge carriers accumulated and in such cases it is used as a fitting parameter that is adjusted to best fit measurement data. Thus, the only unknown, V_{int}, can be calculated easily using the core drain current model given in (2.6.6) by sweeping the drain voltage values. The current under each gate should be calculated in such a manner until the saturation of the virtual gate is reached. This operating regime can be characterized by calculating the saturation voltage.

After the start of saturation at the region under the virtual gate, the length of the virtual gate length will not remain intact anymore since the saturation point continues to move towards the source of the virtual gate (or towards the drain of the main gate). Therefore, for (3.1.1) still to hold the appropriate modification of the length of the virtual gate region used in the right hand side of the equation should be made. The modified length of the channel under the virtual gate is calculated as

$$l_{2,mod} = l_2 - \Delta l_2. \tag{3.1.2}$$

The length of the depleted region, Δl_2, can be calculated using the expression shown later in (3.1.5). Once again, the current across each gate should be calculated as long as the depletion region under the virtual gate, Δl_2, does not exceed the length of the virtual gate length, l_2. When the drain voltage is increased continuously, finally the whole length of the virtual gate will be depleted and the saturation point reaches the drain end of the main gate. After this point the virtual gate (virtual transistor) will be treated as a simple voltage drop in the gate-drain region in series with the gate-drain region access resistance. This indicates the commencement of saturation under the main gate. The voltage at which this occurs is taken as the new saturation voltage of the main gate. This new saturation voltage of the main transistor can be calculated as

$$V_{sat} = V_{sat,Vir} + V_{dep} \tag{3.1.3}$$

where V_{dep} is the voltage drop across the full length of the virtual gate. Here, it is calculated using the expressing derived to calculate a voltage drop at a point in a depleted region [19]. Thus,

$$V_{dep} = \lambda_0 E_S sinh\left(\frac{l_2}{\lambda_0}\right). \tag{3.1.4}$$

Equations (3.1.3) and (3.1.4) utilize the great potential of the virtual gate modeling approach. They enable to reproduce the shift in saturation point, observed after a DC stress, of the main gate, in comparison with the saturation point before stress. Moreover, the saturation shift, V_{dep}, is calculated using the appropriate physical factors that determine the level of the saturation point shift. After the saturation of the region under the main gate is reached a further increase in voltage will once again move the depletion region into the main gate region towards the source. This depletion region extension will reduce the length of the channel under the main gate. The modified length of the channel under the main gate is calculated as $L - \Delta L$. The length of the depleted region can be calculated from the expression of voltage drop in a depleted region, (3.1.4), as

$$\Delta L = asinh\left(\frac{V_{int} - V_{sat}}{\lambda E_S}\right)\lambda_0. \tag{3.1.5}$$

Note that (3.1.5) is also used to calculate Δl_2 using the appropriate drain and saturation voltages. The gradual saturation, of first the virtual gate and then the main gate, is illustrated in Fig. 3.1.12. Fig. 3.1.12(a) shows the status of the channels under each gate and the values of the voltages at each terminal before the start of saturation. The beginning of saturation just at the drain end of the virtual gate is shown in Fig. 3.1.12(b). Fig. 3.1.12(c) shows the movement of the saturation point towards the source of the virtual gate at an arbitrary point when the drain voltage is further increased. The depletion region in the virtual gate region increases in such a manner and finally the saturation point reaches at the drain of the main gate as shown in Fig. 3.1.12(d).

3.2 A DC Equivalent Circuit Including the Virtual-gate

In (3.1.1) it was assumed that the current under each gate is the same, the current continuity assumption. In numerical solvers such as MATLAB, (3.1.1) can be solved numerically using a certain iterative algorithm. This, however, is not an attractive alternative as far as compact modeling is concerned.

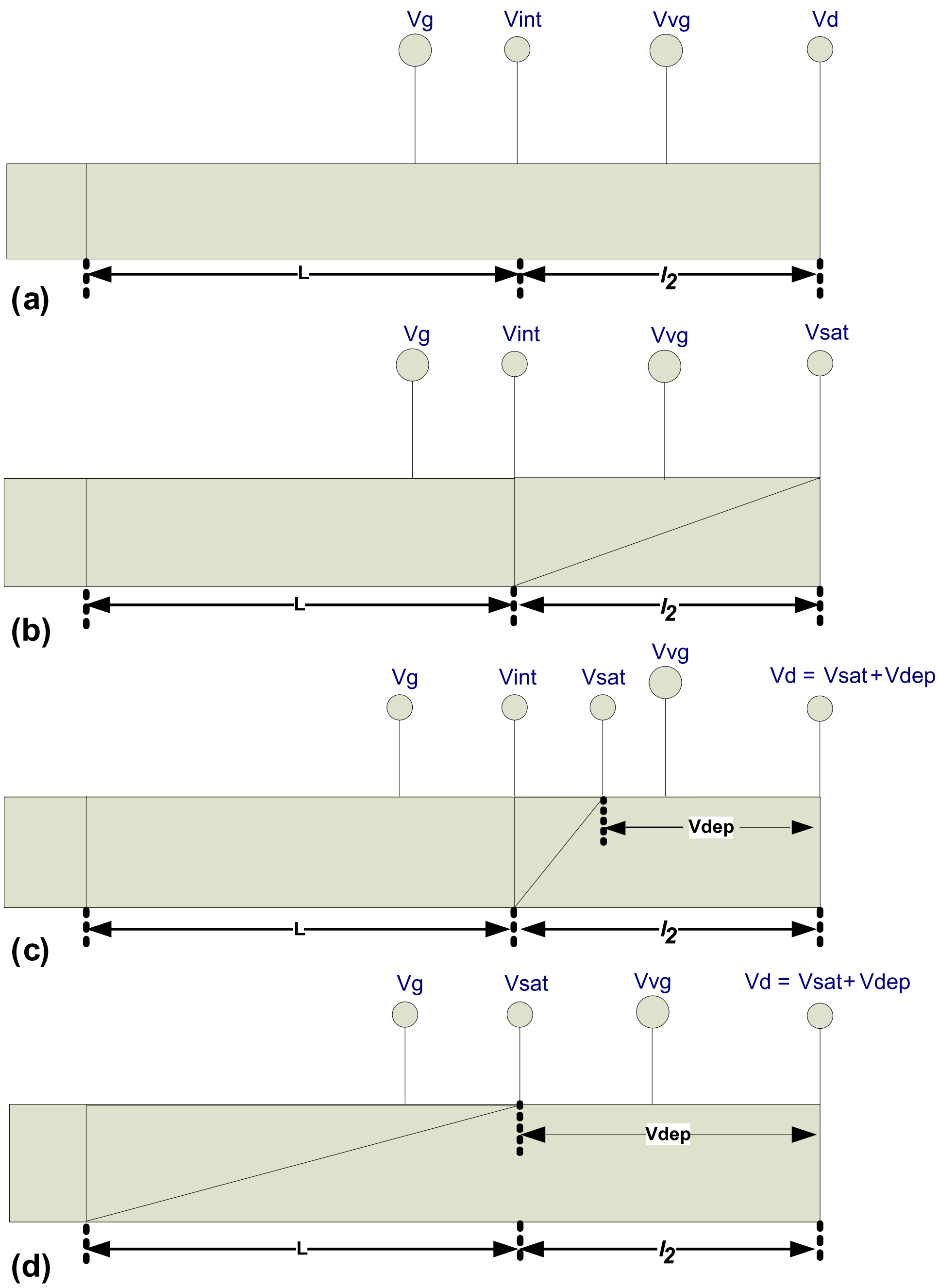


Figure 3.1.12: Gradual saturation of the virtual gate (virtual transistor) and the channel under the main gate.

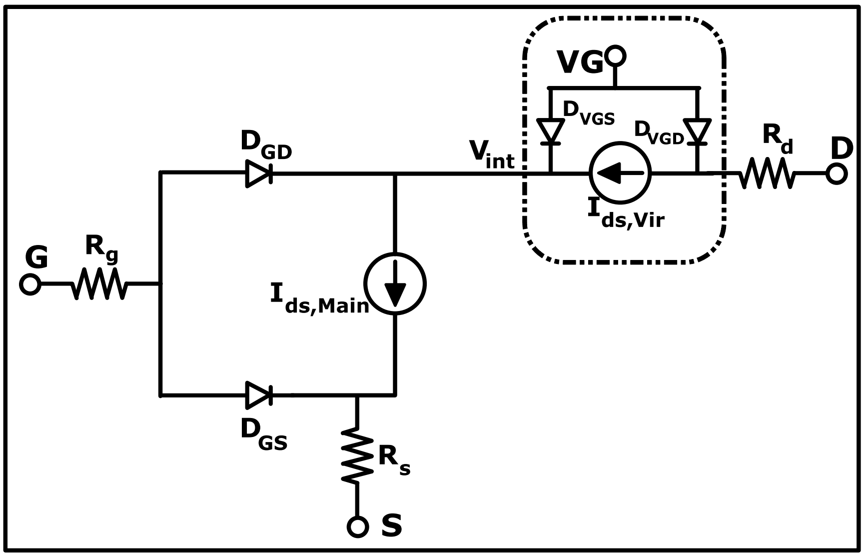


Figure 3.2.1: A large signal equivalent circuit for a HEMT device including a virtual gate.

To utilize the virtual gate modeling approach in circuit simulators, an equivalent circuit, shown in Fig. 3.2.1, is used here. The virtual gate is incorporated in the gate drain region via two diodes similarly to the main gate. It is now considered as the fourth port of the normally three terminal device. This equivalent circuit lay out is implemented using the standard compact modeling language, Verilog-A. This enables easy implementation of the model in available commercial circuit simulators. Here, the circuit simulator Advanced Design Systems (ADS) from Agilent is used.

The simple circuit layout in Fig. 3.2.2 shows the set up used to apply the model in the circuit simulator. The four ports of the transistor symbol represent the four terminals of the equivalent circuit given in Fig. 3.2.1. A dedicated fixed bias is applied to the virtual gate. As mentioned earlier,the bias applied to the virtual gate is adjusted to fit measurement data. However, if analytical equations that relate the virtual gate voltage with the appropriate factors are formulated, the accuracy of the model can be greatly improved. Some of the factors that should be considered while formulating analytical expression of the virtual gate voltage may include the value of the maximum drain voltage

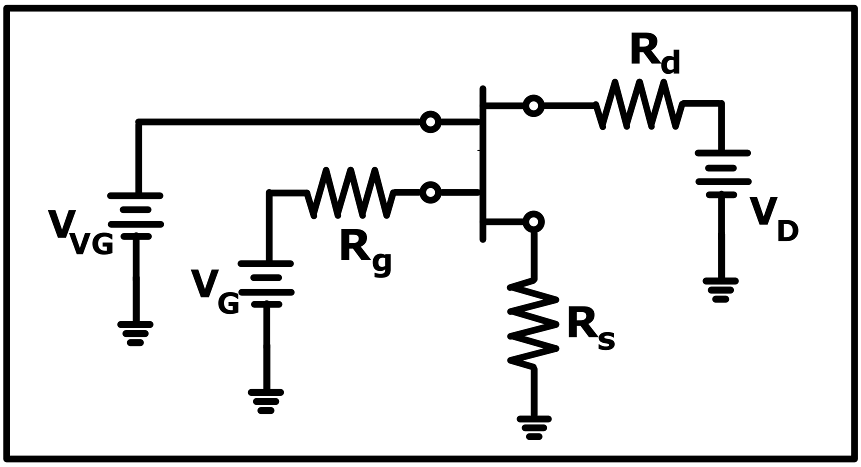


Figure 3.2.2: A four port transistor scheme is used in the circuit simulator with the fourth port being the virtual gate terminal where a negative bias proportional to the surface trapped charge carriers is applied.

applied and the duration of a stress. If one has to use analytically calculated value of the virtual gate, it only suffice to connect the output of the equation solver to the virtual gate port. In the mean time, the fixed virtual gate voltage value can be tuned within a reasonable range of values.

3.3 Results

The virtual gate modeling approach presented in sections 3.2 and 3.3 has been used to reproduce current collapse effects observed in typical HEMT devices. Two devices with different sizes that has been put into different levels of stress are considered. The first one has a gate length of $0.25\mu m$ and a total width of $0.25mm$ [23] and the second one has a $1\mu m$ gate length and $0.15mm$ width [5]. First the standard output characteristics of the devices before the application of any stress are simulated using the drain current model given in (2.6.6). This is done in order to assure the validity of the drain current model for these devices before applying the virtual gate model based on it. Fig. 3.3.1

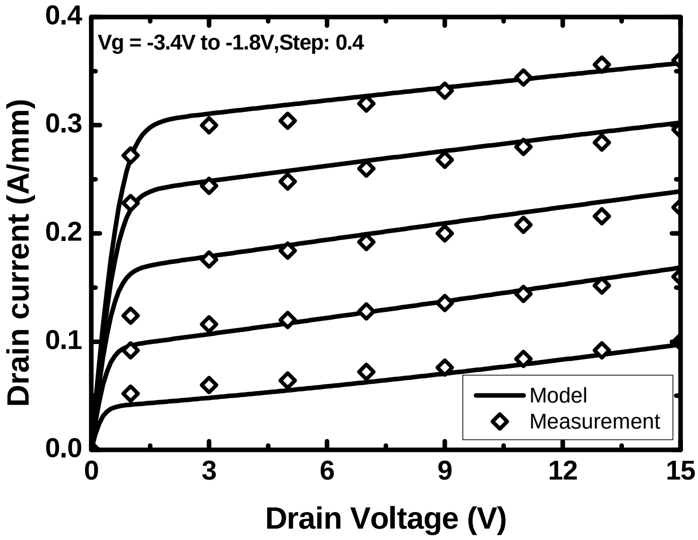


Figure 3.3.1: Output characteristics of a $0.25\mu m$ gate length device, measured (symbols) and modeled (solid lines) before stress, for V_g values of $-3.4V$ to $-1.8V$ with $0.4V$ step from bottom to top, data taken from [23].

and Fig. (3.3.2) show the good agreement between the current model and measured output characteristics of the devices. In Fig. (3.3.2) self-heating effect is observed in the output characteristics of the device. This is because the device is measured up to higher maximum drain voltages, $30V$ in this case. Since the effect of self-heating is incorporated in the core current model, as described in section 2.7, it was possible to reproduce the self-heating effect exhibited by the device.

The current collapse model is applied to reproduce the I_d-V_d characteristics of the device with $0.25\mu m$ gate length after stress. The $I-V$ curves in Fig. (3.3.3) are measured at the same biasing as those given in Fig. (3.3.1). It is shown that there is a considerable reduction of the drain current, specially in the knee region. The virtual gate model has reproduced the current collapse very well.

The other device considered here, the $1\mu m$ gate length device, has been put into various

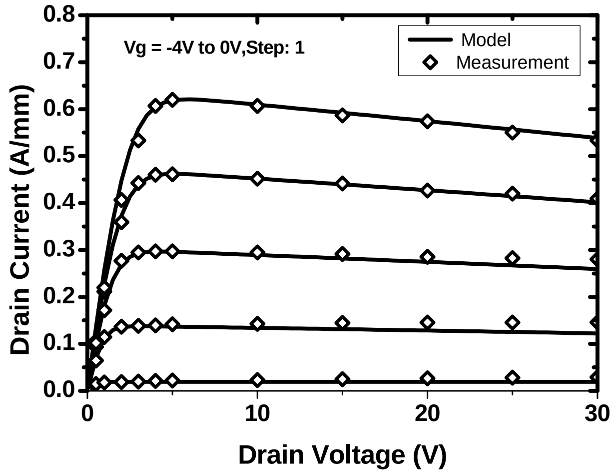


Figure 3.3.2: Output characteristics of a $1\mu m$ gate length device, measured (symbols) and modeled (solid lines) before stress, for V_g values of $-4V$ to $0V$ with $1V$ step from bottom to top, data taken from [5].

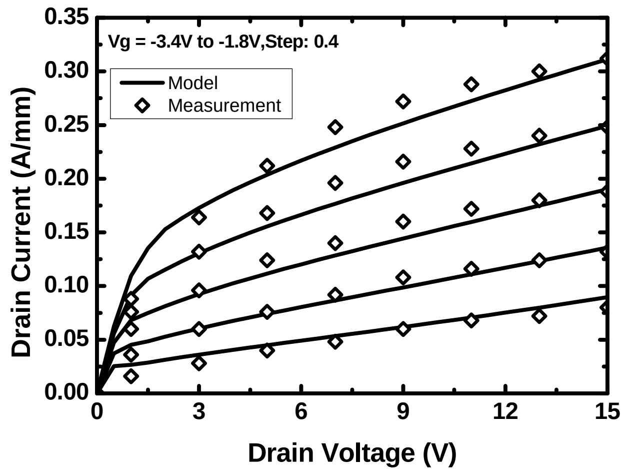


Figure 3.3.3: Measured (symbols) and modeled (solid lines) output characteristics after stress, current collapse, of a $0.25\mu m$ gate length device for V_g values from $-3.4V$ to $-1.8V$ with $0.4V$ step from bottom to top, data taken from [23].

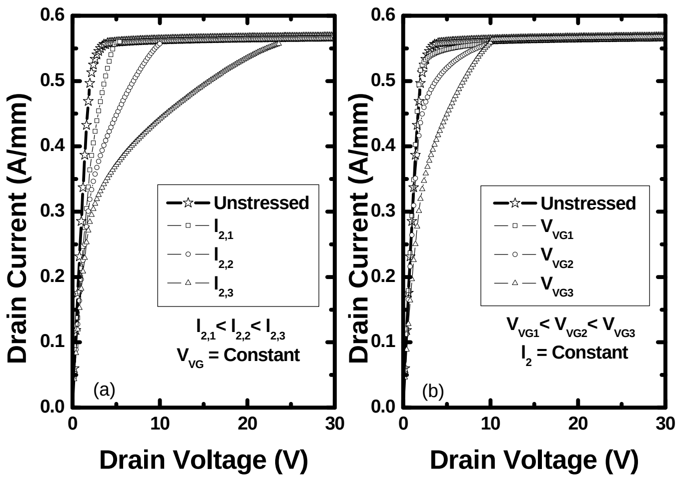


Figure 3.3.4: The significances of the virtual gate length and voltage parameters on the performance of the model when one is varied while keeping the other fixed.

levels of stress. Basically, the maximum voltage and the duration of the stress applied on the device have been varied to identify the impact of each factor on the current collapse the device exhibits. The device was put under four, eight and sixteen hours of stress with a maximum drain voltage of $30V$. The output characteristics of the device are measured after each stress where various levels of current collapse are observed. Here more focus is given on how to give a similar behavior to the virtual gate model.

The two main parameters of the virtual gate model, the length and the voltage of the virtual gate, are considered to enable the model to reproduce different levels of current collapse due to different intensity levels of stresses applied to a device. Fig. (3.3.4) shows the analysis carried out to determine the role of the virtual gate length and voltage parameters in the overall performance of the model.

As shown in Fig. (3.3.4)(a), the length of the virtual gate determines the shift in the saturation point of the main gate. This is exclusively indicated during the calculation of the new saturation voltage, based on the voltage drop across the depleted region which is dependent on the length of the virtual gate. The different levels of current compression and the corresponding saturation point shifts are obtained by varying the length of the virtual gate for a fixed virtual gate voltage. As the length of the virtual gate is increased the part of the knee region affected by the collapse extends more into the saturation region, a larger saturation point shift.

Fig. (3.3.4)(b) shows that the virtual gate voltage value does not take part in determining the saturation point shift as in the case of the virtual gate length. All the current compression levels shown, obtained by varying the virtual gate voltage value while keeping the virtual gate length fixed, have the same saturation point. However, the levels current compressions are different. This shows that, in the model, the value of the virtual gate voltage is used to determine the severity of the current collapse in the affected region. The value of the virtual gate voltage represents the trapped charge carrier concentration in the gate-drain region that corresponds to the electric field that the charge carriers, in the 2DEG under it, experience. Higher trapped charge carrier concentration results in higher depletion of the 2DEG under which in turn results in a stronger current compression and is represented by a larger negative virtual gate voltage in the model.

The two boundaries of the current collapse in the knee region are shown to be controlled by the voltage and length of the virtual gate of the model as shown in Fig. (3.3.4) (a) and (b). Therefore, the model can be used to reproduce various levels of current compression exhibited by a device while being under different levels of stress if the appropriate values of the virtual gate voltage and length are selected carefully. Fig. (3.3.5) shows the output characteristics of the device with a $1\mu m$ gate length measured after the three different levels of stress are applied on it along with the model [5]. The model was able to reproduce the various levels of current collapse with the appropriate selection of core current and virtual gate model parameters. The set of parameters used to model the devices are given in Table 3.1.

Table 3.1: List of parameters used to model the output characteristics of two devices with gate length of $0.25\mu m$ and $1\mu m$ before and after stress.

Parameter	Parameter description	$0.25\mu m$ Device	$1\mu m$ Device
$L(\mu m)$	Channel length	0.25	1
$V_{off}(V)$	Cut-off voltage	-3.6	-4.2
$W(mm)$	Gate width	0.25	0.15
$d(nm)$	Thickness of barrier layer	17.5	25
$v_{sat}(m/s)$	Saturation velocity	$1.19e5$	$1.19e5$
$\mu_0(m^2/Vs)$	Low field mobility	0.1	0.9
$\mu(m^2/Vs)$	Saturation mobility	0.087	0.079
$\lambda_0(nm)$	Characteristics length of saturation region	45	43
$l_2(nm)$	Virtual gate length	36	41(Stress1) 45(Stress2) 47(Stress3)
$V_{VG}(V)$	Virtual gate voltage	-3.42	-4.2(Stress1) -4.3(Stress2) -4.5(Stress3)

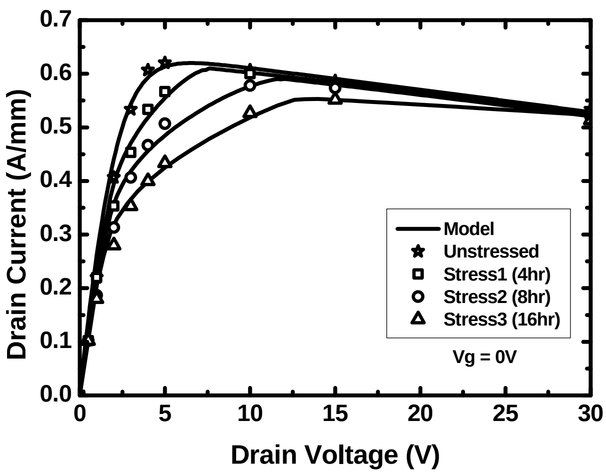


Figure 3.3.5: Measured (symbols) and modeled (solid lines) output characteristics of a $1\mu m$ gate length device. The various levels of current compressions correspond to the various hours of stress at a maximum drain voltage of $30V$, data taken from [5].

3.4 Conclusion

The modeling of permanent or semi-permanent current collapse effect observed in AlGaN/GaN HEMT devices is targeted in this chapter. The effect is observed on devices that have been put under stress by applying high drain voltage for a certain period of time. Experimental and theoretical results that show that entrapment of charge carriers in the gate-drain region to be the cause of current collapse are used as the basis of the model. This assumption, virtual gate modeling approach, is further validated using 2D device simulation with and without additional charge carriers in the gate-drain region where the device showed output characteristics that are very similar to those shown by a device that is said to have undergone current collapse.

An equivalent circuit that incorporate the virtual gate in the gate-drain region is implemented in a circuit simulator. The drain current model developed earlier is used to determine the continuous current under the main and the virtual gates. Moreover, the gradual saturation of the channels under each gate is also considered. The overall model formulation and implementation paves the way to a universally applicable integration of a controlled virtual transistor with various drain current models in circuit simulators. In the absence of current collapse, the virtual gate can be simply ' turned off ' to simulate the ordinary $I-V$ characteristics of a device.

The model is made to capture the intensity and extent of the current collapse using the two main parameters of the virtual gate model, the virtual gate voltage and length. These two parameters are adjusted in accordance with the severity of current collapse shown by a device. The model has reproduced different levels of current compressions exhibited by various devices.

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Chapter 4

Nonlinearity Modeling of AlGaAs/GaAs pHEMTs

In this chapter nonlinearity modeling of 4×50 AlGaAs/GaAs pHEMT devices with a gate length of $0.25\mu m$ from RFMD(UK) (FD25) is presented. Previously, harmonic balance (HB) simulation of the devices had been done using the Angelov large signal FET model. However, here the Volterra series analysis is used.

4.1 Introduction

Modeling of nonlinearities and intermodulation distortion (IMD) is critical in the design and simulation of communication circuits [1, 2, 3, 4]. When a device is operated near the cut-off region for reduced current applications, such as receiver front-end design for wireless communication, analysis and modeling of intermodulation distortion is very important [5]. Harmonic balance simulation and Volterra series analysis are widely used in the analysis of frequency domain nonlinearity of multiple frequency driven circuits

[6, 7, 8].

Volterra series analysis enables to perform accurate intermodulation distortion simulations [9, 10, 11, 12, 13]. In Volterra series non-linearity analysis a FET is represented by an equivalent circuit that contains nonlinear elements [14, 15]. The transconductance, conductance and the gate-source capacitance are identified to be the main sources of device nonlinearity and thus are considered as nonlinear components. Volterra series analysis is known to be a common method when it comes to modeling the weak nonlinearities of a device. In this approach, a nonlinear element will be represented by a truncated Taylor series of a certain order. A coefficient of a term of the Taylor series is directly related to a corresponding higher order derivative of a nonlinear function that expresses a nonlinear component. Therefore, it is a common practice to obtain the coefficients of the Taylor series through successive derivation of the nonlinear function up to the desired order.

The extraction of Taylor series coefficients is the most important part of Volterra series analysis. The method of extracting coefficients of the polynomial function as the derivatives of a nonlinear function loses accuracy as the order of the polynomial is increased. Other relatively direct methods of extracting the coefficients are also available [16, 17, 18]. The extraction technique considered here uses both linear small signal and non linear harmonic measurements to obtain the coefficients of Volterra Series [14]. First, the basics of Volterra series analysis are discussed in section 4.2. A quick review of the extraction method is presented in section 4.3. Important issues related to the linear and harmonic measurements and the corresponding cares that should be taken are then discussed in section 4.4 followed by simulation results in section 4.5. Finally, a conclusion is given in section 5.5.

4.2 Voltera Series Analysis

In Volterra series analysis nonlinear circuit elements are expressed by a Taylor series expansion of their current-voltage $I-V$ and charge-voltage $Q-V$ characteristics in the vicinity of their dc bias voltages [19]. In the equivalent circuit of FET devices three components have been identified to be the main sources of the nonlinearity in the device. These are

1. the nonlinear current source (the transconductance),
2. the nonlinear drain-source resistance (the conductance) and
3. the gate-source capacitance.

The equivalent circuit of a FET that includes these nonlinear elements is shown in Fig. 4.2.1.

For a Volterra analysis, the Taylor series expansion at least up to third order will be used. Thus, the nonlinear current is given as

$$i_{ds} = g_m v_g + g_d v_d + g_{m1} v_g^2 + g_{d1} v_d^2 + g_{m2} v_g^3 + g_{d2} v_d^3 + \dots \tag{4.2.1}$$

Similarly, the $Q-V$ characteristics of the gate-to-source capacitance are given as

$$q_g = c_1 v_g + c_2 v_g^2 + c_3 v_g^3 \tag{4.2.2}$$

where

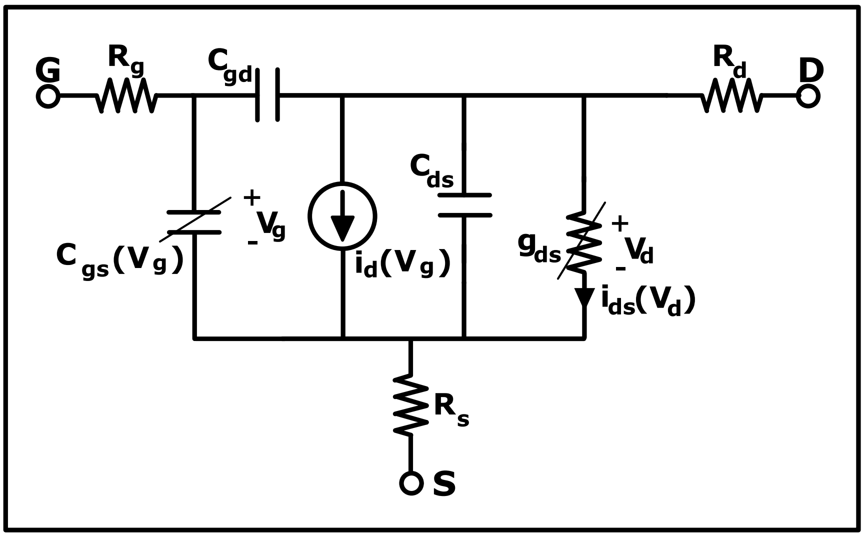

Figure 4.2.1: FET equivalent circuit containing the nonlinear elements.

$$
\begin{aligned}
c_1 &= \frac{dQ_g}{dV_g} \\
c_2 &= \frac{1}{2}\frac{d^2Q_g}{dV_g^2} \\
c_3 &= \frac{1}{6}\frac{d^3Q_g}{dV_g^3}.
\end{aligned}
\tag{4.2.3}
$$

Q_g is the gate charge and c_1 is equivalent to the linear gate-source capacitance, C_{gs}, in linearized equivalent circuit and the gate charge is expressed only using the first term of (4.2.2).

After all the linear components of the nonlinear FET equivalent circuit are determined, the next task is the modeling of these components. The main task in modeling the nonlinear components is to determine the coefficients of the polynomials. As indicated earlier, there are already a number of methodologies to extract the Taylor series coefficients, the one used here is discussed in the next section.

4.3 Coefficient Extraction Methodology Overveiw

The technique used to obtain the Volterra series coefficients involves the use of the fundamental and higher order output current definitions and linear S-parameter and nonlinear harmonic measurements and is briefly described here [14].

Nonlinear Current Source

The extraction of the Volterra series coefficients that is used to model the nonlinearity of the transconductance is mainly based on the definition of nonlinear harmonic components of a current. The fundamental, 2^{nd} harmonic and 3^{rd} harmonic currents are given by

$$I_1 = \frac{g_m V_{gs}}{1 + g_1 R_s} \tag{4.3.1}$$

$$I_2 = \frac{g_{m1}(1 - g_m R_s)V_{gs}^2}{2(1 + g_m R_s)^2} \tag{4.3.2}$$

$$I_3 = \frac{(g_{m1} - 2g_{m1}^2 R_s)(1 - g_1 R_s)V_{gs}^2}{4(1 + g_{m1} R_s)^2} \tag{4.3.3}$$

where V_{gs} is the magnitude of $v_{gs}(t)$, the signal applied to the device, $v_{gs}(t) = V_{gs} cos(\omega t)$. The available power of the signal source is then

$$P_a = \frac{V_{gs}^2}{8R_{in}}. \tag{4.3.4}$$

The ratio of the second harmonic output power to the fundamental output power can be written as

$$IM_2 = \frac{P_2}{P_1} = \frac{I_2^2 R}{I_1^2 R} = \frac{I_2^2}{I_1^2}. \tag{4.3.5}$$

Using the values of I_1 and I_2 from (4.3.1) and (4.3.2) respectively and substituting for V_{gs} from (4.3.4), IM_2 can be written as

$$IM_2 = \frac{2g_{m1}^2 R_{in}(1 + g_m R_s)^2 P_a}{g_m^2 (1 + g_m R_s)^2}. \tag{4.3.6}$$

Similarly, the ratio of the third harmonic output power to the fundamental output power is obtained as

$$IM_3 = \left[\frac{2(g_{m2} - 2g_{m1}^2 R_s)(1 - g_m R_s)R_{in}}{g_m (1 + g_m R_s)^2}\right]^2 P_a^2. \tag{4.3.7}$$

Once the power ratios are obtained, the coefficients can be calculated in such a way that

1. the first coefficient is determined using DC or RF measurements,

2. the ratio of second harmonics power to the fundamental harmonic power can be read from a spectrum analyzer and g_{m1} will be solved from (4.3.5) and

3. the ratio of third harmonics power to the fundamental harmonic power can be read from a spectrum analyzer and g_{m2} will be solved from (4.3.7).

After solving for g_{m1} and g_{m2} the analytical expressions of the coefficients are given as

$$g_m = \frac{|y_{21}|\, g_{d1}\, (R_s + R_d + 1/g_{d1})}{1 - |y_{21}|\, R_s} \tag{4.3.8}$$

$$g_{m1} = g_m (1 + g_m C_R R_s)^2 \sqrt{IM_2/2R_{in}P_{in}} \tag{4.3.9}$$

$$g_{m2} = \frac{2g_{m1}^2 C_R R_s}{1 + g_m C_R R_s} \pm \frac{g_m (1 + g_m C_R R_s)^2 \sqrt{IM_3}}{2R_{in}P_{in}} \tag{4.3.10}$$

where

$$C_R = \frac{1}{g_d\, (R_L + R_d + R_s + 1/g_d)}. \tag{4.3.11}$$

The parameters used in the expression given from (4.3.8) to (4.3.10) can be obtained from linear and nonlinear measurements. The parameters y_{21}, R_s, R_d and g_d can be obtained from S-parameter measurements and IM_2 and IM_3 can be obtained from harmonic measurements carried out at low frequencies.

Nonlinear Gate-source Capacitance

The higher order derivatives of the capacitance can be calculated numerically by extracting C_{gs} at a number of gate voltages. Alternatively, this gate-source capacitance can also be modeled as a classical Shottky-barrier depletion capacitance. Thus,

$$C_{gs}(V_{gs}) = \frac{C_{gs0}}{\sqrt{1 - {}^{V_{gs}}/_{V_{bi}}}} \tag{4.3.12}$$

$$c_2 = \frac{mC_{gs0}}{2V_{bi}\left(1 - {}^{V_{gs}}/_{V_{bi}}\right)^{m+1}} \tag{4.3.13}$$

$$c_3 = \frac{m(m+1)C_{gs0}}{6V_{bi}^2\left(1 - {}^{V_{gs}}/_{V_{bi}}\right)^{m+1}} \tag{4.3.14}$$

where V_{bi} is the built-in voltage of the junction and $m = 0.5$ for the case of Shottky contact. The value of the small signal gate-source capacitance, can be extracted from S-parameter measurements at the bias of interest. The zero voltage capacitance value, is then calculated using (4.3.12). The first and second derivatives of the capacitance can be calculated using the analytical expressions given in (4.3.13) and (4.3.14) respectively. The gate-source capacitance contribution to the overall nonlinearity of the device is very less as compared to the transconductance [20].

Nonlinear Conductance

The values of the drain source conductance at a specific gate voltage and a number of drain voltages is extracted from the small signal measurements at low frequency. The second and third order derivatives of these conductances are then obtained simply as numerical derivatives.

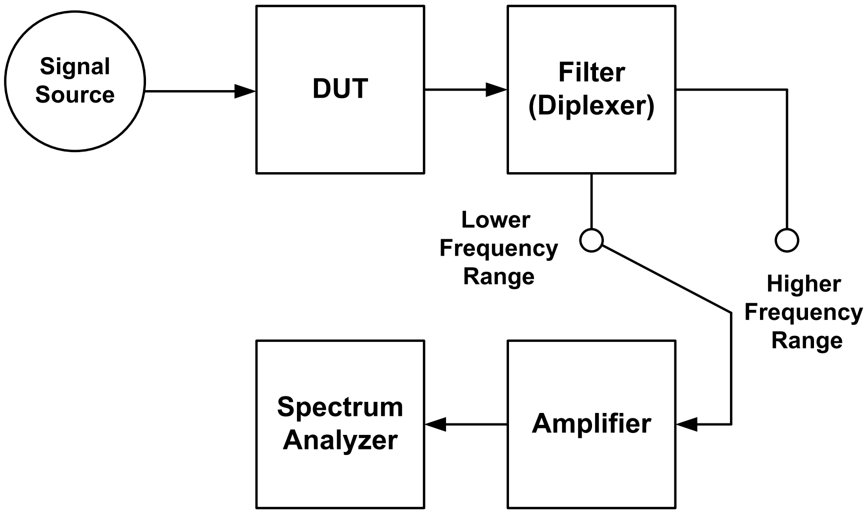

Figure 4.4.1: Harmonic measurement set up for the fundamental and the higher order output power levels.

4.4 Harmonic Measurement Issues

A harmonic measurement has been carried out using the measurement set-up outlined in Fig. 4.4.1. A low level input power is applied from the signal generator. It is necessary to keep this input drive as low as possible so that one can stay in the well-behaved, weak nonlinearity, region of the device. In this region the fundamental, the second and the third harmonic outputs have the ideal slopes, which are 1, 2 and 3 respectively.

While the input drive is made very low in attempt to stay in the well behaved region, the main problem faced will be the difficulty of reading the very small third order harmonic outputs. An amplifier, as shown in the measurement set up, can be used to increase these low level third order output powers. However, the stronger fundamental signal can distort the output from the amplifier. The diplexer can be used to separate this strong fundamental from the weak harmonic power outputs and the amplified fundamental and harmonic outputs can be recorded separately. The gain of the amplifier should be constant throughout the whole frequency range, otherwise the gain variations should be

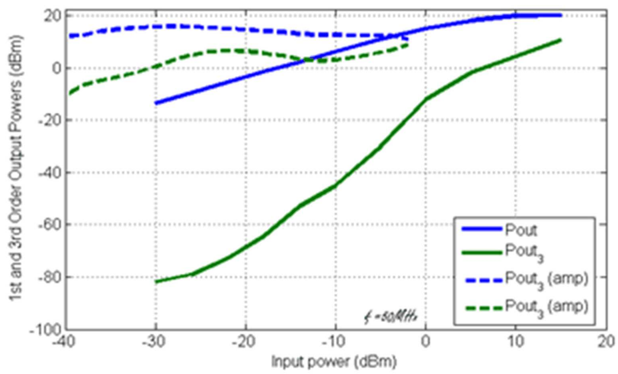

Figure 4.4.2: Fundamental and third order output power levels measured with (dashed lines) and without (solid lines) an amplifier at the same bias point without using a diplexer

accounted for and the recorded data should be corrected.

Fig. 4.4.2 shows a comparison of two measurements carried out with and without an amplifier. The first two doted pairs of lines which are the fundamental and the third harmonic powers measured using the amplifier clearly show the effect of the fundamental signal and what are being measured are not actually the pure harmonics of the device. The two solid lines that show the actual fundamental and third order harmonics were measured without the amplifier. However, it difficult to read the higher order harmonics without amplifying when the input drive is very small ($< -30dBm$). For example, the third order harmonic power in Fig. 2 starts to curl-off at the lower input levels where the readings, very close to the noise floor of the spectrum analyzer, have to be taken.

A possible alternative approach that can be used to read the harmonic power levels at very low input drives, when an amplifier and a diplexer are not being used in the measurement set up, is indicated in Fig. 4.4.3. Fig. 4.4.3 shows the extrapolation of each measurement point to a lower input drive of interest. The extrapolated values of each point can then be plotted against the input drive. From this plot it is possible to differentiate the

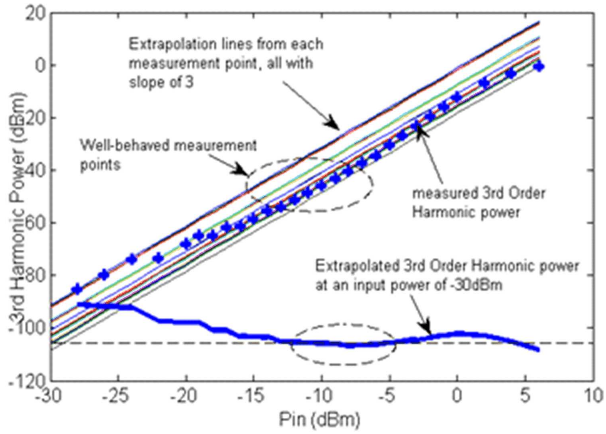

Figure 4.4.3: Extrapolation of each measurement point of the third order output power to a lower input level. The extrapolation of the well-behaved region points should be used to get more accurate power ratios.

extrapolations of the points from well-behaved regions. These extrapolation points are identified as a set of lower straight lines that resulted from the constant value of the slope of the well-behaved region.

A set of power ratios can be calculated using the harmonic power readings at different input levels. The best set of harmonic power ratios that led to more accurate coefficients are calculated using power outputs where the slops are well-behaved. In this regard, it is important to notice the analogy with finding the set of input power drives that give the highest third order intermodulation output power (OIP3).

4.5 Simulation Results

The nonlinear model can be implemented in circuit simulators such as Microwave office from AWR or ADS where the extracted Volterra coefficients are used in a two tone harmonic balance simulations. Microwave Office provides a dedicated set of Volterra

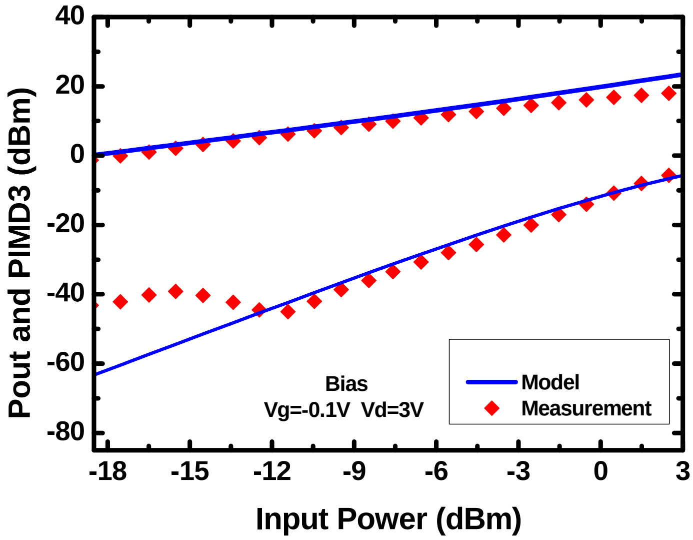

Figure 4.5.1: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.1V$ and $V_d = 3V$.

Series components. It contains models for the nonlinear current source, the nonlinear drain-source resistance and the nonlinear gate-source capacitance. These models are available so that they can be used in any circuit setup independently. In addition, it also provides one complete Volterra-FET model component which combines all of the nonlinear components into one single FET model. The model can also be implemented in ADS using a similar approach. Symbolically defined devices (SDD) can be used to define each nonlinear component. More conveniently, it is also possible to use the nonlinear voltage controlled current source and the nonlinear capacitance components provided in the Equation-Based Nonlinear category of ADS. These nonlinear components can be then connected with the normal lumped element components of the equivalent circuit to form the full nonlinear equivalent circuit.

Here the nonlinear components are defined as SDDs in ADS and a two tone power sweep is carried out at different bias points. The set of coefficients extracted for the nonlinear

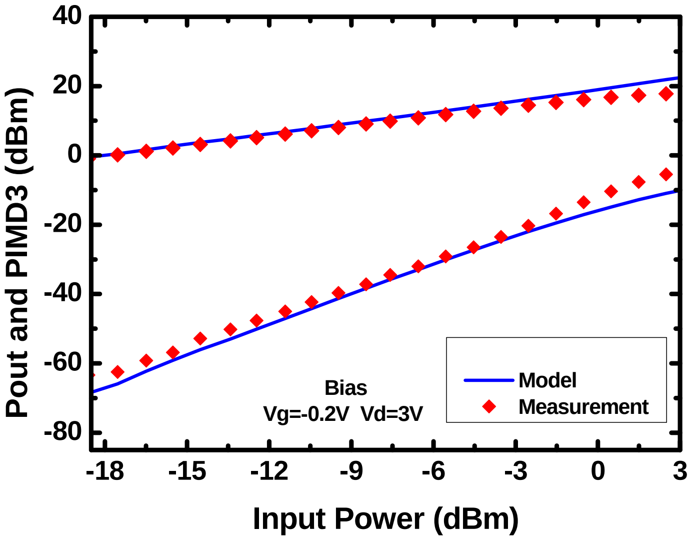

Figure 4.5.2: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.2V$ and $V_d = 3V$.

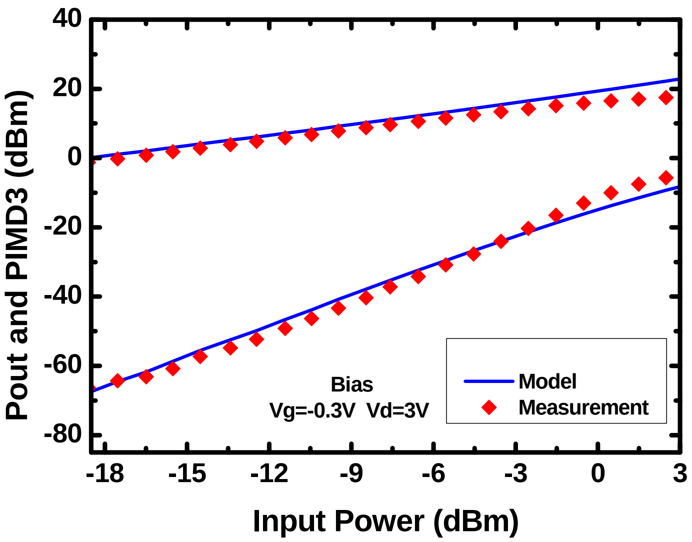

Figure 4.5.3: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.3V$ and $V_d = 3V$.

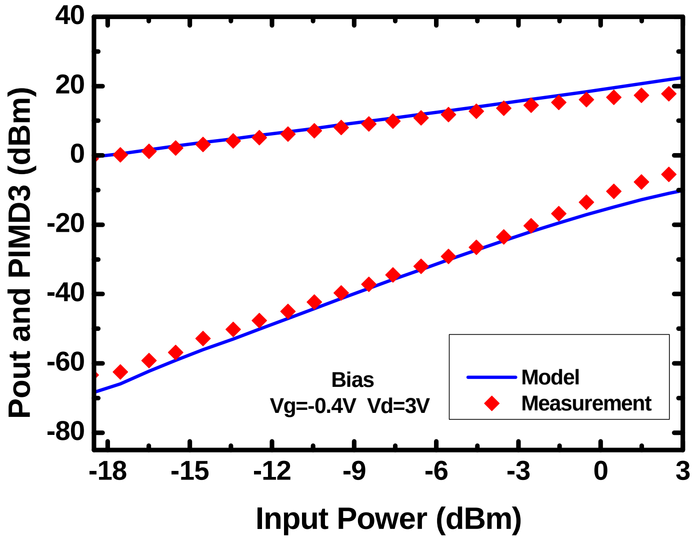

Figure 4.5.4: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.4V$ and $V_d = 3V$.

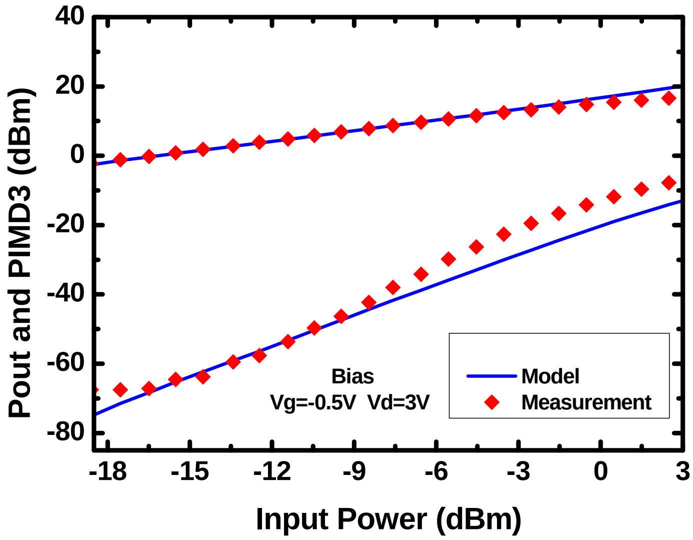

Figure 4.5.5: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.5V$ and $V_d = 3V$.

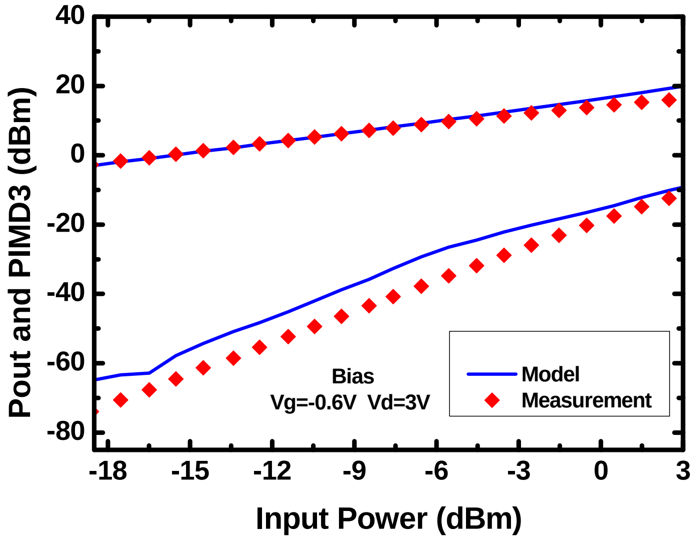

Figure 4.5.6: Measured (symbols) and modeled (solid lines) fundamental and third order IMD power output levels at $V_g = -0.6V$ and $V_d = 3V$.

Table 4.1: Volterra series coefficients extracted at a number of gate voltage biases with the drain voltage set at $3V$.

V_g	g_m	g_{m1}	g_{m2}	g_d	g_{d1}	g_{d2}
-0.1	0.1198	-0.0169	-0.02	0.0028	$-5e-4$	$-3e-4$
-0.2	0.1088	0.0016	-0.0229	0.0029	$-4.7e-4$	$-1.4e-3$
-0.3	0.1225	0.0282	-0.0366	0.00303	$-5.9e-4$	$-8.2e-4$
-0.4	0.1019	0.0316	-0.0227	0.00301	$-5.9e-4$	$-8.6e-4$
-0.5	0.0958	0.0315	0.00271	0.00289	$-2.62e-5$	$-1.3e-3$
-0.6	0.0889	0.0451	-0.0209	0.00281	$-9.7e-5$	$6.8e-5$

transconductance and conductances, up to third order, are shown in Table 4.1. Since truncated polynomial approximations such as Volterra series are best to model the weak nonlinearity of a circuit, the simulation of the fundamental and the third order harmonic power was carried out up to the limit of the weak nonlinearity region or before the device is driven into a strong nonlinearity. Fig. 4.5.1 to Fig. 4.5.6 show the comparison between measured and modeled first and third harmonic power outputs. The model is able to reproduce the IMD power levels that are measured in the weak nonlinearity region of the device. When the device is driven into stronger nonlinearity operation region, the discrepancy between measured and modeled IMD power levels increases.

4.6 Conclusion

In this chapter the application of Volterra series analysis to characterize the nonlinearity of commercial pHEMT AlGaAS/GaAs devices from RFMD is presented. In particular, the Taylor series coefficients extraction technique that is used as the base of the nonlinear Volterra components in the circuit simulator Microwave Office from AWR is tested by applying it on these devices. The extraction technique involves the use of both linear S-parameter and non-linear harmonic measurements. The linear S-parameter measurements are used to determine the transconductance in a more straight forward manner. The harmonic measurements are used to calculate harmonic power ratios, the second and third harmonics to that of the first, which are then used to determine the higher order Taylor series coefficients.

Although the harmonic measurements required are simple and direct, the fact that they have to be performed at very low input drives makes them tricky and vulnerable to errors. Care should be taken while reading the third order harmonics. An amplifier can be used to raise the third order harmonic power outputs well above the noise floor and enable a more easier and accurate reading. However, it is important to make sure that the fundamental output power is not affecting the output of the amplifier. A diplexer with two outputs, one for the fundamental and the other for the harmonics, can be used to avoid such erroneous harmonic power output readings. While doing the measurement without a diplexer, the use of an amplifier can also be avoided and the third order harmonic outputs of the very low input drives, which normally curl-off deep into the noise floor, can be determined by extrapolating points from a well behaved region measured at relatively higher input drives.

The nonlinear equivalent circuit is implemented in circuit simulators where the extracted coefficients are used in the Taylor series expressions that are used to model the nonlinear components. The agreements between simulated and measured power sweeps show that the coefficient extraction technique used is viable to model the nonlinearity of these devices. The nonlinear model is able to determine intermodulation power output up to a certain power level. This power level is different at different biases. However, generally, it is the point where the device comes out of its weak nonlinearity and is driven into strongly nonlinear region. This, indeed, is in agreement with the fact that Volterra series nonlinearity modeling approach works best in the weakly nonlinear regions.

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Chapter 5

Conclusion

5.1 Summary

Compact modeling of AlGaN/GaN HEMT devices for circuit simulation entirely based on device physics is discussed. Analytical expressions have been derived for the terminal characteristics. Fundamental electrostatic analysis of the hetero-junction and the 2DEG region are used as the basis of the core drain current and gate charge models. Careful consideration of the 2DEG area is very essential if an accurate physics-based model development is desired.

The expressions that relate the important parameters of the 2DEG region are mainly transcendental due to the inherent interdependence that exist between the parameters. This, indeed, puts a tough challenge in the formulation of analytical relations that can be used to construct compact models. Usually, iterative numerical solving is used to obtain solutions which could result in longer simulation time and convergence issues. This has always been pointed out as the major drawback of physics-based compact models. Otherwise, their high level of accuracy and stability make them desirable. The analytical expressions developed here demonstrate that the undesirable features of such models can be avoided by formulating simple analytical relations using various modeling techniques.

Reasonable assumptions and approximations based on established theoretical and experimental results are one of the important tools that can be used in the formulation of analytical models. However, it is important to make sure that the accuracy of the model is not sacrificed to an unacceptable level while making assumptions and approximations to simplify it. In the formulation of the gate charge and drain current models here, simplifying assumptions and approximation based on justified results were used while keeping the model accuracy as proved by the model validations.

Empirical or physics-based models of non-ideal effects can be incorporated as needed with the core models. In this regard, the main non-ideal effects that arise due to device structure, operating condition and environment are incorporated with the core models. This has made the models to be applicable for the simulation of a wide range of device sizes in different operating conditions.

The approach used here is based on widely accepted experimental results that showed that the trapping of charge carriers by surface states is the main cause of current collapse. This is further elaborated using 2D device simulation. In the 2D device simulation, it is shown that defining extra charge carriers in the gate-drain produced I-V characteristics that are very similar to those obtained from experimental measurements of real device that is said to have exhibited current collapse. Some of the earlier modeling approaches have included the effect of these trapped charges as an increment in the gate-drain access region resistance. The modeling approach that conforms much better with the actual physical occurrence observed in the region is the virtual gate approach where a secondary virtual gate is assumed to exist in the gate-drain region right next to the main gate that represents the charge carriers trapped at the surface.

The concentration and distribution of the trapped charge carriers determines the extent and intensity of the current compression. Using the main parameters of the virtual gate modeling approach, the model is also made to assume such behavior. Since little is known about the actual trapped charge distribution, pre-assumed virtual gate voltage and length are used to to fir measurement data.

The Volterra series analysis was used in order to model the nonlinearity of AlGaAs/GaAS pHEMT devices. The coefficient extraction method used, recommended as a standard extraction method in the circuit simulator Microwave Office from AWR, requires linear and nonlinear measurements to be performed in order to obtain more precise coefficients. The nonlinear measurements that need to be done at very low input drives make the reading of third order intermodulation power levels difficult. An amplifier can be used for an easier reading of the third order power levels. However, it is important to use a diplexer so that the fundamental can be safely filtered while reading the higher level harmonic power outputs. Two-tone intermodulation simulations carried out using the extracted coefficients, after the nonlinear elements have been defined and the total non-linear equivalent circuit that contains these elements with the linear components is implemented in a circuit simulator. The comparison between Two-Tone intermodulation simulations and measurements show that the model is able to reproduce weak nonlinearities of the device that are measured at lower input drives. The model deviates from measurement as the device is driven into strong nonlinearity by applying higher input power drives.

5.2 Future Work Prospects

As a device model is never complete, all the core and non-ideal effect modeling approaches used should be put under constant revision and improvement in consistence with the dynamic device fabrication. The possible future extensions of the research work fall into two groups: consideration of some important features that are not considered here and improvement of some of the modeling approaches used here.

A gate current model needs to be developed that can be used with the core current model. Device noise modeling is also required in order to make a much more complete device simulation. The model is shown to be continuous which makes it suitable for non-linear simulations. Therefore, it should be combined with an appropriate nonlinear modeling scheme to get the best out of it.

Regarding the virtual gate model the first and the most important should be formulation of analytical relations between the main virtual gate parameters and device geometry and biasing conditions. Such a model is also expected to have capability of considering previous biasing history of the device, so as to take into account the memory effects. Development of such a model requires a closer study of the charge distribution and sufficient number measurements with the device being under a range of stresses. Formulation of such analytical relations will avoid the need to use pre-assumed parameters of the virtual gate model.

The Volterra series analysis performed on the AlGaAs/GaAs pHEMTs can also be applied to the AlGaN/GaN HEMTs. In this case it would be interesting to use the higher order derivatives of the GaN HEMT current model as the coefficients instead of those extracted using the coefficient extraction method discussed in Chapter 4. This enables to test the continuity and robustness of the current model and at the same time the significance of the Volterra coefficient extraction technique presented and make comparisons between the two.

Appendix A

Calculating the Conduction Band Bending

Assuming depletion approximation in the space charge region of the large band gap material, the potential and the electric field in the region obey the Poisson's equation, Thus

$$\frac{d^2V_2(x)}{dx^2} = -\frac{q}{\varepsilon_2}N_A(x)\,. \tag{A.1}$$

If the heterojunction interface is taken as origin, then the electric field is zero at the end of the space charge region of the wide band gap semiconductor, d_2, and it is $-F_{i2}$ at the interface. Thus,

$$\left(\frac{dV_2}{dx}\right)_{x=0} = F_{i2} \quad and \quad \left(\frac{dV_2}{dx}\right)_{x=-d_2} = 0\ . \tag{A.2}$$

Thus, after first integral we have

$$\frac{dV_2\left(x\right)}{dx} = -\frac{q}{\varepsilon_2}\int_0^x N_A(x')dx' + F_{i2}. \tag{A.3}$$

Integrating in the total width of the space charge region of the wide band gap semiconductor, the potential at the end of the depletion region during the neutral state can be written as

$$V_2(-d_2) = V_{20} = \int_0^{-d_2}\left(-\frac{q}{\varepsilon_2}\int_0^x N_A(x')dx'\right)dx + \int_0^{-d_2} F_{i2}dx \tag{A.4}$$

$$V_{20} = F_{i2}d_2 - \frac{q}{\varepsilon_2}\int_0^{-d_2} dx \int_0^x N_A(x')dx'. \tag{A.5}$$

The boundary conditions of the donor density distribution are

$$\begin{aligned} N_A(x) &= 0 \qquad for - d_S < x < 0 \\ N_A(x) &= N_A \quad for - d_2 < x < -d_S. \end{aligned} \tag{A.6}$$

Using these

$$V_{20} = F_{i2}d_2 - \frac{q}{\varepsilon_2}\int_0^{-d_2} dx N_A \int_{-d_s}^{x} dx' \tag{A.7}$$

$$V_{20} = F_{i2}d_2 - \frac{qN_A}{\varepsilon_2}\int_0^{-d_2}(x+d_s)dx \tag{A.8}$$

$$V_{20} = F_{i2}d_2 - \frac{qN_A}{\varepsilon_2}\left[\frac{1}{2}\left(d_2^2 - d_s^2\right) - d_s\left(d_2 - d_s\right)\right]. \tag{A.9}$$

From the Poisson's equation written for the electric field in the region, one can easily obtain

$$\varepsilon_2 F_{i2} = qN_A(d_2 - d_S). \tag{A.10}$$

Thus, substituting for the electric field gives

$$V_{20} = \frac{qN_A(d_2 - d_S)d_2}{\varepsilon_2} - \frac{qN_A}{\varepsilon_2}\left[\frac{1}{2}\left(d_2^2 - d_s^2\right) - d_s\left(d_2 - d_s\right)\right] \tag{A.11}$$

$$V_{20} = \frac{qN_A}{\varepsilon_2}\left[(d_2 - d_S)d_2 - \frac{1}{2}\left(d_2^2 - d_s^2\right) + d_s\left(d_2 - d_s\right)\right]. \tag{A.12}$$

Thus,

$$V_{20} = \frac{qN_A}{2\varepsilon_2}\left(d_2^2 - d_s^2\right). \tag{A.13}$$

Appendix B

Simple Charge Control Model Derivation

The simple charge control model in section 2.5 is derived from the fundamental equations that relate the Fermi-level, the sub-band energy levels and the carrier concentration using a systematic mathematical approach as follows.

Considering only the first energy level, as discussed in section 2.5, we have

$$n_s = DV_{th} \ln\left(e^{\frac{\left(E_f - E_0\right)}{V_{th}}} + 1\right). \tag{B.1}$$

This can be simplified as

$$e^{\frac{n_s}{DV_{th}}} = e^{\frac{E_f - E_0}{V_{th}}} + 1 \tag{B.2}$$

$$1 = \frac{e^{\frac{E_f - E_0}{V_{th}}} + 1}{e^{\frac{n_s}{DV_{th}}}} = e^{\frac{E_f - E_0}{V_{th}} - \frac{n_s}{DV_{th}}} + e^{\frac{-n_s}{DV_{th}}} \tag{B.3}$$

$$1 = e^{\frac{D\left(E_f - E_0\right) - n_s}{DV_{th}}} + e^{\frac{-n_s}{DV_{th}}} \tag{B.4}$$

$$e^{\frac{n_s}{DV_{th}}} = e^{\frac{\left(E_f - E_0\right)}{V_{th}}} + 1 \tag{B.5}$$

$$e^{\frac{\left(E_f - E_0\right)}{V_{th}}} = -1 + e^{\frac{n_s}{DV_{th}}} \tag{B.6}$$

$$\frac{E_f - E_0}{V_{th}} = \ln\left(-1 + e^{\frac{n_s}{DV_{th}}}\right) \tag{B.7}$$

$$E_f = V_{th} \ln\left(-1 + e^{\frac{n_s}{DV_{th}}}\right) + E_0. \tag{B.8}$$

Substituting for E_0 from $E_0 = \gamma_0 n_s^{2/3}$ gives

$$E_f = V_{th} \ln\left(-1 + e^{\frac{n_s}{DV_{th}}}\right) + \gamma_0 n_s^{2/3}. \tag{B.9}$$

From $n_s = \frac{\varepsilon}{qd}\left(V_{g0} - E_f\right)$ one can simplify for V_{g0} as

$$V_{g0} = \frac{qd}{\varepsilon} n_s + E_f. \tag{B.10}$$

Substituting for E_f gives

$$V_{g0} = \frac{qd}{\varepsilon} n_s + V_{th} \ln\left(-1 + e^{\frac{n_s}{DV_{th}}}\right) + \gamma_0 n_s^{2/3}. \tag{B.11}$$

The Taylor series expansion of the term $e^{\frac{n_s}{DV_{th}}}$ can be written as

$$e^{\frac{n_s}{DV_{th}}} = 1 + \frac{\frac{n_s}{DV_{th}}}{1!} + \frac{\left(\frac{n_s}{DV_{th}}\right)^2}{2!} + \cdots \tag{B.12}$$

and taking only up to the first order gives

$$V_{g0} = \frac{q_d}{\varepsilon} n_s + \gamma_0 n_s^{\frac{2}{3}} + V_{th} \ln\left(\frac{n_s}{DV_{th}}\right). \tag{B.13}$$

For a more accurate result the higher order terms of the Taylor series can be used. However, taking only the first order has gave satisfactory results and using the higher orders will make the expression very complex without improving the accuracy considerably.