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Design and Analysis of a Novel Multilevel Active-Clamped Power-Converter

Tesis doctoral presentada para acceder al grado de Doctor por la Universitat Politècnica de Catalunya, dentro del Programa de Doctorado en Ingeniería Electrónica

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A mi familia y a Laura

Un millón de gracias a todos

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CONTENTS

ABSTRACT

Multilevel converter technology has been receiving increasing attention during the last years due to its important advantages compared to conventional two-level conversion. Multilevel converters reduce the voltage across each semiconductor. These converters also synthesize waveforms with better harmonic spectrum, and in most cases, increasing the efficiency of the power conversion system. However, a larger quantity of semiconductors is needed and the modulation strategy to control them becomes more complex. There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Numerous hybrid configurations combining them and other multilevel topologies have also been presented in the literature.

A novel multilevel active-clamped (MAC) topology is the subject of study of the present thesis. This topology is derived from the generalized multilevel topology by simply removing all flying capacitors. The topology can also be seen as an extension into an arbitrary number of levels of the three-level active neutral-point-clamped (ANPC) topology. The novel converter is controlled using a proper set of switching states and a switching state transition strategy, which permits to obtain the maximum benefits from the converter.

In this thesis, the performance and operating capabilities of the MAC topology are studied through comprehensive efficiency and fault-tolerance analyses.

The efficiency analysis comprises a study of power-device conduction and switching losses in the topology, followed by analytical and experimental efficiency comparisons between the MAC converter and conventional two-level converters.

In the analysis of the fault-tolerance capacity of the MAC topology both open- and short-circuit faults are considered and the analysis is carried out under single-device and two-simultaneous-device faults. Switching strategies to overcome the limitations caused by faults and topology variations to increment the fault-tolerance ability of the MAC converter are proposed.

The thesis also proposes guidelines to guarantee a proper MAC converter design and improve its performance.

NOMENCLATURE

Acronyms and Abbreviations

ANPC	Active neutral-point-clamped
IGBT	Insulated-gate bipolar transistor
FPGA	Field-programmable gate array
GDPS	Gate-driver power-supply
IC	Integrated circuit
MAC	Multilevel active-clamped
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral-point-clamped
PWM	Pulse-width modulation
RMS	Root mean square
SSI	Switching scheme I
SSII	Switching scheme II
SVD	Space-vector diagram
SVPWM	Space-vector pulse-width modulation
THD	Total harmonic distortion
V^2PWM	Virtual-space-vector pulse-width modulation

Symbols

Topology parameters

m	Number of levels of the topology
i_k ; $k \in \{1, 2, \dots, m\}$	Input terminal k of the topology
c_k ; $k \in \{1, 2, \dots, m-1\}$	Control variables for controlling the MAC converter
$c_{\mathrm{S}_x,\mathrm{i}_k}$; $k \in \{1, 2, \dots, m\}$	Per-unit value of leg output current i_o flowing through device S_x when the output terminal is connected to the input terminal i_k

Time and Frequency

t	Time
t_k	Instant in which output terminal is connected to the input terminal i_k
T_s	Switching (or modulation) period
f	Frequency
f_s	Switching frequency
ω	Output fundamental angular frequency of inverter
T_v	Period of time in which voltage v_ds changes from 0 V to V_ds, or vice versa
T_i	Period of time in which voltage i_d changes from 0 A to I_d, or vice versa
t	Dead time. Time between the turn off and the turn on of devices in a switching-state transition

Devices

S_{xkj} ; $x \in \{\mathrm{p}, \mathrm{n}\}$; $k \in \{1, 2, \dots, m-1\}$; $j \in \{1, 2, \dots, m-1\}$	MAC-leg devices (device j belonging to diagonal xk in a MAC leg)
S_x ; $x \in \{\mathrm{p}kj, \mathrm{n}kj\}$; $k \in \{1, 2, \dots, m-1\}$; $j \in \{1, 2, \dots, m-1\}$	MAC-leg devices
S_x ; $x \in \{\mathrm{p}, \mathrm{n}\}$	Two-level-leg devices
$\mathrm{S}_{\mathrm{p}kj}$; $k \in \{1, 2, \dots, m-1\}$; $j \in \{1, 2, \dots, m-1\}$	Upper devices of the basic cells of the MAC leg
$\mathrm{S}_{\mathrm{n}kj}$; $k \in \{1, 2, \dots, m-1\}$; $j \in \{1, 2, \dots, m-1\}$	Lower devices of the basic cells of the MAC leg
S_p	Upper device of a two-level leg

S_n	Lower device of a two-level leg
S_{ak} ; $k \in \{2, m-1\}$	Additional devices included in solution II of hardware variations to increase the MAC fault-tolerance ability
S_{abk} ; $k \in \{1,2,\dots,m\}$	Additional bidirectional switches included in solution III of hardware variations to increase the MAC fault-tolerance ability
S_{axkj} ; $x \in \{p, n\}$; $k \in \{1, 2, \dots, m-1\}$; $j \in \{1, 2, \dots, m-1\}$	Auxiliary MOSFET of the GDPS of power device S_{xkj}
S_{test}	Device under test for measuring its switching losses
$D_{S_{test}}$	Additional antiparallel diode of device S_{test}
D_{zxkj}	Zener diode of the GDPS of device S_{xkj}
D_{bxkj}	Blocking diode of the GDPS of device S_{xkj}

Passives components

C_{xkj}	Output capacitor of the GDPS of device S_{xkj}
R_{axkj}	Auxiliary resistor of the GDPS of device S_{xkj}
C	Dc-link capacitor

Passives values

R	Resistance
L	Inductance
C	Capacitance
Z	Impedance
R_L	Load resistance
C_L	Load capacitance
Z_L	Load impedance

$L_x\ ;\ x \in \{a, b, c\}$	Inductance filter (load) of phase leg *x*
$R_{\mathrm{ds(on)}}$	ON-state drain-to-source resistance
$r_{\mathrm{ds(on)}}$	ON-state drain-to-source resistivity (per-unit-area resistance)
$R_{\mathrm{ds(on),200}}$ or $R_{\mathrm{ds(on),STP20NF20}}$	ON-state drain-to-source resistance of 200 V MOSFET STP20NF20
$R_{\mathrm{ds(on),600}}$ or $R_{\mathrm{ds(on),STP13NM60N}}$	ON-state drain-to-source resistance of 600 V MOSFET STP13NM60N
$R_{\mathrm{ds(on)},S_x,\mathrm{2L}}$	ON-state drain-to-source resistance of any device S_x belonging to the two-level leg
$R_{\mathrm{ds(on)},S_x,\mathrm{4L}}$	ON-state drain-to-source resistance of any device S_x belonging to the four-level leg
R_{eq,i_k} ; $k \in \{1, 2, \dots, m\}$	Equivalent ON-resistance between the leg output terminal and the corresponding input terminal i_k
$R_{\mathrm{eq},i_k,\mathrm{norm}}$; $k \in \{1, 2, \dots, m\}$	Normalized equivalent ON-resistance between the leg output terminal and the corresponding input terminal i_k
R_{eq}	Equivalent resistance
C_{xkj}	Capacitance of capacitor C_{xkj} of the GDPS of device S_{xkj}
C_{oss}	Output parasitic capacitance of a MOSFET device

Voltages

V	Voltage value between adjacent input terminals of the MAC leg
V_{dc}	Voltage value of a dc source
$V_{\mathrm{dc-link}}$	Dc-link voltage value
v_{o}	Instantaneous leg output voltage
$v_x\ ;\ x \in \{a, b, c\}$	Instantaneous leg *x* output voltage
$V_{\mathrm{l-l,pk}}$	Peak value of fundamental component of the line-to-line voltage
$v_{xy}\ ;\ x \in \{a, b, c\}$ $y \in \{a, b, c\}$	Instantaneous line-to-line converter output voltage

v_{ck} ; $k \in \{1, 2, \dots, m-1\}$	Instantaneous dc-link capacitor voltages between input terminals k and k+1
v_{ds}	Instantaneous drain-to-source voltage of a MOSFET device
$v_{\mathrm{ds(S}_x\mathrm{)}}$	Instantaneous drain-to-source voltage of MOSFET device S_x
V_{ds}	Drain-to-source voltage value of a MOSFET device when it is in OFF-state
v_{ak}	Instantaneous anode-to-cathode voltage of a diode
v_{gs}	Instantaneous gate-to-source voltage of a MOSFET device
V_{test}	Voltage value used for performing the tests to measure switching losses
V_{gs}	Gate-to-source voltage value of a MOSFET device when it is in ON-state
v_{cxkj}	Instantaneous voltage of capacitor C_{xkj} of the GDPS
BV_{ds}	MOSFET blocking voltage

Currents

i_o	Instantaneous leg output current
i_x ; $x \in \{a, b, c\}$	Instantaneous leg x output current
i_{d}	Instantaneous drain current flowing through a MOSFET device
$i_{\mathrm{d(S}_x\mathrm{)}}$	Instantaneous drain current flowing through MOSFET S_x
I_{d}	MOSFET drain current value when it is in ON-state
I_{o}	Dc leg output current value
$I_{\mathrm{o,pk}}$	Peak value of output current i_{o}
i_{rr}	Instantaneous reverse-recovery current
$I_{\mathrm{d(RMS)}}$	RMS value of device drain current i_d
i_{ak}	Instantaneous diode current from anode to cathode
I_{ak}	Value of diode current from anode to cathode when it is in ON-state

i_{dis}	Instantaneous discharging current of the device output parasitic capacitance C_{oss}

Energy

$E_{\text{cond,leg},T_S}$	Conduction energy loss in the converter leg during T_S
$E_{\text{cond,leg},dt}$	Conduction energy loss in the converter leg during an infinitesimal differential of time dt
E_{cond,S_x,T_S}	Conduction energy loss in device S_x during a switching period T_S
$E_{\text{cond},S_x,dt}$	Conduction energy loss in device S_x during an infinitesimal differential of time dt
E_{on}	Turn-on energy loss
E_{off}	Turn-off energy loss
E_{rr}	Reverse-recovery energy loss
$E_{\text{on}\_k\text{D}}\ ;\ k \in \{1,2,3\}$	Turn-on energy loss with k diodes connected in parallel presenting reverse-recovery processes.
$E_{\text{rr}\_k\text{D}}\ ;\ k \in \{1,2,3\}$	Reverse-recovery energy lost by k diodes connected in parallel.
$E_{\text{sw,leg},T_S}$	Switching energy loss in the converter leg during a switching period T_S
$E_{\text{on}\_k\text{D,200}}\ ;\ k \in \{1,2,3\}$	Turn-on energy loss of 200 V MOSFET STP20NF20 with k diodes connected in parallel presenting reverse-recovery processes
$E_{\text{on\_1D,600}}$	Turn-on energy loss of 600 V MOSFET STP13NM60N with one diode connected in parallel presenting reverse-recovery processes
$E_{\text{off,200}}$	Turn-off energy loss of 200 V MOSFET STP20NF20
$E_{\text{off,600}}$	Turn-off energy loss of 600 V MOSFET STP13NM60N
$E_{\text{rr}\_k\text{D,200}}\ ;\ k \in \{1,2,3\}$	Reverse-recovery energy lost by k antiparallel diodes of 200 V MOSFET STP20NF20 connected in parallel.
$E_{\text{rr\_1D,600}}$	Reverse-recovery energy lost by the antiparallel diode of 600 V MOSFET STP13NM60N connected in parallel.

Power

P_{cond}	Conduction power loss

$P_{\mathrm{cond,leg}}$	Conduction power loss in the converter leg
P_{cond,S_x}	Conduction power loss in device S_x
P_{sw}	Switching power loss
P_{rg}	Power loss in the gate resistor
P_{drv}	Power loss in the gate-driver integrated circuit
P_{rc}	Power loss in the resistors connected in parallel with the dc-link capacitors to facilitate their charging/discharging
$P_{t,m\mathrm{L}}$; $t \in \{\mathrm{cond}, \mathrm{sw}, \mathrm{rg}, \mathrm{drv}, \mathrm{rc}\}$; $m \in \{2, 4\}$	Power loss of type *t* in the *m*-level leg
P_{out}	Converter output power
P_{in}	Converter input power
P_{loss}	Converter power loss
P_{S_x}	Total power loss in device S_x
$p_{\mathrm{loss-on}}$	Instantaneous power loss in the turn-on transition
$p_{\mathrm{loss-off}}$	Instantaneous power loss in the turn-off transition
$p_{\mathrm{loss-rr}}$	Instantaneous power loss in the reverse-recovery transition
p_{o}	Instantaneous leg output power

Temperatures

T_{s}	Heat-sink temperature
T_{j,S_x}	Junction temperature of device S_x
$T_{\mathrm{j},S_x,\mathrm{max}}$	Predefined maximum value of T_{j,S_x}

Angles

θ	Line-cycle angle

φ	Load line-to-neutral impedance angle

Modulation Parameters

mi	Modulation index ($V_{\mathrm{l-l,pk}}/V_{\mathrm{dc-link}}$).
$d_k\ ;\ k \in \{1,2,\dots,m\}$	Duty ratio of connection of the leg output terminal to the input terminal i_k
d_{offset}	Added offset to original duty ratios d_{yk}

Device parameters

Q_{g}	MOSFET gate charge
Q_{rr}	MOSFET reverse-recovery charge
$R_{\mathrm{th,js}}$	Junction-to-heat-sink thermal resistance
$R_{\mathrm{th,jc}}$	Junction-to-case thermal resistance
$R_{\mathrm{th,cs}}$	Case-to-heat-sink thermal resistance
A_{S_x}	Chip area of device S_x
A_{S}	Chip area of device S

Other parameters

s_{v}	Slope of voltage v_{ds} in a switching transition
s_{i}	Slope of current i_{d} in a switching transition

CHAPTER 1

INTRODUCTION

Abstract — This opening chapter presents a review of the multilevel conversion concept and the different multilevel converter topologies. Then, the thesis objective is defined, and finally, the outline of the thesis is presented.

1.1. Multilevel conversion concept

The essence of the multilevel concept consists of using multiple voltage levels in the process of power conversion. Fig. 1.1 presents a functional schematic of a converter leg having different number of levels. Fig. 1.1(a) corresponds to the conventional two-level leg, Fig. 1.1(b) corresponds to the three-level case, and Fig. 1.1(c) to an *m*-level leg. The converters are classified according to the number of dc-link voltage levels available to synthesize the output phase voltage v_{o}.

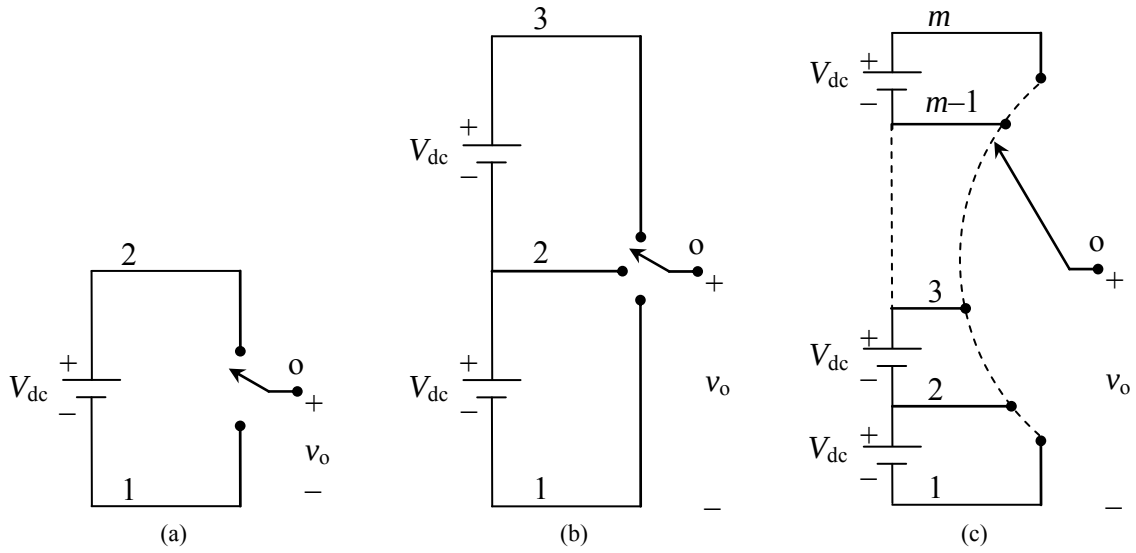


Fig. 1.1. Functional schematic of a converter leg having different number of levels. (a) Two levels. (b) Three levels. (c) m levels.

Multilevel power conversion [1]-[4] has been receiving special attention during the last two decades due to their significant advantages compared to conventional two-level topologies. Thanks to their advantages, multilevel converters have opened a door for advances in the electrical energy conversion technology.

These converters are typically considered for high power applications because they allow operating at higher dc-link voltage levels with the current available semiconductor technology. But

they can also be attractive for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features.

The advantages of multilevel converters compared to the conventional two-level converters could be summarized as follows:

- The voltage across each semiconductor is reduced. For converter power ratings where only a single device for position is needed in the two-level topology, multilevel converters allow using devices with a lower voltage rating (by a factor of m–1) having higher performance characteristics. Similarly, for a given semiconductor technology, an m-level multilevel converter allows increasing the dc-bus voltage by a factor m–1, increasing the converter power rating by m–1, without the problems associated to the series connection of devices.
- The total harmonic distortion (THD) of the output ac-voltage is significantly reduced (for the same dc-link voltage), allowing to reduce the output filter cost and size, which also leads to improve the dynamic response of the controlled converter.
- They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
- They can generate output voltages with lower *dv/dt*.
- They draw input current with very low distortion.
- They produce lower switching losses for a given current THD.

However, using multilevel converters, the control and modulation strategies become more complex. Moreover, they require a bigger quantity of semiconductors and its corresponding gate drive circuits, which increases the cost.

1.2. Multilevel converter topologies

Multilevel conversion technology has probably its origin in 1962 [5], in which multiple levels are achieved by adding the outputs of several inverters operating in parallel through phase shifting transformers. This technique is no longer attractive for most applications due to the large reactive elements used. A closer concept to the nowadays multilevel topologies is proposed in [6] and [7], in which some configurations are proposed based on proper connections of transistors, thyristors and capacitors that permit to synthesize multilevel voltage waveforms.

Topologies commonly used today for implementing multilevel converters include an array of power semiconductors. There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate dc-sources. A number of variations and combinations of these topologies, and new topologies, have been proposed and analyzed in the literature. In the following, a review of the main multilevel topologies proposed along the last decades is presented.

1.2.1. Cascaded H-bridge converter

The first one in appear of the three main multilevel topologies was the cascaded H-bridge topology, introduced by Baker in [8]. This topology is based on a very simple idea to generate multilevel voltages, which consists of the series connection of single phase H-bridge inverters with separate dc-sources. Fig. 1.2 presents the cascaded H-bridge topology. Fig. 1.2(a) corresponds to the topology using two H-bridge inverters, which permits to generate five output different levels, and Fig. 1.2(b) corresponds to the arbitrary case of *m* H-bridge inverters, which permits to generate 2*m*+1 levels. An important inconvenient of the cascaded H-bridge multilevel converter is the necessity of using independent and isolated dc-sources (dc-power supplies).

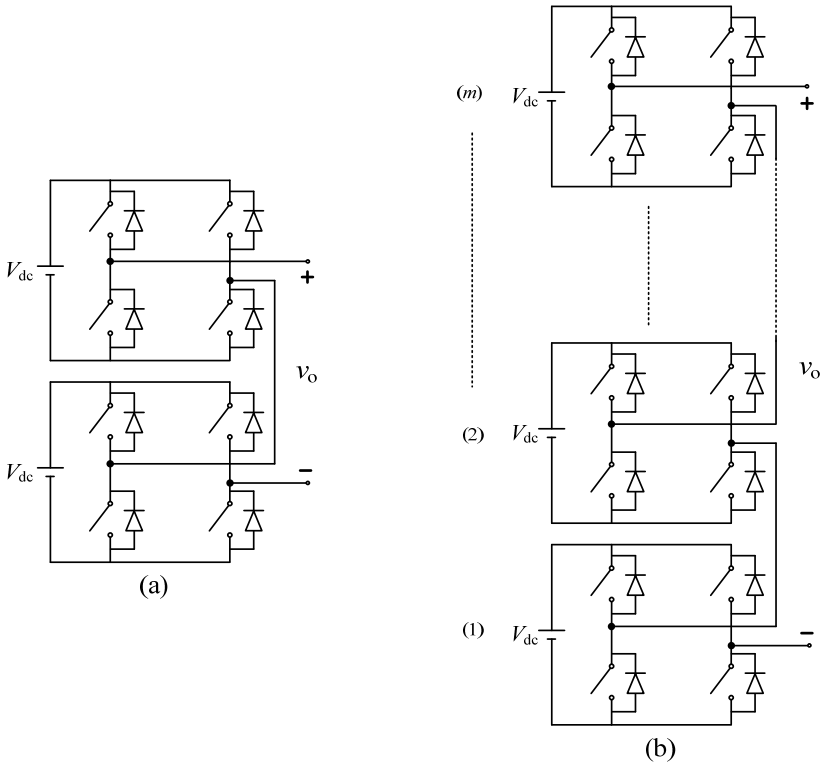


Fig. 1.2. Cascaded H-bridge converter. (a) Two-H-bridges leg topology. (b) m-H-bridges leg topology.

1.2.2. Diode-clamped converter

The three-level diode-clamped topology, also called neutral-point-clamped (NPC) topology, was introduced by Nabae in [9]. In this circuit, the dc-bus voltage is split into three levels by means of the series connection of two capacitors. The middle point of the dc-link bus is called the neutral point. Diode-clamped topology was generalized into *m* levels in [10], [11]. Fig. 1.3 shows the diode clamped topology. Fig. 1.3(a) corresponds to the three-level case and Fig. 1.3(b) corresponds to the five-level case.

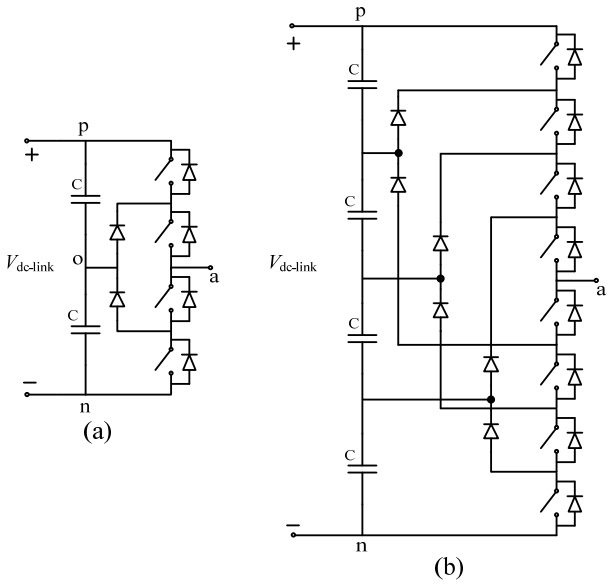


Fig. 1.3. Diode-clamped multilevel converter. (a) Three-level leg topology. (b) Five-level leg topology.

The neutral-point-clamped converter has become the most used multilevel topology in industry applications, thanks to its implementation simplicity and its better performance, compared to other topologies.

However, capacitor voltage balancing has long been an important problem of diode-clamped topologies [12]. Correct operation of the diode-clamped converters requires that the voltage across dc-link capacitors be the same. With the utilization of conventional modulation strategies, voltage balancing can not be guaranteed for certain operating conditions.

Some authors have been proposing different solutions modifying the control and modulation strategies [13]-[23] and today it could be said that this problem has been solved.

1.2.3. Capacitor-clamped converter

The flying-capacitor converter, also called capacitor clamped, was introduced in [24]. In Fig. 1.4, it is depicted the flying capacitor multilevel topology. Fig. 1.4(a) corresponds to the three-level

case and Fig. 1.4(b) corresponds to the five-level case. The circuit presents independent capacitors clamping the device voltage to one capacitor voltage level. An important inconvenient of this topology is the high current spikes that can be produced when capacitors with different voltages are connected in parallel.

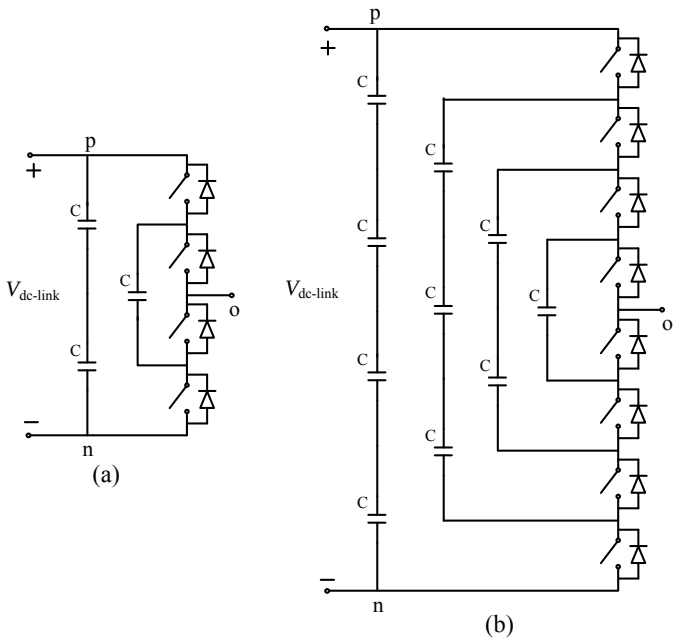


Fig. 1.4. Flying capacitor multilevel converter. (a) Three-level leg topology. (b) Five-level leg topology.

1.2.4. Variations of the three main multilevel topologies and hybrid configurations

A big number of different multilevel topologies have been created based on the three main multilevel topologies: diode clamped, flying capacitor, and cascaded H-bridge. Singular variations of them and numerous hybrid configurations combining them have been proposed in the literature.

References [25]-[31] propose different singular variation concepts of the cascaded H-bridge multilevel converter. Asymmetric configurations as binary [25], [28], quasi-linear [26]-[27] or trinary [27]-[28] configuration propose a change of the values of the adjacent dc-link voltage sources with the aim of incrementing the number of available levels for the output voltage using the same number of dc sources. In the original H-bridge cascaded topology, each dc-source presents the same voltage value and the number of levels that could be generated is equal to $2m+1$.

Fig. 1.5 presents the three mentioned configurations. Fig. 1.5(a) corresponds to the binary configuration, Fig. 1.5(b) corresponds to the quasi-linear configuration, and Fig. 1.5(c) to the trinary configuration. In the binary configuration, the values of each dc-link voltage source are equal to $V_{dc}\cdot 2^{k-1}$ (V_{dc}, $2\cdot V_{dc}$, $4\cdot V_{dc}$, $8\cdot V_{dc}$,…, $2^{m-1}\cdot V_{dc}$), and it is possible to generate $2^{m+1}-1$ levels. In

the quasi-linear configuration, the values of each dc-link voltage source are equal to $V_{dc} \cdot 2 \cdot 3^{k-2}$ (V_{dc}, $2 \cdot V_{dc}$, $6 \cdot V_{dc}$, $18 \cdot V_{dc}$,…, $2 \cdot 3^{m-2} \cdot V_{dc}$), and it is possible to generate $2 \cdot 3^{m-1}+1$ levels. Finally, in the trinary configuration, the values of each dc-link voltage source are equal to $V_{dc} \cdot 3^{k-1}$ (V_{dc}, $3 \cdot V_{dc}$, $9 \cdot V_{dc}$, $27 \cdot V_{dc}$,…, $3^{m-1} \cdot V_{dc}$), and it is possible to generate 3^m levels. The need of using devices with different blocking voltages is an important inconvenient of these topologies. Reference [29] presents a survey of cascaded multilevel topologies.

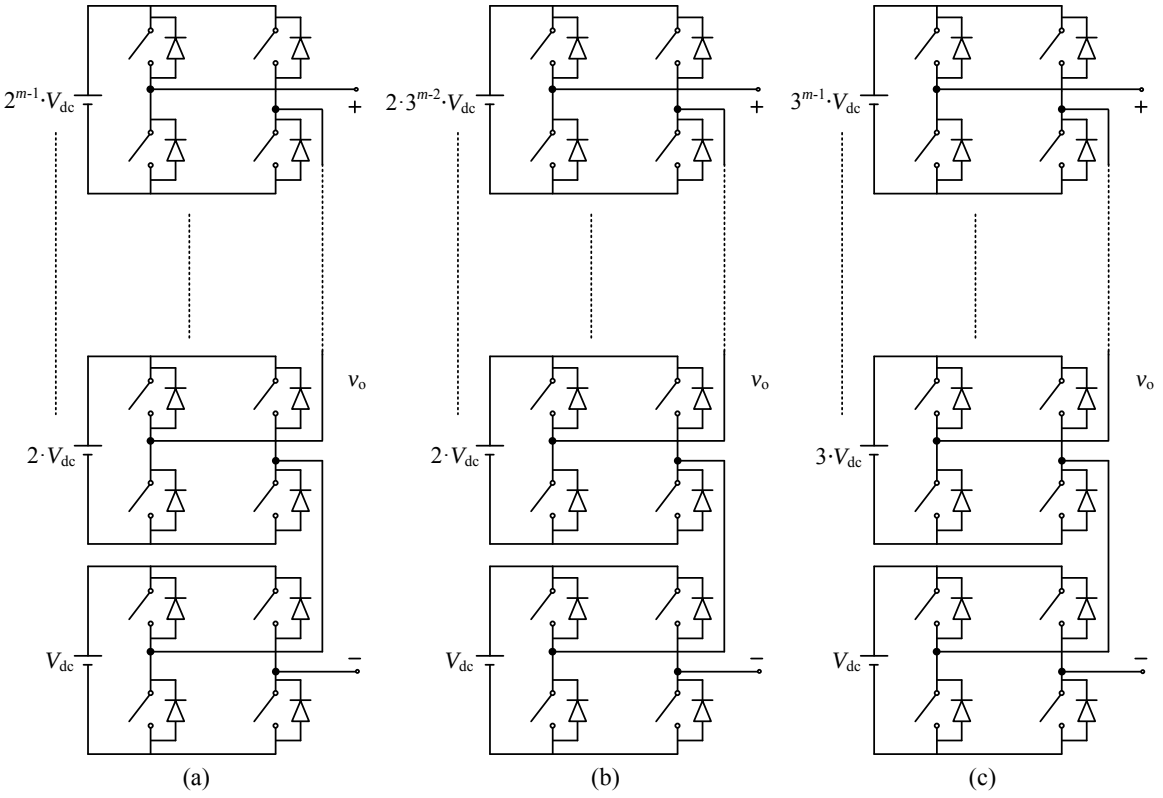


Fig. 1.5. Three singular variations of the cascaded H-bridge topology. (a) Binary configuration leg. (b) Quasi-linear configuration leg. (c) Trinary configuration leg.

Regarding the capacitor-clamped converter, some singular variations of this topology are proposed in [32]-[35]. Reference [32] proposes a single-phase flying-capacitor-half-bridge 5-level inverter in which a traditional half-bridge inverter is connected in parallel with the capacitor-clamped converter. A very similar concept is presented in [33], where it is proposed a topology which also presents two legs in parallel, and one of them is the capacitor clamped leg. The other leg is similar to a conventional half-bridge leg, but in this case there are four transistors instead of two, which permits to control the charge and discharge of the clamping capacitor. As in the previous case, five voltage levels are generated on the ac terminal of the proposed inverter. In [34], it is proposed a multilevel modular capacitor-clamped dc-dc converter (MMCCC), which presents an inherent modular structure and can be designed to achieve any conversion ratio. Each modular

block has one capacitor and three transistors leading to three terminal points. Finally, reference [35] proposes a zero-voltage switching (ZVS) scheme for a three-level capacitor clamping inverter based on a true pulse-width modulation (PWM) pole.

Regarding the diode-clamped converter, some singular variations of this topology are proposed in [36]-[40]. References [36]-[37] propose a single-phase five-level asymmetric inverter in which a traditional half-bridge inverter is connected in parallel with the diode-clamped converter, but each reference proposes a different control strategy. In [38], a novel multi output dc-dc converter connected to a diode-clamped topology is proposed. This converter, in certain cases, is able to regulate the capacitor voltage to provide an appropriate input voltage for NPC regardless of load changes, which can avoid the neutral-point balancing problem in such converters. References [39]-[40] present the active neutral-point-clamped (ANPC) converter, in which the two clamping diodes of the neutral point clamped converter are replaced by two transistors. This topology is explained in more detail in the following section.

As mentioned above, a lot of hybrid topologies combining the three main multilevel topologies have also been proposed. References [41]-[47] are some examples. Reference [41] presents a mixed topology that combines clamping capacitors and clamping diodes introducing capacitors in parallel with the clamping diodes. This topology is depicted in Fig. 1.6(a). Reference [42] presents the same concept, but in this case it is used an ANPC instead of a diode clamped converter. Reference [43] presents a different concept of mixed multilevel converter which combines diode clamped or flying capacitor converters with two-level bridge legs. Fig. 1.6(b) shows a combined diode clamped multilevel converter. General cascaded hybrid topologies, which are summarized in [44], use diode-clamped or flying-capacitor legs to replace the H-bridge as the basic module of the cascaded H-bridge converter in order to reduce the number of the isolated dc-link voltage sources. Fig. 1.6(c) presents a hybrid cascaded topology built upon a diode-clamped and a capacitor-clamped converter. Other cascaded hybrid topologies are presented in [45]-[47].

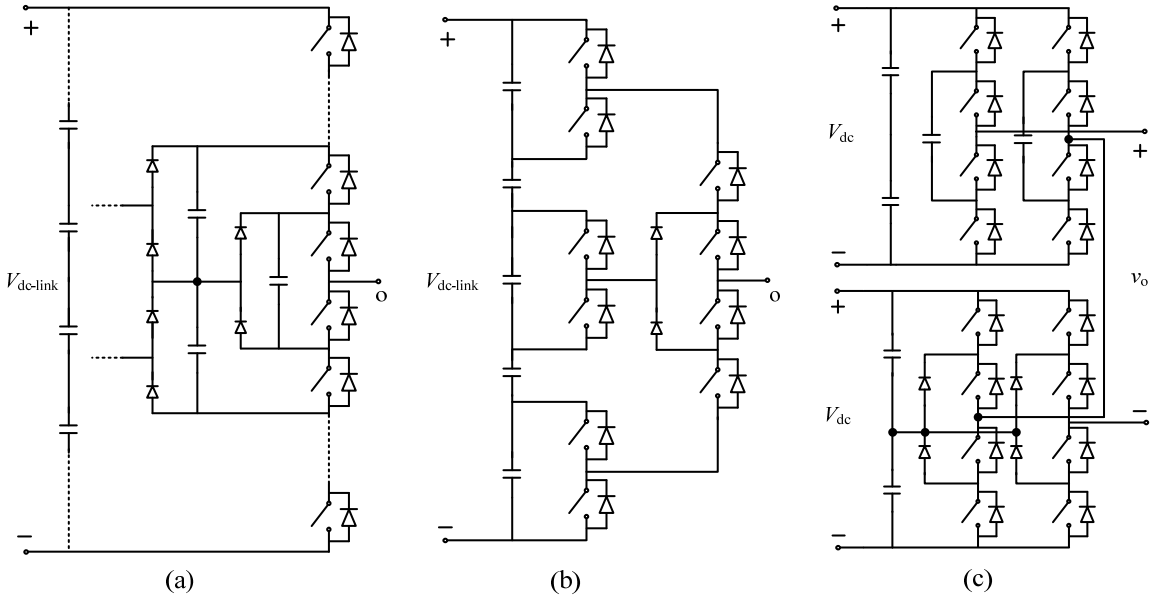


Fig. 1.6. Some hybrid multilevel leg topologies. (a) Topology that combines clamping capacitors and clamping diodes (m-level). (b) Combined diode-clamped multilevel inverter with two-level bridge legs. (c) Hybrid cascaded topology built upon a diode-clamped and a capacitor-clamped converter

1.2.5. Active neutral-point-clamped converters

The ANPC topology [39]-[40] is a variation of the three-level diode-clamped topology, in which the two clamped diodes are replaced by two transistors. This converter is introduced to balance the loss distribution of semiconductor devices in the conventional NPC converter, and consequently increase its output power rating or switching frequency. Fig. 1.7 shows the ANPC topology.

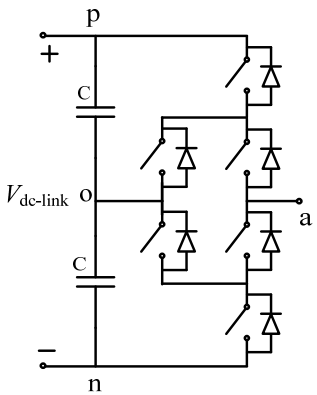


Fig. 1.7. ANPC topology.

Other active neutral-point-clamped topologies with more than three levels have also been proposed in the literature [48]-[50]. Reference [48] proposes a five-level and a seven-level active

neutral-point-clamped converter (ANPC5L and ANPC7L) and the concept of how to increment the topology into an arbitrary odd number of levels. The configuration proposed in [48] is shown in the Fig. 1.8. Fig. 1.8(a) presents the five-level case and Fig. 1.8(b) presents the seven-level case.

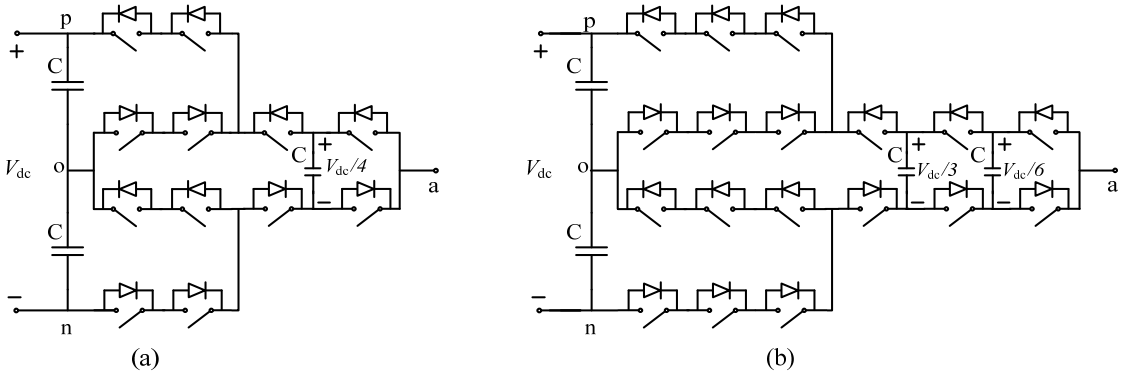


Fig. 1.8. Multilevel ANPC converters. (a) Five-level leg topology. (b) Seven-level leg topology.

As it can be seen, the converter is a combination of the ANPC with flying capacitor cells. In general, an *m*-level converter can be obtained by adding capacitor cells, according to Fig. 1.8.

Reference [49] introduces a common cross connected stage (C^3S) for the ANPC5L topology. Reference [50] shows the ANPC9L and proposes other different 9-level active neutral-point-clamped topologies based on a very similar concept.

1.2.6. Generalized multilevel topology

The generalized multilevel topology is introduced by Peng in [51]. Fig. 1.9 shows one leg of the generalized multilevel converter topology. The topology is formed by a pyramidal connection of $m \cdot (m-1)/2$ instances of the basic cell defined in the inset of Fig. 1.9. The leg presents one output terminal (o) and m input terminals i_k ($k \in \{1, 2, \ldots, m\}$), where m is the number of converter levels. A capacitor or a voltage source is connected across every two adjacent input terminals, being the dc voltage of each of these components typically the same ($V_{\mathrm{dc-link}}/(m-1)$). In this case, and if the converter is properly operated under the principle presented in [51], each device of the basic cell (capacitor, switch, and diode) has to withstand a voltage equal to $V_{\mathrm{dc-link}}/(m-1)$.

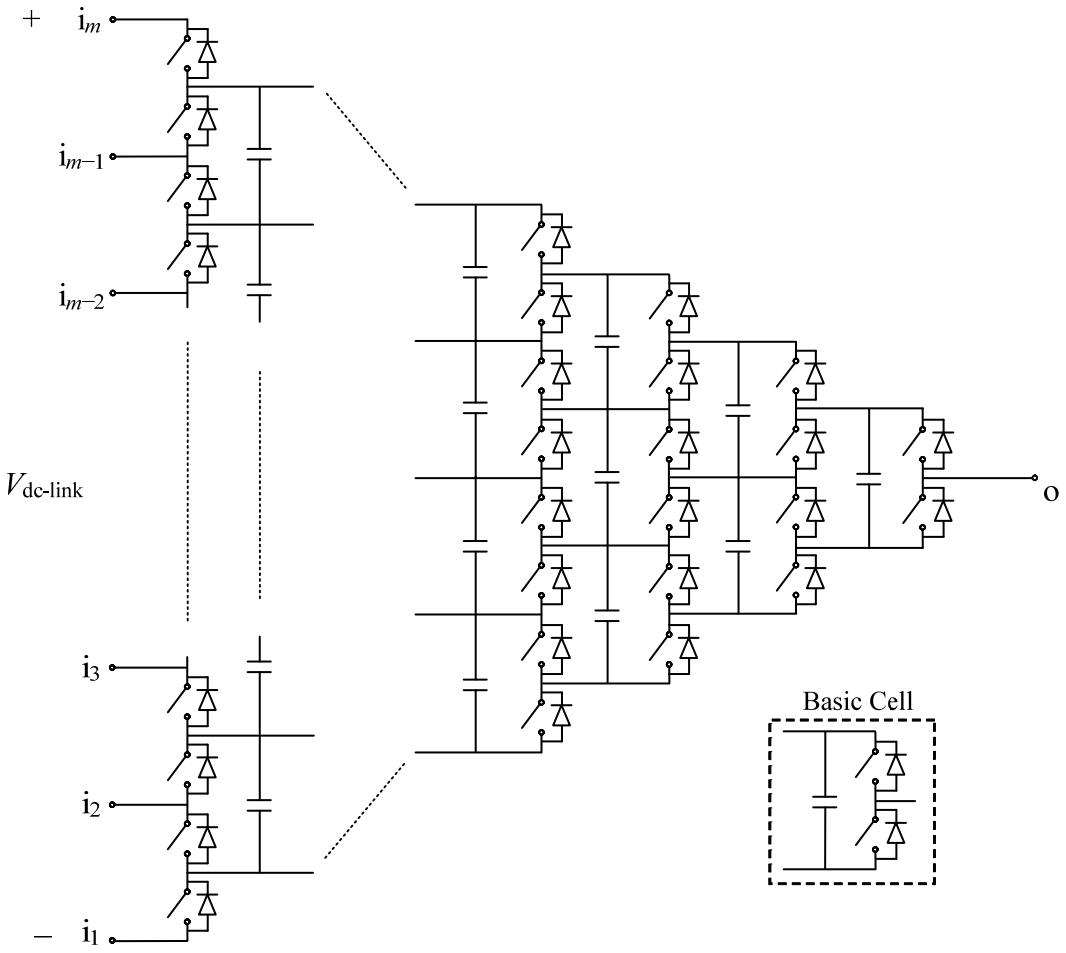


Fig. 1.9. Generalized multilevel leg topology.

The topology is general, in the sense that several topologies can be derived from this one. For instance, as discussed in [51], removing the clamping switches and diodes of Fig. 1.9 yields the capacitor-clamped multilevel topology. Diode-clamped multilevel converter can be obtained by eliminating all clamping switches and capacitors. Besides, another diode-clamped multilevel topology can be obtained by swapping diode clamping paths [51].

Other different topologies derived from the generalized multilevel converter have also been proposed in the literature [52]-[54].

In [52], another multilevel topology with fault tolerant ability derived from the generalized multilevel converter is proposed. This topology, shown in Fig. 1.10, only keeps the flying capacitors nearest to the dc-side, and removes all other flying capacitors. Besides, two additional devices to increase the fault-tolerance capacity of the topology are added, as it can be seen in Fig. 1.10.

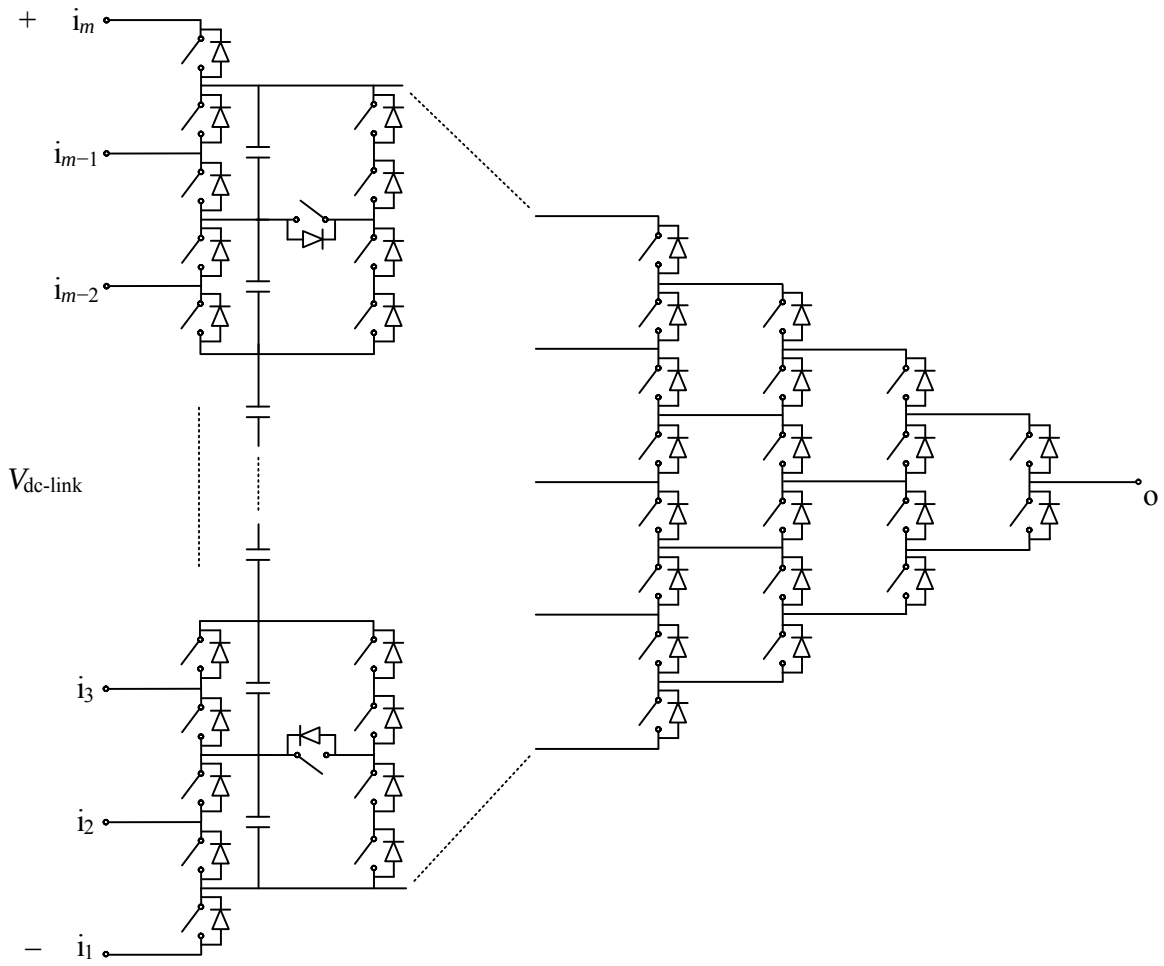


Fig. 1.10. Multilevel leg topology with fault tolerant ability derived from the generalized multilevel topology.

This topology, developed through the analysis of different power device-failure modes, improves the fault-tolerance capacity of the generalized multilevel topology. The power conversion can be maintained even under a failure scenario. Its fault-tolerant ability results from the redundant nature of the multi-switching-state topology and from control signal modification.

Reference [53] proposes a multilevel topology, clamped by active and passive devices (diodes). This topology keeps the clamping capacitors nearest to the dc-side, and removes other flying capacitors, just as the one proposed in [52]. In [54], a new topology is generated by keeping the outer basic cells of the generalized multilevel topology and eliminating the inner ones. This topology is very similar to the modular multilevel converter (M^2LC) proposed in [55]. The difference between them is that topology presented in [54] employs a middle basic cell in the leg with three terminals (two input terminals, one connected to the upper cells and the other one connected to the lower cells, and one output terminal, which represents the leg output terminal), which is not used in the original M^2LC.

Reference [56] introduces a novel multilevel active-clamped (MAC) topology derived from the generalized multilevel topology by simply removing all flying capacitors. The topology can also be seen as an extension of the three-level ANPC topology into an arbitrary number of levels. This topology will be the subject of study of the present thesis.

1.3. Thesis objective

The general objective of the proposed thesis is the study of the performance and operating capabilities of the MAC topology proposed in [56], through comprehensive efficiency and fault-tolerance analyses.

More specifically, the goals can be listed as follows:

- Definition of the MAC topology and operating principle.
- Definition of design guidelines for the MAC converter.
- Experimental verification of the MAC converter functionality.
- Exhaustive analysis of the MAC converter losses, comparing its efficiency with a two-level baseline design.
- Comprehensive study of the fault-tolerance capacity of the MAC converter, with proposals to improve it.

1.4. Thesis outline

The thesis is organized as follows.

Chapter 2 comprises the definition of the MAC topology together with the operating principle. Its functionality is verified through simulation and experimental tests.

In Chapter 3, an assessment of the MAC converter efficiency is carried out. First, a study of power-device conduction and switching losses is performed and analytical models to calculate them are presented. Then, efficiencies of MAC converter and a conventional two-level converter are compared analytically and experimentally, operating under a basic control scheme intended to infer general conclusions and to validate the analytical loss models. The analytical models are then used to compare the efficiency between the MAC and a two-level converter operating as three-phase inverters. Finally, a study to compare the minimum silicon chip area of the MAC topology versus the two-level topology is also presented.

Chapter 4 contains an analysis of the fault-tolerance capacity of the MAC topology. Both open- and short-circuit faults are considered and the analysis is carried out under single-device and two-simultaneous-device faults. Switching strategies to overcome the limitations caused by faults are proposed. Furthermore, some hardware-topology variations to increment the fault-tolerance ability of MAC converter are suggested.

The thesis is concluded in Chapter 5, where possible future extensions of the work accomplished are also proposed.

Appendix A presents design issues of the MAC topology. Guidelines are proposed to guarantee a proper MAC converter design and improve its performance.

Appendix B presents the experimental equipment used to perform the experimental tests.

Appendix C analyses the correlation between the device junction-to-sink thermal resistance $R_{\mathrm{th\,j,s}}$ and the device silicon area. This correlation is used in Chapter 3.

CHAPTER 2

MULTILEVEL ACTIVE-CLAMPED TOPOLOGY

Abstract — This chapter presents a the multilevel active-clamped converter topology, which is an extension to m levels of the three-level active neutral-point-clamped topology. The operating principle is established through the definition of a proper set of switching states and a transition strategy between adjacent switching states. The benefits of the proposed converter topology and control in comparison to alternative multilevel converter topologies are discussed. Simulation and experimental results of a simple four-level dc-dc converter configuration are presented to illustrate the converter performance features. Experimental results of a four-level three-phase dc-ac converter are also presented to further validate the proposed topology and operating principle.

2.1. Introduction

This chapter presents a multilevel topology built upon a single semiconductor device. This topology is based on the generalized multilevel topology introduced by Peng in [51], and represents an extension into an arbitrary number of levels of the popular three-level ANPC topology [39]. A proper set of switching states and a switching state transition strategy are defined to obtain the maximum benefits from the proposed topology.

This chapter is organized as follows. Section 2.2 presents the converter leg topology and defines the operating principle. Section 2.3 discusses the features of the proposed topology compared to alternative topologies and the possible converter configurations built upon the converter leg presented in Section 2.2. Section 2.4 presents simulation results in a four-level dc-dc converter configuration to illustrate the operation features. Section 2.5 presents experimental results of a four-level converter prototype, and Section 2.6 outlines the conclusions.

2.2. Topology

Fig. 1.9 presents one leg of the generalized multilevel converter proposed in [51]. As commented in the previous chapter, several multilevel topologies can be derived by removing some elements of that topology. Another option to simplify the topology is to remove all the flying capacitors. This leads to the active-clamped topology presented in Fig. 2.1. The topology is formed by a pyramidal connection of $m \cdot (m-1)/2$ instances of the basic cell defined in the inset of Fig. 2.1. The leg presents one output terminal (o) and m input terminals ($\mathrm{i}_k, k \in \{1, 2, \dots, m\}$), where m is the number of converter levels. A capacitor or a voltage source is connected across every two

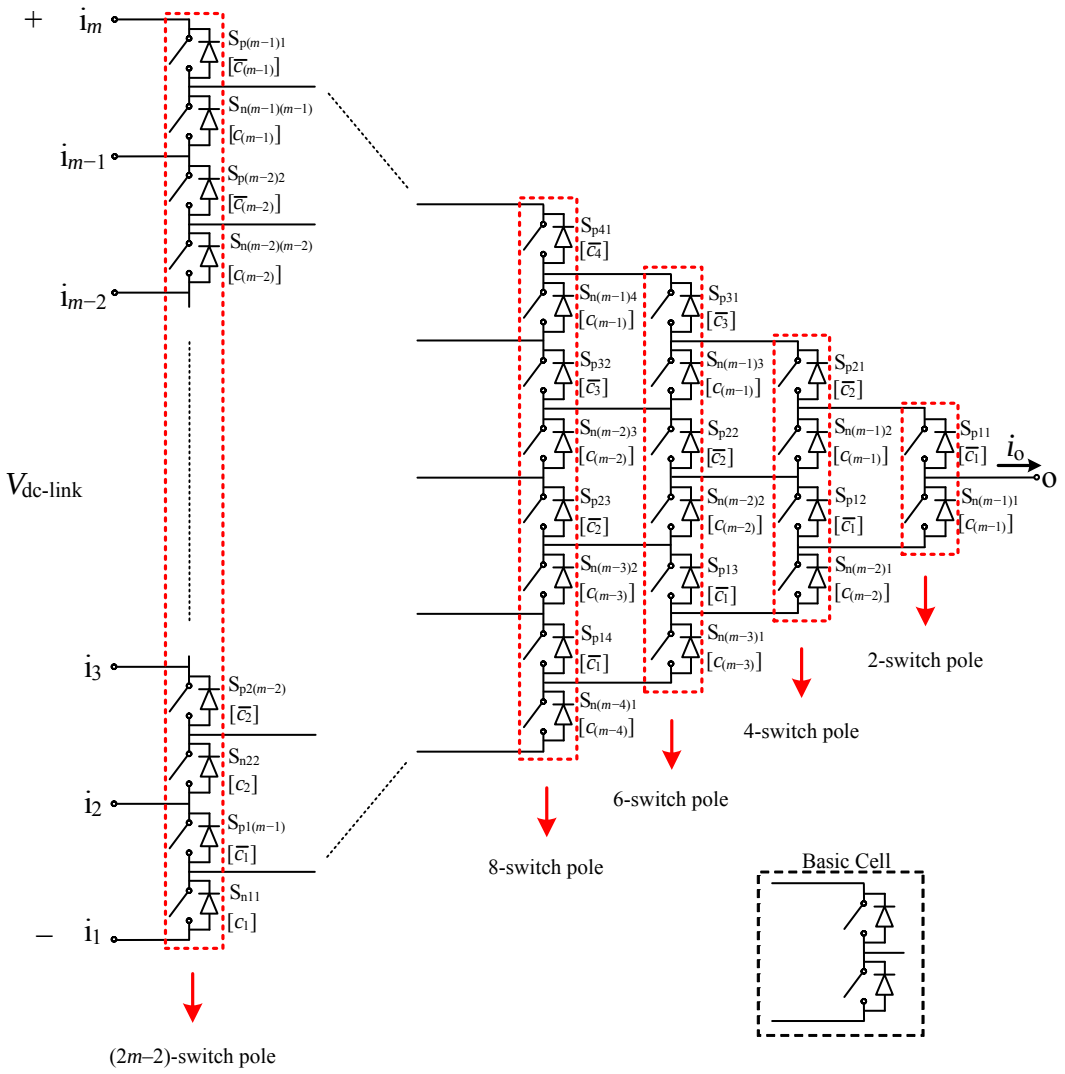


Fig. 2.1. Multilevel active-clamped converter leg topology (m-level leg).

adjacent input terminals, being the dc voltage of each of these components typically the same $(V_{\mathrm{dc-link}}/(m-1))$.

Removing all the flying capacitors allows generating the topology from a single device (e.g., metal-oxide semiconductor field-effect transistor (MOSFET), where the diodes in the topology of Fig. 2.1 can be implemented through the MOSFET body diode) and opens new operational possibilities that are explored in next sections.

The topology proposed in [52] and presented in Fig. 1.10 is similar to the one presented here. However, in that topology the pole of flying capacitors closer to the input terminals is preserved. Besides preserving these flying capacitors, the operating principle proposed in [52] differs significantly from the one presented here.

2.2.1. Operating principle

The functional model of the converter leg in Fig. 2.1 is equivalent to the functional model of a diode-clamped converter, where a single-pole *m*-throw switch allows the connection of the output terminal (o) to each of the *m* possible input terminals (i_k). A set of *m* switching states are defined to implement these *m* possible connections. The switching states are defined with the aid of *m*–1 independent control variables ($c_k\,; k \in \{1, 2, \ldots, m-1\}$) and their complementary values ($\bar{c}_k$), representing the state (ON: 1, OFF: 0) of the switches in Fig. 2.1. Each switch has an associated control variable, indicated within brackets in Fig. 2.1.

To connect the output terminal (o) to the input terminal (i_k), the control variable values are

$$\begin{aligned} c_j &= 0 \; (j < k) \\ c_j &= 1 \; (j \geq k) \; . \end{aligned} \tag{2.1}$$

Table 2.1 presents a summary of the *m* possible switching states, defined according to (2.1).

Switching State	Connection of 'o' to	c_1	c_2	c_3	…	c_k	…	c_{m-1}
1	i_1	1	1	1	…	1	…	1
2	i_2	0	1	1	…	1	…	1
3	i_3	0	0	1	…	1	…	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
k	i_k	0	0	0	…	1	…	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
m	i_m	0	0	0	…	0	…	0

Table 2.1. Control variables to define the switching states.

Fig. 2.2 presents these switching states in the particular case of a five-level converter leg. The uncircled switches are OFF-state devices. The circled switches are ON-state devices. The solid-line circled switches connect the output terminal to the desired input terminal and conduct the output terminal current (i_o), highlighted in red in Fig. 2.2. The arrows indicate the direction of the current flow through these switches if output current i_o is positive. The dotted-line circled switches do not conduct any significant current and simply clamp the blocking voltage of the OFF-state devices to the voltage across adjacent input terminals (i_k and i_{k+1}), which is usually equal to $(V_{\mathrm{dc-link}}/(m-1))$.

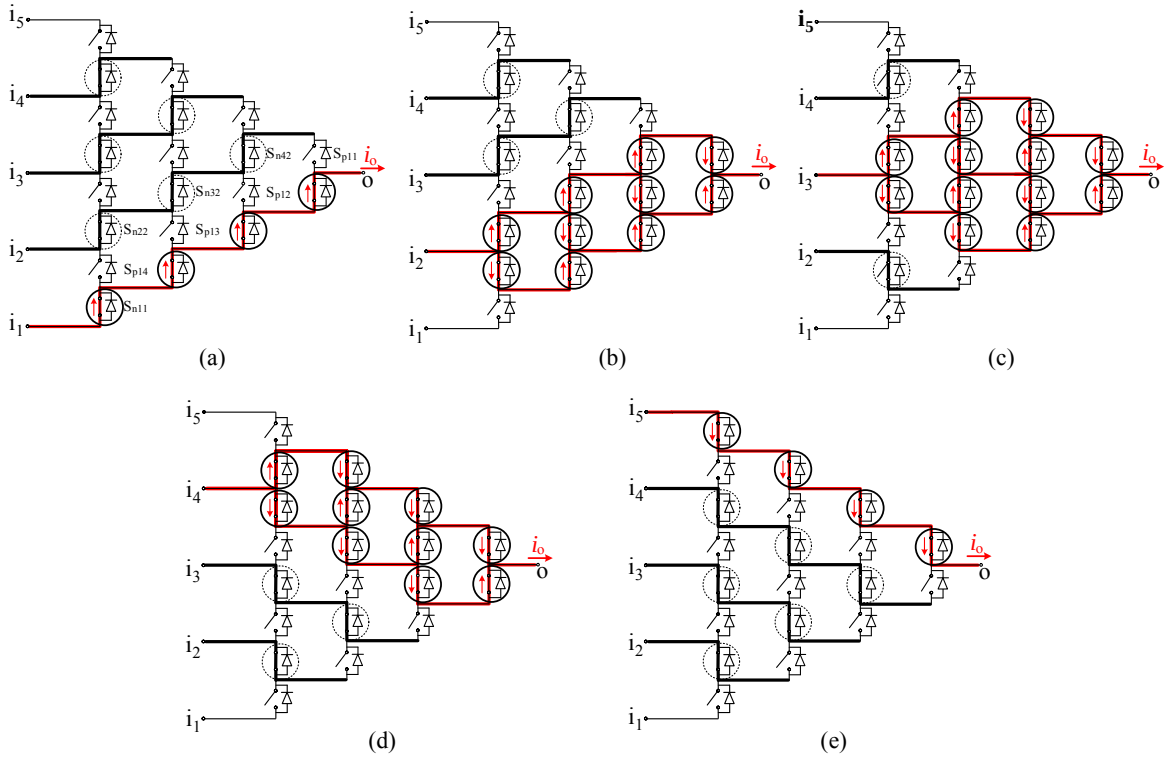


Fig. 2.2. Five-level converter-leg switching states. (a) Connection to node i_1. (b) Connection to node i_2. (c) Connection to node i_3. (d) Connection to node i_4. (e) Connection to node i_5.

It can be observed that the connection of the output terminal to the inner input terminals i_k $(k \in \{2, \ldots, m-1\})$ presents more than one path of m–1 series-connected ON-state switches to conduct the output current. The distribution of the output current i_o through the different current paths will depend upon the switch characteristics, state, and parasitics. If MOSFETs are used, in which the ON resistance presents a positive temperature coefficient, current will be properly distributed through the solid-line circled devices.

In the five-level example of Fig. 2.2, the transition from switching state 1 (Fig. 2.2(a)) to switching state 2 (Fig. 2.2(b)) requires changing the state of five switches: S_{n11} has to be turned off and S_{p11}, S_{p12}, S_{p13}, S_{p14} have to be turned on. Note that S_{n22}, S_{n32}, and S_{n42} do not need to change their control state because they were already ON in Fig. 2.2(a). As can be observed in Fig. 2.2, the transition between any two other switching states also requires changing the state of only five switches.

In a general m level converter leg, the transition between two adjacent switching states (k and k+1) requires changing the state of m switches. The transition from switching state k to switching state k+1 requires turning off k diagonal switches (S_{nkj}, j = 1, 2, …, k) and turning on m–k diagonal switches (S_{pkj}, j = 1, 2, …, m–k). Obviously, the transition from switching state k+1 to

switching state k requires turning off $m–k$ switches (S_{pkj}, j = 1, 2, …, $m–k$) and turning on k diagonal switches (S_{nkj}, j = 1, 2, …, k).

In the transition between adjacent switching states, it is required to first turn off the devices to be turned off. Then, after a proper dead time, we can proceed to turn on the devices to be turned on. Although m devices change their state, the switching losses (turn-on and turn-off losses) are basically concentrated in one device.

If $(k_f–k_i)\cdot i_o<0$, where k_i and k_f are the initial and final switching states, respectively; then, the switching losses concentrate on the last switch being turned off. All the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is nearly zero.

If $(k_f–k_i)\cdot i_o>0$; then, the switching losses concentrate on the first switch being turned on. As before, all the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is nearly zero.

2.3. Discussion

The converter leg in Fig. 2.1 can be employed to implement the same converter configurations as with a diode-clamped topology. Fig. 2.3(a) and Fig. 2.3(c) show two possible configurations connecting capacitors between adjacent input terminals to form a dc-link. Fig. 2.3(a) represents a five-level boost-buck dc-dc converter with common grounding for the source and load systems [57]. Fig. 2.3(c) represents a multiphase dc-ac conversion system (it can also be used for dc-dc conversion applications not requiring a common grounding for the load and source). In a single phase configuration, two converter legs are needed. In a multiphase system with p phases, p converter legs are needed. The balancing of the dc-link capacitor voltages can be guaranteed in every switching cycle through using appropriate PWM strategies ([21]-[22]) and controls [23], without the need of introducing additional hardware. The balance is achieved by extracting, in every switching cycle, a zero average current from the inner dc-link points. Alternatively, other solutions can be employed [58].

If the dc-link capacitors can be replaced by dc-voltage sources, the operational capabilities of the converter significantly improve (higher efficiency, lower output-voltage distortion, …), because the capacitor voltage balance is no longer a problem and more degrees of freedom are available to design the PWM strategies. Fig. 2.3(b) shows an example of a possible dc-dc or dc-ac converter configuration using a single converter leg.

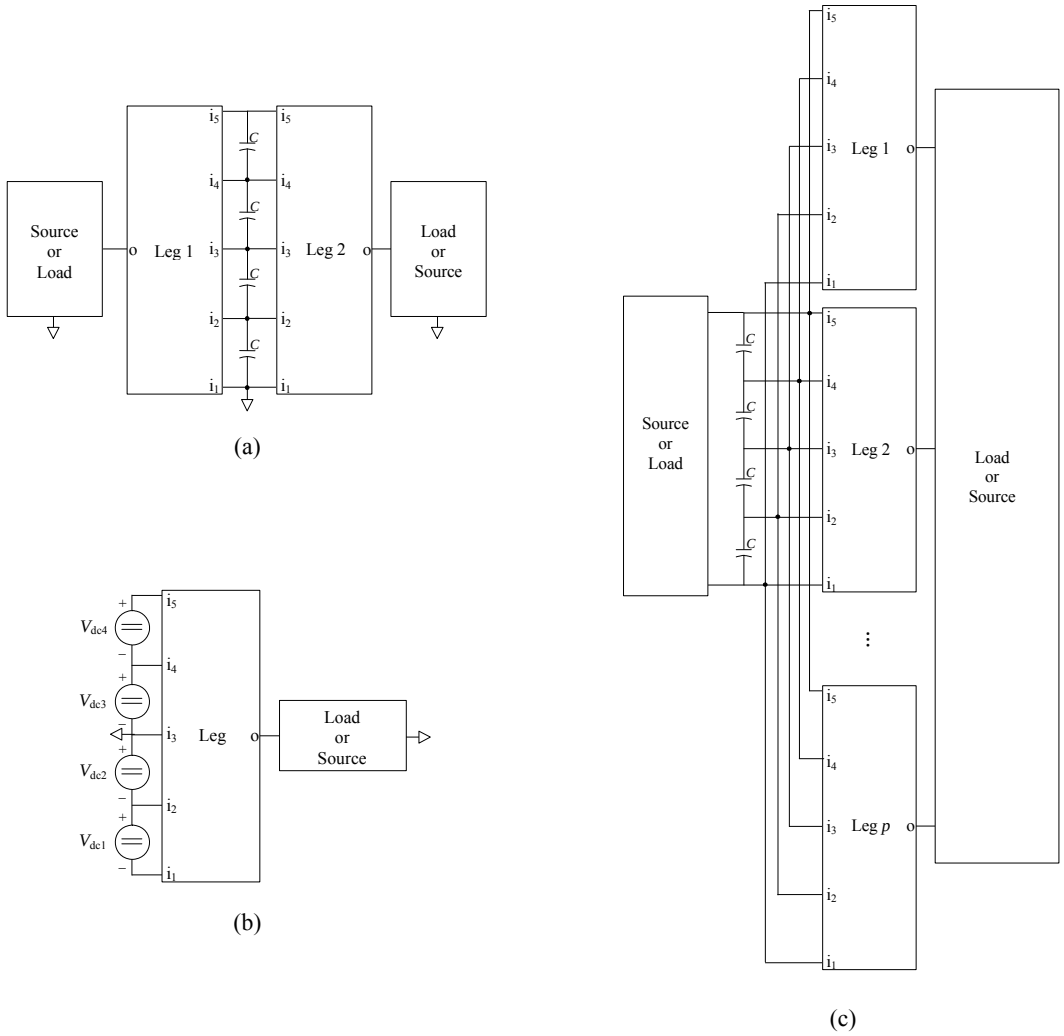


Fig. 2.3. Converter configurations (five-level example). (a) Boost-buck dc-dc converter with dc-link capacitors. (b) Dc-dc or dc-ac single-phase converter with dc-link voltage sources. (c) Multiphase dc-ac converter with dc-link capacitors.

The converter leg topology of Fig. 2.1 presents a total of $m\cdot(m–1)$ controlled switching devices. The number of switches is clearly higher than in alternative topologies. However, these extra switches provide some advantages.

Compared to diode-clamped topologies, the proposed topology clamps the blocking voltage of all devices to $V_{\mathrm{dc-link}}/(m-1)$ (this is not the case in diode-clamped topologies under certain operating conditions [39]), may present lower conduction losses (due to the availability of several paths for the current to flow, while there is only one possible path in diode-clamped topologies), and allows distributing the switching losses among all the devices (see Chapter 3) while in a diode-clamped topology, switching losses arise in the available switches.

Compared to topologies with flying capacitors, the proposed topology avoids dealing with the precharge of the flying capacitors or the losses and high spike currents that occur when flying

capacitors with different voltages are connected in parallel [51]. The cost and reliability of these capacitors can also be a problem.

In cases where separate dc-voltage sources are available (e.g. Fig. 2.3(b)), the comparison with cascaded H-bridge topologies is also meaningful. Despite using a significantly higher number of devices, the proposed topology allows operating with a common dc-link for all legs and dc-link node voltages that are constant with respect to ground. In a cascaded H-bridge topology, these dc-link node voltages may oscillate at high frequency, requiring galvanic isolation of the dc voltage source terminals and producing common mode currents through parasitic elements that could be a problem in the design.

Against conventional two-level converter configurations, efficiency is expected to be higher since both conduction losses and switching losses should be lower if proper devices are selected. With regard to reliability, it might be seen as an important drawback of the presented topology because of the use of a high number of components. However, while in a two-level converter the failure of one switch usually leads to a full system shut down, here the converter may continue operating, with obviously some reduction of the converter performance capabilities.

In Chapters 3 and 4, the efficiency and the fault-tolerance ability of the proposed MAC converter are analyzed in depth, respectively.

In principle, the proposed topology could be used to replace diode-clamped topologies in any application where these topologies are of interest, because both topologies are functionally equivalent. It is the understanding of the author that the proposed topology can be competitive in applications with a reasonable number of levels and requiring devices with voltage ratings lower than 600 V (due to a major feasibility of integrating the controlled device auxiliary circuits: gate driver, gate driver power supply, etc.). In particular, medium and low power/voltage motor drives could be an interesting application, where the advantage of using multilevel diode-clamped converters has already been proven [59], [60]. For instance, the proposed topology could be of interest for the traction inverter of electric vehicles. Typically, the voltage of the battery powering the conventional two-level inverter is limited (e.g., to 300 V) due to the difficulties in balancing the charge of a high number of battery cells in series. This leads to high motor currents or to the need to include a boost converter to raise the dc-link voltage level of the inverter. The proposed topology would allow connecting in series several batteries to raise the dc-link voltage and, with a proper modulation strategy and control, guarantee the charge balance among these batteries.

2.4. Simulation results

This section presents simulation results to illustrate the performance of the proposed topology and control strategy. A simple four-level boost-buck dc-dc converter configuration, shown in Fig. 2.4, is selected to facilitate the presentation and discussion of results. The modulation strategy applied is described in [57]. Modulation Scheme 2 and a value of the modulation parameter $\delta = 0.25$ are chosen to produce an output voltage equal to the input voltage (V_A=V_B) [57]. The simulations are performed using SPICE-based software.

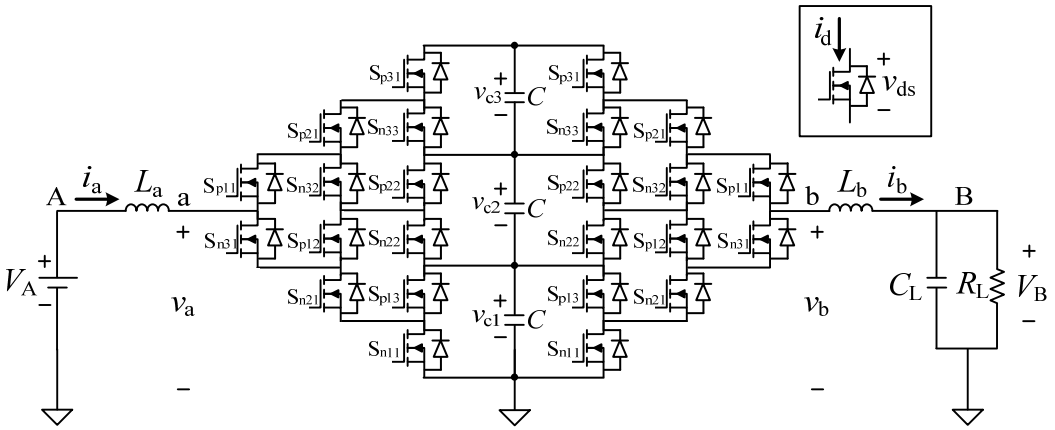
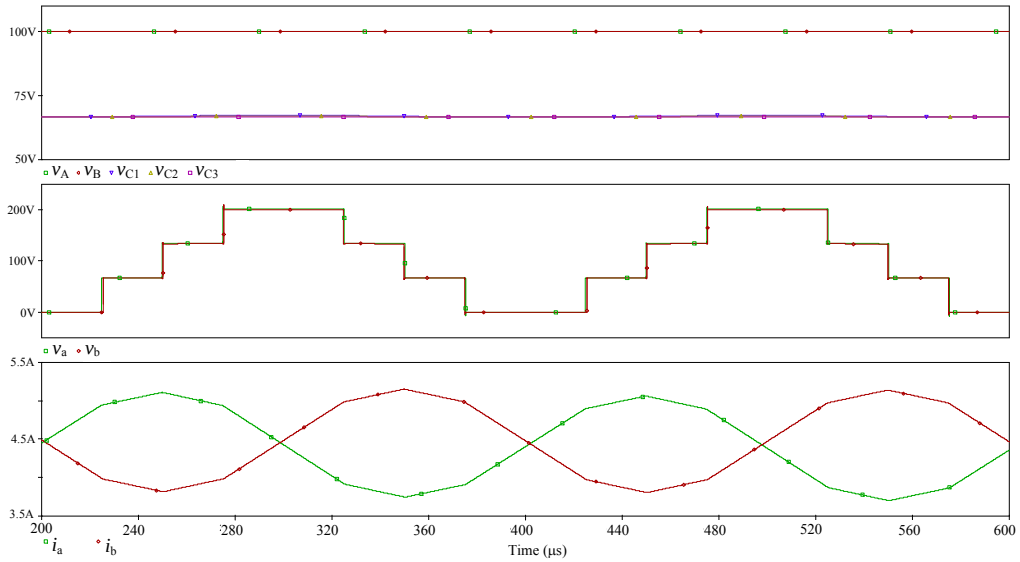


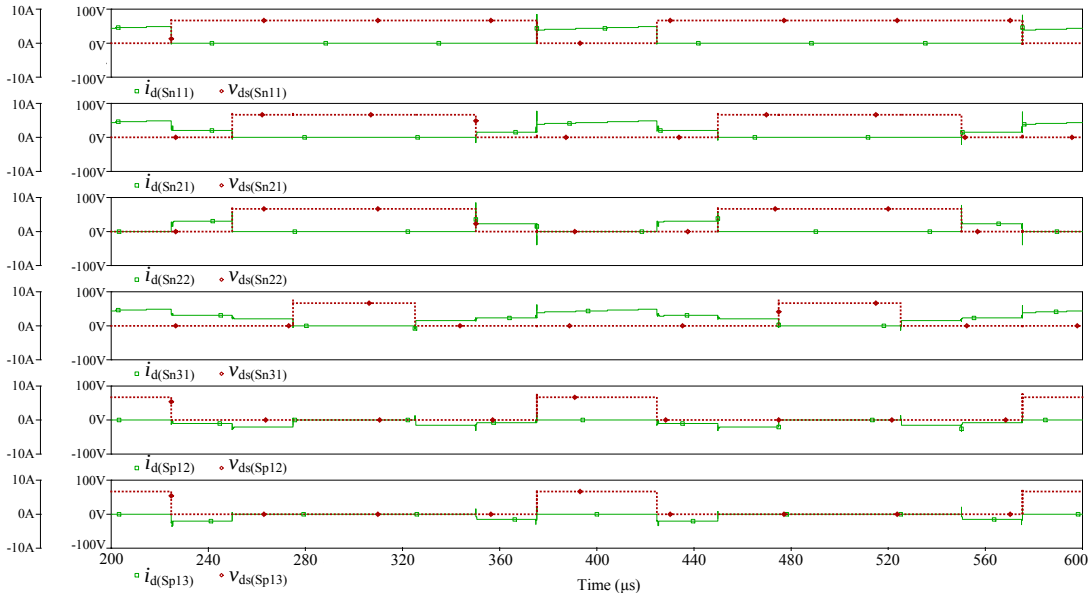
Fig. 2.4. Four-level boost-buck dc-dc converter implemented with MOSFETs.

Fig. 2.5 presents relevant waveforms over two switching cycles. In Fig. 2.5(a), note that the dc-link capacitor voltages (v_{c1}, v_{c2}, and v_{c3}) are balanced at the end of every switching cycle because a zero switching-cycle-averaged current is injected into the inner dc-link points. Note also that the output leg currents (i_a and i_b) present an almost sinusoidal shape. This implies that the output leg currents present essentially only one harmonic at the switching frequency (see Fig. 2.6), as opposed to a conventional two-level converter, where the output leg currents, presenting a triangular shape, include additional harmonics at multiples of the switching frequency.

Fig. 2.5(b) presents the current and voltage of each switch in the bottom half of the input converter leg. As can be observed, in each switching state, the output current is conducted through all ON-state devices that connect the corresponding input terminal to the output terminal. The output current is shared by all possible current paths. The average conduction losses are in general different for each device.



(a)



(b)

Fig. 2.5. Simulation results over two switching cycles in the following conditions: V_A = 100 V, C_L = 100 µF, $L_a = L_b$ = 5 mH, R_L = 22 Ω, C = 470 µF, switching frequency f_s = 5 kHz, FDPF3860T (100 V, 20 A MOSFETs), gate resistance R_g = 10 Ω, gate supply voltage V_g = 10 V, dead time t_d = 500 ns, and no output voltage regulation (open-loop control). (a) Input and output dc voltages (v_A, v_B), dc-link capacitor voltages (v_{C1}, v_{C2}, v_{C3}), leg-output voltages (v_a, v_b), leg-output currents (i_a, i_b). (b) Voltages and currents of the switches from the bottom half of the input converter leg.

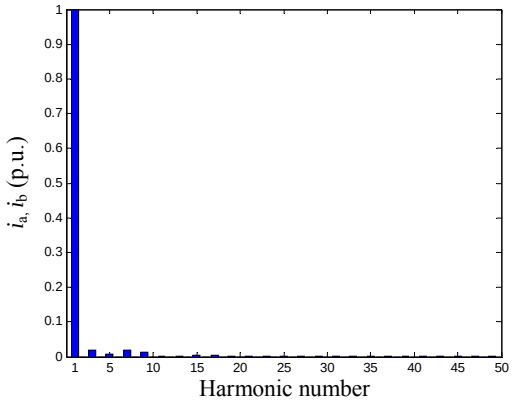
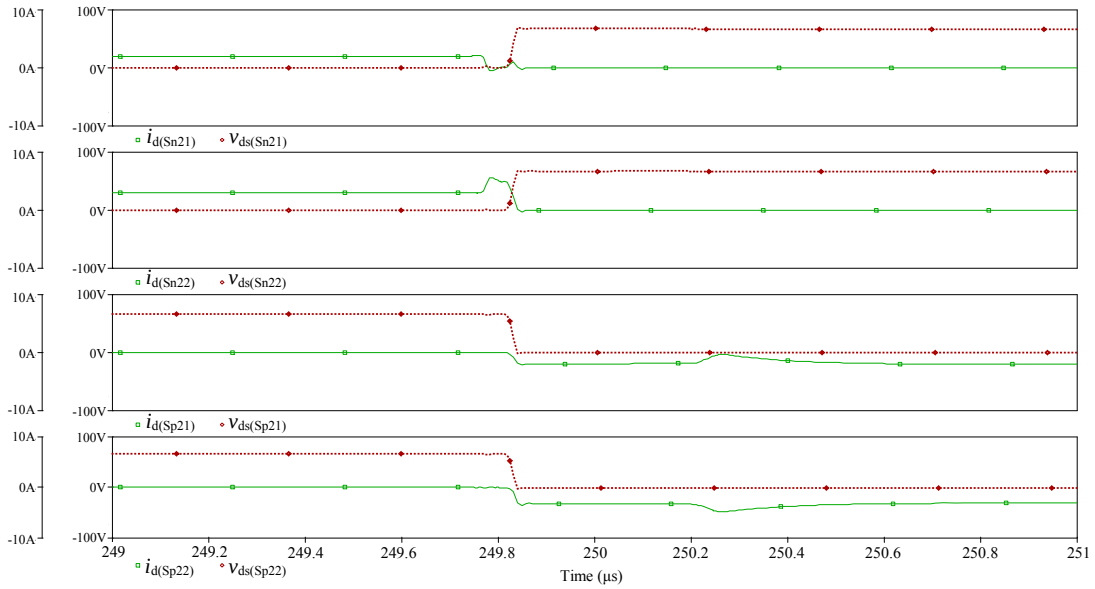
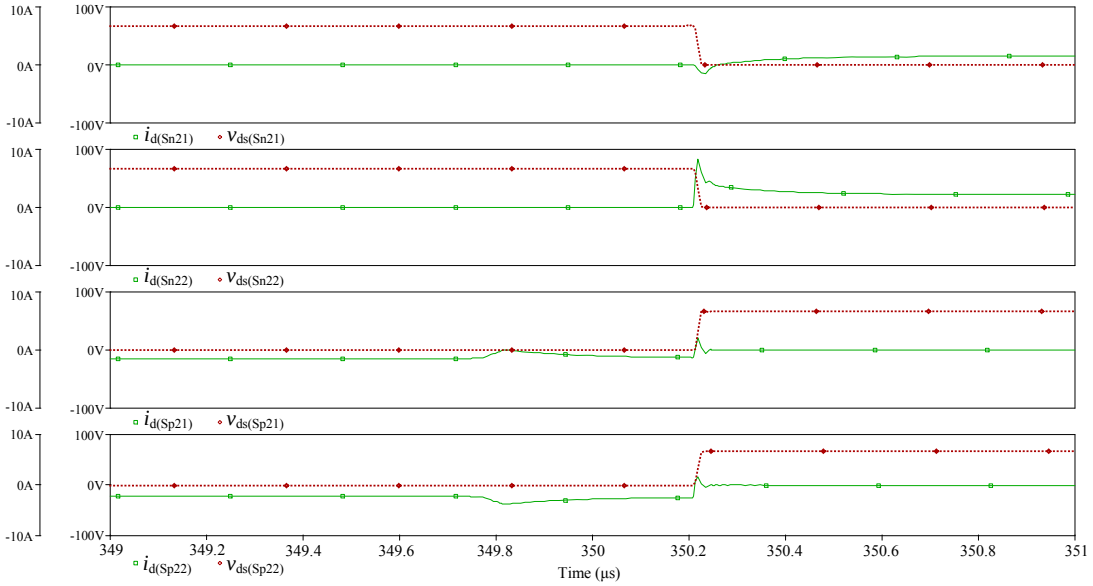


Fig. 2.6. Per unit harmonic spectrum of the leg-output currents (i_a, i_b).

The gating signals of the last six-switch pole (S_{n11}, S_{p13}, S_{n22}, S_{p22}, S_{n33}, and S_{p31}) have been adjusted so that these devices are the first to be turned-on and the last to be turned-off in a switching state transition and, therefore, they concentrate the switching losses. Fig. 2.7 presents the relevant switch current and voltage waveforms under a transition from switching state 2 to 3 (Fig. 2.7(a)) and a transition from switching state 3 to 2 (Fig. 2.7(b)). In Fig. 2.7(a), S_{n21} is initially turned off at *time* = 249.75 μs. S_{n22} is turned off 50 ns later. At *time* = 250.2 μs, S_{p22} is turned on. S_{p21} is turned on 50 ns later. In Fig. 2.7(b), S_{p21} is initially turned off at *time* = 349.75 μs. S_{p22} is turned off 50 ns later. At *time* = 350.2 μs, S_{n22} is turned on. S_{n21} is turned on 50 ns later. In both cases, as desired, switch S_{n22} concentrates the switching losses. The other devices change their state at zero voltage with no significant losses.



(a)



(b)

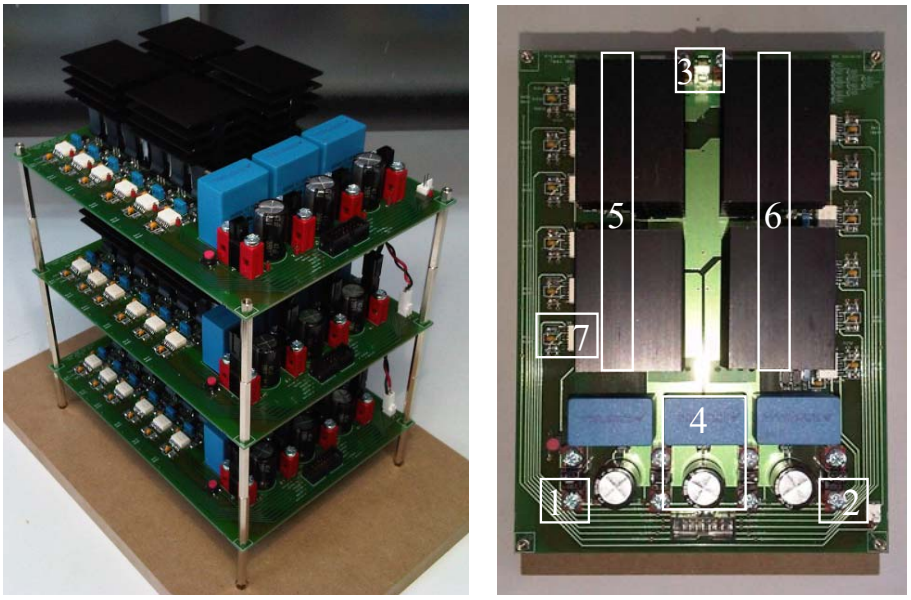
Fig. 2.7. Simulation results over switching state transitions in the same conditions of Fig. 2.5. (a) Transition from switching state 2 to switching state 3. (b) Transition from switching state 3 to switching state 2.

2.5. Experimental results

A four-level three-leg converter prototype with small dc-link capacitors has been designed and built using FDPF3860T (100 V, 20 A) MOSFETs (see Fig. 2.8). The converter consists in three identical legs. Each leg contains twelve MOSFETs and their corresponding drivers. Each gate driver is powered through a simple and small circuit connected across the controlled device, as it is explained in Appendix A. This circuit recycles part of the switching losses to power the gate driver. As a result, no external gate driver power supplies are required [61].

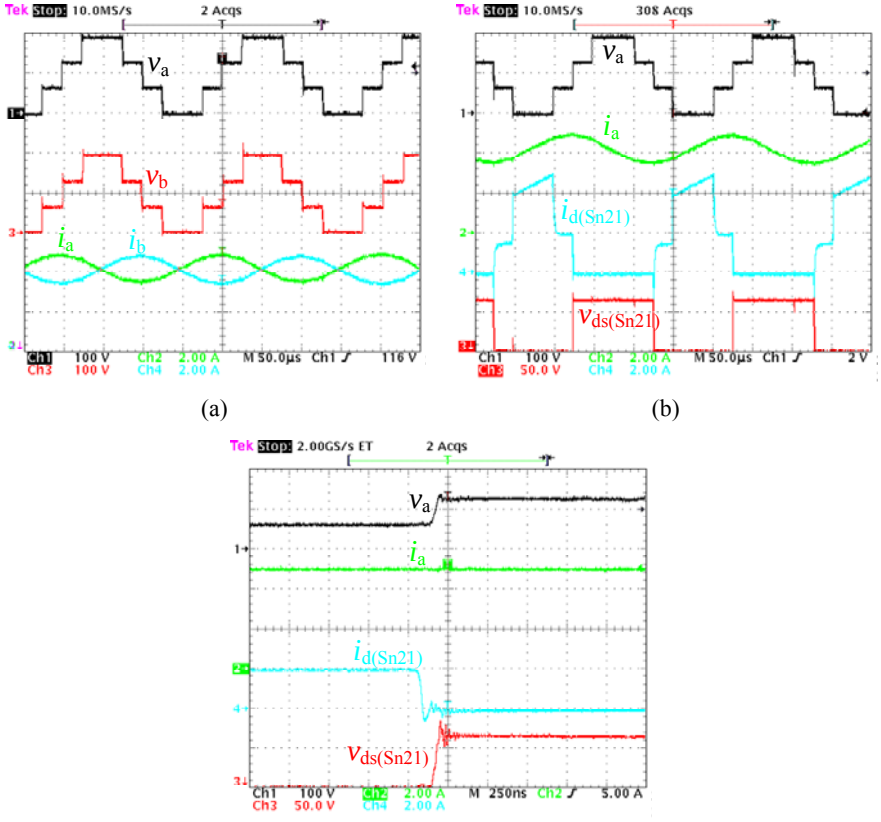
Fig. 2.9 presents experimental results with the converter configuration of Fig. 2.4 (dc-dc converter with two legs) and conditions of Fig. 2.5. The converter control, PWM strategy, and the generation of the switch control signals are implemented using dSpace DS1103 and an Altera EPF10K70 programmable logic device. Fig. 2.9(a) and Fig. 2.9(b) show the leg output voltages, the leg output currents, and the voltage and current through device S_{n21} over 2.5 switching cycles. Fig. 2.9(c) shows the detail of the soft turn-off of S_{n21} during the transition from switching state 2 to switching state 3. The experimental results fairly agree with the simulations.

Fig. 2.10 presents experimental results of a four-level three-phase dc-ac converter with a single dc-voltage source ($V_{\mathrm{dc-link}}$) connected across the dc-link and a three-phase wye-connected series resistive-inductive load. In this case, the virtual-space-vector pulse-width-modulation (V^2PWM) proposed in [22] is applied. Clean sinusoidal output current waveforms are generated



(a) (b)

Fig. 2.8. Four-level three-leg converter prototype with dc-link capacitors. (a) Full converter built upon three legs. (b) Top view of one leg (1: Input terminal i_1; 2: Input terminal i_4; 3: Output terminal; 4: middle dc-link capacitors; 5: Six bottom switches; 6: Six upper switches; 7: Internal gate-driver power-supply circuit).



(a) (b)

(c)

Fig. 2.9. Experimental results in the same conditions of Fig. 2.5. (a) Leg-output voltages and currents. (b) Voltage and current of switch S_{n21} with the corresponding leg output voltage and current as a reference. (c) Detail of the soft turn-off of S_{n21} during the transition from switching state 2 to switching state 3.

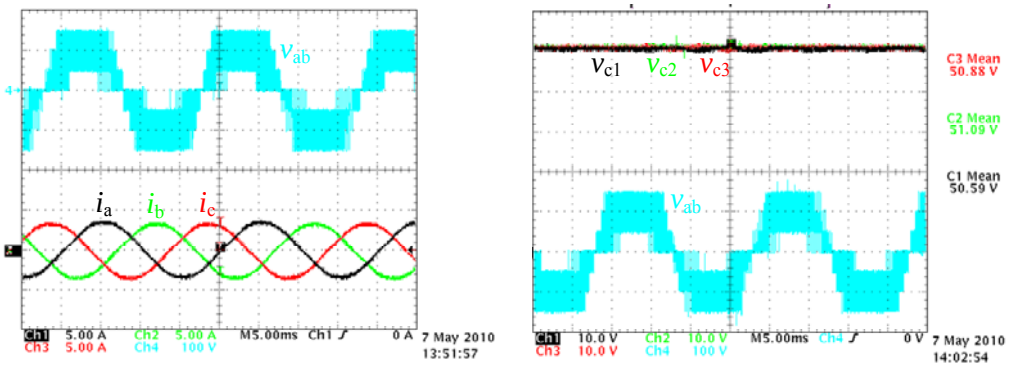


Fig. 2.10. Experimental results in a four-level three-phase dc-ac converter under the V²PWM for the output line-to-line voltage (v_{ab}), phase currents (i_a, i_b, and i_c), and dc-link capacitor voltages (v_{c1}, v_{c2}, and v_{c3}), in the following conditions: $V_{dc\text{-}link}$ = 150 V, mi = 0.75, C = 155 μF, f_s = 5 kHz, and a balanced load with per-phase impedance Z_L = 17.2 Ω∠16° (series R-L load).

with balanced dc-link capacitor voltages under a fairly high modulation index ($mi = V_{\text{l-l,pk}}/V_{\text{dc-link}}$, where $V_{\text{l-l,pk}}$ is the peak value of the fundamental component of the line-to-line voltage) and under the absence of any additional hardware.

On the other hand, this modulation produces a higher number of switching transitions per leg and switching cycle than alternative modulations, which implies higher degrees of freedom to balance the losses among the devices (thanks to the possibility of concentrating the switching losses in selected devices). In addition, since this modulation extends the portion of the line cycle where individual devices turn on and off at the carrier frequency (better switch utilization), it produces lower junction temperature variations than conventional modulation strategies [62].

2.6. Conclusion

The multilevel active-clamped topology and its operating principle have been defined. The topology is an extension of the three-level active neutral-point-clamped converter. Switching states are defined so that all possible current paths connect the corresponding input terminal to the output terminal and blocking voltages are clamped to the desired level.

If a particular device (e.g., MOSFET) at specific voltage and current ratings is available with good performance, low cost, and ideally integrated auxiliary circuitry (gate driver, gate driver power supply [61], ...); then, this topology and control could be applied to implement a universal and easily scalable converter to be used in a number of applications.

CHAPTER 3

EFFICIENCY ASSESSMENT OF THE MULTILEVEL ACTIVE-CLAMPED TOPOLOGY

Abstract — One of the key features to evaluate in the MAC converter is its efficiency. This chapter presents an in-depth analysis of losses and efficiency of the MAC topology. Initially, power-device conduction and switching losses are analyzed, providing the models to calculate them in the MAC topology. Then, the efficiency of the novel topology is assessed comparing it with conventional two-level converters under a particular selection of MOSFETs. Comparisons are performed under different scenarios and by means of analytical studies and experimental tests. The efficiency of the MAC topology is higher in all the switching-frequency range. Finally, an additional study comparing the minimum chip area needed for the MAC topology and for a conventional two-level topology is presented.

3.1. Introduction

The necessity of conceiving highly-efficient power-conversion systems has always been an important challenge for power-converter designers. Nowadays, applications such as photovoltaic grid inverters, rectifiers, or automotive motor drive systems, among others, demand for an outstanding efficiency at low cost, size and weight. In order to have small passive components and a light-weight system, the switching frequency has to be increased, which leads to higher switching losses and lower system efficiency.

According to several analyses reported in the literature [57], [60], [62]-[68], multilevel converters present a higher efficiency than conventional two-level converters for high switching frequencies, since the converter losses present a flatter dependency on the switching frequency.

References [57], [60], [63]-[65] present analytical comparisons between different multilevel converter structures and conventional two-level topologies for different low-, medium-, and high-voltage applications. In general, these studies conclude that multilevel converters present a higher efficiency than two-level converters, mainly when switching frequency is above 5-10 kHz. Reference [66] verifies experimentally the higher efficiency of five- and nine-level diode-clamped topologies compared to a conventional two-level one, operating as inverters. Reference [67] compares analytically the efficiency of the NPC topology with the ANPC topology. The efficiency is similar in both cases but the ANPC presents better loss distribution. In reference [68], a loss and efficiency analysis of a three-level capacitor-clamped dc-dc converter is presented. Losses and efficiency are first estimated and then are measured experimentally. Finally, both results are compared.

This chapter presents an analysis of losses and efficiency of the MAC topology. The chapter is organized as follows.

Section 3.2 discusses the fundamental benefits of multilevel conversion in power-device conduction and switching losses. Section 3.3 studies the conduction and switching losses in the MAC topology and provides analytical loss models to calculate them. In Section 3.4, an efficiency comparison between a four-level MAC leg and a conventional two-level leg operating at low voltage under a simple control scheme is carried out. The losses and efficiency are first estimated according to the loss models presented in Section 3.3. Then, experimental tests are performed to measure the overall losses and efficiency of both topologies. Finally, the estimated and experimental results are compared to validate the analytical loss models. Using the validated loss models, Section 3.5 presents an efficiency comparison between the MAC converter and a two-level converter operating as three-phase inverters. In Section 3.6, a theoretical approach to calculate the minimum chip area of a topology is presented. Using the method, the chip areas of a four-level MAC leg and a conventional two-level leg operating under the control scheme defined in Section 3.4 are calculated and compared. Finally, Section 3.7 outlines the conclusions.

3.2. Fundamental factors of loss reduction in multilevel conversion

The objective of this section is to highlight the fundamental benefits of multilevel converters in conduction and switching losses. For the different analyses, let us assume that MOSFETs are used. Some of the deductions presented, however, are also applicable for other controlled power switches, e.g., IGBTs.

3.2.1. Conduction losses

One important particularity of MOSFET devices is that their per-unit-area ON-state drain-to-source resistance $r_{\mathrm{ds(on)}}$ increases rapidly with the device blocking voltage. Traditionally, this fact has discarded MOSFET devices for being used in high-voltage two-level converters. Trying to reduce this dependence has always been a big challenge for power-device designers. In the past, according to [69], [70], the resistivity $r_{\mathrm{ds(on)}}$ as a function of the device blocking voltage BV_{ds} could be expressed as

$$r_{\mathrm{ds(on)}} = k\,(BV_{\mathrm{ds}})^{2.5\sim2.7}\,, \tag{3.1}$$

where k represents a constant that depends on the device geometry. Nevertheless, with nowadays developed technology for MOSFET devices based on the compensation principle [70], the

dependence of the resistivity $r_{\mathrm{ds(on)}}$ on BV_{ds} has been drastically reduced. According to [70], the correlation can be now expressed as

$$r_{\mathrm{ds(on)}} = k\,(BV_{\mathrm{ds}})^{1.3}\,. \tag{3.2}$$

Although the resistivity $r_{\mathrm{ds(on)}}$ has been decreased significantly, it still presents an appreciable exponential dependency with respect to the device blocking voltage.

In an arbitrary multilevel converter of *m* levels, in most topologies, a total of *m*–1 devices connected in series conduct the total output current. This means that multilevel converters may present lower conduction losses than conventional two-level converters if MOSFET devices are properly selected, according to (3.2). The conduction losses become lower as the number of converter levels is increased.

In the MAC topology, besides, there are several available paths in parallel for the current to flow when the output terminal is connected to the inner input terminals $\mathrm{i}_k\ \left(k \in \{2, \ldots, m-1\}\right)$ which further decreases the equivalent ON resistance. This represents an additional advantage of the MAC topology compared to two-level topologies and other multilevel topologies.

3.2.2. Switching losses

Let us analyze how the switching losses vary depending on the number of levels of a converter leg. The study is based on an analysis done in [57].

To simplify the study, it is initially assumed that diodes are ideal (lossless) and therefore they do not suffer reverse-recovery processes. Fig. 3.1 shows the switching patterns of ideal hard-switching turn-on and turn-off transitions under inductive load, where $v_{\mathrm{ds}}(t)$ and $i_{\mathrm{d}}(t)$ are the voltage across the switch and the current through the switch, respectively.

The energy lost in each one of the switching transitions is

$$E_{\mathrm{on}} = E_{\mathrm{off}} = \frac{V_{\mathrm{ds}} \cdot I_{\mathrm{d}} \cdot (T_{\mathrm{v}} + T_{\mathrm{i}})}{2}. \tag{3.3}$$

The voltage V_{ds} is equal to $V_{\mathrm{dc-link}}/(m-1)$, being *m* the number of levels of the leg (it is also valid in a two-level leg). Let us assume that the absolute values of the voltage slope during transitions $s_{\mathrm{v}} = v_{\mathrm{ds}}/T_{\mathrm{v}}$ and the current slope $s_{\mathrm{i}} = I_{\mathrm{d}}/T_{\mathrm{i}}$ are constant regardless of the number of

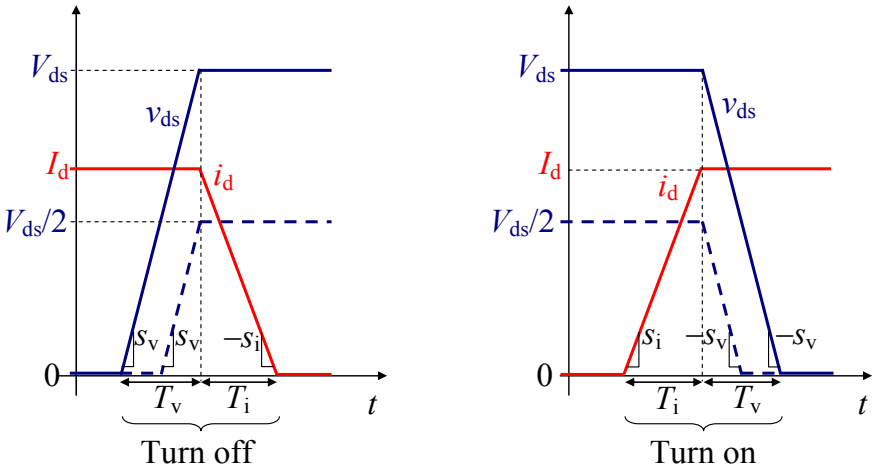


Fig. 3.1. Voltage and current waveforms during switching transitions in the controlled devices concentrating the switching losses.

levels m; i.e., independent of the value of V_{ds}. This assumption is based on the fact that these slopes can be adjusted properly through the gate-driver design parameters, and their value is typically limited by electromagnetic interferences and other specifications. With this assumption, the energy lost in a device in a turn-on or a turn-off transition is

$$E_{on} = E_{off} = \frac{V_{dc-link}{}^2 \cdot I_d}{2 \cdot s_v \cdot (m-1)^2} + \frac{V_{dc-link} \cdot I_d{}^2}{2 \cdot s_i \cdot (m-1)}. \tag{3.4}$$

Assuming a modulation scheme as the one presented in Fig. 3.2 in which the output terminal is connected to all the input levels, there are a total of $2 \cdot (m-1)$ switching-state transitions within the modulation period.

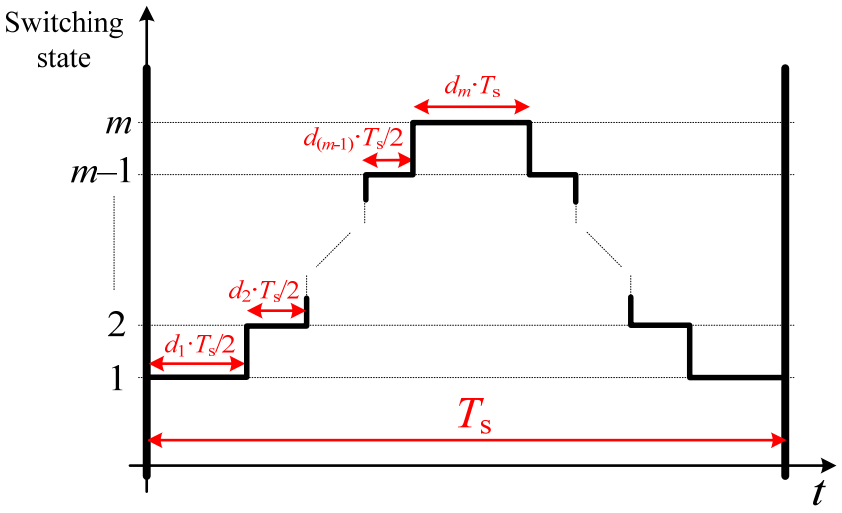


Fig. 3.2. Switching pattern within a modulation period of a m-level leg.

In each one of these transitions, one single device concentrates the switching losses (turn-on or turn-off losses depending on the current polarity and the initial and the final switching state). Thus the total switching energy loss in the *m*-level leg in a modulation period could be expressed as

$$E_{\mathrm{sw,leg},T_\mathrm{S}} = 2\cdot(m-1)\cdot\left[\frac{{V_{\mathrm{dc-link}}}^2\cdot I_\mathrm{d}}{2\cdot s_\mathrm{v}\cdot(m-1)^2}+\frac{V_{\mathrm{dc-link}}\cdot {I_\mathrm{d}}^2}{2\cdot s_\mathrm{i}\cdot(m-1)}\right]=\frac{{V_{\mathrm{dc-link}}}^2\cdot I_\mathrm{d}}{s_\mathrm{v}\cdot(m-1)}+\frac{V_{\mathrm{dc-link}}\cdot {I_\mathrm{d}}^2}{s_\mathrm{i}}. \quad (3.5)$$

As it can be seen in the expression (3.5), the energy loss becomes lower as the number of levels increases. This also can be deduced from Fig. 3.1. The dashed blue line would correspond to a device withstanding the half of voltage V_ds with the same slope s_v. It can be deduced that two times the energy loss of this device is less than one time the energy loss of a device withstanding the total voltage V_ds. The energy lost during T_i remains equal independently of the number of levels, but the energy lost during T_v decreases as the number of level increases. This means that the total reduction in switching losses will depend on the ratio between these two times.

Please also note that the modulation scheme of Fig. 3.2 represents the worst scenario for a multilevel leg since the output terminal is connected to all the input terminals, which implies the highest possible number of transitions within the switching cycle.

3.3. Loss analysis of the MAC topology

The conduction losses are analyzed first in Section 3.3.1 and the switching losses are analyzed later in Section 3.3.2.

The analysis of conduction losses is organized as follows. First, the distribution of the output current among the devices and the values of equivalent ON resistances for three-to-seven-level MAC legs are presented. Then, the expressions to calculate the conduction losses in an arbitrary *m*-level leg and individually for each device of the topology are deduced. Finally, the expressions obtained for calculating the conduction losses are applied to the case in which the MAC converter operates as a three-phase inverter under the V^2PWM.

The analysis of switching losses is organized as follows. First, the switching state transitions and the corresponding switching losses in a general *m*-level MAC leg are analyzed. Then, the switching losses for the particular case of a four-level leg are defined more accurately.

3.3.1. Conduction losses

3.3.1.1. Distribution of output current among the devices and equivalent ON-resistance

Fig. 3.3-Fig. 3.7 present the distribution of the output current among the devices for a three-, four-, five-, six-, and seven-level MAC leg. The coefficients c_{S_x,i_k}, presented in red color within brackets, represent the per-unit value of the total leg output current i_o that flows through the device S_x when the output terminal is connected to the input terminal i_k. Only the half of total connections to the leg input terminals are shown in due to the symmetry. Please also note the equivalent ON-resistances R_{eq,i_k} between the output terminal and the corresponding input terminal i_k in the insets of Fig. 3.3-Fig. 3.7. The values of coefficients c_{S_x,i_k} and resistances R_{eq,i_k} have been calculated assuming that all devices present the same ON resistance $R_{ds(on)}$.

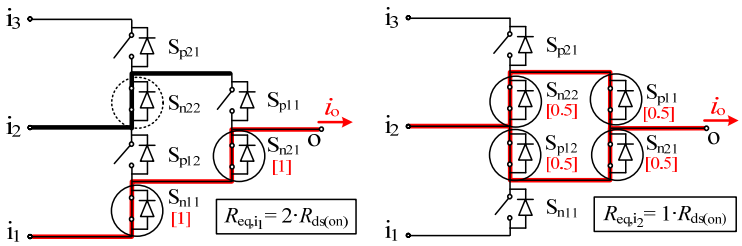


Fig. 3.3. Distribution of output current in a three-level MAC leg. (a) Connection to input terminal i_1. (b) Connection to input terminal i_2.

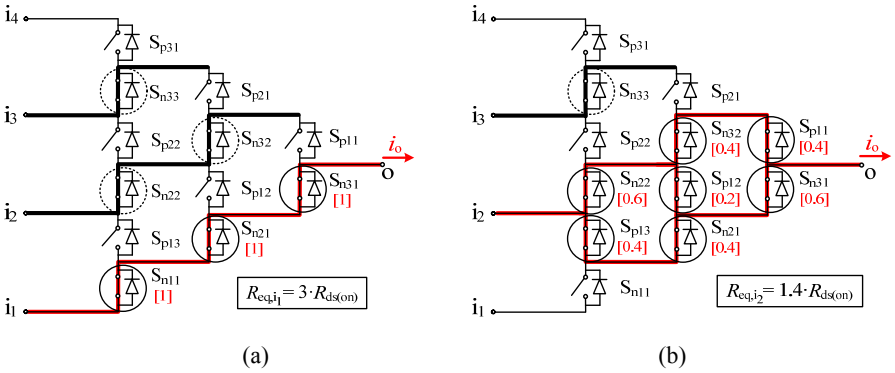


Fig. 3.4. Distribution of output current in a four-level MAC leg. (a) Connection to input terminal i_1. (b) Connection to input terminal i_2.

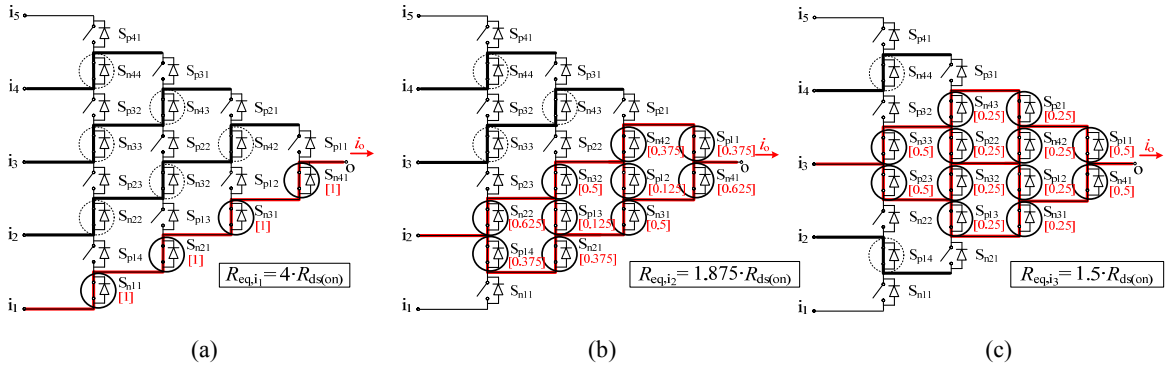


Fig. 3.5. Distribution of output current in a five-level MAC leg. (a) Connection to input terminal i_1. (b) Connection to input terminal i_2. (c) Connection to input terminal i_3.

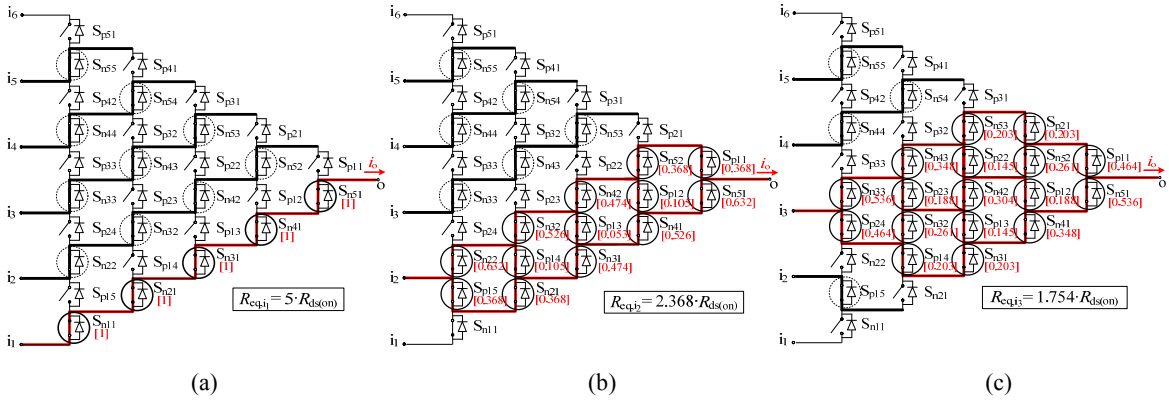
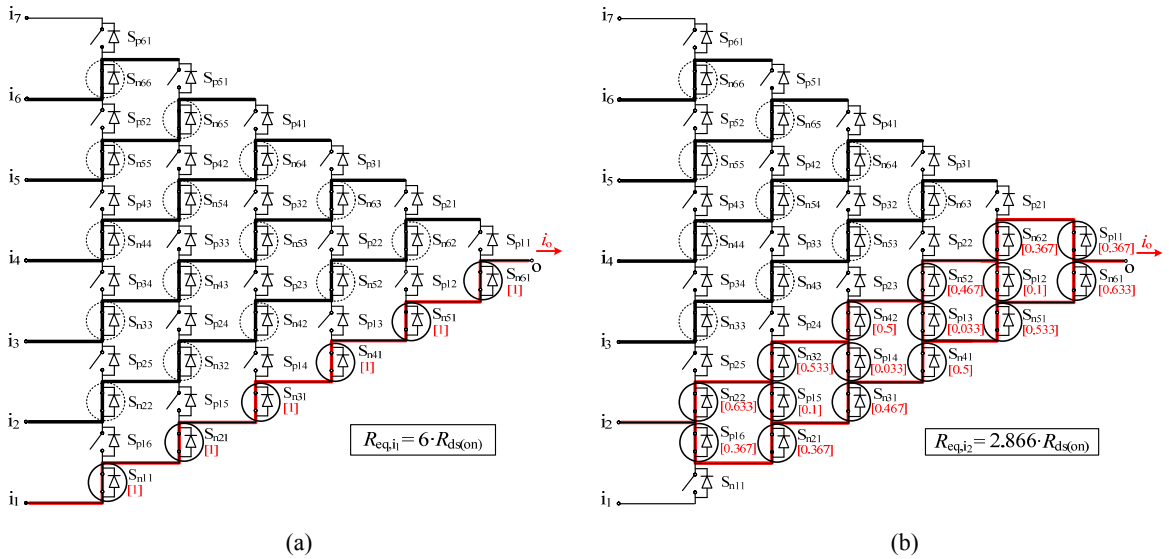


Fig. 3.6. Distribution of output current in a six-level MAC leg. (a) Connection to input terminal i_1. (b) Connection to input terminal i_2. (c) Connection to input terminal i_3.



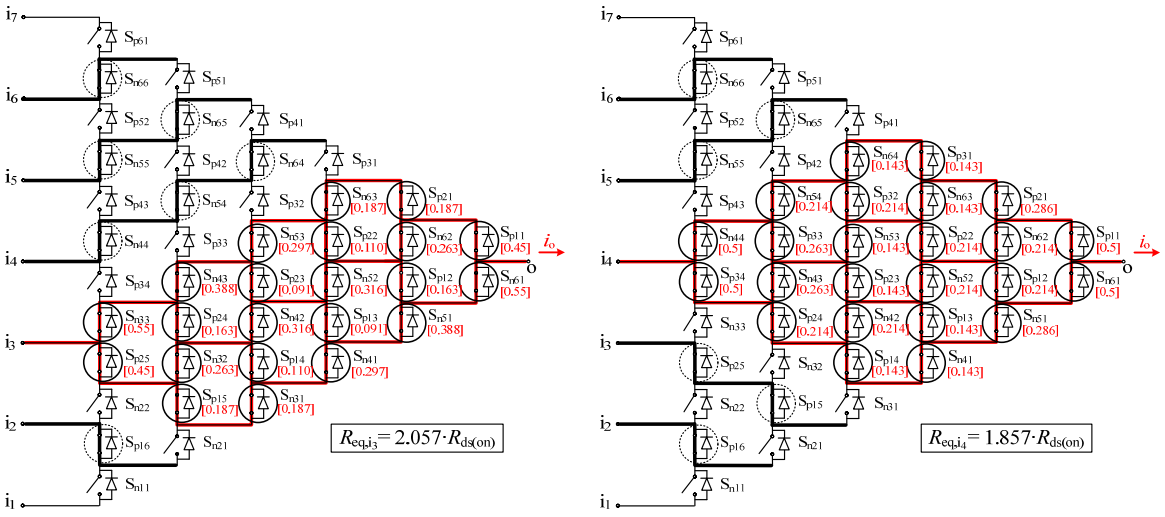


Fig. 3.7. Distribution of output current in a seven-level MAC leg. (a) Connection to input terminal i_1. (b) Connection to input terminal i_2. (c) Connection to input terminal i_3. (d) Connection to input terminal i_4.

It is important to have in mind that the values of coefficients $c_{\mathrm{S}_x,\mathrm{i}_k}$ are valid independently of the current direction. In case of using MOSFETs, for example, the value of the drain-to-source ON resistance $R_{\mathrm{ds(on)}}$ of each device is almost identical when the drain current flows in negative polarity as long as the MOSFET is in ON-state; i.e., most charges flow through the MOSFET channel instead of flowing through the antiparallel body diode. If IGBTs were used, for example, the distribution of current presented in Fig. 3.3-Fig. 3.7 would not be valid since IGBTs present different behavior depending on the current polarity.

Please note that for a certain switching state, the addition of coefficients $c_{\mathrm{S}_x,\mathrm{i}_k}$ that correspond to the same switch pole is always equal to 1. As an example, in a seven-leg, $c_{\mathrm{S_{n54}},\mathrm{i}_4} + c_{\mathrm{S_{p33}},\mathrm{i}_4} + c_{\mathrm{S_{p43}},\mathrm{i}_4} + c_{\mathrm{S_{p24}},\mathrm{i}_4} = 0.286 + 0.214 + 0.214 + 0.286 = 1$, see Fig. 3.7(d). This fact is logical since the total output current flows through each one of the leg switch poles. Coefficients $c_{\mathrm{S}_x,\mathrm{i}_k}$ are used to calculate the power-device conduction losses, as it is explained in the following sections.

Table 3.1 presents the normalized equivalent resistances $R_{\mathrm{eq,i}_k,\mathrm{norm}}$ for a three-, four-, five-, six-, and seven-level MAC leg. These values correspond to the $R_{\mathrm{eq,i}_k}$ presented in Fig. 3.3-Fig. 3.7, divided by $R_{\mathrm{ds(on)}} \cdot (m-1)$.

Switching state	3-level leg	4-level leg	5-level leg	6-level leg	7-level leg
1	1	1	1	1	1
2	0.5	0.4666	0.46875	0.4736	0.47766
3	1	0.4666	0.375	0.35072	0.34283
4	-	1	0.46875	0.35072	0.3095
5	-	-	1	0.4736	0.34283
6	-	-	-	1	0.47766
7	-	-	-	-	1

Table 3.1. Normalized equivalent ON-resistances $R_{eq,i_k,norm}$ of a three-, four-, five-, six-, and seven-level MAC leg.

From the analysis of Table 3.1, it can be better appreciated how much the conduction losses are reduced if the number of levels is increased. Regardless of the applied modulation scheme, the weight of all duty ratios of connection to the inner levels should increase as the number of levels increases; i.e., the weight of duty ratios of connection to the outer levels 1 and *m* should be lower. Consequently, overall conduction losses become lower as the number of levels increases.

Please also consider that in order to further reduce conduction losses, the devices of the outer diagonals could be parallelized with another equal device, reducing to one half the equivalent resistance of connection to the outer levels.

3.3.1.2. Conduction losses in a general m-level MAC leg

The conduction energy loss in a m-level leg during a switching period T_S can be calculated as

$$E_{\text{cond,leg},T_S} = \sum_{k=1}^{m} \left[\int_{t_k}^{t_k + d_k \cdot T_S} R_{\text{eq},i_k} \cdot {i_o}^2 \cdot dt \right], \tag{3.6}$$

where d_k represents the duty ratio of connection of the output terminal to the input terminal i_k, and t_k the instant of initial connection to i_k.

3.3.1.2.1. Constant output current

In case that output current i_o is constant, then the expression to calculate the leg conduction energy loss can be simplified as

$$E_{\text{cond,leg},T_S} = {I_o}^2 \cdot T_S \cdot \sum_{k=1}^{m} d_k \cdot R_{\text{eq,i}_k} . \tag{3.7}$$

Thus, the total conduction power loss of a leg if the output current is constant can be expressed as

$$P_{\text{cond,leg}} = {I_o}^2 \cdot \sum_{k=1}^{m} d_k \cdot R_{\text{eq,i}_k} . \tag{3.8}$$

It is assumed that duty ratios d_k are also constant.

3.3.1.2.2. Variable output current

As the switching period T_S is a very short time, the output current practically does not vary its magnitude within the switching period. Therefore, it can be assumed that the output current is constant within a switching cycle. As a result, (3.7) is also valid for a variable output current. If the switching period T_S is considered to be a differential of time dt, then the energy lost in a m-level leg during a differential of time dt can be expressed as

$$E_{\text{cond,leg},dt} = {i_o}^2 \cdot dt \cdot \sum_{k=1}^{m} d_k \cdot R_{\text{eq,i}_k} . \tag{3.9}$$

The total leg conduction-power-losses can be calculated as

$$P_{\text{cond,leg}} = \frac{1}{T_o} \int_0^{T_o} E_{\text{cond,leg},dt} \ , \tag{3.10}$$

where the time T_o is the period of the output current i_o. Combining (3.9) and (3.10), the leg conduction-power-losses can be calculated as

$$P_{\text{cond,leg}} = \frac{1}{T_o} \cdot \sum_{k=1}^{m} \left[R_{\text{eq,i}_k} \cdot \int_0^{T_o} \left(d_k \cdot {i_o}^2 \cdot dt \right) \right]. \tag{3.11}$$

If the leg operates as an inverter, the fundamental component of current i_o can be expressed as

$$i_o = I_{o,pk} \cdot \cos(\omega t - \varphi), \tag{3.12}$$

where $I_{\mathrm{o,pk}}$ is the peak value of the output current i_{o}, ω is the output current angular frequency in rad/s, and φ is the load line-to-neutral impedance angle. Substituting the output current i_{o} in (3.11) and applying the variable change $\theta = \omega t$, the final expression to calculate the leg conduction losses can be expressed as

$$P_{\mathrm{cond,leg}} = \frac{{I_{\mathrm{o,pk}}}^2}{2\pi} \cdot \sum_{k=1}^{m} \left[R_{\mathrm{eq,i}_k} \cdot \int_0^{2\pi} (d_k \cdot \cos^2(\theta - \varphi) \cdot d\theta \,) \right], \tag{3.13}$$

where angle θ corresponds to the line-cycle angle. Equation (3.13) is valid for a general *m*-level MAC leg under any modulation scheme.

3.3.1.3. Conduction losses per device in a general m-level MAC leg

The conduction energy lost in a device S_x during a switching period T_{S} can be calculated as

$$E_{\mathrm{cond,S}_x,T_{\mathrm{S}}} = \int_0^{T_{\mathrm{S}}} R_{\mathrm{ds(on)}} \cdot {i_{\mathrm{d(S}_x)}}^2 \cdot dt \,. \tag{3.14}$$

The device current $i_{\mathrm{d(S}_x)}$ depends on the connection to the input terminal i_k and the output current i_{o}, according to the coefficients $c_{\mathrm{S}_x,\mathrm{i}_k}$ defined above. Then, the device energy lost can be defined as

$$E_{\mathrm{cond,S}_x,T_{\mathrm{S}}} = R_{\mathrm{ds(on)}} \cdot \sum_{k=1}^{m} \left[\int_{t_k}^{t_k + d_k \cdot T_{\mathrm{S}}} \left(c_{\mathrm{S}_x,\mathrm{i}_k} \cdot i_{\mathrm{o}} \right)^2 \cdot dt \right]. \tag{3.15}$$

3.3.1.3.1. Constant output current

In case that output current i_{o} is constant, then the expression to calculate the energy loss can be simplified as

$$E_{\mathrm{cond,S}_x,T_{\mathrm{S}}} = R_{\mathrm{ds(on)}} \cdot {I_{\mathrm{o}}}^2 \cdot T_{\mathrm{S}} \cdot \sum_{k=1}^{m} \left[d_k \cdot {c_{\mathrm{S}_x,\mathrm{i}_k}}^2 \right]. \tag{3.16}$$

Thus, if the output current is constant, the device conduction power loss can be expressed as

$$P_{\mathrm{cond,S}_x} = R_{\mathrm{ds(on)}} \cdot {I_{\mathrm{o}}}^2 \cdot \sum_{k=1}^{m} \left[d_k \cdot {c_{\mathrm{S}_x,\mathrm{i}_k}}^2 \right]. \tag{3.17}$$

As before, it is assumed that duty ratios d_k are constant.

3.3.1.3.2. Variable output current

As before, the output current is approximately constant over a switching cycle. Thereby, (3.16) is also valid for variable output current. As before, if the switching period T_S is considered to be a differential of time dt, then the energy lost in a m-level leg during a differential of time dt can be expressed as

$$E_{\text{cond,S}_x,dt} = R_{\text{ds(on)}} \cdot {i_o}^2 \cdot dt \cdot \sum_{k=1}^{m} \left[d_k \cdot {c_{\text{S}_x,\text{i}_k}}^2 \right]. \tag{3.18}$$

The expression above is valid for any device of an m-level MAC leg under any modulation scheme. The device conduction-power-losses can be calculated as

$$P_{\text{cond,S}_x} = \frac{1}{T_o} \int_0^{T_o} E_{\text{cond,S}_x,dt} \ . \tag{3.19}$$

Combining (3.18) and (3.19), the device conduction-power-losses can be calculated as

$$P_{\text{cond,S}_x} = \frac{R_{\text{ds(on)}}}{T_o} \cdot \sum_{k=1}^{m} \left[{c_{\text{S}_x,\text{i}_k}}^2 \cdot \int_0^{T_o} \left(d_k \cdot {i_o}^2 \cdot dt \right) \right]. \tag{3.20}$$

If the leg operates as an inverter, the final expression to calculate the device conduction losses can be expressed as

$$P_{\text{cond,S}_x} = \frac{R_{\text{ds(on)}} \cdot {I_{\text{o,pk}}}^2}{2\pi} \cdot \sum_{k=1}^{m} \left[{c_{\text{S}_x,\text{i}_k}}^2 \cdot \int_0^{2\pi} (d_k \cdot \cos^2(\theta - \varphi) \cdot d\theta \ ) \right]. \tag{3.21}$$

Obviously, the overall conduction losses in a m-level MAC leg can also be calculated as the addition of the conduction losses of all the devices of the leg:

$$P_{\text{cond,leg}} = \sum_{\forall \ \text{S}_x \in Leg} P_{\text{cond,S}_x} \ . \tag{3.22}$$

3.3.1.4. Conduction losses in a three-phase MAC inverter under the V²PWM

The modulation scheme V²PWM proposed in [22] is suitable for the MAC topology when it operates as a three-phase inverter. This control scheme, which can be implemented for any number of levels, presents the benefit of guaranteeing the dc-link capacitor voltage balance in every switching cycle provided that the addition of the three output leg currents equals zero (in case that

the configuration consists in one dc-link voltage-supply and capacitors connected across every two adjacent input terminals).

Table 3.2 presents the mathematical expressions of duty ratios along the line period for a *m*-level leg. These expressions correspond to the duty ratios of one of the phases, e.g., phase a; the expressions of the duty ratios for the other two phases are the same, but phase-shifted 120º and 240º. Modulation index $mi \in [0,1]$ is defined as $V_{\mathrm{l-l,pk}}/V_{\mathrm{dc-link}}$, where $V_{\mathrm{l-l,pk}}$ is the peak value of the fundamental component of the line-to-line voltage.

Duty ratios	$0 < \theta < \frac{\pi}{3}$	$\frac{\pi}{3} < \theta < \frac{2\pi}{3}$	$\frac{2\pi}{3} < \theta < \pi$	$\pi < \theta < \frac{4\pi}{3}$	$\frac{4\pi}{3} < \theta < \frac{5\pi}{3}$	$\frac{5\pi}{3} < \theta < 2\pi$
$\boldsymbol{d_1}$	0	$mi \cdot cos\left(\theta - \frac{5\pi}{6}\right)$		$mi \cdot cos\left(\theta + \frac{5\pi}{6}\right)$		0
$\boldsymbol{d_i}$ $(\mathbf{1} < \boldsymbol{i} < \boldsymbol{m})$	$\frac{1 - d_1 - d_m}{m - 2}$					
$\boldsymbol{d_m}$	$mi \cdot cos\left(\theta - \frac{\pi}{6}\right)$		0		$mi \cdot cos\left(\theta + \frac{\pi}{6}\right)$	

Table 3.2. Duty ratio expressions according to the V²PWM [22].

Fig. 3.8 shows the pattern of these duty ratios. As well as the duty ratios, Fig. 3.8 depicts the waveform of the expression $\cos^2(\theta - \varphi)$, with $\varphi = 90°$, which is equal to $\left(i_{\mathrm{o}}/I_{\mathrm{o,pk}}\right)^2$ and corresponds to the expression that appears in the integrals of (3.13) and (3.21).

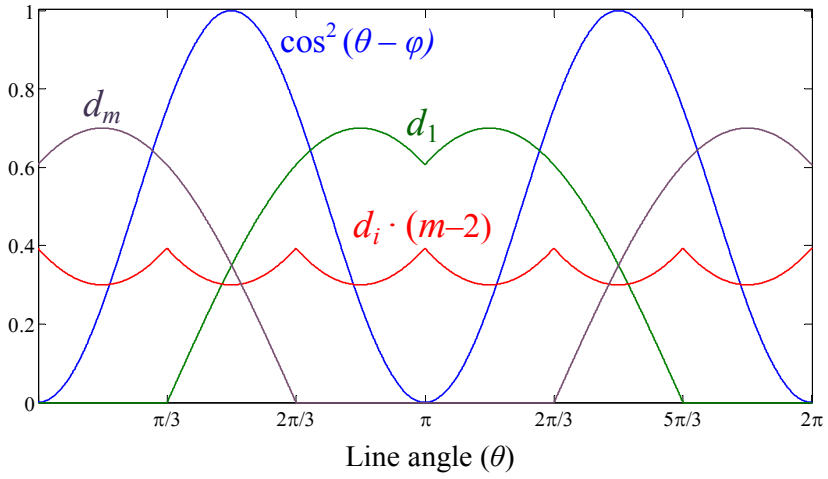


Fig. 3.8. Duty-ratio waveforms according to the V²PWM (mi=0,7) in a line cycle together with waveform of expression $\cos^2(\theta - \varphi)$.

Using the duty-ratio expressions presented in Table 3.2, the integrals of (3.13) and (3.21) can be solved. The solutions are

$$\begin{aligned} i = 1 \implies & \int_0^{2\pi} (d_1 \cdot \cos^2(\theta - \varphi) \cdot d\theta\,) = \frac{3}{2} mi \\ 1 < i < m \implies & \int_0^{2\pi} (d_i \cdot \cos^2(\theta - \varphi) \cdot d\theta\,) = \frac{\pi - 3mi}{m-2} \\ i = m \implies & \int_0^{2\pi} (d_m \cdot \cos^2(\theta - \varphi) \cdot d\theta\,) = \frac{3}{2} mi\,. \end{aligned} \tag{3.23}$$

As it can be observed in (3.23), the solutions of the integrals are very simple expressions independent from the value of the load angle φ, which apparently is not obvious. Thereby, the final expressions to calculate both the total conduction losses of a m-level MAC leg and the individual conduction losses of a device S_x, operating under the V^{2}PWM, are

$$P_{\text{cond,leg}} = \frac{{I_{\text{o,pk}}}^2}{2\pi} \cdot \left(\left(R_{\text{eq,i}_1} + R_{\text{eq,i}_m} \right) \cdot \frac{3}{2} mi + \sum_{k=2}^{m-1} R_{\text{eq,i}_k} \cdot \left(\frac{\pi - 3mi}{m-2} \right) \right) \tag{3.24}$$

$$P_{\text{cond,S}_x} = \frac{R_{\text{ds(on)}} \cdot {I_{\text{o,pk}}}^2}{2\pi} \cdot \left(\left({c_{\text{S}_x,\text{i}_1}}^2 + {c_{\text{S}_x,\text{i}_m}}^2 \right) \cdot \frac{3}{2} mi + \sum_{k=2}^{m-1} {c_{\text{S}_x,\text{i}_k}}^2 \cdot \left(\frac{\pi - 3mi}{m-2} \right) \right). \tag{3.25}$$

As examples, in a four-level MAC leg, the total conduction losses $P_{\text{cond,leg}}$ and the individual losses $P_{\text{cond,S}_{\text{n31}}}$ of device S_{n31} are calculated as

$$\begin{aligned} P_{\text{cond,leg}} &= \frac{{I_{\text{o,pk}}}^2}{2\pi} \cdot \left(\left(2 \cdot 3 \cdot R_{\text{ds (on)}} \right) \cdot \frac{3}{2} mi + \left(2 \cdot 1.4 \cdot R_{\text{ds(on)}} \right) \cdot \left(\frac{\pi - 3mi}{2} \right) \right) \\ &= \frac{R_{\text{ds (on)}} \cdot {I_{\text{o,pk}}}^2}{2\pi} \cdot \left(9\, mi + 2.8 \cdot \left(\frac{\pi - 3mi}{2} \right) \right) \end{aligned} \tag{3.26}$$

$$\begin{aligned} P_{\text{cond,S}_{\text{n31}}} &= \frac{R_{\text{ds(on)}} \cdot {I_{\text{o,pk}}}^2}{2\pi} \cdot \left((1^2 + 0^2) \cdot \left(\frac{3}{2} mi \right) + (0.6^2 + 0.4^2) \cdot \left(\frac{\pi - 3mi}{2} \right) \right) \\ &= \frac{R_{\text{ds(on)}} \cdot {I_{\text{o,pk}}}^2}{2\pi} \cdot \left(\frac{3}{2} mi + 0.52 \cdot \left(\frac{\pi - 3mi}{2} \right) \right), \end{aligned} \tag{3.27}$$

where $I_{\mathrm{o,pk}}$ is calculated as

$$I_{\mathrm{o,pk}} = \frac{mi \cdot V_{\mathrm{dc-link}}}{Z \cdot \sqrt{3}}, \tag{3.28}$$

where Z is the phase impedance.

Fig. 3.9 presents the normalized leg conduction losses operating under the V^{2}PWM. These waveforms are obtained from (3.24), dividing $P_{\mathrm{cond,leg}}$ by $R_{\mathrm{ds\,(on)}} \cdot (m-1) \cdot {I_{\mathrm{o,pk}}}^2$. It can be appreciated that conduction losses are lower as the number of levels increases, and mainly for lower modulation indexes. This is due to the fact that duty ratios of inner levels increase as the modulation index decreases. Please note that ON resistances $R_{\mathrm{ds\,(on)}}$ should vary according to (3.2). Then, the reduction of losses will be higher as the number of levels increases.

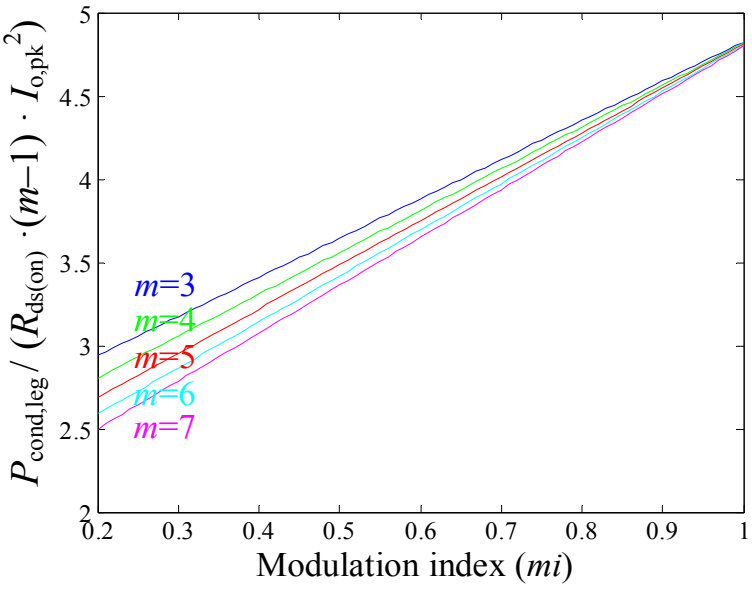


Fig. 3.9. Normalized total MAC leg conduction losses as a function of the modulation index for different numbers of levels operating under the V^{2}PWM.

3.3.2. Switching losses

Some important aspects regarding switching losses that have already been introduced in Chapter 2 are here repeated at the beginning. Then, the analysis goes further.

In a general m-level converter leg, the transition between two adjacent switching states (k and k + 1) requires changing the state of m switches. However, the switching losses (turn-on and turn-off losses) are basically concentrated in one device. In the transition between adjacent

switching states, it is required to first turn off the devices to be turned off. Then, after a proper dead time, we can proceed to turn on the devices to be turned on.

If $(k_f–k_i)\cdot i_o<0$, where k_i and k_f are the initial and final switching states, respectively; then, the switching losses concentrate on the last switch being turned off. All the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is nearly zero.

If $(k_f–k_i)\cdot i_o>0$; then, the switching losses concentrate on the first switch being turned on. As before, all the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is nearly zero. Besides, in these cases, k_i diode reverse-recovery processes take place in the transition if $i_o>0$, and k_f reverse-recovery processes take place if $i_o<0$.

An interesting strategy to distribute the switching losses among the devices is to alternate the first device being turned-on and to alternate the last device being turned-off in every transition between adjacent switching states. Alternatively, those devices experiencing lower conduction losses could be selected to concentrate the switching losses so that all devices present similar overall losses, and ultimately similar junction temperatures. If a measurement or estimation of the device temperature is available, the devices with lower temperature can be selected to concentrate the switching losses. A possible solution to distribute the switching losses among the devices consists of selecting the switches that belong to the (2*m*–2)-switch pole (see Fig. 2.1) to concentrate the switching losses. It is simple to implement and these devices present low conduction losses.

3.3.2.1. Switching losses in a four-level leg

As an example to illustrate the switching losses, let us consider the particular case of a four-level MAC leg. The extension into a higher number of levels can be easily deduced.

As it can be deduced from Fig. 3.10, in a four-level leg, a total of four switches change their state in a transition between two adjacent switching states.

Fig. 3.11 presents the switching state transition from connection to node i_3 to connection to node i_4 with positive output current i_o in a four-level MAC leg to illustrate the process. Fig. 3.11(a) shows the switching state in which the output terminal is connected to node i_3. In the first step of the transition, devices S_{n31}, S_{n32}, and S_{n33} are turned off. Since the load current flows through the diodes of these three devices, the output terminal continues connected to node i_3, as it is depicted in Fig. 3.11(b). Then, after a proper dead time, device S_{p31} is turned on and the current starts flowing through this device connecting the output terminal to node i_4, see Fig. 3.11(c). At this point of the

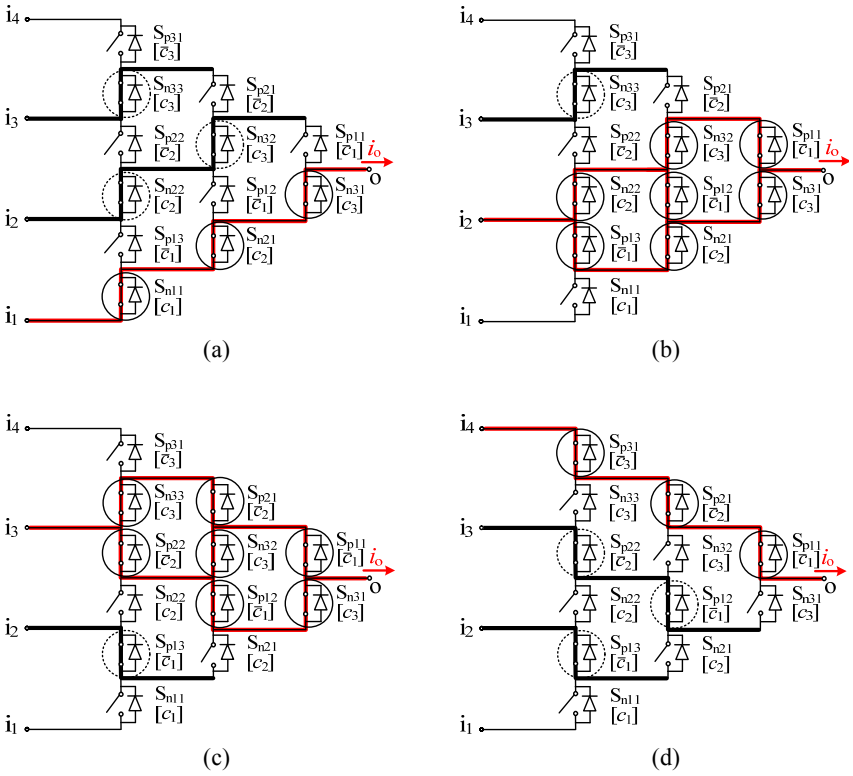


Fig. 3.10. Switching states in a four-level MAC leg. (a) Connection to node i_1. (b) Connection to node i_2. (c) Connection to node i_3. (d) Connection to node i_4.

transition, the diodes of devices S_{n31}, S_{n32}, and S_{n33} suffer a reverse-recovery process and the reverse-recovery currents flow through S_{p31} at turn on, increasing the switching losses. Finally, after a short transient, the steady-state connection of the output terminal to node i_4 is reached, as shown in Fig. 3.11(d).

Table 3.3 summarizes the switching losses of a four-level leg that take place in each one of the switching state transitions, and taking into account the current polarity. In Table 3.3, it has been assumed that the 6-switch-pole devices are selected to concentrate the switching losses (the symbol $^{(*)}$ indicates those cases in which it could be possible to choose another device to concentrate the switching losses).

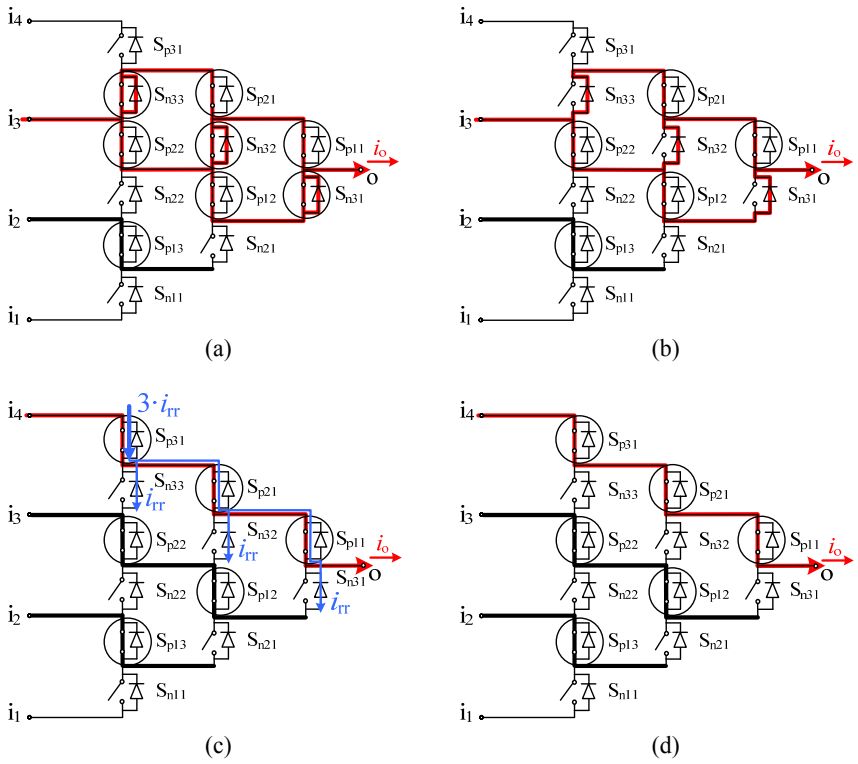


Fig. 3.11. Transition between switching state 3 to switching state 4 with positive output current i_o. (a) Connection to node i_3. (b) First transient state. (c) Second transient state (three diode-reverse-recovery processes). (d) Connection to node i_4.

Current polarity	Switching state transition	Devices that concentrate the switching losses (turn on/turn off)	Devices whose diodes present reverse recovery	Total losses in the transition
$(i_o > 0)$	1 → 2	S_{p13} (on) (*)	S_{n11}	$E_{on\_1D} + E_{rr\_1D}$
	2 → 3	S_{p22} (on) (*)	S_{n21}, S_{n22}	$E_{on\_2D} + E_{rr\_2D}$
	3 → 4	S_{p31} (on)	S_{n31}, S_{n32}, S_{n33}	$E_{on\_3D} + E_{rr\_3D}$
	4 → 3	S_{p31} (off)	-	E_{off}
	3 → 2	S_{p22} (off) (*)	-	E_{off}
	2 → 1	S_{p13} (off) (*)	-	E_{off}
$(i_o < 0)$	1 → 2	S_{n11} (off)	-	E_{off}
	2 → 3	S_{n22} (off) (*)	-	E_{off}
	3 → 4	S_{n33} (off) (*)	-	E_{off}
	4 → 3	S_{n33} (on) (*)	S_{p31}	$E_{on\_1D} + E_{rr\_1D}$
	3 → 2	S_{n22} (on) (*)	S_{p21}, S_{p22}	$E_{on\_2D} + E_{rr\_2D}$
	2 → 1	S_{n11} (on)	S_{p11}, S_{p12}, S_{p13}	$E_{on\_3D} + E_{rr\_3D}$

Table 3.3. Switching losses in each switching state transition of the four-level MAC leg.

3.4. Experimental efficiency comparison between a four-level MAC leg and a conventional two-level leg under a basic operating mode

In this section, an efficiency comparison between a four-level MAC leg and a conventional two-level leg operating at low voltage is carried out. Section 3.4.1 details the conditions in which the efficiency comparison is performed; i.e., the circuit configuration and control scheme. In Section 3.4.2, the different loss models of both topologies are presented. Aside from calculating the conduction and switching losses using the models presented in Section 3.3, other significant losses such as gate-driving-related losses are also estimated. To estimate the switching losses, experimental tests are conducted to measure the device energy lost in one switching transition. Finally, Section 3.4.3 presents experimental tests to measure the overall losses and the efficiency of both converter legs. The obtained results are compared with the estimations to validate the loss models.

3.4.1. Efficiency comparison scenario

To perform the efficiency comparison between the MAC converter and a conventional two-level converter, many different circuit configurations and control schemes can be used. In order to achieve a simple and balanced comparison that allow us to infer general conclusions, and also to validate the analytical loss models, a simple configuration and operating mode have been used.

The circuit configuration consists of a single leg of each topology, a four-level leg of the MAC topology and a two-level leg, using a series resistive-inductive load, as it is depicted in Fig. 3.12. Dc-voltage sources are connected across every two adjacent input terminals in the MAC leg.

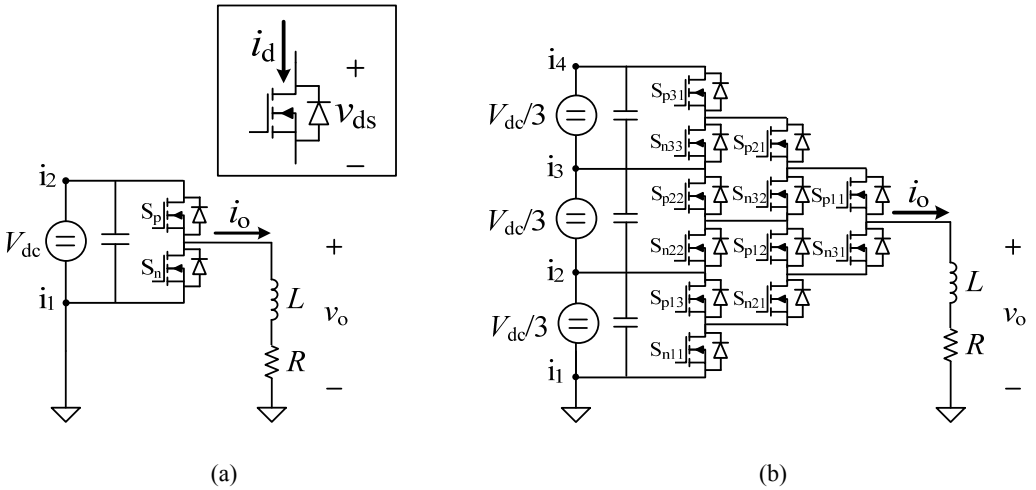


Fig. 3.12. Circuit configurations used to perform the efficiency comparison. (a) Two-level leg. (b) Four-level MAC leg.

To simplify the estimation of losses, it is interesting to keep the output current constant. In order to achieve this, a modulation pattern that defines the same average output voltage in every switching cycle together with a large output inductance are used. For simplicity and to apply the same weight to all switching states, the switching pattern consists in equally-distributed duty ratios to connect the output terminal to each one of the input terminals; i.e., duty ratios equal to 0.25 for each one of the levels in the four-level leg, and duty ratios of 0.5 in the two-level leg. The distribution of duty ratios within the switching period is shown in Fig. 3.13.

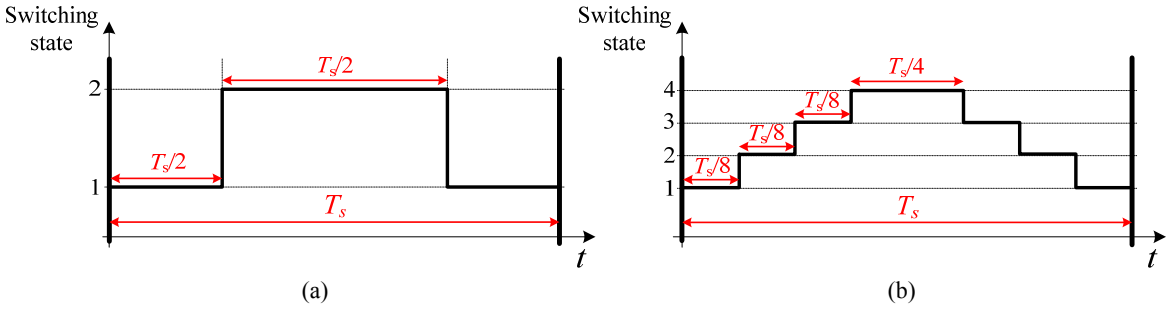


Fig. 3.13. Switching pattern within a modulation period used for the efficiency comparison. (a) Two-level leg. (b) Four-level MAC leg.

As the analysis is performed at low voltage, MOSFETs are used as power devices. 200 V MOSFETs STP20NF20 are used in the MAC leg, and 600 V MOSFETs STP13NM60N are used in the two-level leg. These devices have been selected so that the ON-resistance of 600 V MOSFETs $\left(R_{\mathrm{ds(on)},600}\right)$ is three times the one of 200 V MOSFETs $\left(R_{\mathrm{ds(on)},200}\right)$, being both from the same manufacturer.

3.4.2. Loss models

This section presents the expressions to estimate the different losses of both converters as a function of the electrical parameters and variables. They are classified as device conduction losses, device switching losses and other losses.

3.4.2.1. Device conduction losses

3.4.2.1.1. Two-level leg

Conduction losses of devices S_p and S_n can be estimated as

$$P_{\mathrm{cond,S_p}} = P_{\mathrm{cond,S_n}} = R_{\mathrm{ds(on)},600} \cdot {I_{\mathrm{d(RMS)}}}^2 . \tag{3.29}$$

As the output current i_o is approximately constant, the RMS current of each device is

$$I_{\mathrm{d\,(RMS)}} = \frac{I_{\mathrm{o}}}{\sqrt{2}}. \tag{3.30}$$

Combining (3.29) and (3.30), the final expression to estimate the overall conduction losses in the two-level leg is

$$P_{\mathrm{cond,2L}} = P_{\mathrm{cond,S_p}} + P_{\mathrm{cond,S_n}} = R_{\mathrm{ds(on),600}} \cdot {I_{\mathrm{o}}}^2 . \tag{3.31}$$

3.4.2.1.2. Four-level MAC leg

Applying (3.8), the total conduction losses can be calculated as

$$P_{\mathrm{cond,4L}} = {I_{\mathrm{o}}}^2 \cdot 0.25 \cdot (3 + 3 + 1.4 + 1.4) \cdot R_{\mathrm{ds(on),200}} = 2.2 \cdot R_{\mathrm{ds(on),200}} \cdot {I_{\mathrm{o}}}^2. \tag{3.32}$$

Considering that $R_{\mathrm{ds(on),200}}$ is the third of $R_{\mathrm{ds(on),600}}$, it can be deduced that total conduction losses will be lower in the four-level leg:

$$P_{\mathrm{cond,4L}} = 2.2 \cdot \frac{R_{\mathrm{ds(on),600}}}{3} \cdot {I_{\mathrm{o}}}^2 = 0.73 \cdot P_{\mathrm{cond,2L}}$$

3.4.2.2. Device switching losses

To estimate the overall switching losses in both topologies, experimental tests to measure turn-off, turn-on, and diode reverse-recovery losses of the used MOSFETs have been carried out. Fig. 3.14 presents the circuit used to do the tests (in Appendix B, a picture of the board is presented). This circuit allows measuring the switching losses of device $\mathrm{S_{test}}$ under a desired voltage and current level. The gate-pulse amplitude defines the desired current level.

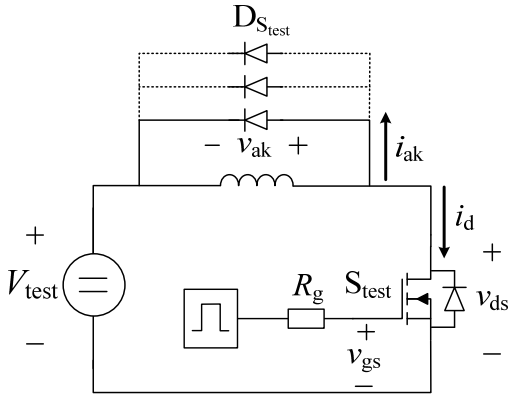


Fig. 3.14. Circuit used to measure power-device switching losses.

An additional antiparallel diode of device $\mathrm{S_{test}}$ is used as diode $\mathrm{D_{S_{test}}}$. In order to emulate the switching transitions that take place in the four-level MAC leg in which two and three diodes

present a reverse-recovery process, tests using one, two, and three diodes connected in parallel have been done, see Fig. 3.14. Both turn-on losses that take place in device S_{test} and reverse-recovery losses that take place in the diode are measured using one, two, and three diodes.

Fig. 3.15-Fig. 3.19 present some experimental waveforms of different switching transitions. Fig. 3.15 shows turn-off transitions of both 200 V and 600 V MOSFETs at 6 A of current. The area between cursors of signal $p_{loss\text{-}off}$ represents the energy E_{off} lost in the transition (10.179 μJ for the 200 V MOSFET and 19.89 μJ for the 600 V MOSFET). Fig. 3.16 and Fig. 3.17 show turn-on transitions of both 200 V and 600 V MOSFETs at 6 A of current. Fig. 3.16 shows the voltage and current waveforms of MOSFET under test S_{test}, while the reverse-recovery waveforms of diode $D_{S_{test}}$ are shown in Fig. 3.17. Please note in Fig. 3.16 the significant difference in the turn-on energy lost E_{on_1D} between both MOSFETs. The effect of the multiple reverse recoveries taking place at the same transition can be appreciated in Fig. 3.18 and Fig. 3.19 for the 200 V MOSFET. Fig. 3.18 shows the voltage and current waveforms of MOSFET under test S_{test}, while the reverse-recovery waveforms of diodes $D_{S_{test}}$ are shown in Fig. 3.19. In Fig. 3.18(a) and Fig. 3.19(a), two diodes are connected in parallel, while in Fig. 3.18(b) and Fig. 3.19(b), three diodes are connected in parallel.

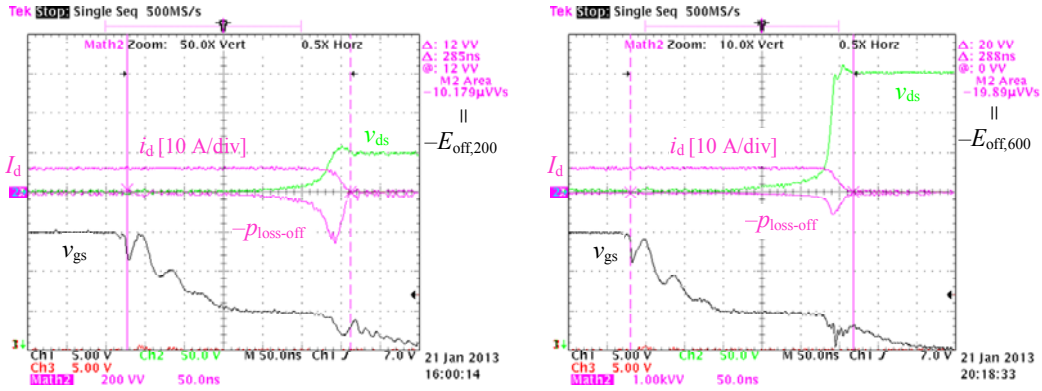


Fig. 3.15. Experimental turn-off switching waveforms at I_d=6 A with R_g=56 Ω. (a) 200 V MOSFET under V_{test} = 50 V ($p_{loss\text{-}off} = v_{ds} \cdot i_d$). (b) 600 V MOSFET under V_{test} = 150 V.

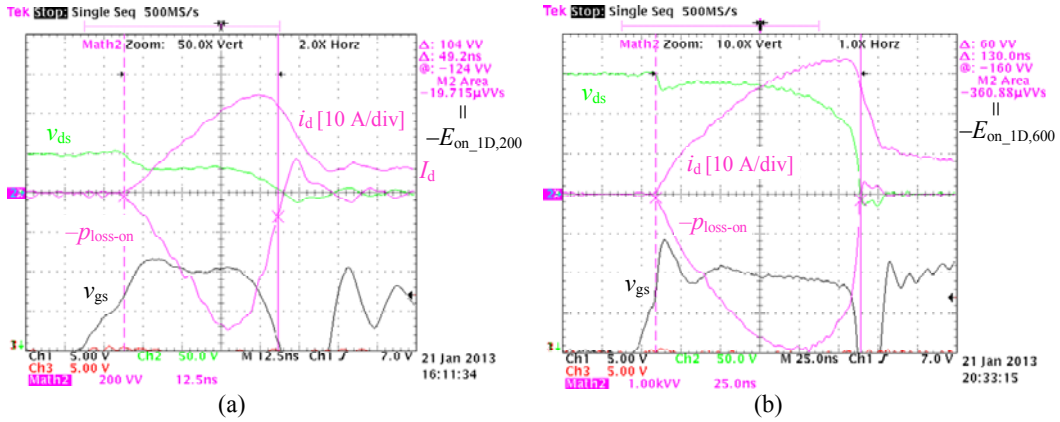


Fig. 3.16. Experimental turn-on switching waveforms at I_d=6 A with R_g=56 Ω. (a) 200 V MOSFET under V_{test} = 50 V ($p_{loss\text{-}on} = v_{ds} \cdot i_d$). (b) 600 V MOSFET under V_{test} = 150 V.

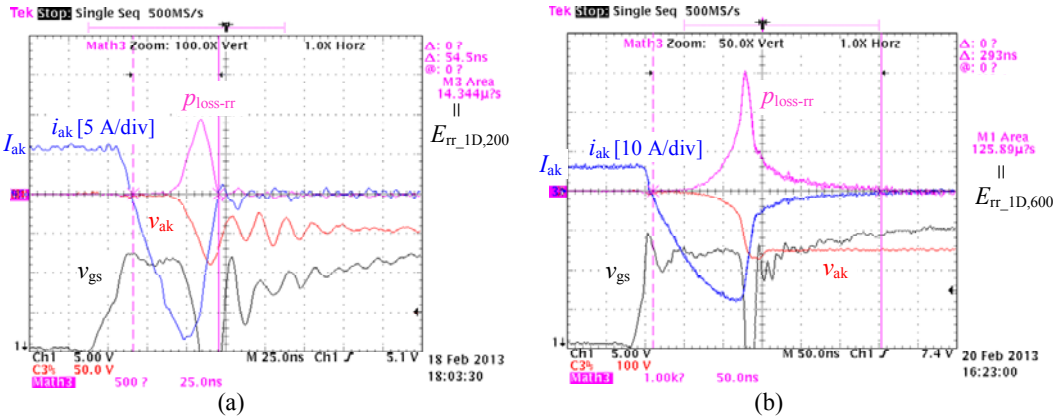


Fig. 3.17. Experimental turn-on switching waveforms at I_{ak}=6 A with R_g=56 Ω. (a) Reverse-recovery of 200 V MOSFET under V_{test} = 50 V ($p_{loss\text{-}rr} = v_a \cdot i_{ak}$). (b) Reverse-recovery of 600 V MOSFET under V_{test} = 150 V.

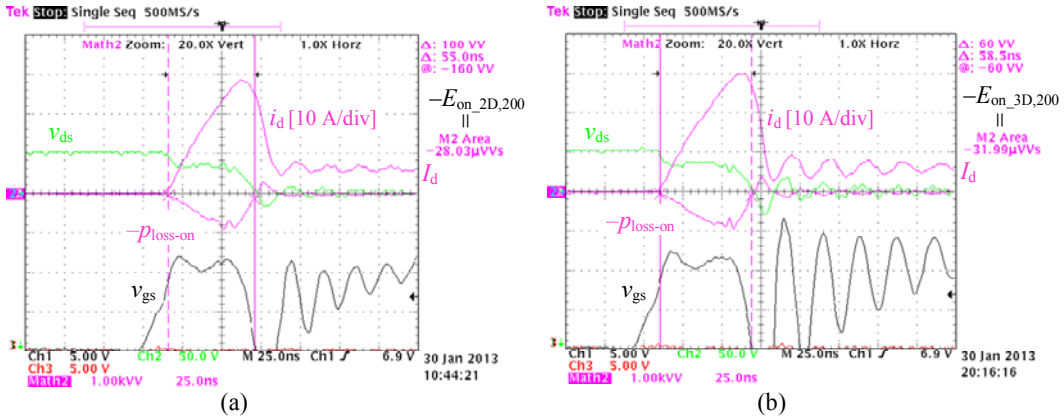


Fig. 3.18. Experimental turn-on switching waveforms of 200 V MOSFET with I_d=6 A, R_g=56 Ω, and V_{test} = 50 V, under multiple reverse recoveries. (a) Two diodes presenting reverse-recovery. (b) Three diodes presenting reverse-recovery.

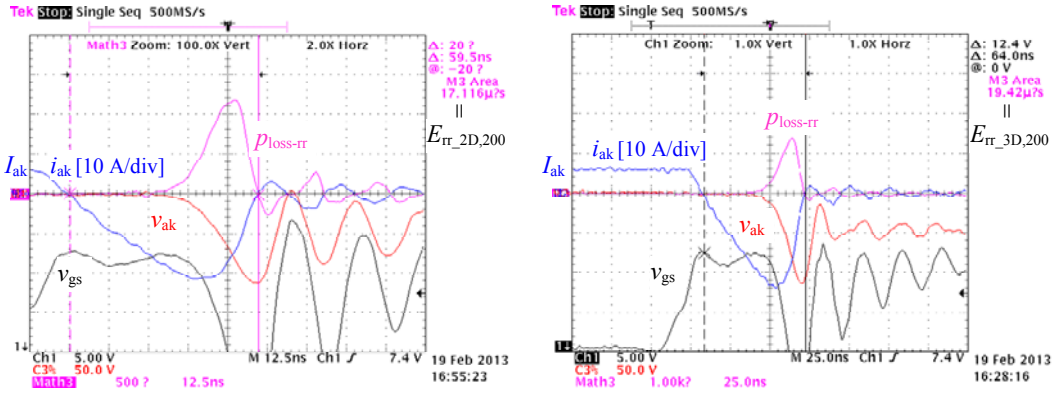


Fig. 3.19. Experimental turn-on reverse-recovery switching waveforms of 200 V MOSFET with I_d=6 A, R_g=56 Ω, and V_{test} = 50 V, under multiple reverse recoveries. (a) Two diodes presenting reverse-recovery. (b) Three diodes presenting reverse-recovery.

The tests presented above have been done under different values of current in order to obtain a linear or quadratic expression of the device energy loss as a function of current. Fig. 3.20 and Fig. 3.21 present the results and the obtained expressions for both MOSFETs. These expressions are used to estimate the switching losses.

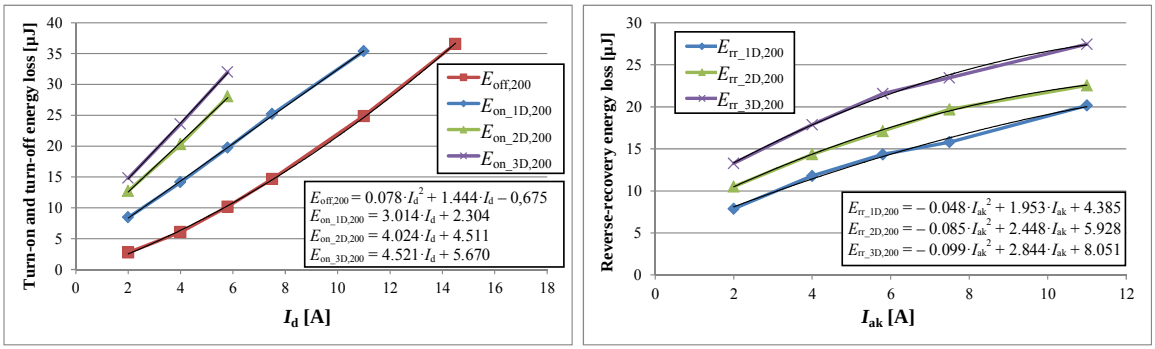
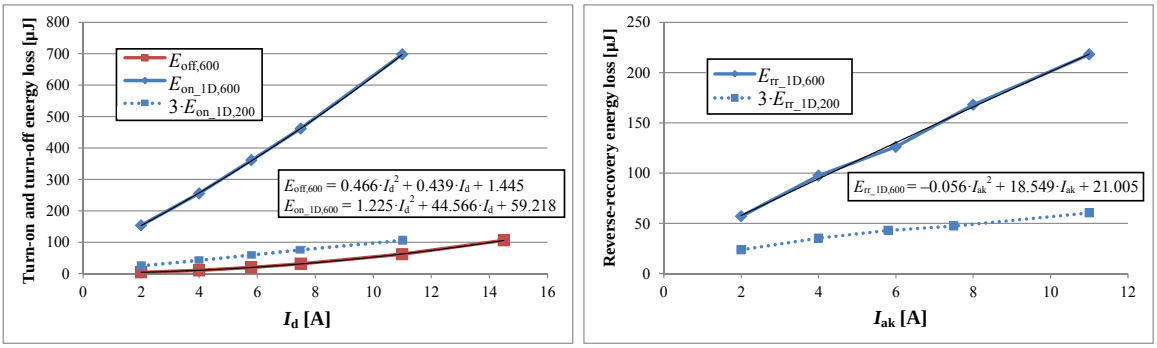


Fig. 3.20. Switching losses of 200 V MOSFET as a function of current, with R_g=56 Ω and V_{test} = 50 V. (a) Device turn-on and turn-off energy loss. (b) Diode reverse-recovery losses.



(a) (b)

Fig. 3.21. Switching losses of 600 V MOSFET as a function of current, with R_g=56 Ω and V_{test} = 150 V. (a) Device turn-on and turn-off energy loss. (b) Diode reverse-recovery losses.

Please note in Fig. 3.21 that the turn-on energy-loss in the 600 V MOSFET is much higher than three times the one in 200 V MOSFETs. There is also a large difference in diode reverse-recovery losses.

3.4.2.2.1. Two-level leg

According to the control scheme presented in Section 3.4.1 and shown in Fig. 3.13(a), there are two transitions in the modulation period. In the first transition, from connection to terminal i_1 to connection to i_2, device S_p concentrates the losses at the instant that it is turned on since the output current i_o is positive. Besides, the antiparallel diode of device S_n presents a reverse-recovery process. In the second switching transition, from connection to i_2 to connection to i_1, again device S_p concentrates the losses when it is turned off. Thus, the overall switching losses can be estimated as

$$P_{sw,2L} = f_s \cdot \left(E_{on\_1D,600} + E_{rr\_1D,600} + E_{off,600}\right), \tag{3.33}$$

where f_s is the switching frequency, $E_{on\_1D,600}$ and $E_{rr\_1D,600}$ represent the turn-on and reverse-recovery losses in the transition from i_1 to i_2, respectively; and $E_{off,600}$, represents the turn-off losses in the transition from i_2 to i_1. The values of these energies are taken from the equations of Fig. 3.21(a) and Fig. 3.21(b), according to the current level.

3.4.2.2.2. Four-level MAC leg

According to Table 3.3 and taking into account the control scheme presented in Section 3.4.1 and shown in Fig. 3.13(b), the overall switching losses can be estimated as

$$P_{\mathrm{sw,4L}} = f_s \cdot \left(E_{\mathrm{on\_1D,200}} + E_{\mathrm{on\_2D,200}} + E_{\mathrm{on\_3D,200}} + E_{\mathrm{rr\_1D,200}} + E_{\mathrm{rr\_2D,200}} + E_{\mathrm{rr\_3D,200}} + 3 \cdot E_{\mathrm{off,200}}\right). \quad (3.34)$$

The values of the energies in (3.34) are taken from the equations of Fig. 3.20(a) and Fig. 3.20(b), according to the current level.

3.4.2.3. Other losses

3.4.2.3.1. Gate-driver-circuit losses

a) Gate-resistor losses

The loss dissipated in a gate resistor can be estimated as

$$P_{\mathrm{rg}} = f_{\mathrm{s}} \cdot V_{\mathrm{gs}} \cdot Q_{\mathrm{g}}, \quad (3.35)$$

where V_{gs} is the gate-to-source voltage in ON-state; and Q_{g} is the MOSFET gate charge, which is equal for both selected MOSFETs. Considering that the two-level leg presents two drivers, and the four-level leg presents twelve drivers, the expressions for each one of the legs are

$$P_{\mathrm{rg,2L}}\,[\mathrm{W}] = 1.56 \cdot 10^{-6} \cdot f_{\mathrm{s}}\,[Hz] \quad (3.36)$$

$$P_{\mathrm{rg,4L}}\,[\mathrm{W}] = 9.36 \cdot 10^{-6} \cdot f_{\mathrm{s}}\,[\mathrm{Hz}]. \quad (3.37)$$

b) Gate-driver integrated-circuit (IC) losses

The driver used in both converter prototypes is the HCPL-316J. According to the driver's datasheet, the IC losses can be calculated as

$$P_{\mathrm{drv}} = P_{\mathrm{drv\_bias}} + P_{\mathrm{drv\_sw}} = I_{\mathrm{cc2}} \cdot V_{\mathrm{cc2}} + E_{\mathrm{sw}} \cdot f_{\mathrm{s}}, \quad (3.38)$$

where $P_{\mathrm{drv\_bias}}$ is the steady-state power dissipation in the driver due to biasing the device, and it is equal to the product of I_{cc2}, the average bias output supply current, by V_{cc2}, the average output supply voltage. $P_{\mathrm{drv\_sw}}$ is the transient power dissipation in the driver due to charging and discharging of the power-device gate, and it is equal to E_{sw}, the average energy dissipated in the integrated circuit due to switching of the power device over one switching cycle, multiplied by f_{s}. The energy E_{sw} depends on the used device (mainly on the device gate-charge Q_{g}), and the used

gate resistance; This energy has been estimated as 3.5 μJ for both MOSFETs. Thus, the expressions for each one of the converters are

$$P_{\mathrm{drv,2L}}\,[\mathrm{W}] = 0.22 + 7 \cdot 10^{-9}\,\mathrm{J} \cdot f_{\mathrm{s}}\,[\mathrm{kHz}] \tag{3.39}$$

$$P_{\mathrm{drv,4L}}\,[\mathrm{W}] = 1.32 + 42 \cdot 10^{-9}\,\mathrm{J} \cdot f_{\mathrm{s}}\,[\mathrm{kHz}]\,, \tag{3.40}$$

In both converters, each one of the gate drivers is powered through a simple and small circuit connected across the controlled device, as explained in Section A.3 of Appendix A. Part of the energy to power the gate-driver comes from the dc-bus and part of the energy comes from a recycling of the device switching losses. As a result, no external gate-driver power-supplies are required and therefore the gate driver IC losses have to be calculated to estimate the overall efficiency of the converters.

3.4.2.3.2. Losses of the capacitor-discharging resistors

In order to facilitate the discharging of dc-link capacitors when the converter is shut down, some resistors are connected in parallel with them. These resistors produce the following losses:

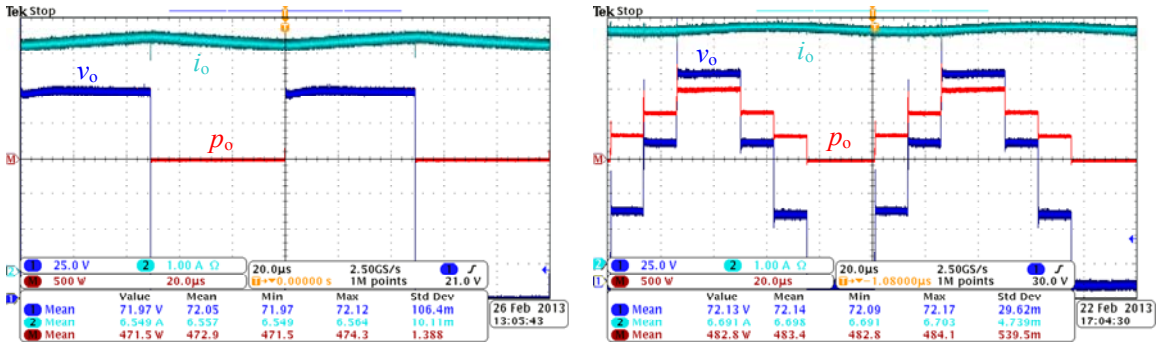
$$P_{\mathrm{rc,2L}} = 0.227\ \mathrm{W} \tag{3.41}$$

$$P_{\mathrm{rc,4L}} = 0.227\ \mathrm{W}\,. \tag{3.42}$$

3.4.3. Experimental and analytical results

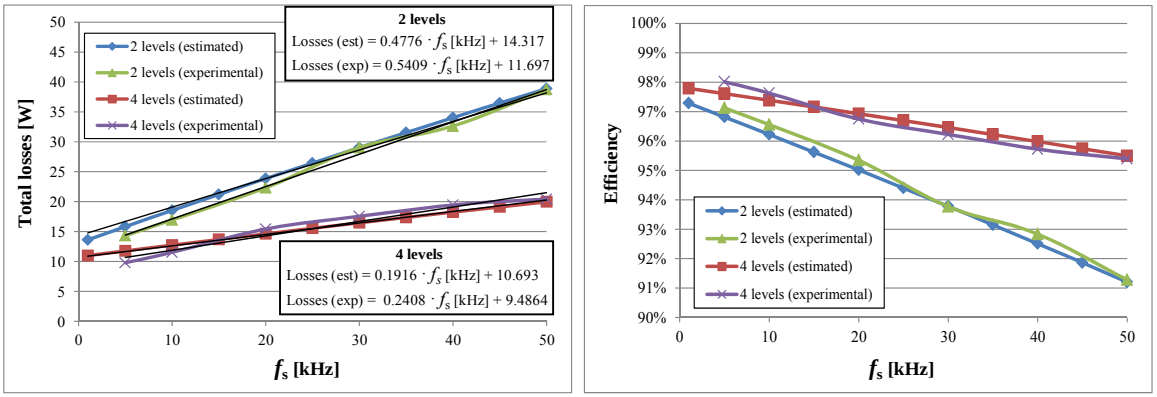
Experimental tests have been done in order to directly measure the overall losses and the efficiency of both topologies, and then compare these results with the estimation from the loss models. Fig. 3.22 depicts the output voltage, the output current, and the output power for both topologies in a particular condition (in Fig. 3.22(a), red signal p_{o} is located just behind the blue signal v_{o} and for this reason is not well appreciated).

As there is a certain variation in the measured losses of experimental tests, repeated tests with the same conditions have been carried out in order to obtain averaged values of losses and efficiency of converters. Fig. 3.23 and Fig. 3.24 present the final estimated and experimental results for different switching frequencies using two different load conditions. It can be seen that the results obtained through the experiments are close to the estimations. The four-level MAC converter presents a higher efficiency than the two-level converter for all switching frequencies. The difference increases with the switching frequency, just as expected, since switching losses are significantly higher in the two-level converter.



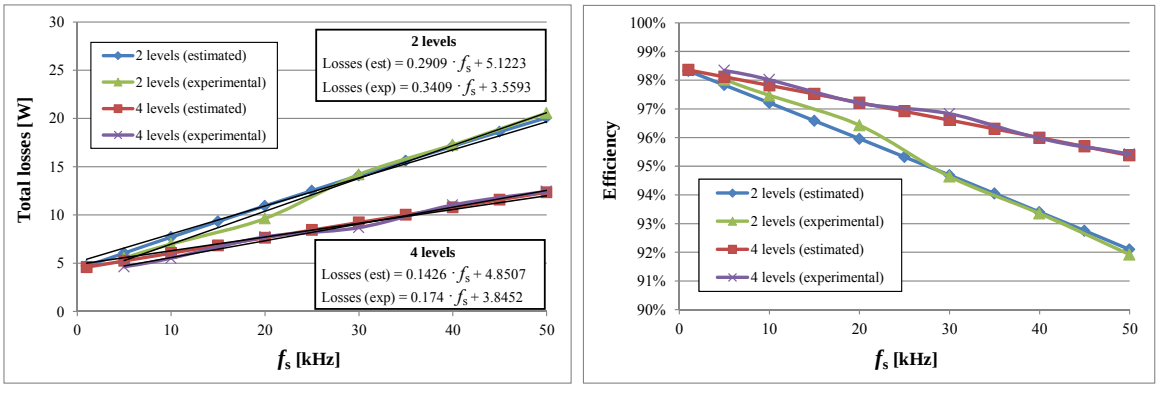
(a) (b)

Fig. 3.22. Experimental results for v_o, i_o, and $p_o = v_o \cdot i_o$ with the setup presented in Section 3.4.1 and the following conditions: V_{dc} = 150 V, L = 60 mH, R = 8 Ω, and f_s = 5 kHz. (a) Two-level leg. (b) Four-level leg.



(a) (b)

Fig. 3.23. Final estimated and experimental results with the following conditions: V_{dc} = 150 V, L = 60 mH, and R = 8 Ω. (a) Total losses vs. switching frequency. (b) Efficiency vs. switching frequency.



(a) (b)

Fig. 3.24. Final estimated and experimental results with the following conditions: V_{dc} = 150 V, L = 60 mH, and R = 16 Ω. (a) Total losses vs. switching frequency. (b) Efficiency vs. switching frequency.

Assuming that switching losses are linearly dependent on the switching frequency (it can be assumed since quadratic dependence is very small), linear regressions have been obtained for both estimated and experimental losses, see Fig. 3.23(a) and Fig. 3.24(a). The y-intercept of linear regressions basically represents the MOSFETs conduction-losses, plus other losses that do not depend on the switching frequency ($P_{\mathrm{cond}} + P_{\mathrm{drv\_bias}} + P_{\mathrm{rc}}$), while the slope basically represents the MOSFET switching-losses, plus other losses that depend on the switching frequency ($P_{\mathrm{sw}} + P_{\mathrm{rg}} + P_{\mathrm{drv\_sw}}$), at 1 kHz. The slopes of MAC topology are significantly lower (around half) than the ones from the two-level topology. Besides, it can be seen that slopes from the estimated losses are lower than the ones from experimental tests (around 20% for the MAC and around 10-15% for the half bridge). It is possibly due to the fact that some switching-frequency-dependent losses have not been taken into account in the loss models.

It is relevant to consider that the MAC prototype has not been optimized in order to obtain the highest efficiency. Some adjustments could be done in order to increase it, like for example reducing the gate resistance to decrease the MOSFETs switching-losses, selecting other more suitable MOSFETs that present lower conduction-losses and/or lower switching-losses, etc. Furthermore, it is important to bear in mind that the measured efficiency takes into account the gate-driver circuit losses. In spite of all this, the efficiency of the MAC converter is around 98% at switching frequencies around 5-10 kHz and above 95% at a frequency of 50 kHz.

The close proximity between the estimation and experimental results validates the obtained results from both approaches, and supports the conclusions presented above.

3.5. Efficiency comparison between a four-level three-phase MAC dc-ac converter and a conventional two-level three-phase dc-ac converter

In this section, an analytical efficiency comparison is performed using the validated loss models in Section 3.4.

3.5.1. Efficiency comparison scenario

The converter configurations consist of a four-level three-phase MAC inverter and a conventional three-phase voltage source inverter (VSI), using a three-phase wye-connected inductive-resistive load impedance, as it is depicted in Fig. 3.25. Dc-voltage sources connected across every two adjacent input terminals are considered in the MAC inverter to perform the study.

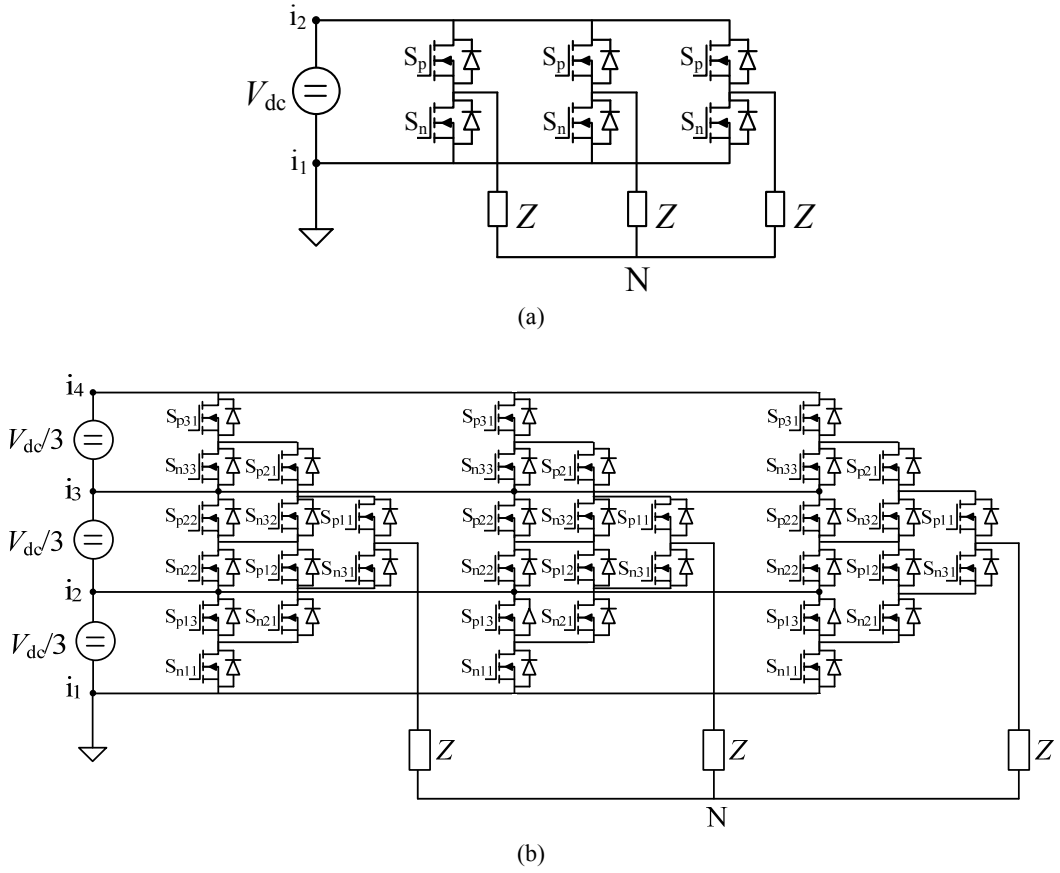


Fig. 3.25. Circuit configurations used to perform the efficiency comparison. (a) Three-phase two-level inverter. (b) Three-phase four-level MAC inverter.

The implemented modulation scheme for the four-level inverter is the V^2PWM, whose duty-ratio expressions appear in Table 3.2. The modulation applied for the two-level inverter is the SVPWM with centered active pulses in which the two zero vectors are alternately used with the same weight [71]. The same MOSFETs used in Section 3.4 are considered here (200 V MOSFETs STP20NF20 in the four-level inverter, and 600 V MOSFETs STP13NM60N in the two-level inverter).

3.5.2. Loss modeling implementation

The losses of both converters are estimated using the previously validated loss models. Only the power-device conduction losses and power-device switching losses are estimated (the losses associated to the gate drivers and other losses are not considered).

In order to estimate the device conduction losses of the four-level MAC inverter, (3.24) is used. To estimate the conduction losses of the two-level inverter, the device energy lost in a line

cycle is calculated as the addition of the energy lost in each one of the switching periods. Then, the conduction power loss is obtained multiplying this value by the line frequency (50 Hz).

In order to estimate the switching losses of the four-level inverter, the obtained expressions from Fig. 3.20 are used (in the range 0 A to 2 A, a linear expression is used so as to produce 0 energy loss at 0 A and the measured loss at 2 A). The switching energy loss is calculated for each switching period within a line period according to Table 3.3, considering the instantaneous level of current i_o. The addition of these switching-period energies represents the energy loss in the line period, which is finally multiplied by the line frequency to obtain the overall switching power loss. Please note from Table 3.3 that for switching periods whose line angle is within the range $\frac{2\pi}{3} < \theta < \frac{4\pi}{3}$, the duty ratio d_4 equals 0 and therefore transitions 3 → 4 and 4 → 3 do not take place. The same thing happens when the angle is within the range $\frac{-\pi}{3} < \theta < \frac{\pi}{3}$, where the duty ratio d_1 equals 0 and transitions 1 → 2 and 2 → 1 do not occur. The switching losses of the two-level converter are estimated with the same procedure of the four-level converter, using the obtained expressions from Fig. 3.21 (as before, the expressions have been approximated linearly within the range 0 A to 2 A).

3.5.3. Comparison results

Efficiency comparison results are shown in Fig. 3.26 for different combinations of values of the switching frequency f_s, the modulation index mi, the load phase angle φ, and the phase impedance Z. The efficiency is calculated as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_{out} + P_{sw} + P_{cond}}. \tag{3.43}$$

As it can be seen in Fig. 3.26, the efficiency of the MAC inverter is always higher than the efficiency of the two-level inverter. It can be observed in Fig. 3.26(a), Fig. 3.26(b), and Fig. 3.26(c) that the efficiency of both converters decreases as the frequency increases, and the difference between the efficiency of the two converters becomes higher too, just as expected.

Fig. 3.26(a) and Fig. 3.26(d) show that the efficiency difference between the two converters becomes lower as the modulation index increases. The impact of the modulation index for the MAC leg also depends on the switching frequency, as it can be observed in Fig. 3.26(a). For low switching frequencies, the efficiency is higher as the modulation index is lower, but for high switching frequencies, the efficiency becomes higher for high modulation indexes.

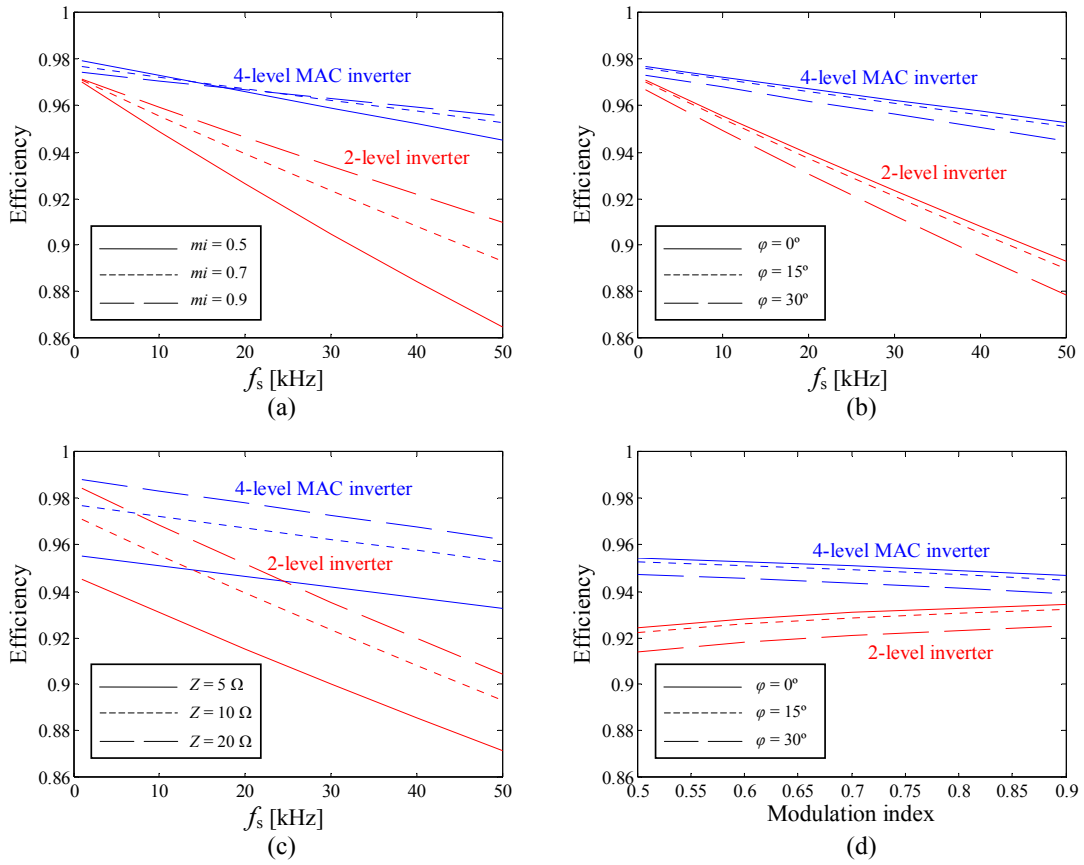


Fig. 3.26. Comparison results of three-phase two-level and four-level MAC inverter with V_{dc} = 50 V. (a) Efficiency vs. f_s with φ=0º and Z=10 Ω. (b) Efficiency vs. f_s with mi=0.7 and Z=10 Ω. (c) Efficiency vs. f_s with mi=0.7 and φ=0º. (d) Efficiency vs. mi with f_s=10 kHz and Z=10 Ω.

Regarding the effect of the load angle φ, the efficiency decreases slightly when the angle increases, see Fig. 3.26(b) and Fig. 3.26(d). It is basically due to the fact that P_{out} decreases while P_{loss} remains practically equal. Therefore, according to (3.43), the efficiency becomes lower.

Finally, the influence of the impedance Z can be appreciated Fig. 3.26(c). The efficiency is lower as the impedance decreases. This happens because the output current i_{o} becomes higher, and the conduction losses are proportional to the square of the peak value of output current $I_{\text{o,pk}}$, while the output power is only linearly proportional to $I_{\text{o,pk}}$.

It is important to remember that in these results, only the power-device conduction and switching losses are considered. This means that if losses associated to the gate-drivers and other losses had been taken into account, the real efficiencies would be a little lower. The difference between the efficiencies of the two inverters would also be reduced, since the MAC leg presents thirty six gate drivers, while the two-level converter presents only six.

3.6. Chip-area-based comparison between a four-level MAC leg and a conventional two-level leg

The switch cost, which usually represents around 25-30% of the total converter cost [72], is directly dependent on the semiconductor chip area [65]. The MAC topology presents a higher number of switches than conventional two-level topologies, and the difference is larger as the number of levels increases. This fact may give the impression that the total silicon area in a MAC converter can be much higher than in a two-level topology. However, the minimum total silicon area needed can be surprisingly lower in a MAC converter compared to a conventional two-level topology for certain operating conditions. A theoretical study is carried out in this section in order to compare the minimum total chip area of a four-level MAC converter versus a conventional two-level leg.

3.6.1. Description of the methodology

The methodology used to compare the required total semiconductor chip area of both topologies is based on the approach introduced in [72] and also used in [65]. The basic concept of the method relies on the fact that junction-to-heat-sink thermal resistance $R_{\mathrm{th,js}}$ and switch losses P_{S_x} (conduction losses $P_{\mathrm{cond,S}_x}$ + switching losses $P_{\mathrm{sw,S}_x}$) are dependent on the semiconductor chip area A_{S_x}. For a certain chip area A_{S_x} and device operating conditions (switch voltage and current, and switching frequency), the total switch power-loss P_{S_x} and the $R_{\mathrm{th,js}}$ can be estimated (to calculate P_{S_x}, a real device with a particular area is taken as a reference). Thereby, for a given heat sink temperature T_{s}, the resulting device junction temperature $T_{\mathrm{j,S}_x}$ can be calculated as

$$T_{\mathrm{j,S}_x} = T_{\mathrm{s}} + R_{\mathrm{th,js}}\left(A_{\mathrm{S}_x}\right) \cdot P_{\mathrm{S}_x}\left(A_{\mathrm{S}_x}\right). \tag{3.44}$$

The implemented algorithm, presented in Fig. 3.27, determines the minimum required semiconductor chip area A_{S_x} for an individual switch such that its maximum average junction temperature $T_{\mathrm{j,S}_x}$ is equal to a predefined maximum value $T_{\mathrm{j,S}_x,\mathrm{max}} = 125$ °C.

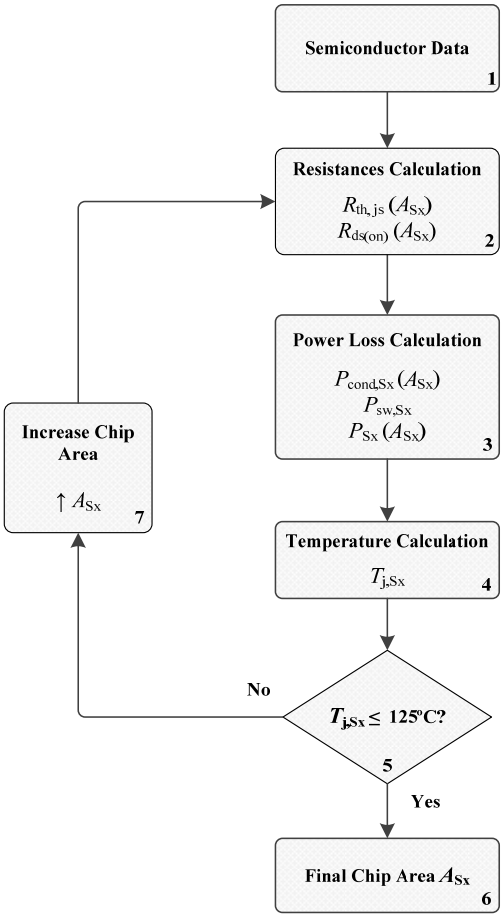


Fig. 3.27. Diagram of chip area optimization algorithm (based on Fig. 6 from [65]).

Initially, the chip area A_{S_x} is significantly small and the temperature T_{j,S_x} is higher than 125ºC. Then, the area is slightly increased. As thermal resistance $R_{th,js}$ and device conduction losses P_{cond,S_x} vary inversely with the chip area A_{S_x} variation, the resistance $R_{th,js}$ and semiconductor losses P_{S_x} decrease, and consequently the device junction temperature T_{j,S_x} also decreases, as it can be deduced from (3.44). This process is repeated until the temperature T_{j,S_x} reaches the value of 125ºC. Please note that the dependence of switching losses on the chip area has been assumed negligible.

The algorithm is performed to each one of the devices of the topology and then the total chip area of the topology is obtained adding up all the individual switch chip areas A_{S_x}.

3.6.2. Chip-area comparison scenario

The comparison is done using the same circuit configuration, operating mode and operating point (voltage and current rates) used in Section 3.4 to perform the efficiency comparison (see Fig.

3.12 and Fig. 3.13), since it represents simple and balanced conditions that allows inferring general conclusions.

The MOSFETs used in the previous section are taken as references to perform the chip-area comparison (200 V STP20NF20 in the four-level MAC leg and 600 V STF13NM60N in the two-level leg). In MOSFETs, the antiparallel body diode is inherently built with the transistor. As a result, the semiconductor chip area A_{S_x} includes both the transistor and the antiparallel diode, and total loss P_{S_x} comprises both the transistor and diode losses. This is an important difference compared to the studies presented in [72] and [65], where IGBTs are used as power switches, and diode and transistor chip areas are optimized independently, since in IGBTs, the diode and the transistor are implemented in separate silicon dies.

3.6.3. Algorithm implementation. Thermal and loss modeling

3.6.3.1. Resistances calculation (Block 2)

In order to obtain the value of the thermal resistance $R_{\mathrm{th,js}}$ as a function of the chip area A_{S_x}, some discrete MOSFETs have been opened to measure their chip areas and see their correlation with their datasheet values of $R_{\mathrm{th,js}}$. The complete results are presented in Appendix C. The obtained correlation is the following one:

$$R_{\mathrm{th,js}}\left(A_{S_x}\right) = 8.5\ \frac{^{\circ}\mathrm{C}}{\mathrm{W}\cdot\mathrm{mm}^2}\cdot {A_{S_x}}^{-0.6}\,. \tag{3.45}$$

This equation gives us a good estimation of the value of $R_{\mathrm{th,js}}$ since the value of $R_{\mathrm{th,js}}$ is essentially dependent on geometrical aspects, e.g., the chip area (it does not depend on the chip technology, e.g., the pn-doping distribution).

The strategy used to determine the correlation between $R_{\mathrm{th,js}}$ and A_{S_x} can not be used to determine the correlation between $R_{\mathrm{ds(on)}}$ and A_{S_x} since the value of $R_{\mathrm{ds(on)}}$ of a MOSFET does not only depend on the geometry (area), but also depends significantly on other factors like the voltage rating or the pn-doping distribution. As an example, for two devices with the same area, a thicker and more lightly doped epi layer allows it withstanding higher voltage but the on-resistance is increased.

Considering two MOSFETs (MOSFET 1 and MOSFET 2) with the same voltage rating and using the same pn-doping distribution, they should verify

$$R_{\mathrm{ds(on)},\mathrm{MOSFET\ 1}} \cdot A_{\mathrm{S}_x,\mathrm{MOSFET\ 1}} = R_{\mathrm{ds(on)},\mathrm{MOSFET\ 2}} \cdot A_{\mathrm{S}_x,\mathrm{MOSFET\ 2}} \cdot \tag{3.46}$$

Taking (3.46) into account, the value of $R_{\mathrm{ds(on)}}$ as a function of the area A_{S_x} can be obtained independently for the two topologies taking their respective MOSFETs as references:

$$R_{\mathrm{ds(on)},\mathrm{S}_x,4\mathrm{L}}\left(A_{\mathrm{S}_x}\right) = R_{\mathrm{ds(on)},\mathrm{STP20NF20}} \cdot \frac{A_{\mathrm{S}_x,\mathrm{STP20NF20}}}{A_{\mathrm{S}_x}} = \frac{0.097\ \Omega \cdot 9.88\ \mathrm{mm}^2}{A_{\mathrm{S}_x}} \tag{3.47}$$

$$R_{\mathrm{ds(on)},\mathrm{S}_x,2\mathrm{L}}\left(A_{\mathrm{S}_x}\right) = R_{\mathrm{ds(on)},\mathrm{STP13NM60N}} \cdot \frac{A_{\mathrm{S}_x,\mathrm{STP13NM60N}}}{A_{\mathrm{S}_x}} = \frac{0.28\ \Omega \cdot 11.20\ \mathrm{mm}^2}{A_{\mathrm{S}_x}}. \tag{3.48}$$

3.6.3.2. Power loss calculation (Block 3)

In order to calculate the device losses, the equations presented in Section 3.4.2.1 for device conduction losses and Section 3.4.2.2 for device switching losses are used. The switching losses of devices are exactly the same since they are not dependent on the chip area. The conduction losses, however, are calculated using the $R_{\mathrm{ds(on)}}$ as a function of A_{S_x} ((3.47) and (3.48)).

3.6.3.3. Temperature calculation (Block 4)

Equation (3.44) represents the thermal model to obtain the temperature $T_{\mathrm{j},\mathrm{S}_x}$. The temperature of the heat sink T_{s} is assumed to be 80°C.

3.6.4. Chip-area optimization results

Fig. 3.28 presents the ratio between the total required chip areas for both topologies under different switching frequencies. It can be seen that for frequencies above 25-30 kHz, the total chip area of the four-level MAC leg is lower than the two-level leg despite having a higher number of devices (twelve devices against two).

It is important to note that these results have been obtained in the particular case of devices STP20NF20 and STP13NM60N, since they have been taken as references to calculate the losses and subsequently the resulting chip area. Device STP13NM60N presents a particularly low on-resistance for a 600 V MOSFET, which makes it specially suitable for low switching frequencies. This fact possibly causes that for low switching frequencies, the two-level leg requires less area than the four-level leg. If other devices were chosen, it would be possible that the total area required by the four-level leg be lower than the required by the two-level leg for all the frequency range.

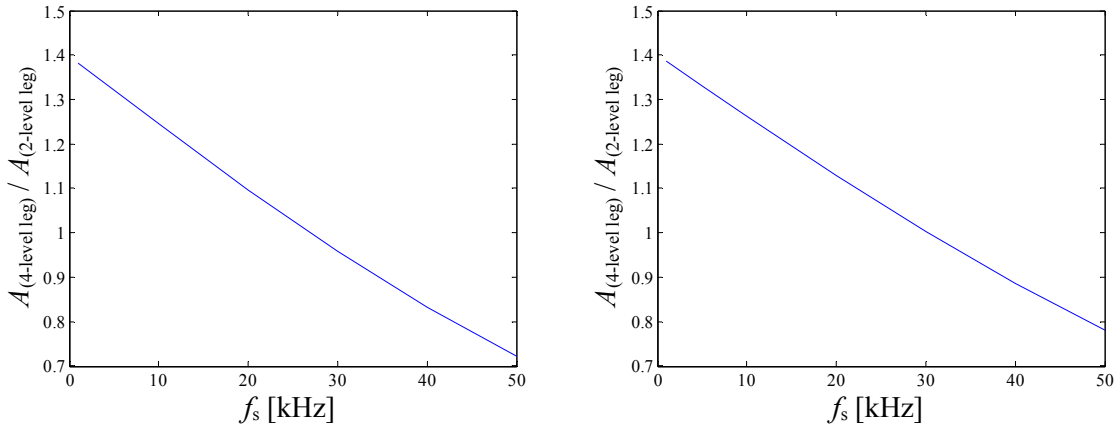


Fig. 3.28. Leg-chip-area ratio with the setup presented in Section 3.4.1. (a) Conditions: V_{dc} = 150 V, L = 60 mH, and R = 8 Ω. (b) V_{dc} = 150 V, L = 60 mH, and R = 16 Ω.

3.7. Conclusion

An assessment of the MAC converter efficiency has been performed in this chapter. First, device conduction and switching losses have been analyzed in depth. Then, the efficiency of the MAC topology has been assessed through analytical and experimental comparisons with to conventional two-level converters.

According to the analysis of conduction and switching losses it can be concluded that, if devices are properly selected for a certain operating point, both conduction losses and switching losses should be lower in the MAC topology than in a two-level topology. Regarding the conduction losses, on one hand, the fact that $r_{\mathrm{ds(on)}}$ varies exponentially with the device blocking voltage, as shown in (3.2), and on the other hand, the reduced equivalent ON resistance thanks to the parallel conduction of current, lead to a reduction of overall conduction losses. In regard to switching losses, they should be lower not only because low-voltage-rated devices can be used with better relative performance features, but also because all switching transitions occur at lower blocking voltage levels, which in principle should produce lower switching losses for the same switching frequency and switching characteristics, as deduced from (3.5).

Compared to other multilevel converters, conduction losses should be lower in the MAC topology thanks to the parallel conduction of current. With regard to switching losses, they should be similar to other multilevel topologies. Nevertheless, in the MAC topology there is certain degree of freedom to distribute the switching losses among the devices.

The efficiency of a four-level MAC leg has been compared analytically and experimentally with a two-level leg, under a simple and balanced control pattern that allow us inferring general

conclusions. The efficiency of the MAC leg is higher in all the frequency-range. Losses that depend on the switching frequency (mainly power-device switching-losses) are significantly lower in the four-level MAC leg. This is an important advantage of the MAC topology since it permits to increase the switching frequency, which allows reducing the size, the weight, and the cost of passive components. The close proximity between analytical and experimental results supports the obtained conclusions of the study and validates the analytical loss models.

The efficiency of the MAC converter has also been compared analytically with a two-level converter operating as three-phase inverters. The comparison has been performed for several combinations of values of the switching frequency, the modulation index, the phase load angle, and the phase load impedance. The efficiency of the four-level MAC inverter is higher under all conditions. The advantage is also more significant as the switching frequency increases.

Finally, a theoretical study to determine the minimum chip area needed for both topologies has also been carried out. The minimum area is lower in the MAC leg for switching frequencies above 20-30 kHz despite presenting twelve devices instead of two.

It is important to note that all these comparisons have been carried out for a particular selection of MOSFETs. The results would vary if other devices had been selected.

CHAPTER 4

FAULT-TOLERANCE CAPACITY OF THE MULTILEVEL ACTIVE-CLAMPED CONVERTER

Abstract — Thanks to the inherent redundancy to generate the different output voltage levels, the MAC topology presents an important fault-tolerance ability which makes it interesting for several applications. This chapter presents an analysis of the fault-tolerance capacity of the MAC converter. Both open-circuit and short-circuit faults are considered and the analysis is carried out under single-device and two-simultaneous-device faults. Switching strategies and different hardware modifications to overcome the limitations caused by faults are proposed. Experimental tests with a four-level MAC prototype are presented to validate the analysis.

4.1. Introduction

In a recent industry-based survey of reliability in power electronic converters [73], semiconductor power devices are largely considered the most fragile components, and appear to be one of the main concerns regarding power-converters reliability. This confirms that device-fault-tolerance requirements in power converters are of extreme importance at present time, especially for those safety-critical applications in which the consequences of stopping the process would be very serious or expensive.

At a first glance, multilevel topologies may appear to have a lower reliability than conventional two-level topologies because they present a large number of devices. Nevertheless, the lower voltage and current ratings of switches in multilevel converters, together with the usage of higher voltage and current margins, lead to a reduced device electrical and thermal stress, which may decrease their probability of failure. In addition, multilevel converters present a better fault-tolerance capacity thanks to their inherent redundancy. As a consequence of these facts, multilevel converters may present a higher reliability than conventional two level converters. However, it is important to realize that in most multilevel topologies some switches may experience higher voltages or currents under fault-handling management. This usually implies the need of selecting devices with higher voltage and current ratings to take advantage of the multilevel-converter fault-tolerance capacity.

Several fault-tolerance analyses and solutions to improve the fault-tolerance capacity of multilevel converters under open-circuit and short-circuit faults have been reported in the literature [52], [74]-[80]. Reference [74] presents a comprehensive review of the numerous proposals to

detect faults and to operate under faulty conditions for the three basic multilevel topologies. In [75], an analysis of the fault-tolerance capacity of the ANPC topology [40] is presented. Furthermore, switching states different to the ones presented in [40] are proposed to be used under single-device short-circuit and open-circuit faults. Reference [52] proposes the topology presented in Fig. 1.10 in which two additional switches are included and some flying capacitors are removed from the generalized multilevel topology in order to improve the fault-tolerance ability against short-circuit and open-circuit faults.

This chapter analyzes the fault-tolerance capacity of the MAC topology. The chapter is divided as follows. Section 4.2 details the assumptions of the fault-tolerance analysis of the MAC topology. Section 4.3 presents the analysis and switching strategy under short-circuit faults, and Section 4.4 under open-circuit faults. Section 4.5 presents experimental results to validate the previous analyses. In Section 4.6, three hardware modifications to improve the fault-tolerance ability of the MAC topology are presented, and Section 4.7 outlines the conclusions.

4.2. Fault-tolerance analysis assumptions

To carry out the analysis, the following assumptions are made:

1) Fault types: Since a single device may fail in open or short-circuit depending on the fault characteristics, both open-circuit and short-circuit faults are considered for the analysis. Typically, a single device fails in open-circuit when drain current is exceeded, which causes the bond wires to break creating an open-circuit. A fault in the gate-driver circuit is another cause of open-circuit conditions (if normally-off devices are used). For the analysis, it is considered that an open-circuit fault implies an open-circuit condition in the whole device (switch + antiparallel diode). Short-circuit faults typically occur when the maximum junction temperature or the maximum blocking voltage is exceeded.

2) Fault diagnosis: It is assumed that the fault detection system is capable of identifying device short-circuit and open-circuit faults, and it is able to transmit this information (failed device and fault type) fast enough to change the switching control scheme immediately, if necessary. This fault detection system could be integrated into the gate-driver circuitry. In fact, most gate-driver circuits already incorporate detection and protection functions [74]. A possibility to implement the fault diagnosis system into the gate-driver circuitry has been presented in [81], where the delay time of the fault detection system is less than 3 μs. The switching control scheme could be implemented for example in a FPGA, including the whole programming to be able to change instantaneously the switching strategy in case of a fault detection.

3) Converter configuration: Dc-voltage sources connected across every two adjacent input terminals are considered, see Fig. 4.1(left). The analysis would also be valid if batteries across adjacent input terminals were considered. Fig. 4.1(right) presents the four-level case of a proposed converter leg representation to facilitate the analysis of the converter operation under device faults. Note the representation of the four possible device states in the inset of Fig. 4.1.

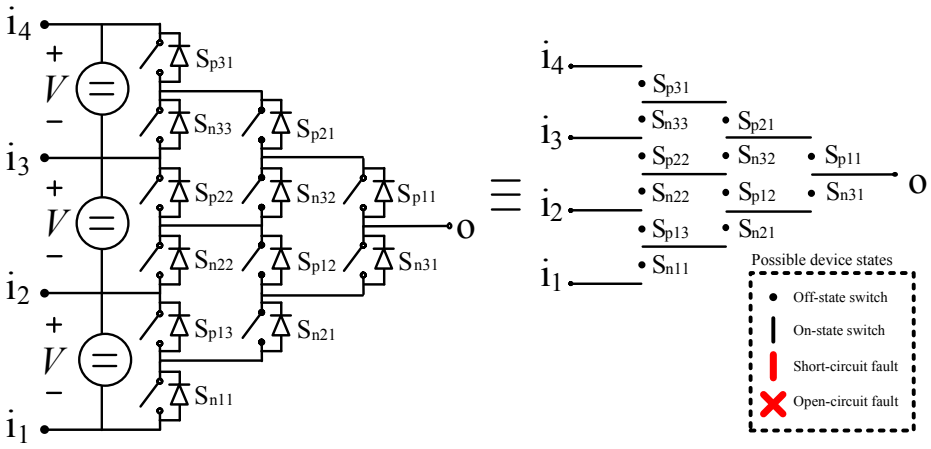


Fig. 4.1. Four-level MAC converter leg representation.

4.3. Fault-tolerance analysis under short-circuit faults

Using original switching states presented in Section 2.2.1, if one device fails in short circuit, it would not be possible to connect the output terminal to some input terminals, because a dc-voltage source would be short circuited. Fig. 4.2 shows some examples for a four-level leg. In Fig. 4.2(a) it can be seen that the connection to level 4 under a short-circuit fault in device S_{n31} would produce a short-circuit path in the dc-voltage source connected across input terminals i_3 and i_4. Similar examples can be observed in Fig. 4.2(b), Fig. 4.2(c), and Fig. 4.2(d) when a short-circuit fault occurs in devices S_{p12} and S_{n21}.

Table 4.1 presents a summary of available levels for a four-level leg when one device fails in short-circuit and original switching states are used. Table 4.1 only shows the bottom half devices due to symmetry. If two devices fail simultaneously, the overall lost levels would be the addition of lost levels caused by a fault of each one of the failed devices, according to Table 4.1. Thus, for example, if S_{n31} and S_{p12} fail simultaneously, levels 1 and 4 would be lost.

The fault-tolerance ability can be improved by properly modifying some of the original switching states, as it is explained below.

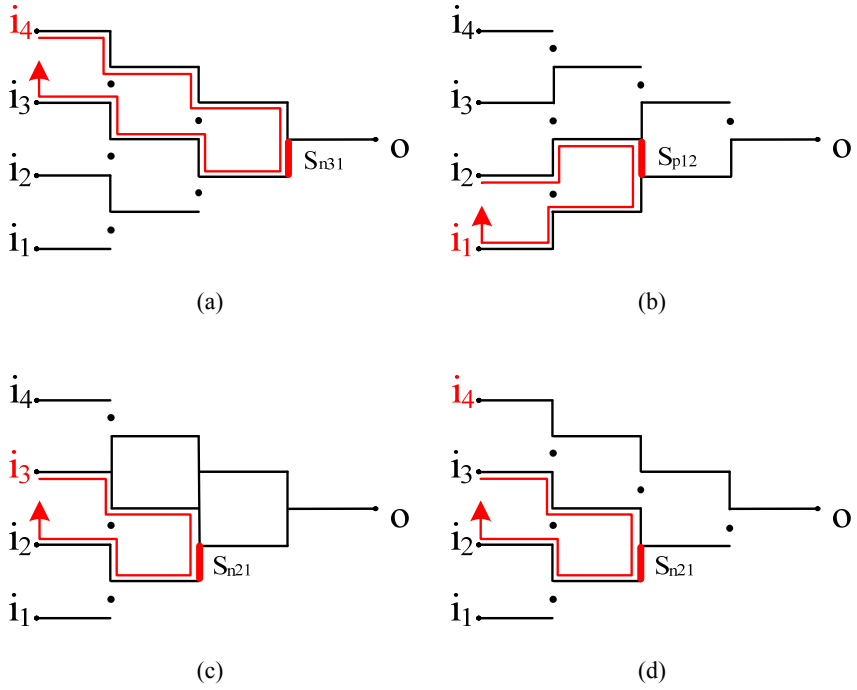


Fig. 4.2. Some examples of single-device short-circuit faults using original switching states. (a) Connection to level 4 under a short-circuit fault in device S_{n31}. (b) Connection to level 1 under a short-circuit fault in device S_{p12}. (c) Connection to level 3 under a short-circuit fault in device S_{n21}. (d) Connection to level 4 under a short-circuit fault in device S_{n21}.

Failed device	Levels			
	1	2	3	4
S_{n31}	✓	✓	✓	✗
S_{p12}	✗	✓	✓	✓
S_{n21}	✓	✓	✗	✗
S_{n22}	✓	✓	✗	✗
S_{p13}	✗	✓	✓	✓
S_{n11}	✓	✗	✗	✗

Table 4.1. Available levels under a short-circuit fault using original switching states in a four-level leg.

There are some critical devices in which a short-circuit fault necessarily implies the loss of one level. For example, a short-circuit fault in devices S_{p11}, S_{p12}, or S_{p13} implies the loss of level 1. Similarly, a short-circuit fault in symmetrical devices S_{n31}, S_{n32}, or S_{n33} implies the loss of level 4. This is due to the fact that the connection of the output terminal to lower level 1 and upper level 4 do not present redundant paths for the load current to flow. This fact can be appreciated in the two examples of Fig. 4.3. In Fig. 4.3(a), it can be seen that if it is desired to connect the output to level 4 under a fault in device S_{n31}, a short-circuit path would be formed through the antiparallel diodes of devices S_{p12} and S_{p22}. A similar scenario is presented in Fig. 4.3(b).

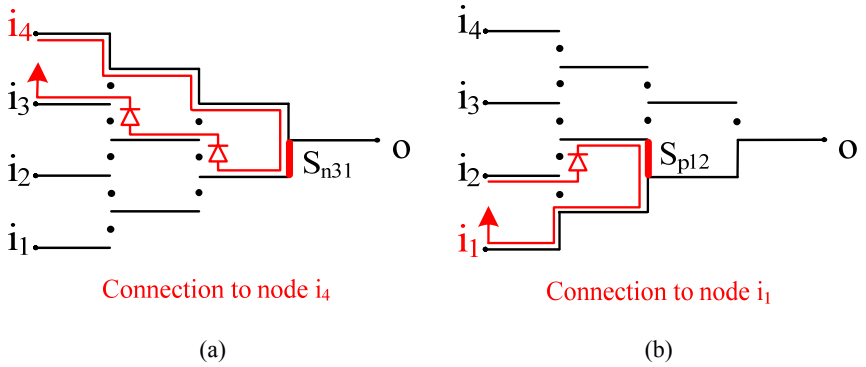


Fig. 4.3. Two examples in which a short-circuit fault necessarily implies the loss of one level. (a) Loss of level 4 due to a short-circuit fault in device S_{n31}. (b) Loss of level 1 due to a short-circuit fault in device S_{p12}.

Nevertheless, if one of the remaining devices (S_{n11}, S_{n21}, S_{n22}, S_{p31}, S_{p21}, and S_{p22}) fails in short-circuit, it will be possible to connect the output to all four input terminals through the definition of new switching states, thanks to the inherent redundancy of the MAC topology. However, in some cases, it will produce an increase of the blocking voltage in certain devices. As an example, Fig. 4.4 presents two new switching states to connect the output to levels 3 and 4 under a short-circuit fault of device S_{n21}. Note that the blocking voltage of device S_{n31} increases to $2V$ in the connection to node i_4.

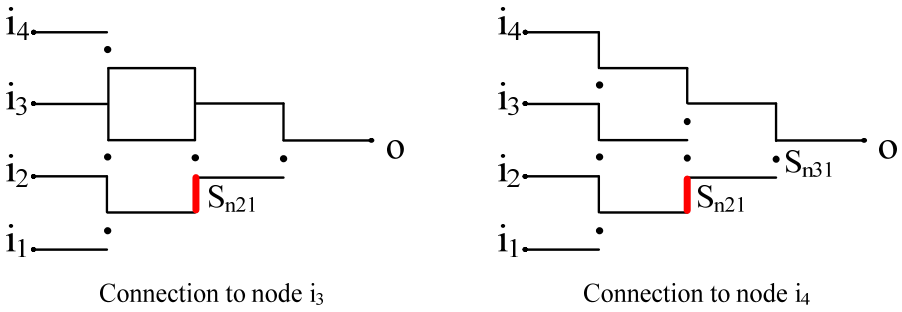


Fig. 4.4. Modified switching states under a short-circuit fault in device S_{n21}.

Now let us consider a case in which two devices fail simultaneously. For example, Fig. 4.5 presents the four new switching states to connect the output to all the input terminals when devices S_{p22} and S_{n21} fail at the same time. In this interesting case, no levels are lost despite of the failure of two devices.

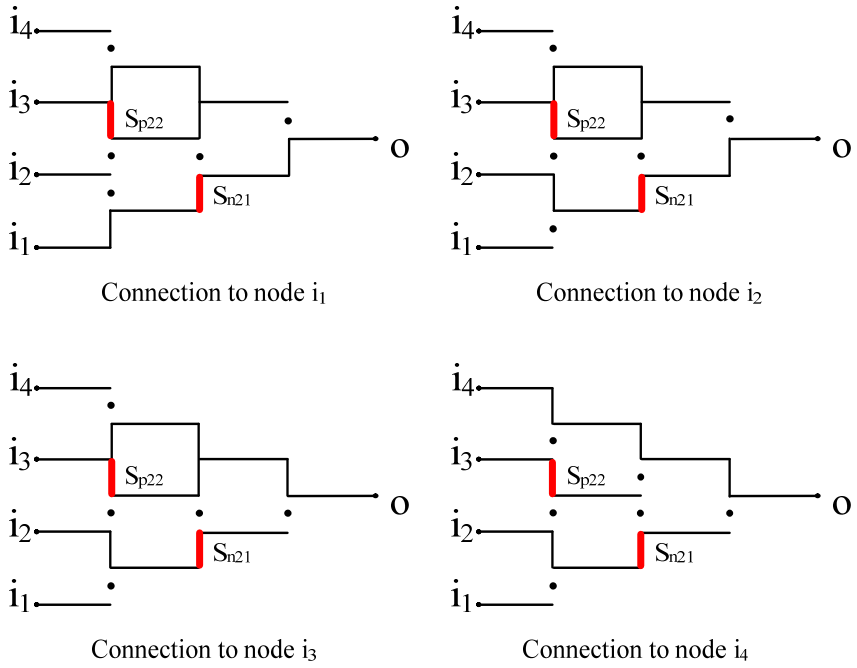


Fig. 4.5. Modified switching states under simultaneous short-circuit faults in devices S_{n21} and S_{p22}.

The following rules are applied to define the new switching states:

i) Do not leave floating points; i.e., all open devices have to withstand an integer multiple of *V*.

ii) Minimize the maximum blocking voltage of devices.

iii) In order to reduce the conduction losses, maximize the number of parallel current paths, provided that it does not imply an increase of the maximum blocking voltage of devices.

As explained above, in some device faults, new switching states can be defined to avoid the short-circuit paths that are produced with the original switching states. However, the blocking voltage of some devices is increased in some cases. According to this, two different switching schemes are proposed. The first of them prioritizes the number of available levels. In the second one, the highest priority is to maintain the original device blocking voltage.

4.3.1. Switching scheme I (SSI): Prioritization of number of levels

SSI consists in using, whenever possible, new switching states in order to maximize the number of available levels, although in some cases it implies an unavoidable increase of the blocking voltage of some devices. The rules presented above are used to define the new switching states.

Table 4.2 presents a summary of the four-level MAC converter leg operating features under one and two short-circuit faults applying the proposed SSI. Table 4.2 only shows relevant cases due to symmetry. Note the large short-circuit fault-tolerance capacity of the MAC topology. The four-level MAC converter can always continue operating under a single-device short-circuit fault maintaining at least three of the four levels. Regarding two simultaneous device faults, the converter generally can continue operating with at least two levels, and in most cases, with three or even four levels.

Fault case	Failed devices	Levels				Devices under overvoltage
		1	2	3	4	
1	S_{n31}	✓[a]	✓	✓	✗[b]	None
2	S_{p12}	✗	✓	✓	✓	None
3	S_{n21}	✓	✓	✓[c]	✓	S_{n31} (2V)
4	S_{n22}	✓	✓	✓	✓	S_{n31}, S_{n32} (2V)
5	S_{p13}	✗	✓	✓	✓	None
6	S_{n11}	✓	✓	✓	✓	S_{n21} (2V)
7	S_{n31}, S_{p12}	✗	✓	✓	✗	None
8	S_{n31}, S_{n21}	✓	✓	✗	✗	None
9	S_{n31}, S_{n22}	✓	✓	✗	✗	None
10	S_{n31}, S_{p13}	✗	✓	✓	✗	None
11	S_{n31}, S_{n11}	✓	✓	✓	✗	S_{n21} (2V)
12	S_{n31}, S_{n32}	✓	✓	✓	✗	None
13	S_{n31}, S_{p21}	✓	✓	✓	✗	S_{p11} (2V)
14	S_{n31}, S_{p22}	✓	✓	✓	✗	S_{p11}, S_{p12} (2V)
15	S_{n31}, S_{n33}	✓	✓	✓	✗	None
16	S_{n31}, S_{p31}	✓	✓	✓	✗	S_{p21} (2V)
17	S_{p12}, S_{n21}	✗	✓	✓	✓	S_{n31}, S_{n32} (2V)
18	S_{p12}, S_{n22}	✗	✓	✓	✓	S_{n31}, S_{n32} (2V)
19	S_{p12}, S_{p13}	✗	✓	✓	✓	None
20	S_{p12}, S_{n11}	✗	✓	✓	✓	S_{n21} (2V)
21	S_{p12}, S_{p21}	✗	✓	✓	✓	None
22	S_{p12}, S_{p22}	✗	✗	✓	✓	None
23	S_{p12}, S_{n33}	✗	✓	✓	✗	None
24	S_{p12}, S_{p31}	✗	✓	✓	✓	S_{p21} (2V)
25	S_{n21}, S_{n22}	✓	✓	✓	✓	S_{n31}, S_{n32} (2V)
26	S_{n21}, S_{p13}	✗	✓	✓	✓	S_{p11} (2V)
27	S_{n21}, S_{n11}	✓	✓	✓	✓	S_{n31} (3V), S_{p12} (2V)
28	S_{n21}, S_{p22}	✓	✓	✓	✓	S_{n31}, S_{p12}, S_{p11} (2V)
29	S_{n21}, S_{n33}	✓	✓	✓	✗	None
30	S_{n21}, S_{p31}	✓	✓	✓	✓	S_{p21} (2V)
31	S_{n22}, S_{p13}	✗	✓	✓	✓	S_{n31}, S_{n32} (2V)
32	S_{n22}, S_{n11}	✓	✓	✓	✓	S_{n31}, S_{n32} (2V)
33	S_{n22}, S_{n33}	✓	✓	✓	✗	S_{n31}, S_{n32} (2V)
34	S_{n22}, S_{p31}	✓	✓	✗	✓	S_{n31}, S_{n32}, S_{p21} (2V)
35	S_{p13}, S_{n11}	-	-	-	-	-
36	S_{p13}, S_{p31}	✗	✓	✓	✓	None
37	S_{n31}, S_{p11}	✗	✓	✓	✗	None
38	S_{p12}, S_{n32}	✗	✓	✓	✗	None
39	S_{n21}, S_{p21}	✓	✓	✓	✓	S_{n31}, S_{p11} (2V)
40	S_{n22}, S_{p22}	-	-	-	-	-
41	S_{p13}, S_{n33}	✗	✓	✓	✗	None
42	S_{n11}, S_{p31}	✓	✓	✓	✓	S_{n21}, S_{p21} (2V)

(a) The level is achievable using the original switching state.

(b) The level is lost.

(c) The level is achievable using a new defined switching state.

Table 4.2. Four-level leg operating features under one or two short-circuit faults applying SSI.

The failure of one device may also require changes in the converter control (in particular, the modulation strategy). As an example, let us analyze a four-level three-phase MAC inverter. Fig. 4.6 presents the space vector diagram (SVD) for the four-level three-phase MAC inverter [82].

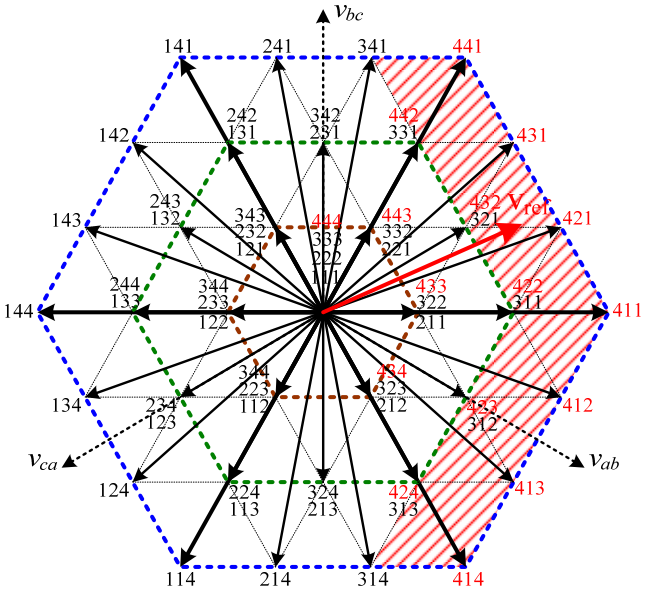


Fig. 4.6. SVD for the four-level three-phase MAC inverter.

In failure cases in which no levels are lost, the SVD remains identical; i.e., all the original vectors can be synthesized by properly modifying the original switching states in any of the three phases.

In cases in which a level is lost, the resultant SVD is different to the original one. Let us consider a failure case in phase *a* in which level 4 is lost. In this case, the red switching states of Fig. 4.6 are lost, so the resultant SVD would be the same one of Fig. 4.6, but removing the vectors corresponding with switching states 441, 431, 421, 411, 412, 413, and 414. As a result, reference vector V_{ref} could not be synthesized in the red zone of Fig. 4.6. Therefore, the applicable SVD region would be the medium green hexagon. This resultant applicable SVD would be the same if either level 1 or level 4 is lost in one, two, or the three phases of the inverter. Similarly, it can be deduced that in cases in which level 1 and 2 or level 3 and 4 are lost in one, two or the three phases, the resultant applicable SVD would be the small brown hexagon. In cases in which just an inner level (level 2 or 3) is lost, some vectors are removed from the SVD, but it is always possible to synthesize the reference vector within the large blue hexagon (increasing the total harmonic distortion).

4.3.1.1. Observations in a general m-level leg using SSI

In the following, the lost levels are specified as a function of the failed devices in a general *m*-level leg, considering one- and two-failed-device cases.

a) One-failed-device cases

i) If the failed device is one of the devices S_{p1j} (for j = 1, 2, …, m–1), level 1 is lost. Fig. 4.7 presents these devices circled with a blue solid line. As they form a diagonal, it will be referred as the "short-circuit level-1 critical diagonal".

ii) If the failed device is one of the devices $S_{n(m-1)j}$ (for j = 1, 2, …, m–1), level m is lost. Fig. 4.7 presents these devices circled with a red dotted line. It will be referred as the "short-circuit level-*m* critical diagonal". This diagonal and the previous one form the two "short-circuit critical diagonals".

iii) If the failed device does not belong to any of the two short-circuit critical diagonals, all levels are preserved.

b) Two-failed-device cases

i) If both failed devices belong to the short-circuit level-1 critical diagonal, only level 1 is lost. If both failed devices belong to the short-circuit level-*m* critical diagonal, only level m is lost.

ii) If one of the two failed devices belongs to the short-circuit level-1 critical diagonal, and the other one belongs to the short-circuit level-*m* critical diagonal, both level 1 and m are lost.

iii) If neither of both failed devices belongs to any of the two short-circuit critical diagonals, no levels are lost, except if the fault case is a "short-circuit fatal special case" or a "short-circuit inner special case" (special cases are explained below).

iv) If one of the two failed devices belongs to the short-circuit level-1 critical diagonal, and the other one does not belong to any of the two short-circuit critical diagonals, only level 1 is lost, except if the fault case is a "short-circuit fatal special case," a "short-circuit stair special case," or a "short-circuit chain special case". The reasoning is analogous for level m.

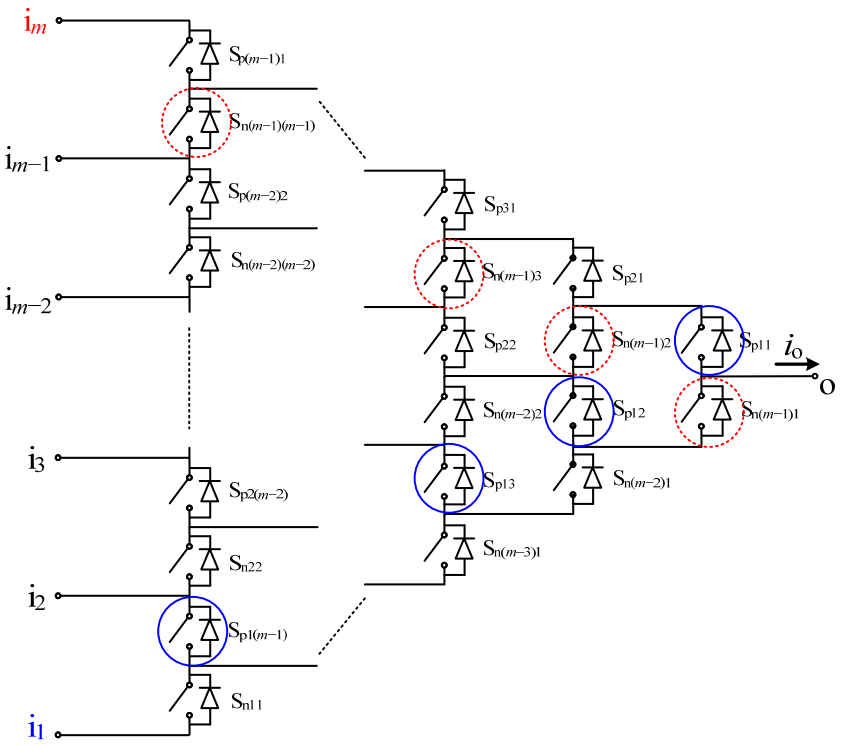


Fig. 4.7. Short-circuit critical diagonals in a general m-level leg.

The two-failed-device short-circuit special cases are the following:

- Short-circuit fatal (scf) special case: the m–1 scf special cases occur when the two failed devices are S_{nkk} and $S_{pk(m-k)}$ (for k = 1, 2, …, m–1). These two devices are connected across one of the dc-voltage sources. Therefore, short-circuit faults in these devices would cause an unavoidable short-circuit of the associated dc-voltage source, see Fig. 4.8(a).

- Short-circuit inner (sci) special case: the m–2 sci special cases occur when the two failed devices are S_{nkk} and $S_{p(k+1)(m-k-1)}$ (for k = 1, 2, …, m–2). In this special case, one of the inner levels is lost, see Fig. 4.8(b).

- Short-circuit stair (scs) special case: the 2·(m–2) scs special cases occur when the two failed devices are S_{p1j} and S_{p2j} (for j = 1, 2, …, m–2), or $S_{n(m-1)j}$ and $S_{n(m-2)j}$ (for j = 1, 2, …, m–2). In this special case, both level 1 and level 2 are lost if S_{pkj} devices fail, see Fig. 4.8(c), and both level m and level m–1 are lost if S_{nkj} devices fail.

- Short-circuit chain (scc) special case: the 2·(m–3) scc special cases occur when the two failed devices are S_{p1j} and $S_{p2(j+1)}$ (for j = 1, 2, …, m–3), or $S_{n(m-1)j}$ and $S_{n(m-2)j}$ (for j = 1, 2, …, m–3). As in the previous case, both level 1 and level 2 are lost if S_{pkj} devices fail, see Fig. 4.8(d), and both level m and level m–1 are lost if S_{nkj} devices fail.

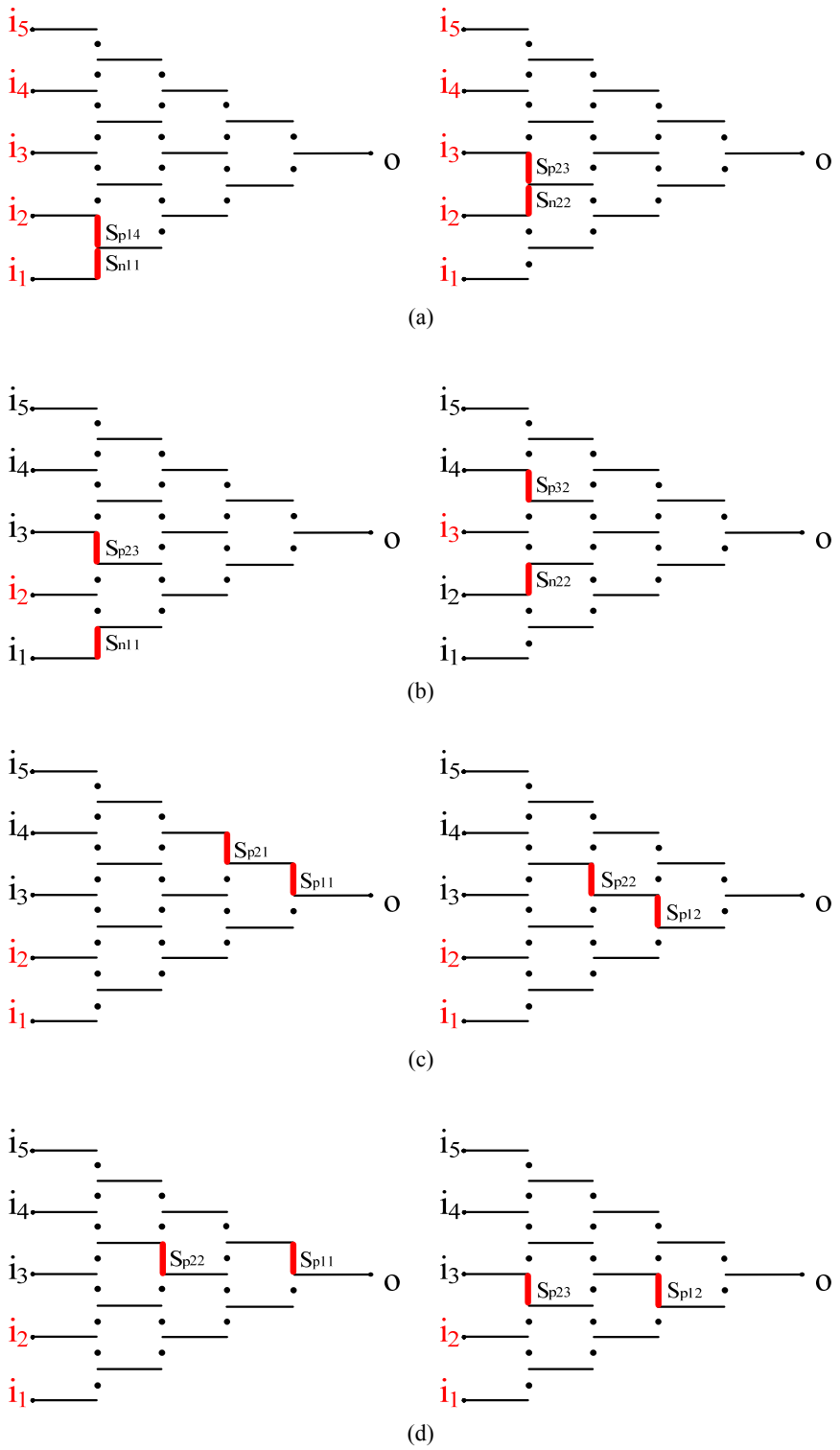


Fig. 4.8. Short-circuit special cases in a five-level MAC converter. (a) Two examples of scf special case. (b) Two examples of sci special case. (c) Two examples of scs special case. (d) Two examples of scc special case.

From the analysis above, we can conclude that a *m*-level MAC converter leg under an arbitrary two-failed-device fault only loses a maximum of two levels regardless of the number of levels of the converter (except in the short-circuit fatal special cases).

It is also possible to establish a general rule for an *m*-level MAC converter in order to determine which switching states have to be redefined as a function of the failed devices. The following rule is valid for one- and two-failed device cases.

i) If one of the failed devices corresponds to a device S_{nkj}, switching states for connecting the output to levels k+1, k+2, …, and m, have to be redefined.

ii) If one of the failed devices corresponds to a device S_{pkj}, switching states for connecting the output to levels 1, 2…, and k, have to be redefined.

4.3.2. Switching scheme II (SSII): Prioritization of the blocking voltage

As it can be seen in Table 4.2, using SSI, the blocking voltage of some devices increases in some cases. This implies the need to select devices with high breakdown voltage. To avoid this, a new switching scheme is proposed equal to SSI but removing all switching states that produce a blocking voltage higher than V. Table 4.3 summarizes the operating features of a four-level leg operated with SSII.

4.3.2.1. Observations in a general m-level leg using SSII

The particular analysis for SSII regarding the lost levels as a function of the failed devices is detailed in the following.

a) One-failed-device cases

i) If the failed device is S_{pkj} (for any value of k and j), level 1 is lost.

ii) If the failed device is S_{nkj} (for any value of k and j), level m is lost.

b) *Two-failed-device cases*

i) If one failed device is $S_{p(k1)(j1)}$ (for any value of $k1$ and $j1$) and the other failed device is $S_{n(k2)(j2)}$ (for any value of $k2$ and $j2$), levels 1 and m are lost.

ii) If the two failed devices are $S_{n(k1)(j1)}$ and $S_{n(k2)(j2)}$, level m is lost. If $k1 > k2$ and $(k1–j1) > (k2–j2)$, level $m–1$ is also lost. The cases in which the failed devices are S_{pkj} correspond to symmetrical cases. Thus, the conclusions are the same, but for levels 1 and 2 instead of levels m and $m–1$.

Fault case	Failed devices	Levels				Devices under overvoltage
		1	2	3	4	
1	S_{n31}	✓	✓	✓	✗	None
2	S_{p12}	✗	✓	✓	✓	None
3	S_{n21}	✓	✓	✓	✗	None
4	S_{n22}	✓	✓	✓	✗	None
5	S_{p13}	✗	✓	✓	✓	None
6	S_{n11}	✓	✓	✓	✗	None
7	S_{n31}, S_{p12}	✗	✓	✓	✗	None
8	S_{n31}, S_{n21}	✓	✓	✗	✗	None
9	S_{n31}, S_{n22}	✓	✓	✗	✗	None
10	S_{n31}, S_{p13}	✗	✓	✓	✗	None
11	S_{n31}, S_{n11}	✓	✓	✗	✗	None
12	S_{n31}, S_{n32}	✓	✓	✓	✗	None
13	S_{n31}, S_{p21}	✗	✓	✓	✗	None
14	S_{n31}, S_{p22}	✗	✓	✓	✗	None
15	S_{n31}, S_{n33}	✓	✓	✓	✗	None
16	S_{n31}, S_{p31}	✗	✓	✓	✗	None
17	S_{p12}, S_{n21}	✗	✓	✓	✗	None
18	S_{p12}, S_{n22}	✗	✓	✓	✗	None
19	S_{p12}, S_{p13}	✗	✓	✓	✓	None
20	S_{p12}, S_{n11}	✗	✓	✓	✗	None
21	S_{p12}, S_{p21}	✗	✓	✓	✓	None
22	S_{p12}, S_{p22}	✗	✗	✓	✓	None
23	S_{p12}, S_{n33}	✗	✓	✓	✗	None
24	S_{p12}, S_{p31}	✗	✗	✓	✓	None
25	S_{n21}, S_{n22}	✓	✓	✓	✗	None
26	S_{n21}, S_{p13}	✗	✓	✓	✗	None
27	S_{n21}, S_{n11}	✗	✓	✓	✗	None
28	S_{n21}, S_{p22}	✗	✓	✓	✗	None
29	S_{n21}, S_{n33}	✓	✓	✓	✗	None
30	S_{n21}, S_{p31}	✗	✓	✓	✗	None
31	S_{n22}, S_{p13}	✗	✓	✓	✗	None
32	S_{n22}, S_{n11}	✓	✓	✓	✗	None
33	S_{n22}, S_{n33}	✓	✓	✓	✗	None
34	S_{n22}, S_{p31}	-	-	-	-	-
35	S_{p13}, S_{n11}	-	-	-	-	-
36	S_{p13}, S_{p31}	✗	✓	✓	✓	None
37	S_{n31}, S_{p11}	✗	✓	✓	✗	None
38	S_{p12}, S_{n32}	✗	✓	✓	✗	None
39	S_{n21}, S_{p21}	✗	✓	✓	✗	None
40	S_{n22}, S_{p22}	-	-	-	-	-
41	S_{p13}, S_{n33}	✗	✓	✓	✗	None
42	S_{n11}, S_{p31}	✗	✓	✓	✗	None

Table 4.3. Four-level leg operating features under one or two short-circuit faults applying SSII.

Using SSII, as using SSI, an *m*-level MAC converter leg under an arbitrary two-failed-device fault only loses a maximum of two levels regardless of the number of converter levels except in the scf or sci special cases. If a sci special case takes place, it is not possible to define a new switching state without increasing the blocking voltage of some devices.

4.4. Fault-tolerance analysis under open-circuit faults

Using original switching states under open-circuit faults represents a good solution since it maximizes the number of available levels and the maximum device blocking voltage only increases slightly; all this without the necessity of defining new switching states. However, if any level is

lost, it is necessary to adjust the modulation strategy to the new set of available levels, according to the discussion previously presented in Section 4.3.

As in short-circuit cases, there are some critical devices in which an open-circuit fault implies a level to be lost. For example, in a four-level leg, an open-circuit fault in devices S_{n11}, S_{n21}, or S_{n31} implies the loss of level 1. Similarly, a fault in their symmetrical devices implies the loss of level 4. As an example, Fig. 4.9 presents the case in which S_{n31} fails in open circuit.

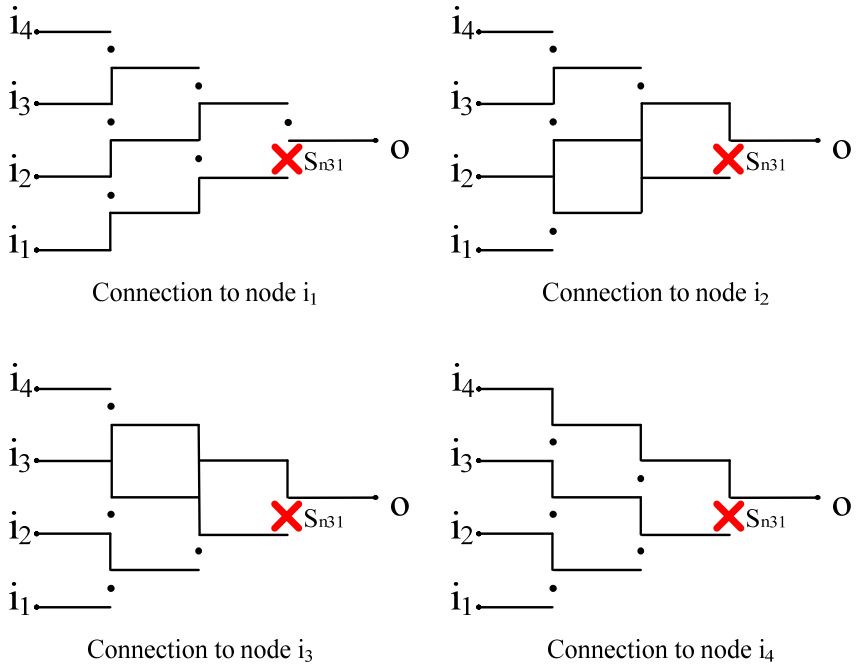


Fig. 4.9. Open-circuit fault of device S_{n31} in a four-level leg.

Fig. 4.10 shows the case of an open-circuit fault of S_{p12} in which the connection to all four levels is achievable. As it can be observed in the case of connection to level 4, a floating point appears. In order to eliminate this floating point, one possibility may be to turn on S_{n31} or S_{n21}, but the maximum blocking voltage would increase to $2V$. Using the original switching state, the blocking voltage of devices S_{n31} and S_{n21} is in principle undetermined. However, these blocking voltage values can be determined if OFF-state balancing-resistors are embedded in the converter hardware.

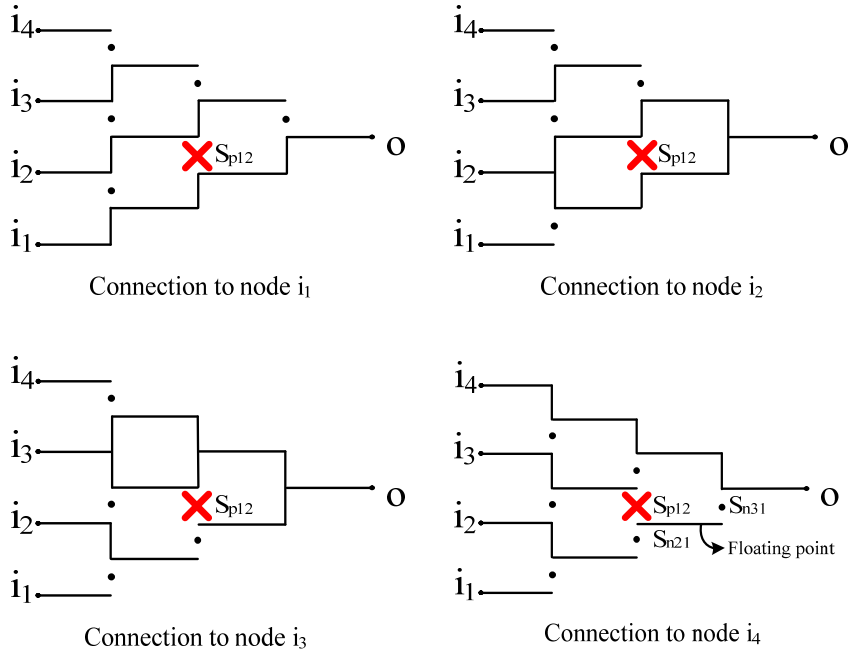


Fig. 4.10. Open-circuit fault of device S_{p12} in a four-level leg.

OFF-state balancing-resistors are high-value resistors used to balance the blocking voltage of all devices when they are all in OFF state, see Appendix A. Fig. 4.11(a) shows the relative values of these resistors in a four-level leg. Fig. 4.11(b) shows the relevant relative values in the case of connection to level 4 under a fault in S_{p12}. The resulting blocking voltage of S_{n31} is equal to $1.25V$.

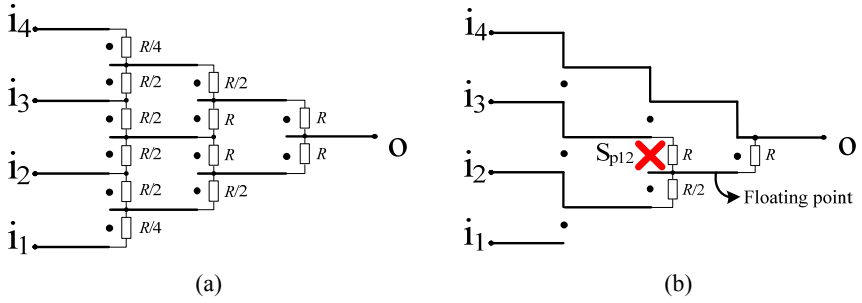


Fig. 4.11. OFF-state balancing resistors. (a) Relative values in a four-level leg. (b) Relevant relative values under an open-circuit fault of device S_{p12}.

Table 4.4 presents a summary of the four-level leg operating features under one and two open-circuit faults. As it can be observed, the fault-tolerance capacity of the MAC topology against open-circuit faults is also very high, since the converter can always continue operating under a single-device fault maintaining at least three of the four levels. In two-failed-device cases, the converter can continue operating in almost all cases with at least two levels, and in most cases, with three or even four levels.

Fault case	Failed devices	Levels				Devices under overvoltage
		1	2	3	4	
1	S_{n31}	✗	✓	✓	✓	None
2	S_{p12}	✓	✓	✓	✓	S_{n31} (1.25V)
3	S_{n21}	✗	✓	✓	✓	None
4	S_{n22}	✓	✓	✓	✓	S_{p11}. S_{p12} (1.25V)
5	S_{p13}	✓	✓	✓	✓	S_{n21} (1.25V)
6	S_{n11}	✗	✓	✓	✓	None
7	S_{n31}, S_{p12}	✗	✓	✓	✓	None
8	S_{n31}, S_{n21}	✗	✓	✓	✓	None
9	S_{n31}, S_{n22}	✗	✓	✓	✓	None
10	S_{n31}, S_{p13}	✗	✓	✓	✓	S_{n21} (1.25V)
11	S_{n31}, S_{n11}	✗	✓	✓	✓	None
12	S_{n31}, S_{n32}	✗	✗	✓	✓	None
13	S_{n31}, S_{p21}	✗	✓	✓	✗	None
14	S_{n31}, S_{p22}	✗	✓	✓	✓	S_{n32} (1.25V)
15	S_{n31}, S_{n33}	✗	✓	✓	✓	S_{p21} (1.25V)
16	S_{n31}, S_{p31}	✗	✓	✓	✗	None
17	S_{p12}, S_{n21}	✗	✓	✓	✓	S_{n31} (1.25V)
18	S_{p12}, S_{n22}	✓	✓	✓	✓	S_{n31} (1.25V)
19	S_{p12}, S_{p13}	✓	✓	✓	✓	S_{n31} (1.43V)
20	S_{p12}, S_{n11}	✗	✓	✓	✓	S_{n31} (1.25V)
21	S_{p12}, S_{p21}	✗	✓	✓	✓	None
22	S_{p12}, S_{p22}	✓	✓	✓	✓	S_{n31} (1.3V). S_{n32} (1.22V)
23	S_{p12}, S_{n33}	✓	✓	✓	✓	S_{n31}. S_{p21} (1.25V)
24	S_{p12}, S_{p31}	✗	✓	✓	✓	None
25	S_{n21}, S_{n22}	✗	✗	✓	✓	None
26	S_{n21}, S_{p13}	✗	✓	✓	✓	None
27	S_{n21}, S_{n11}	✗	✓	✓	✓	None
28	S_{n21}, S_{p22}	✗	✓	✓	✓	S_{n31}. S_{n32} (1.25V)
29	S_{n21}, S_{n33}	✗	✓	✓	✓	None
30	S_{n21}, S_{p31}	✗	✓	✓	✗	None
31	S_{n22}, S_{p13}	✓	✗	✓	✓	S_{n21}. S_{p11}. S_{p12} (1.25V)
32	S_{n22}, S_{n11}	✗	✓	✓	✓	None
33	S_{n22}, S_{n33}	✓	✓	✓	✓	S_{n33}. S_{p11}. S_{p12} (1.33V)
34	S_{n22}, S_{p31}	✓	✓	✓	✗	S_{p11}. S_{p12} (1.25V)
35	S_{p13}, S_{n11}	✗	✓	✓	✓	S_{n21} (1.25V)
36	S_{p13}, S_{p31}	✓	✓	✓	✗	S_{n21} (1.25V)
37	S_{n31}, S_{p11}	-	-	-	-	-
38	S_{p12}, S_{n32}	✓	✓	✓	✓	S_{n31}. S_{p11} (1.25V)
39	S_{n21}, S_{p21}	✗	✓	✓	✗	None
40	S_{n22}, S_{p22}	✓	✓	✓	✓	S_{n31}, S_{n32}, S_{p11}, S_{p12}
41	S_{p13}, S_{n33}	✓	✓	✓	✓	S_{n21}, S_{p21} (1.25V)
42	S_{n11}, S_{p31}	✗	✓	✓	✗	None

Table 4.4. Four-level leg operating features under one or two open-circuit faults.

4.4.1. Observations in a general *m*-level leg

Under open-circuit faults, it is also possible to define the lost levels as a function of the failed devices.

a) One-failed-device cases

i) If the failed device belongs to the open-circuit level-1 critical diagonal (S_{nk1}, for k = 1, 2, …, m–1), level 1 is lost. Fig. 4.12 presents these devices circled with a blue-solid-line.

ii) If the failed device belongs to the open-circuit level-*m* critical diagonal (S_{pk1} for k = 1, 2, …, m–1), level m is lost. Fig. 4.12 presents these devices circled with a red-dotted-line.

iii) If the failed device does not belong to any of the two open-circuit critical diagonals, no levels are lost.

b) *Two-failed-device cases*

i) If both failed devices belong to the open-circuit level-1 critical diagonal, level 1 is lost. Similarly, if both failed devices belong to the open-circuit level-*m* critical diagonal, level m is lost.

ii) If one of the two failed devices belongs to the open-circuit level-1 critical diagonal, and the other one belongs to the open-circuit level-*m* critical diagonal, both level 1 and level m are lost.

iii) If none of the failed devices belongs to any of the two open-circuit critical diagonals, no levels are lost, except in an "open-circuit inner special case," (special cases are explained below).

iv) If one of the two failed devices belongs to the open-circuit level-1 critical diagonal, and the other one does not belong to any of the two open-circuit critical diagonals, only level 1 is lost, except in an "open-circuit stair special case". The reasoning is analogous for level m.

The two-failed-device open-circuit special cases are the following:

- Open-circuit fatal (ocf) special case: It occurs when the two failed devices are $S_{n(m-1)1}$ and S_{p11}, which are the ones directly connected to the output terminal, see Fig. 4.13(a).
- Open-circuit inner (oci) special case: the m–2 oci special cases occur when the two failed devices are S_{nkk} and $S_{p(k-1)(m-k+1)}$ (for k = 2, 3, …, m–1). In this case, the inner level k is lost, as it can be seen in Fig. 4.13(b).
- Open-circuit stair (ocs) special case: the 2·(m–2) ocs special cases occur when the two failed devices are S_{nk1} and S_{nk2} (for k = 2, 3, …, m–1), or devices S_{pk1} and S_{pk2} (for k = 1, 2, …, m–2). In this special case, levels 1 and 2 are lost if S_{nk1} and S_{nk2} devices fail, see Fig. 4.13(c), and levels m and m–1 are lost if S_{pk1} and S_{pk2} devices fail, see Fig. 4.13(d).

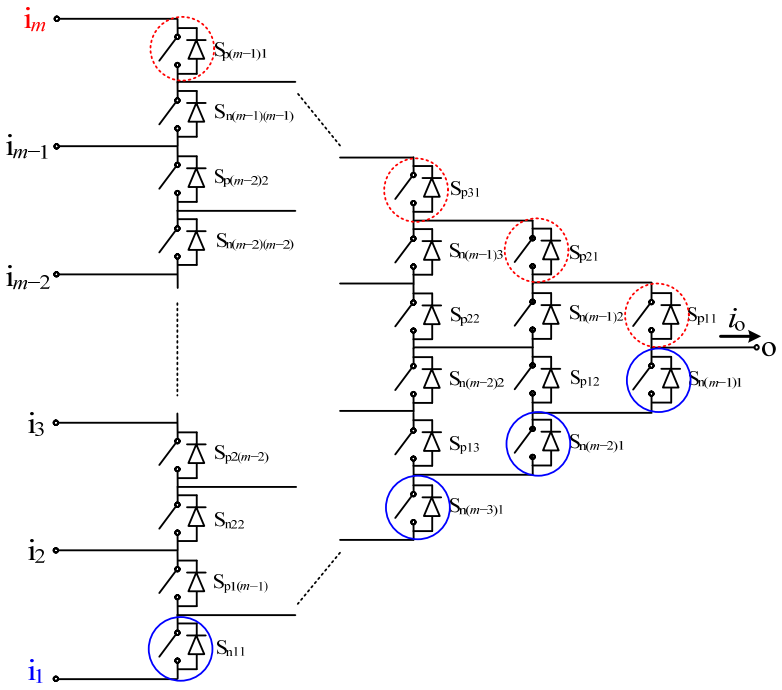


Fig. 4.12. Open-circuit critical diagonals in an m-level leg.

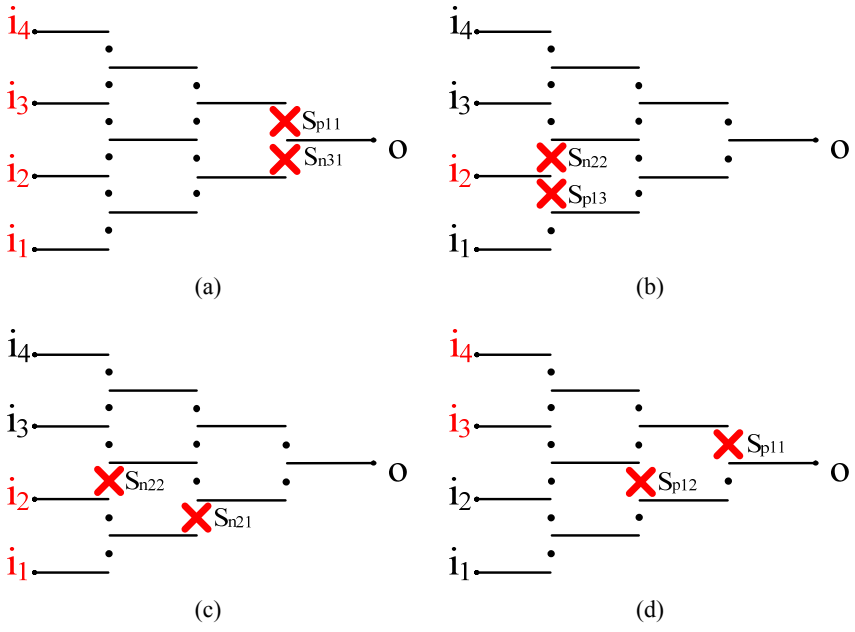


Fig. 4.13. Open-circuit special cases in a four-level leg. (a) The "ocf" special case. (b) The "oci" special case in which level 2 is lost. (c) An example of "ocs" special case in which levels 1 and 2 are lost. (d) An example of "ocs" special case in which levels 3 and 4 are lost.

As in short-circuit cases, a general *m*-level leg under an arbitrary single open-circuit fault only loses one level regardless of the number of levels (except in the ocf special case). Under an arbitrary case with two failed devices, the general *m*-level leg only losses a maximum of two levels.

4.5. Experimental results

The four-level MAC leg prototype with small dc-link capacitors shown in Fig. 2.8 has been used for the experimental tests. The leg prototype contains twelve MOSFETs (FDPF3860T - 100 V) and their corresponding gate-driver circuits. The generation of the switch control signals is implemented through MATLAB-Simulink using dSPACE processor board DS1106 and dSPACE digital waveform output board DS5101, see Appendix B.

Fig. 4.14 illustrates the circuit used for experimental tests. The applied modulation strategy consists of constant and equally-distributed duty ratios of connection of the converter output terminal to each one of the levels; i.e., each duty ratio equals 0.25, see Fig. 3.13(b).

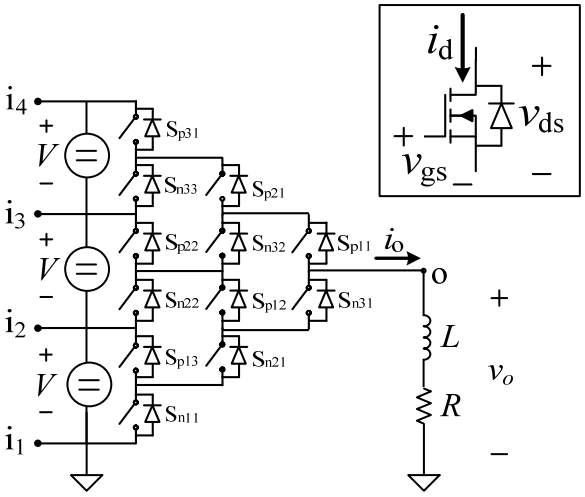
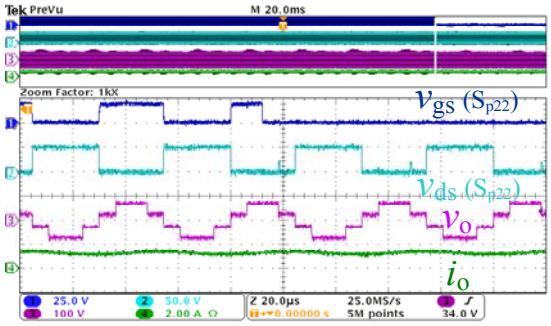


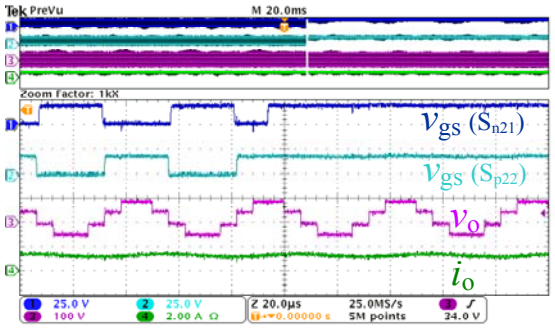
Fig. 4.14. Circuit used for experimental tests.

Fig. 4.15(a) presents relevant waveforms under a transition to an emulated open-circuit fault in device S_{p22}. Device S_{p22} is turned off all along to emulate an open-circuit fault. The original switching states are used all the time without losing any level, since this device does not belong to the open-circuit critical diagonals. Fig. 4.15(b) shows another example, in which devices S_{n21} and S_{p22} are turned on all along to emulate a short-circuit fault in these two devices. In this case, the original switching states are replaced by the new ones presented in Fig. 4.5 (SSI is used). As it can be seen in Fig. 4.15(b), the output terminal can continue being connected to any input terminal after the emulated short-circuit fault. Lastly, Fig. 4.15(c) shows another example in which it is emulated a short-circuit fault in device S_{p12}. In this case, level 1 is lost after the emulated fault since

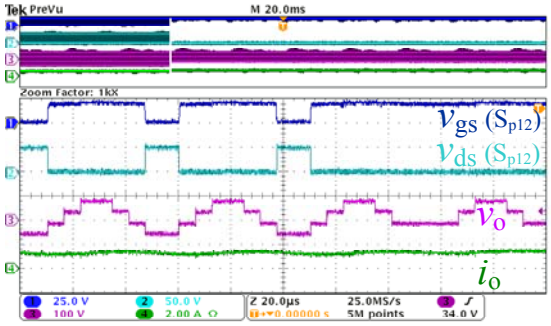
device S_{p12} belongs to the short-circuit level-1 critical diagonal. Consequently, the modulation strategy has to be readjusted to work with the three available levels. In this example, the duty ratio of connection to level 2 becomes 0.5. Original switching states are used for connecting the output terminal to levels 2, 3, and 4 after the emulated fault.



(a)



(b)



(c)

Fig. 4.15. Experimental results under the following conditions: V=50 V, L=5 mH, R=33 Ω, f_S=20 kHz. (a) Emulation of a open-circuit fault in device S_{p22}. (b) Emulation of a short-circuit fault in devices S_{n21} and S_{p22}. (c) Emulation of a short-circuit fault in device S_{p12}.

4.6. Hardware modifications to improve the fault-tolerance ability

4.6.1. Solution I: Parallelization of open-circuit critical diagonals

This proposal consists of the implementation of two devices connected in parallel instead of just one device in the open-circuit critical diagonals. Fig. 4.16 presents this modification in a five-level leg. With the proposed modification, if an open-circuit fault occurs in one of these devices, the corresponding level (level 1 or level *m*) would not be lost because the parallel device would provide a path for the output current to flow.

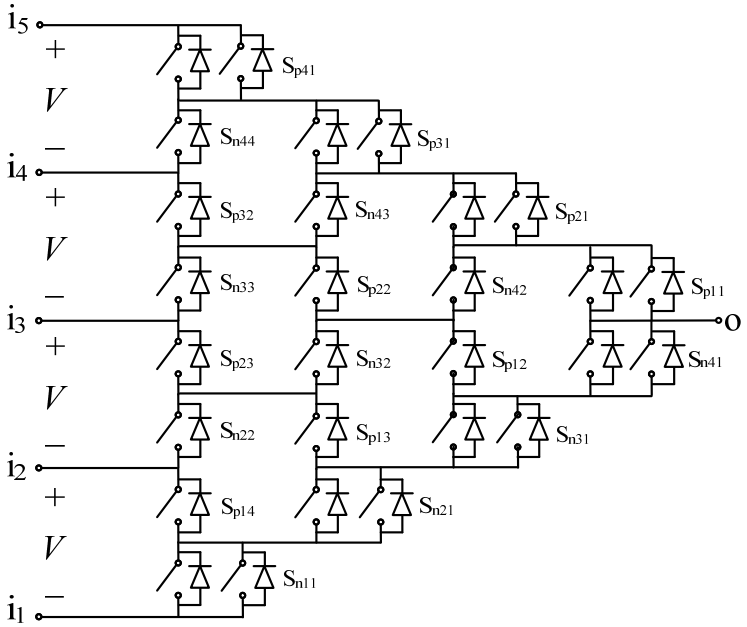


Fig. 4.16. Five-level hardware modified proposal (solution I).

Using one gate-driver circuit for each one of the parallel switches represents a good solution from the point of view of fault-tolerance, since it would permit to continue working with the parallel device in case that one of the two driver circuits fails. Using the same driver circuit for both parallel devices represents a simpler and economical solution.

It is interesting to note that the devices that belong to the open-circuit critical diagonals are the ones that concentrate the highest conduction losses since they conduct all the output current in connections to levels 1 and *m*. Consequently, by forcing the simultaneous conduction of the parallel devices, this hardware modification allows reducing the overall conduction losses and achieving a better distribution of losses among the devices.

4.6.2. Solution II: Inclusion of two additional devices at input terminals i_2 and i_{m-1}

This hardware modification is based on the same concept used in the topology proposed in [52]. Fig. 4.17 presents the particular five-level case of the modified topology. Two auxiliary devices are included at input terminals i_2 and i_{m-1}. These devices are permanently ON under normal operation and have no impact on the circuit fundamental behavior. However, they introduce additional conduction losses. In some short-circuit and open-circuit fault cases, they are switched off to disconnect the corresponding branches, as explained next in the proposed switching schemes.

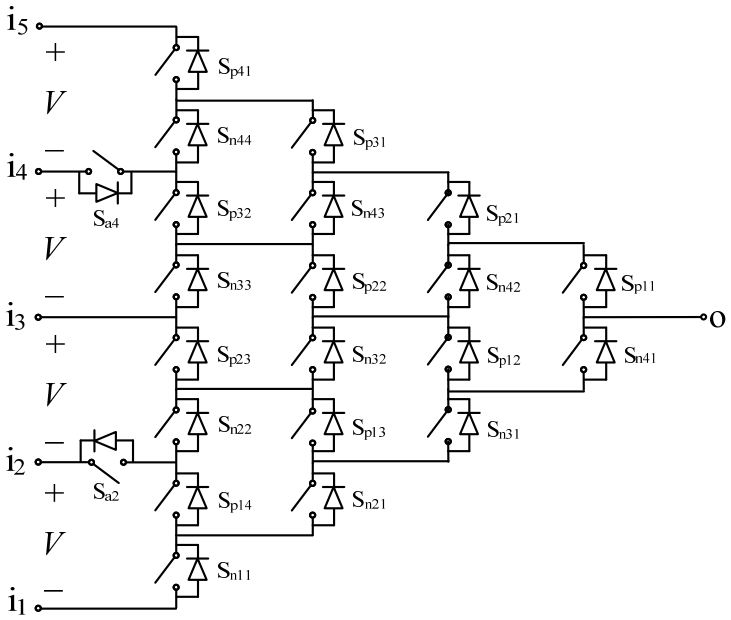


Fig. 4.17. Five-level hardware modified proposal (solution II).

4.6.2.1. Switching scheme under short-circuit faults

The inclusion of the additional devices permits the connection of the output to levels 1 and m when the failed device belongs to any of the two short-circuit critical diagonals. This is achieved by just turning off the corresponding auxiliary switch (S_{a2} for connecting the output to level 1, or $S_{a(m-1)}$ for level m), and then using the corresponding original switching state. Fig. 4.18(a) presents an example of a five-level leg in which S_{a2} is turned off to connect the output terminal to level 1 under a fault in the device S_{p13}.

Please note that the blocking voltage of some devices is unavoidably increased to $2V$. Specifically, devices S_{p2j}, for j = 1, 2, … , m–2, when the output is connected to level 1, and devices $S_{n(m-2)j}$, for j = 1, 2, …, m–2, when the output is connected to level m.

If the failed device does not belong to any of the short-circuit critical diagonals, switching schemes proposed in Section 4.3 can be used maintaining the auxiliary devices in ON state.

4.6.2.2. Switching scheme under open-circuit faults

As under short-circuit faults, the inclusion of the additional devices permits the connection of the output to levels 1 and *m* when the failed device belongs to any of the two open-circuit critical diagonals (except for devices S_{n11} or $S_{p(m-1)1}$).

In this occasion, however, it is necessary to properly modify the switching state, aside from turning off the corresponding auxiliary device. A simple solution is illustrated in the example of Fig. 4.18(b). The used switching state is the original one to connect the output to level *m*–1, but with the device $S_{p(m-1)1}$ in ON state. Besides, the auxiliary device $S_{a(m-1)}$ is turned off to avoid a short-circuit. If the failed device belongs to the level-1 open-circuit critical-diagonal, an analogous solution can be used; i.e., apply the switching state to connect the output to level 2, but with device S_{n11} in ON-state and the auxiliary device S_{a2} in OFF-state.

As under short-circuit faults, the blocking voltage of some devices is unavoidably increased to 2*V*. If the proposed switching states are used, the devices that increase their blocking voltage are the same as under short-circuit faults.

If the failed device does not belong to any of the open-circuit critical diagonals, the original switching states could be used, maintaining the auxiliary devices in ON state.

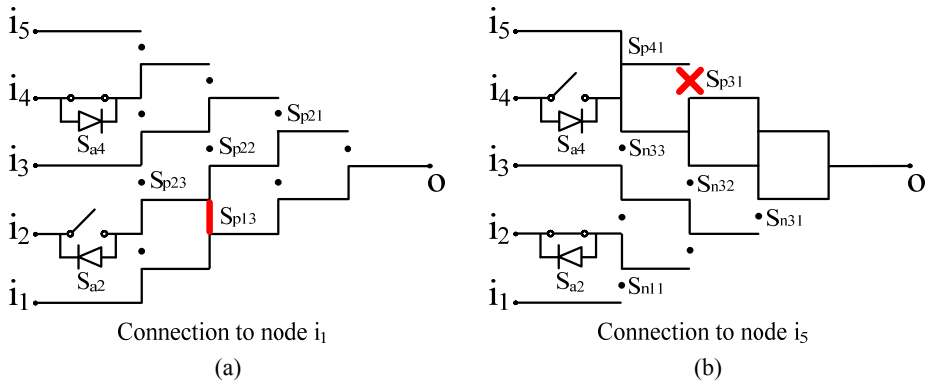


Fig. 4.18. Two examples of operation under faults in Solution II. (a) Short-circuit fault in device S_{p13}. (b) Open-circuit fault in device S_{p31}.

4.6.3. Solution III: Inclusion of one additional device at every input terminal

This hardware modification represents an extension of the previous solution. Fig. 4.19 shows the particular five-level case of the modified topology. A new switching device S_{abk} is included at each one of the converter input terminals. As in the previous case, these devices are permanently ON under normal operating conditions and are switched off in some fault cases to disconnect the corresponding branches.

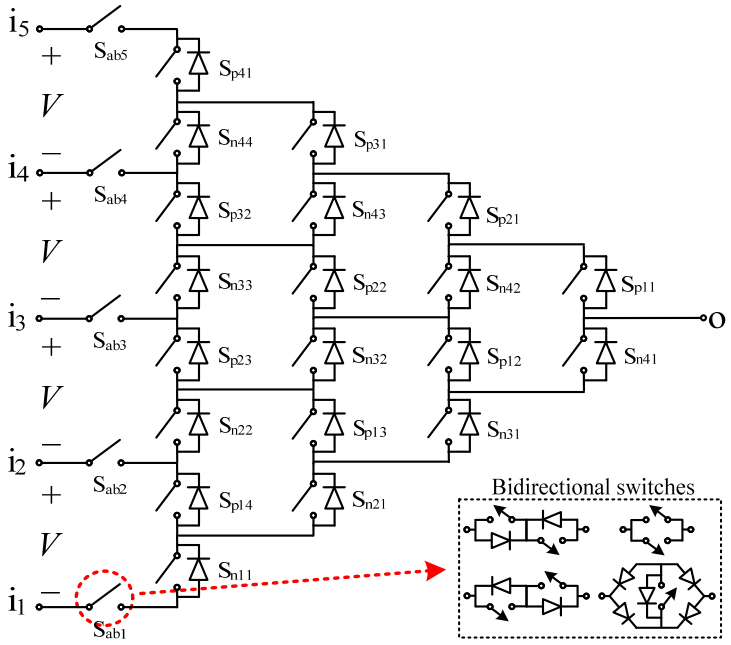


Fig. 4.19. Five-level hardware modified proposal (solution III).

The additional devices have to be bidirectional (capable of conducting currents and blocking voltages in both polarities). At the present time, bidirectional switches are usually realized from different configurations based on single unidirectional switches. Two switches connected in anti-series, two switches with reverse blocking capability connected in anti-parallel, or a diode bridge with a single switch are commonly used configurations, see the inset of Fig. 4.19. These arrangements are available in modular form in the power electronics market. Nevertheless, the research activity on the design and fabrication of monolithically integrated bidirectional switches is active and intense. Recently, these type of bidirectional switches have been fabricated [83], [84], and it is expected that new ones with better performance are going to be available in the market in the near future [85].

It is important to bear in mind that the additional devices would introduce new conduction losses in the converter. If bidirectional switches are built from the different configurations that appear in Fig. 4.19, the losses would be considerable. Nevertheless, in the near future, monolithically integrated bidirectional switches may present significant lower conduction losses.

4.6.3.1. Switching scheme under short-circuit faults

Thanks to the inclusion of the auxiliary devices and to the fact that they are bidirectional, original switching states can be used permanently to connect the output to all the available levels under any number of simultaneous short-circuit faults in the topology switches, assuming that all auxiliary devices are working well. It is only necessary to turn off the proper auxiliary switches to

disconnect the related branches. As an example, in the case of Fig. 4.20, under a fault in S_{n31}, the device S_{ab3} is turned off in the switching states for connecting the output terminal to levels 5 and 4.

In a general *m*-level leg, the proposed switching scheme can be defined as follows:

i) Original switching states are used under any single fault case.

ii) For every failed device S_{nkj}, it is necessary to turn off the auxiliary device S_{abk} in the switching states for the connection of the output terminal to levels k+1, k+2, …, m.

iii) For every failed device S_{pkj}, it is necessary to turn off the auxiliary device $S_{ab(k+1)}$ in the switching states for the connection of the output terminal to levels 1, 2, …, k.

Under any single-device fault, the blocking voltage of some topology devices is increased to $2V$, while the blocking voltage of the auxiliary device which is turned off is equal to V. Regarding two-simultaneous-device faults, the worst cases occur when auxiliary devices of two consecutive input terminals are required to switch off simultaneously. In these cases, the blocking voltage of some topology switches increases to $3V$, while the blocking voltages of the two OFF-state auxiliary devices are $2V$ and V.

4.6.3.2. Switching scheme under open-circuit faults

Regarding single open-circuit faults, this solution does not incorporate any additional advantage compared to solution II, and the switching strategy could be exactly the same (S_{ab2} is equivalent to S_{a2} and $S_{ab(m-1)}$ is equivalent to $S_{a(m-1)}$). Regarding cases with two or more simultaneous device-faults, this structure permits to operate with all levels in all cases, except when the failed devices eliminate any possible path for the output current to flow.

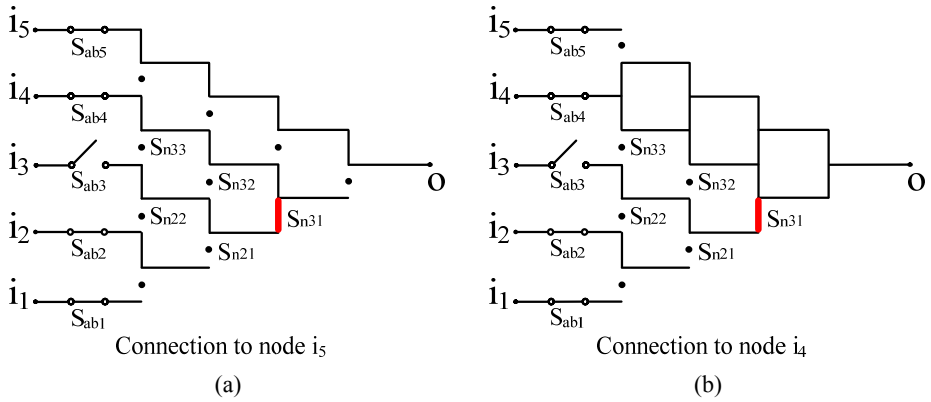


Fig. 4.20. An example of operation under a short-circuit fault in device S_{n31} in Solution III. (a) Connection to level 5. (b) Connection to level 4

4.7. Conclusion

The MAC topology presents the ability to continue operating after a fault condition, which cannot be achieved with conventional two-level converters. This fact makes the MAC topology especially interesting for applications where it is very important to avoid sudden system shut-downs. An *m*-level converter leg with *m*–1 dc-voltage sources is capable to continue operating after a single open- or short-circuit fault with at least *m*–1 levels. For two-simultaneous faults, the converter can continue operating in almost all cases with at least *m*–2 levels.

Open-circuit faults are less detrimental than short-circuit faults because original switching states can be used permanently, and the possibility that a short-circuit path is formed is completely avoided. In this sense, it would be good to somehow ensure that all faults are in open-circuit.

Three different hardware modifications have been proposed to increase the MAC fault-tolerance ability. Solution III appears to be very attractive from the point of view of fault tolerance, since the fault-tolerance capacity is significantly improved under open-circuit faults and especially under short-circuit faults, where the converter can continue operating using original switching states under any number of simultaneous faults. However, the increase of the overall losses in the converter produced by the added bidirectional switches may discard this solution in practice, at least with the current technology.

On the other hand, solution I appears to be very practical since the new additional devices allow reducing the overall conduction losses, and achieving a better distribution of losses among the devices, as well as improving the fault-tolerance capacity against open-circuit faults. Finally, solution II also represents an interesting solution since the fault tolerance against open- and short-circuit faults is significantly improved, while losses are not highly increased.

CHAPTER 5

CONCLUSION

Abstract — This chapter summarizes the thesis contributions and conclusions, and proposes the possible future research work.

5.1. Contributions and conclusions

The main contributions and conclusions can be summarized as follows:

- The thesis focuses on the study of the recently proposed multilevel-active clamped topology and its innovative operating principle. In this converter, switching states are defined so that all possible current paths connect the output terminal to the corresponding input terminal. In addition, blocking voltages are clamped to the desired level. The good performance of the novel topology and the operating principle have been verified through simulation and experiments on a first design and assembly of a four-level three-leg MAC converter prototype.
- An analysis of the MAC converter losses has been performed. Device conduction and switching losses have been carefully analyzed.
  - If devices are properly selected for a certain operating point, both conduction and switching losses should be lower in the MAC topology than in a two-level topology. Regarding conduction losses, the fact that $r_{\mathrm{ds(on)}}$ varies exponentially with the device blocking voltage, and the reduced equivalent ON resistance thanks to the parallel current paths, should result in a decrease of overall conduction losses. Regarding switching losses, they should be lower not only because low voltage-rated devices can be used with better relative performance features, but also because all switching transitions occur at lower blocking voltage levels, which in principle should produce lower switching losses. Compared to other multilevel converters using the same modulation pattern, conduction losses should be lower in the MAC topology thanks to the parallel current paths. With regard to switching losses, they should be similar to other multilevel topologies. Nevertheless, in the MAC topology there is a degree of freedom to distribute the switching losses among the devices.
  - Expressions to calculate conduction losses in the total leg and in each single device, operating under different scenarios, have been derived. The expressions to determine the conduction losses operating as a three-phase inverter under the V^2PWM are very

simple since they are independent from the load impedance angle. The distribution of current among the devices for each switching state has been defined up to the seven-level MAC leg.

- Switching losses have been studied through the analysis of the transitions between adjacent switching states, including the effect of the diode reverse-recovery processes. The particular case of a four-level leg has been analyzed in detail. The extrapolation into a higher number of levels can be directly deduced. An important advantage of the MAC topology is that transitions between switching states can be performed selecting the device that concentrates the switching losses.
- The efficiency of the four-level MAC converter has been compared to a conventional two-level converter under a particular selection of MOSFETs. The efficiency of the MAC converter is higher in all the frequency-range. The close agreement between analytical and experimental results supports the comparison conclusions and validates the analytical loss models. A study to determine the minimum chip area needed for both topologies under specific conditions has concluded that the minimum total area is lower in the MAC topology for switching frequencies above 20-30 kHz despite presenting twelve devices instead of two. It is important to note that all these comparisons have been carried out using a particular selection of MOSFETs. The results could vary if other devices had been selected.

- An analysis of the fault-tolerance capacity of the MAC converter has been performed. The MAC topology can continue operating after a fault condition, which is not possible in conventional two-level converters. This is an important advantage of the MAC topology, especially for those applications in which sudden system shut-downs lead to catastrophic consequences. Open-circuit faults are less detrimental than short-circuit faults. In this sense, it would be useful to somehow ensure that all faults be in open circuit. New switching strategies and different topology modifications have been proposed to overcome the limitations caused by faults, and therefore, increase the fault-tolerance ability. The hardware modification consisting in parallelizing the outer-diagonal devices appears to be very practical since the new additional switches allow reducing the overall conduction losses, achieving a better distribution of losses among the devices, as well as improving the fault-tolerance capacity against open-circuit faults.
- Several basic design guidelines for the MAC converter have also been presented. A network of self-powered gate-driver power-supply circuits is proposed to avoid the need of using isolated external gate-driver circuit power-supplies. Furthermore, it is recommended

to use switches with low output parasitic capacitance and low reverse-recovery current diodes to minimize the device current spikes, and consequently the switching losses.

- If a particular device (e.g., MOSFET) at specific voltage and current ratings is available with good performance, low cost, and ideally integrated auxiliary circuitry (gate driver, gate driver power supply, ...); then, this topology and control could be applied to implement a universal and easily scalable converter to be used in a number of applications.
- It is the understanding of the author that the proposed topology can be competitive in applications requiring devices with voltage ratings lower than 600 V. This is basically due to two reasons. First, there is a major feasibility of integrating the self-powered gate-driver power-supply circuits. And secondly, MOSFETs appear to be more suitable than IGBTs for the MAC topology since they present better performance conducting in parallel. Medium and low power/voltage motor drives, wind power systems, or photovoltaic systems could be interesting applications for the MAC topology, where the advantage of using multilevel diode-clamped converters has already been proven.
- The main disadvantage of the MAC converter compared to other commercial converters is its large number of power devices with their corresponding gate-drive circuits.

These research contributions have already led to the publication of two journal papers [87] and [88] and four conference papers [89]-[92]. Besides, another paper proposal covering the contributions in Chapter 3 is currently being prepared for publication in the *IEEE Transactions on Industrial Electronics*.

5.2. Future research work

Among the many possible future extensions of the research reported here, we would like to highlight the following:

- Extend the efficiency analysis. i) Perform the experimental comparison between the efficiency of the MAC topology and a two-level converter operating as three-phase inverters. ii) Perform the comparison under different sets of power devices and operating conditions. iii) Compare the efficiency of MAC topology with other multilevel topologies.
- Further investigate the switching strategies (selection of the suitable device to concentrate the switching losses in each switching transition) to optimize the distribution of losses among all the semiconductors.

- Analyze the fault-tolerance capacity with a single dc-voltage source and capacitors connected across every two adjacent input terminals, instead of multiple dc-voltage sources.
- Design a fault-tolerant MAC converter including the system to detect the faults and implementing the control scheme capable of instantaneously changing the switching strategy in case of a fault. The fault-detection system could be implemented in the gate-driver circuit and the control scheme could be implemented in a FPGA.
- Explore and quantify the advantages/disadvantages in converter cost, reliability, and performance that we can obtain using the hardware variation consisting in parallelizing the outer-diagonal devices.

APPENDIX A

DESIGN ISSUES OF THE MULTILEVEL ACTIVE-CLAMPED TOPOLOGY

Abstract —This appendix studies design issues of the MAC topology. Several guidelines are proposed to guarantee a proper MAC converter design and improve its performance. The inclusion of a resistor network to balance the blocking voltage of devices when the converter is in OFF state, the use of self-powered gate-driver power-supplies, or the definition of a shut-down sequence to avoid possible device failures are some of the proposals. This appendix also studies the singular device current spikes that appear in the MAC topology during switching state transitions. These spikes occur owing to diode reverse recovery and to the discharging of the device output parasitic capacitances. A proper device selection reduces these current peaks, decreasing the switching losses and the converter electromagnetic interference. Experimental tests are carried out with a four-level MAC prototype to validate the analysis.

A.1. OFF-state balancing resistor network

When the converter is in OFF state (all devices OFF) and assuming the same equivalent resistance per device, the blocking voltage of devices is unbalanced. S_{n11} and $S_{p(m-1)1}$ are the devices that withstand the largest blocking voltage, which for example is equal to $2.11 \cdot V/2$ for $m = 6$ and equal to $2.34 \cdot V/2$ for $m = 7$. The relative blocking voltage of these two devices increases with the number of levels. Consequently, if the number of levels is high, the use of an auxiliary circuit to balance the device blocking voltages could be necessary.

This balancing circuit can consist of simply including additional high-value resistors connected across each device, as shown in Fig. A.1. The value of these resistors should be selected so that the equivalent resistance (R_{eq}) of the parallel connection of the switch, the resistor, and any other additional circuitry, presents the relative values shown in Fig. A.1. If these resistors are embedded in the converter hardware, the system becomes completely balanced and the blocking voltage of all devices (when the converter is in OFF state) is equal to $V/2 = V_{dc\text{-}link}/(2 \cdot (m-1))$. The value of the resistors should be high enough so that they introduce negligible losses.

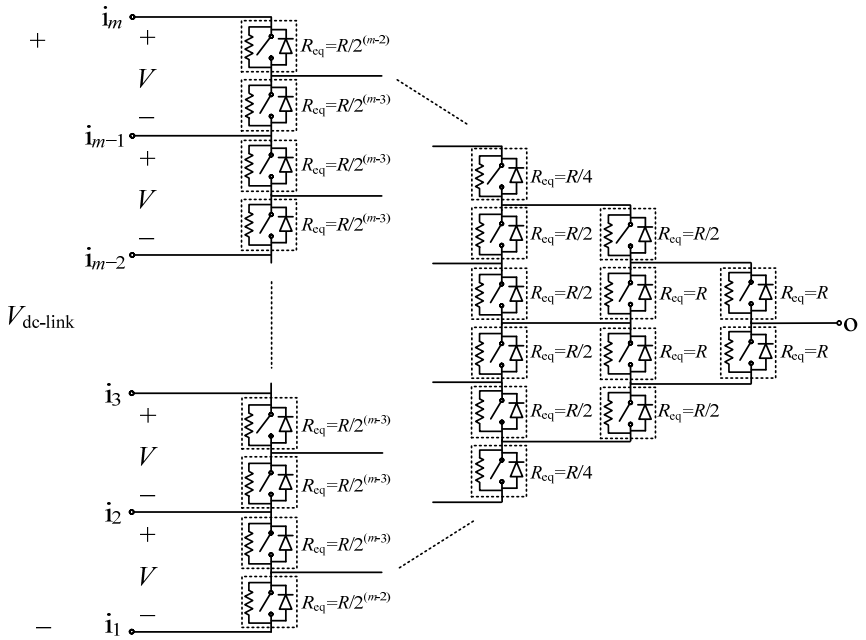


Fig. A.1. OFF-state balancing resistor network.

A.2. Shut-down sequence

In a MAC converter, a non-safe situation could take place during the converter shut-down due to different delays among the turn off of the devices. Consider for example a four-level leg with the state shown in Fig. A.2(a) at the instant previous to shut-down. If the turn-off command is sent to all the switches at the same time, devices S_{p11} and S_{p12} could be the first turning off due to asymmetries. If this situation happens under an inductive load, the output current would flow through the device S_{p13} and through the antiparallel diodes of devices S_{n21} and S_{n31}, as it is shown in Fig. A.2(b). Then, S_{p11} would have to withstand a voltage equal to $2V$. This is a particular case, but other undesirable situations could occur if the shut-down sequence is not properly managed. In the worst case, one single device would have to withstand the full dc-link voltage. For instance, in the state of Fig. A.2(a), if S_{p11}, S_{p12}, and S_{p13} are the first turning off, then device S_{p11} would have to block the entire dc-bus.

To ensure a safe shut-down of the MAC converter in any condition, there are different options. One effective and simple choice consists on the following shut-down sequence, with reference to Fig. 2.1: First, a command is sent to turn off all devices of the (2*m*–2)-switch pole. After a proper blanking time, a command is sent to turn off all devices of the next (2*m*–4)-switch pole. After a proper blanking time, a command is sent to turn off all devices of the next (2*m*–6)-switch pole. This process is repeated until the devices of the last 2-switch pole are turned off. The opposite sequence can be applied to ensure a safe turn on of the MAC converter.

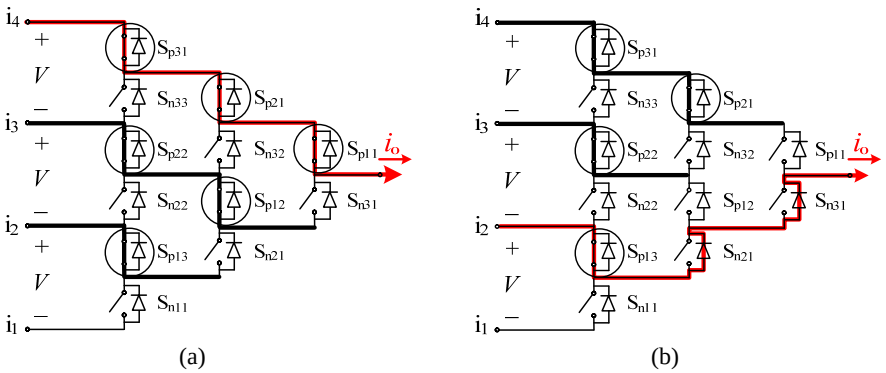


Fig. A.2. Possible failure mechanism in a shut-down process. (a) State of the leg at the instant previous to shut-down. (b) Resulting transient state if devices S_{p11} and S_{p12} are the first in turning off.

A.3. Self-powered gate-driver power-supply network

The MAC topology presents a high number of devices and their corresponding gate drivers. A simple solution to simplify the implementation of the converter hardware consists in using simple self-powered gate-driver power-supplies (GDPS) circuits connected across the devices, which avoids the need of using multiple external isolated gate-driver power-supplies.

One possibility to implement such circuit is the topology presented in Fig. A.3, originally proposed in [86] and applied to a diode-clamped topology in [61]. In this circuit, the energy to drive the device is obtained from the energy that is otherwise lost during the main switch S_{xkj} turn-off transition and, eventually, from the corresponding dc-link capacitor or dc-power supply connected across the switch during its OFF state. This energy is stored in the GDPS capacitor C_{xkj}. The current charging GDPS capacitor C_{xkj} flows through the auxiliary MOSFET S_{axkj}. The zener diode D_{zxkj}, polarized by resistor R_{axkj}, limits the value of v_{cxkj}, and the blocking diode D_{bxkj} prevents the discharging of C_{xkj} when the main power device S_{xkj} is in ON state.

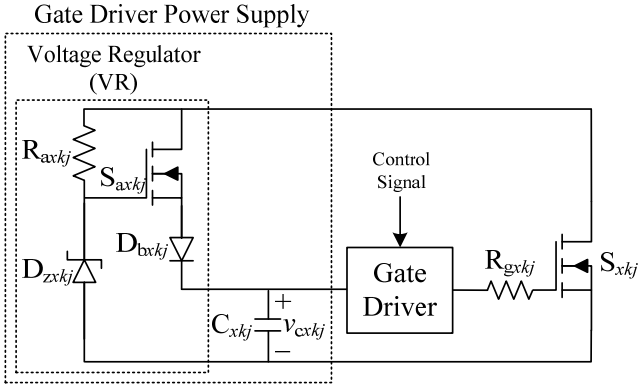


Fig. A.3. Proposed GDPS circuit ($x \in \{n, p\}$, $k \in \{1, 2, .., m–1\}$, and $j \in \{1, 2, .., m–1\}$).

A.3.1. Self-powered gate-driver power-supply network under the V²PWM

To operate the converter as a three-phase inverter, the modulation scheme V²PWM presented in Section 3.3 can be selected. Fig. A.4(a) presents the corresponding leg duty-ratio patterns.

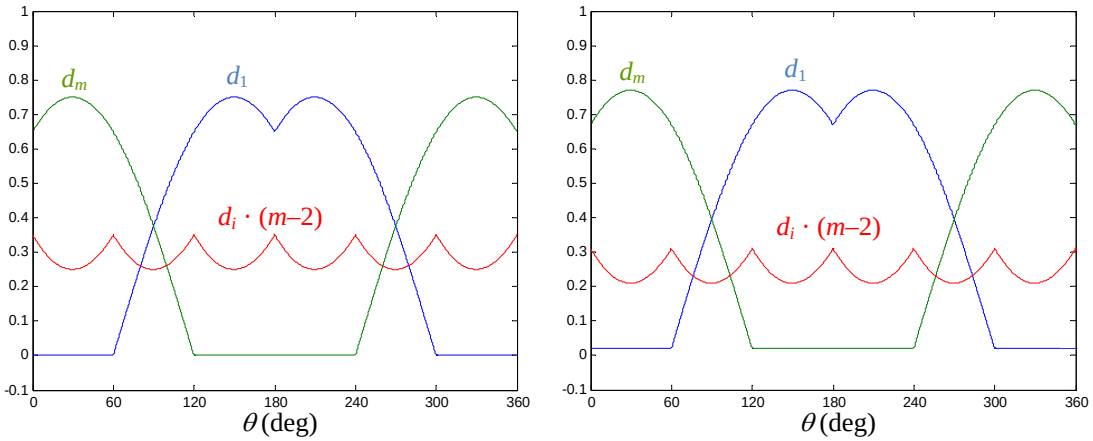


Fig. A.4. Leg duty-ratio pattern for a five-level three-leg converter (mi = 0.75). (a) Original PWM scheme. (b) Modified PWM scheme with d_{offset} = 0.02.

Under this modulation scheme, diagonal devices $S_{n(m-1)j}$ (j = 1, 2, …, m–1) and diagonal devices S_{p1j} remain in ON state during 120º intervals every line cycle, which prevents their corresponding GDPS capacitors C_{xkj} from being charged during this period. For example, in a five-level leg, devices S_{n41}, S_{n42}, S_{n43}, and S_{n44} remain conducting while d_5 equals 0 (from θ=120º to θ=240º in Fig. A.4(a)). These are the dotted-line circled devices in Fig. A.5. Similarly, devices S_{p11}, S_{p12}, S_{p13}, and S_{p14} remain conducting while d_1 equals 0 (from θ=0º to θ=60º, and from θ=300º to θ=360º). These are the solid-line circled devices in Fig. A.5.

In order to prevent the discharging of these GDPS capacitors below the minimum voltage value for correct operation of the gate driver, three possible solutions are proposed:

i) *The use of higher capacitance C_{xkj}*: A simple possibility to solve the problem is to use a large enough capacitance value C_{xkj}, so that this capacitor stores enough energy to supply the gate driver during the 120º in which the device is in ON-state. The required value of C_{xkj} will depend upon the ac-side line-cycle frequency. The lower the frequency is, the higher the required capacitance value will be. If the line-cycle frequency is considerably lower than the switching or carrier frequency, the size of GDPS capacitors would have to be significantly higher than the required size for GDPS capacitors that does not present the discharging problem. This fact

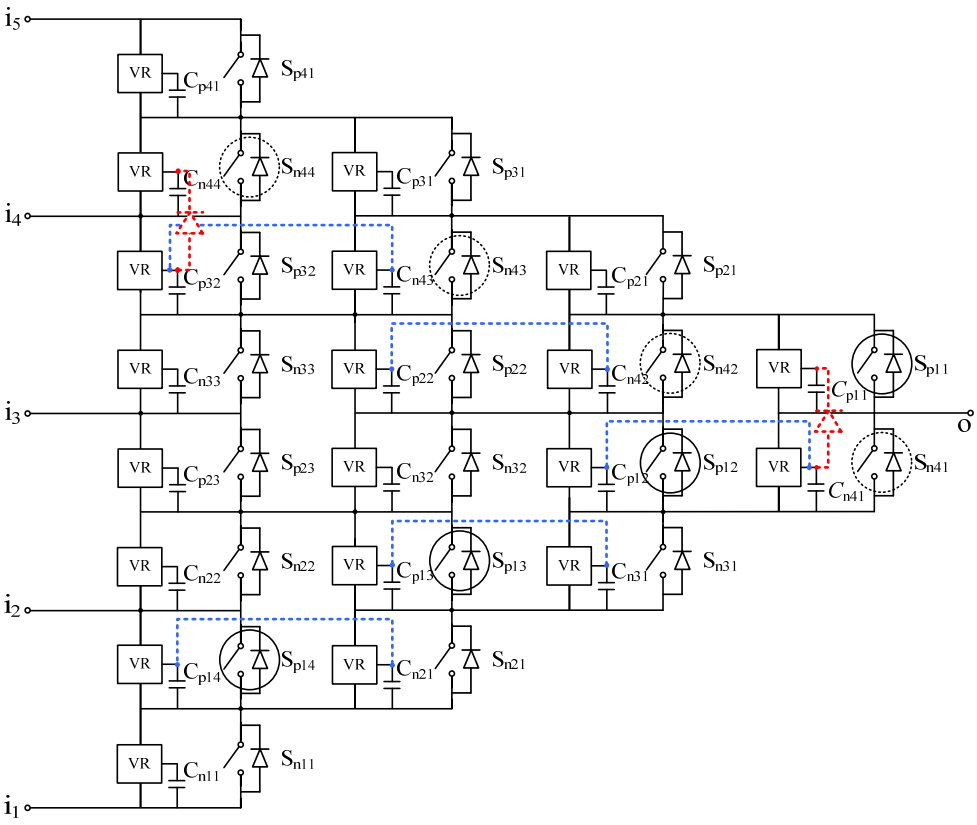


Fig. A.5. Addition of extra circuitry to deal with the discharge of GDPS capacitors C_{xkj}.

represents an important inconvenient of this solution. Furthermore, the recharging efficiency worsens as the capacitances are larger.

ii) *Modifying the converter control:* Another possibility proposed in [61] to overcome the problem without the need of increasing the size of the GDPS capacitors consists in modifying the original PWM strategy adding a small offset d_{offset} in the duty ratios d_1 and d_5. Since all duty ratios are higher than zero, all devices in the converter leg turn on and off in every switching cycle, causing a recharge of all GDPS capacitors in every switching cycle. Fig. A.4(b) presents the modified duty ratio patterns. This solution, however, produces an increase of the switching losses and also a slight increase of the ac-side voltage harmonic distortion.

iii) *Adding extra circuitry:* A third option is to add additional circuitry to the topology in order to feed those GDPS capacitors which experience the discharging problem from other GDPS capacitors. This can be done through the introduction of bootstrap diodes or through the parallel connection of GDPS capacitors with the same reference terminal. Fig. A.5 proposes the simplest configuration to solve the problem in a five-level leg. Connections between capacitors with the same reference terminal

are used whenever possible (represented with blue dotted lines in Fig. A.5) and bootstrap diodes are used in the remaining cases (represented with red dotted lines in Fig. A.5).

A.4. Singular current spikes during switching-state transitions

During transitions between switching states, some singular current spikes appear in some power devices of the topology. These current spikes can be produced owing to two different reasons: the reverse-recovery of diodes and the discharge of the device output parasitic capacitance.

A.4.1. Current spikes owing to diode reverse-recovery

This phenomenon has already been introduced in section 3.3.2. In switching state transitions where one or more diodes go through a hard-switching reverse-recovery process, a current spike flows through the reverse-recovered diode and other devices. In particular, this current spike flows through the first device being turned on during the switching transition, producing extra switching losses.

Fig. A.6 presents the switching state transition from connection to node i_2 to connection to node i_1 with negative output current i_o in a four-level MAC leg to illustrate the phenomenon. Fig. A.6(a) shows the switching state in which the output terminal is connected to the node i_2. In the first step of the transition, devices S_{p11}, S_{p12}, and S_{p13} are turned off. Since the output current flows through the diodes of these three devices, the output terminal continues connected to the node i_2, as it is depicted in Fig. A.6(b). Then, after the dead time, device S_{n11} is turned on and the current starts flowing through this device connecting the output terminal to node i_1 (see Fig. A.6(c)). At this point of the transition, the diodes of devices S_{p11}, S_{p12}, and S_{p13} suffer a reverse-recovery process, and the reverse-recovery currents flow through S_{n11} at turn on, increasing the switching losses. Finally, after a short transient, the steady-state connection of the output terminal to the node i_1 is reached, as shown in Fig. A.6(d).

Table A.1 presents the transitions of a four-level leg in which a reverse-recovery process of one or more diodes occurs. Table A.1 indicates the diodes presenting reverse recovery and the switch that concentrates the associated switching losses, with an indication of the total reverse-recovery current. In Table A.1, it has been assumed that the 6-switch pole devices are selected to concentrate the switching losses (the symbol $^{(*)}$ indicates those cases in which it could be possible to choose another device to concentrate the switching losses).

Using low reverse-recovery current diodes (e.g.; Schottky) will reduce these current peaks.

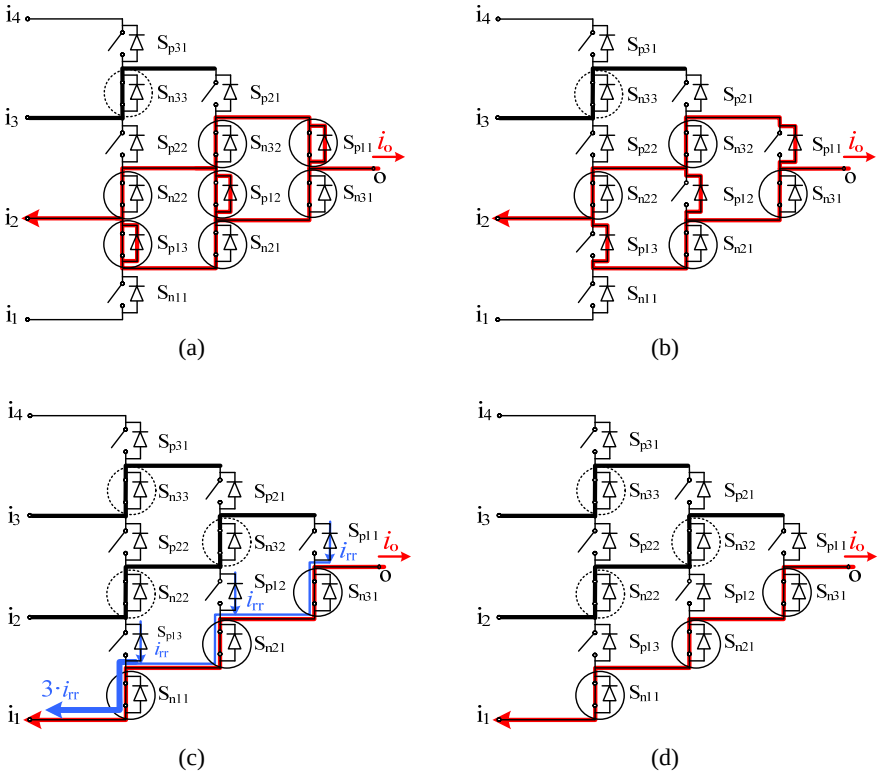


Fig. A.6. Transition between switching state of connection to node i_2 to switching state of connection to node i_1 with negative output current i_o. (a) Connection to node i_2. (b) First transient state of the transition. (c) Second transient state of the transition. (d) Connection to node i_1.

Switching state transition (current polarity)	Devices whose diodes present reverse recovery	Devices that concentrate the associated switching losses (Total reverse-recovery current)
1 → 2 (i_o>0)	S_{n11}	S_{p13} (i_{rr}) (*)
2 → 3 (i_o>0)	S_{n21}, S_{n22}	S_{p22} ($2\cdot i_{rr}$) (*)
3 → 4 (i_o>0)	S_{n31}, S_{n32}, S_{n33}	S_{p31} ($3\cdot i_{rr}$)
4 → 3 (i_o<0)	S_{p31}	S_{n33} (i_{rr}) (*)
3 → 2 (i_o<0)	S_{p21}, S_{p22}	S_{n22} ($2\cdot i_{rr}$) (*)
2 → 1 (i_o<0)	S_{p11}, S_{p12}, S_{p13}	S_{n11} ($3\cdot i_{rr}$)

Table A.1. Switching state transitions that produce reverse-recovery current-spike in a four-level leg.

A.4.2. Current spikes owing to the discharging of the device output parasitic capacitance C_{oss}

In some transitions between switching states, current spikes (i_{dis}) will flow through several devices owing to the discharging of the device output parasitic capacitance C_{oss}.

Fig. A.7 shows the switching state transition from connection to node i_3 to connection to node i_2 with negative output current i_o in a four-level MAC leg to illustrate the phenomenon. Fig. A.7(a) shows the switching state in which the output terminal is connected to node i_3. In the first

step of the transition, devices S_{p22} and S_{p21} are turned off. Since the output current flows through the diodes of these two devices, the output terminal continues connected to node i_3, as it is depicted in Fig. A.7(b). Then, after the dead time, device S_{n22} is turned on (device S_{n22} have been selected to concentrate the switching losses of this transition, and therefore it is turned on a short instant before S_{n21}) and the output current starts flowing through this device connecting the output terminal to node i_2 (see Fig. A.7(c)). At this point of the transition, the blocking voltage of device S_{n21} reduces to 0V through the discharging of its output parasitic capacitance (C_{oss}). The parasitic-capacitance discharging current starts flowing once the device S_{n22} is completely ON, hence the switching losses are not increased. The energy stored in the parasitic capacitance is first transferred to the S_{p12}-S_{n22}-S_{p13}-S_{n21} loop inductance and then dissipated through the devices' ON resistances. Finally, after the short transient, device S_{n21} is turned on and a new path for the output current is available, as it can be seen in Fig. A.7(d).

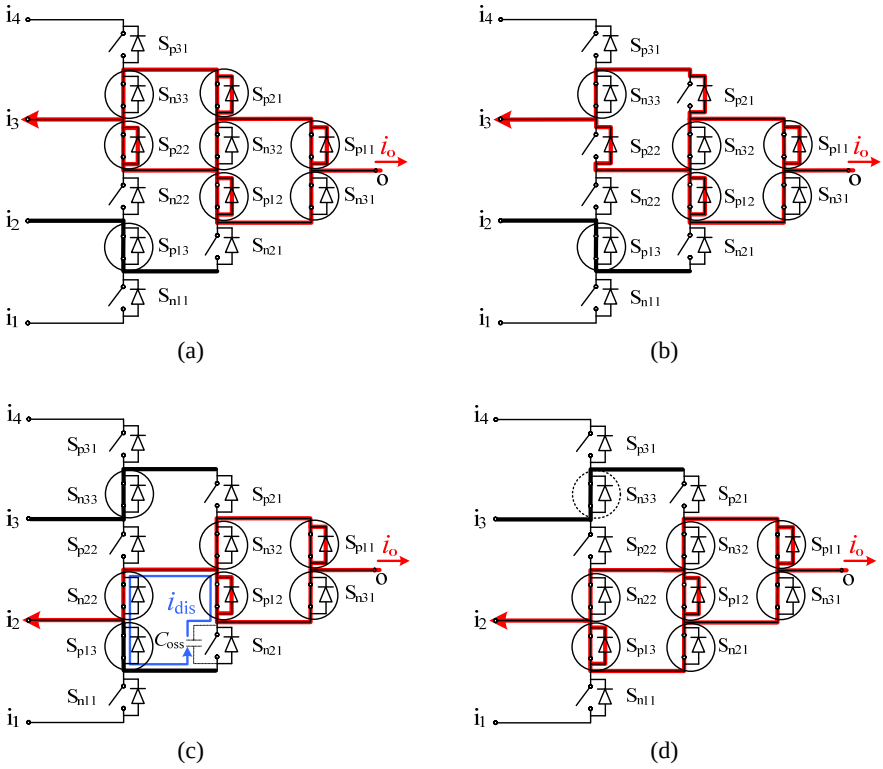


Fig. A.7. Transition between switching state of connection to node i_3 to switching state of connection to node i_2 with negative output current i_o. (a) Connection to node i_3. (b) First transient state of the transition. (c) Second transient state of the transition. (d) Connection to node i_2.

Table A.2 presents all the switching transitions of a four-level leg in which a current spike due to the discharging of a parasitic capacitance C_{oss} occurs. In Table A.2, it is also assumed that the 6-switch pole devices concentrate the switching losses.

The current peak depends on the parasitic capacitance value and the loop impedance (resistance and inductance). Choosing devices with a small parasitic capacitance will reduce the magnitude of these spikes.

Switching state transition (current polarity)	Devices whose parasitic capacitance is discharged
$i_1 \rightarrow i_2$ (i_o>0)	S_{p11}, S_{p12}
$i_2 \rightarrow i_3$ (i_o>0)	S_{p22}
$i_4 \rightarrow i_3$ (i_o<0)	S_{n31}, S_{n32}
$i_3 \rightarrow i_2$ (i_o<0)	S_{n21}

Table A.2. Switching state transitions that produce capacitor-discharging current-spike in a four-level leg.

A.4.3. Experimental tests

A four-level MAC prototype with small dc-link capacitors has been used for the experimental tests. Fig. A.8 illustrates the experimental setup. The applied modulation strategy is the one proposed in [57] (PWM scheme 2), which allows maintaining the dc-link capacitor voltages balanced. Fig. A.9 and Fig. A.10 present relevant experimental waveforms using two different MOSFET devices for comparison. It can be seen that the negative current peak owing to the discharging of the S_{n21} parasitic capacitance is significantly reduced when a MOSFET with a low parasitic capacitance is used (see Fig. A.9(b) and Fig. A.10(b)). Similarly, the current peak in device S_{n11} owing to diode reverse recovery is smaller when devices with a lower reverse-recovery charge Q_{rr} are used. Furthermore, it can be seen that the switching losses of device S_{n11} are also reduced significantly.

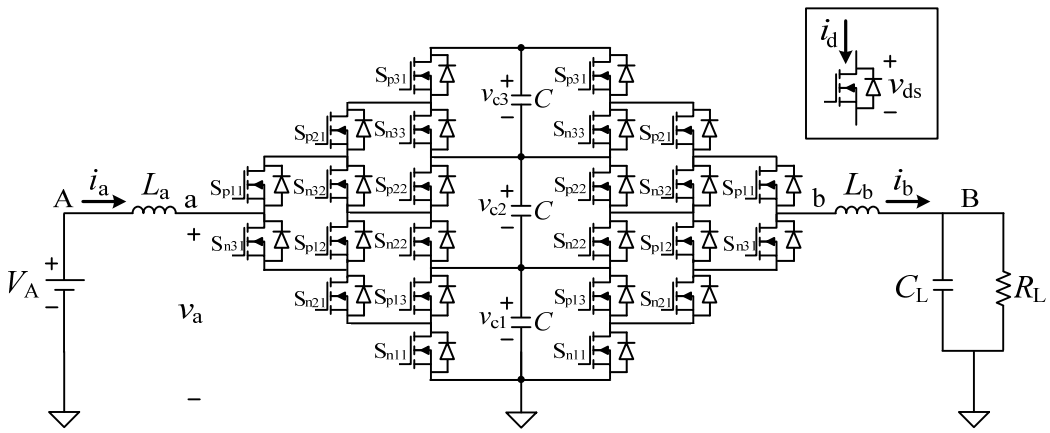


Fig. A.8. Four-level boost-buck dc-dc converter implemented with MOSFETs.

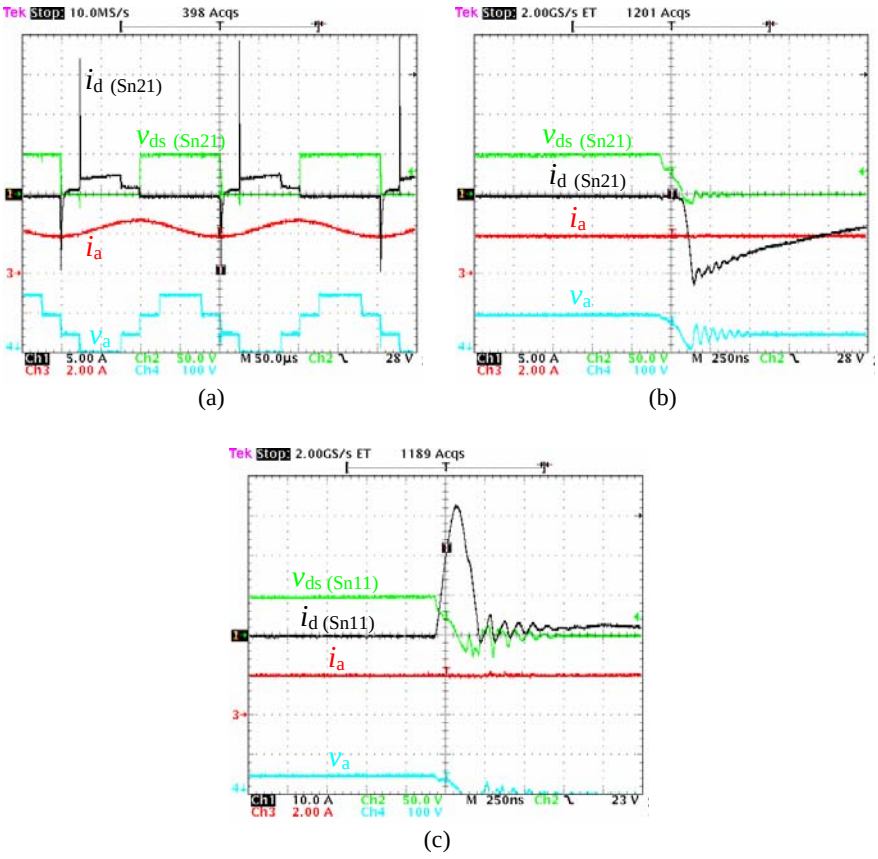
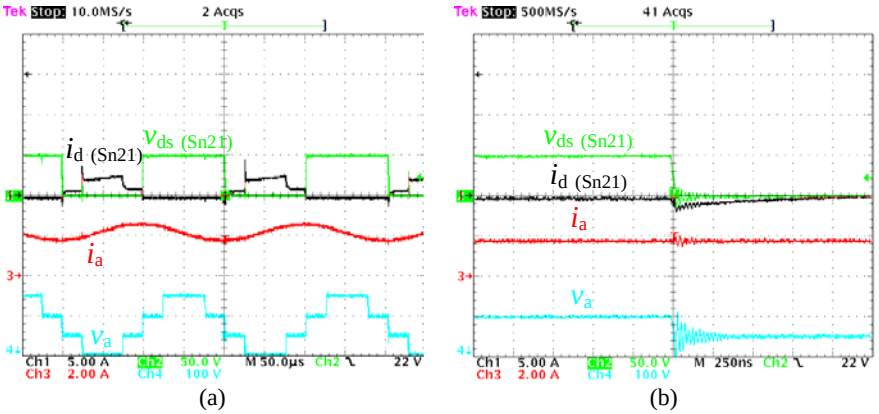
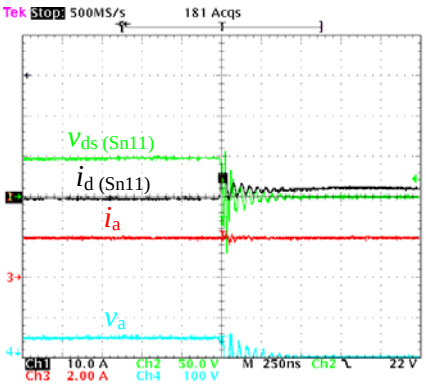


Fig. A.9. Experimental results using MOSFETs IRF3415 (Q_{rr} = 2.2 μC, C_{oss} = 640 pF) in the following conditions: V_A = 75 V, C = 100 μF, L_a = L_b = 5 mH, R_L = 33 Ω, C_L = 470 μF, f_s = 5 kHz, R_g = 20 Ω, t_d = 500 ns. (a) Two-and-a-half-switching-cycle view. (b) Zoom view of the current spike in device S_{n21} due to the discharge of its capacitance C_{oss}. (c) Zoom view of the current spike in device S_{n11} due to the reverse recovery of antiparallel diodes of devices S_{p11}, S_{p12}, and S_{p13}.





(c)

Fig. A.10. Experimental results using MOSFETs FDPF3860T (Q_{rr} = 56 nC, C_{oss} = 145 pF) in the same conditions of Fig. A.9. (a) Two-and-a-half-switching-cycle view. (b) Zoom view of the current spike in device S_{n21} due to the discharge of its capacitance C_{oss}. (c) Zoom view of the current spike in device S_{n11} due to the reverse recovery of antiparallel diodes of devices S_{p11}, S_{p12}, and S_{p13}.

A.5. Conclusion

In this appendix, several design issues of the multilevel active-clamped topology have been discussed. The study identifies the convenience of including a resistance network to balance the blocking voltage of all devices when the converter is in OFF state. A proper and simple shut-down sequence is proposed to avoid device failures due to an excessive blocking voltage. A network of self-powered gate-driver power-supply circuits, with convenient interconnections among them, is also proposed to simplify the integration of those circuits in the topology. Finally, the singular current spikes that occur in switching-state transitions have been analyzed. To minimize these current spikes, it is recommended to use devices with low output parasitic capacitance and low reverse-recovery current diodes.

APPENDIX B

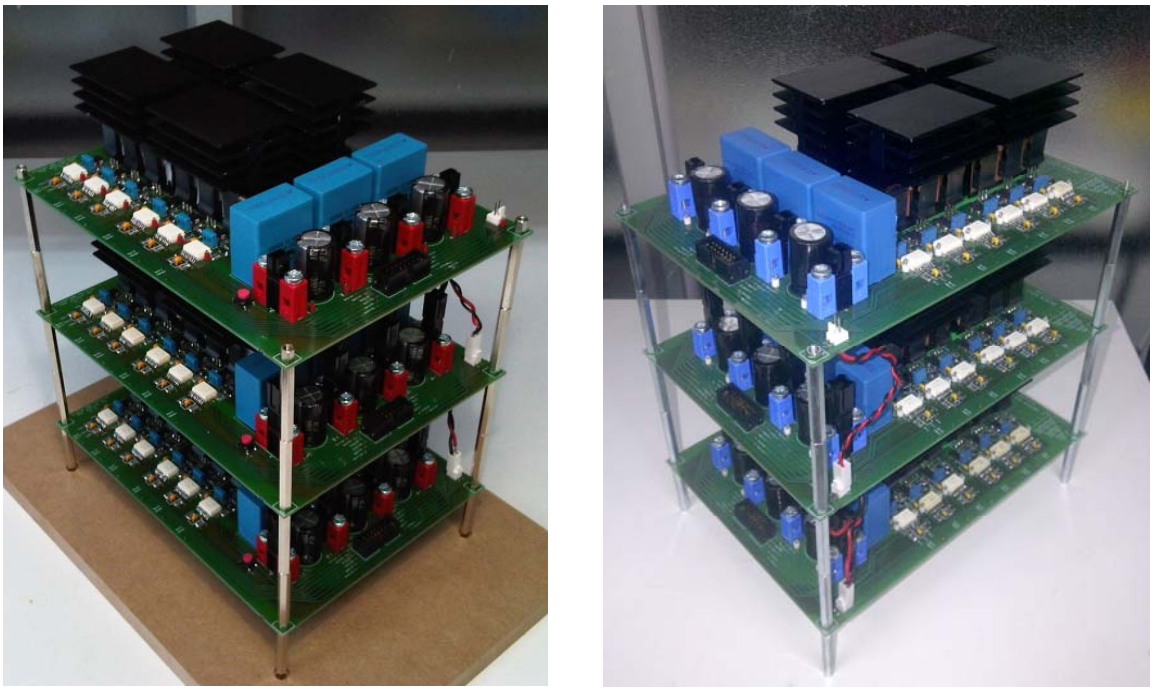
EXPERIMENTAL EQUIPMENT

Abstract —This appendix contains a description of the experimental equipment employed.

B.1. Converter prototypes

B.1.1. Four-level MAC prototypes

Fig. B.1 presents the two MAC converter prototypes assembled for performing the different experimental tests.



(a) (b)

Fig. B.1. Four-level three-leg MAC prototypes. (a) MAC prototype 1. (b) MAC prototype 2.

B.1.2. Two-level prototype

Fig. B.2 shows the two-level prototype built to carry out the efficiency comparison in Section 3.4. As it can be seen in Fig. B.2, the same printed circuit board (PCB) used for the MAC prototypes have been used for the two-level converter.

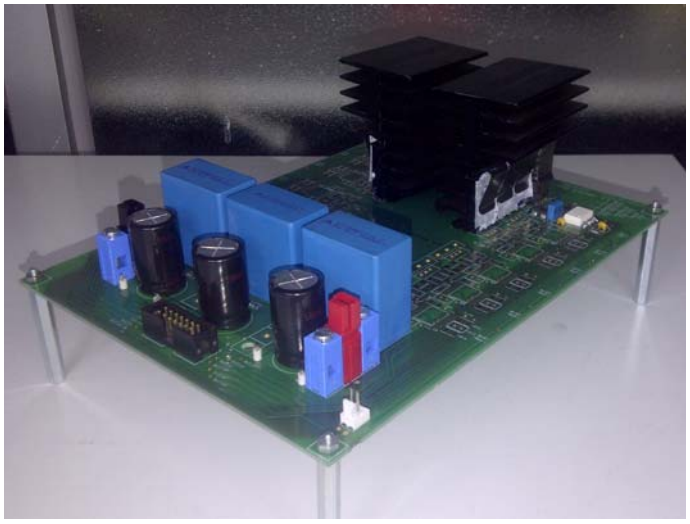


Fig. B.2. Two-level prototype.

B.2. dSPACE system

In most experiments performed, the converter control, PWM strategy, and the generation of the switch control signals have been implemented using a dSPACE system based on processor board DS1006. Fig. B.3 presents a picture of the dSPACE expansion box inside which the different dSPACE boards are placed. The dSPACE expansion box contains the following used boards:

- 1 DS1006 processor board.
- 3 DS5101 digital waveform output (DWO) boards (one for each leg).
- 1 DS2004 A/D board.

Fig. B.3. dSPACE system.

Tests shown in Chapter 2 have been the only ones in which the system previously shown have not been used. These tests have been performed using dSPACE DS1103 and an Altera EPF10K70 programmable logic device.

B.3. Dc-power-sources

Fig. B.4 presents a picture of the three dc power sources used to supply the different levels of the MAC converters. Power supply 1 corresponds to the model 6030A from HP, power supply 2 corresponds to the model SPS80-82 from Amrel, and power supply 3 corresponds to the model 5001-I from California Instruments. Other power sources with lower power rating have also been used to supply auxiliary circuits like, for example, sensors.

Fig. B.4. DC power supplies.

Table B.1, Table B.2, and Table B.3 show the main specifications of the three power supplies.

Maximum dc voltage	200 V
Maximum dc current	17 A
Maximum power	1 kW

Table B.1. Dc power supply HP 6030A specifications.

Maximum dc voltage	80 V
Maximum dc current	82 A
Maximum power	6.6 kW

Table B.2. Dc power supply Amrel SPS80-82 specifications.

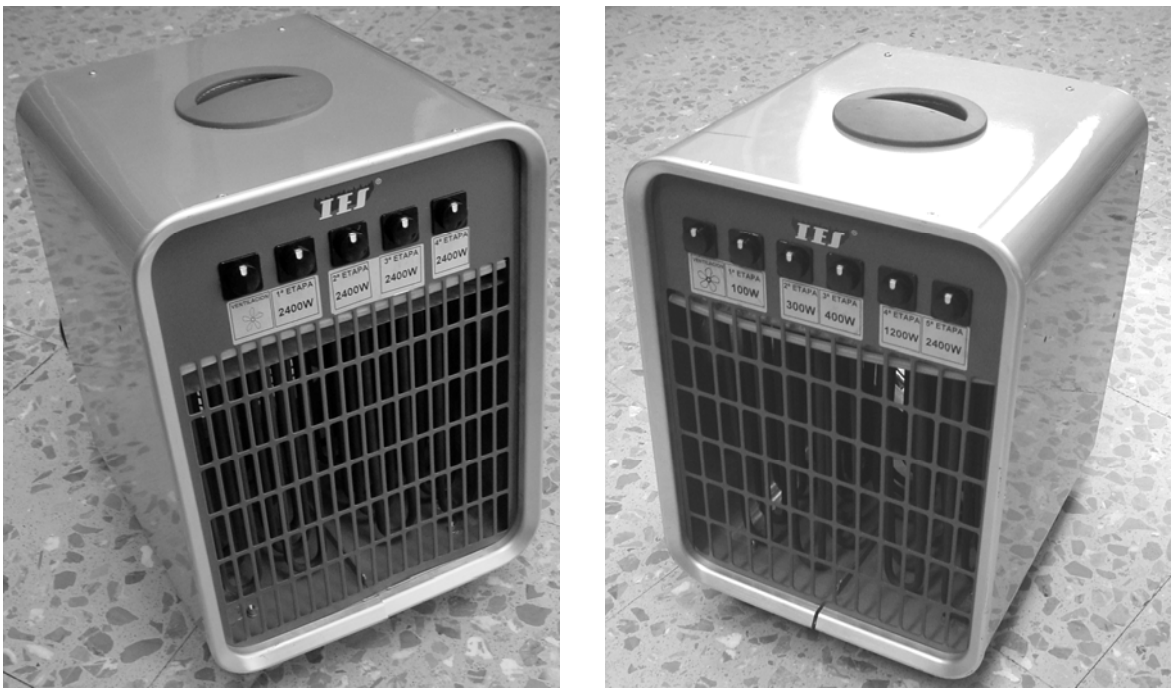
Maximum dc voltage	300 V
Maximum dc current	16.6 A
Maximum power	5 kW

Table B.3. Dc power supply California Instruments 5001-I specifications.

B.4. Loads

B.4.1. Resistive load

The three-phase resistive loads are shown in Fig. B.5.



(a) (b)

Fig. B.5. Three-phase resistive loads. (a) Resistive load 1. (b) Resistive load 2.

Table B.4 and Table B.5 show the main specifications of them.

Maximum input line-to-line voltage	400 V_{rms}
Selectable resistance per phase	[66, 33, 22, 16.5] Ω
Maximum power	9.6 kW

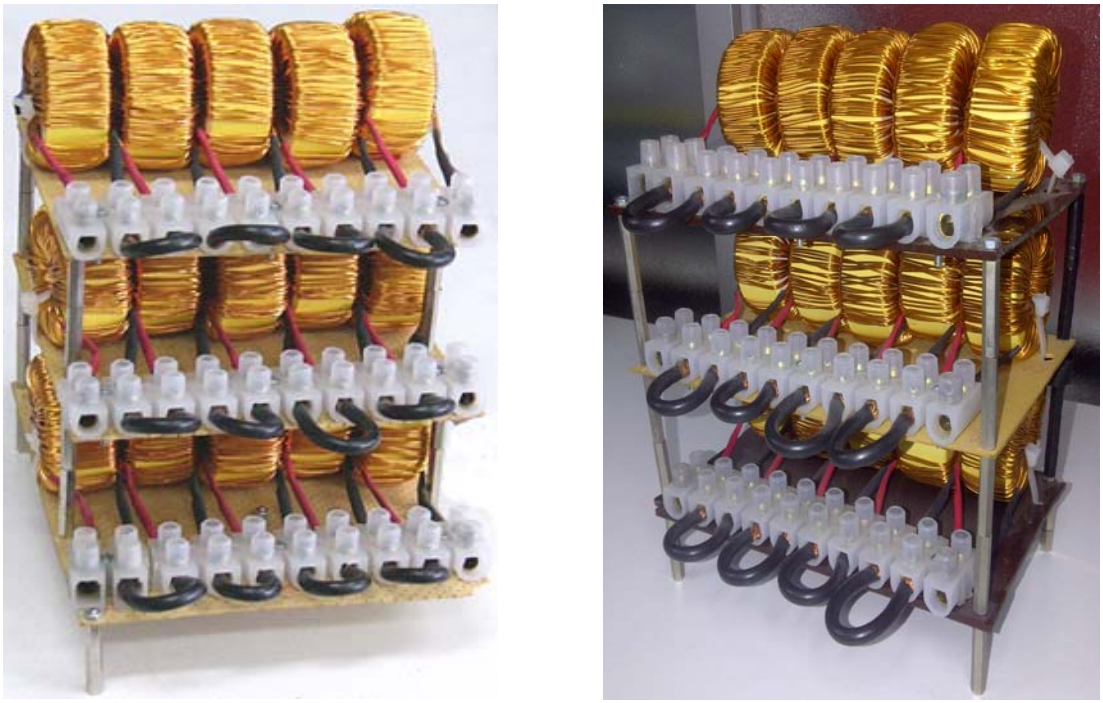
Table B.4. Resistive load 1 specifications.

Maximum input line-to-line voltage	400 V_{rms}
Selectable resistance per phase	[1587,…, 36] Ω
Maximum power	4.4 kW

Table B.5. Resistive load 2 specifications.

B.4.2. Inductive load

The inductive load sets are depicted in Fig. B.6.



(a) (b)

Fig. B.6. Three-phase inductor sets. (a) Inductive load 1. (b) Inductive load 2.

Table B.6 shows the main specifications of a single toroidal inductor.

Core material	Micrometals Iron Powder Mix No. 26
Maximum current	10 A
Average Inductance ([0, 10] A)	2.5 mH
Inductance @ 10 A	1 mH

Table B.6. Single toroidal inductor specifications.

B.5. Scopes

Fig. B.7 and Fig. B.8 show the pictures of the two scopes used.

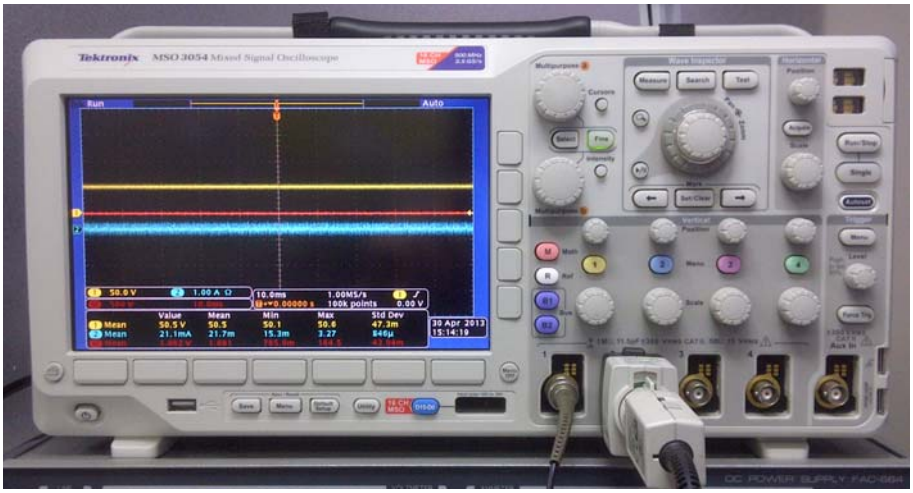


Fig. B.7. Tektronix MSO 3054 scope.

Fig. B.8. Tektronix TDS 714L scope.

B.6. Double pulse board

In order to measure the turn-on, turn-off, and reverse-recovery switching losses (Section 3.4), the double-pulse board (DPB) shown in Fig. B.9 has been used.

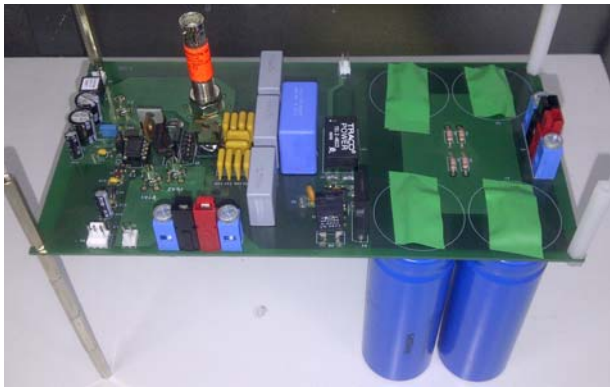


Fig. B.9. Double-pulse board used to measure device switching losses.

B.7. General overview

Most of equipment presented above can be distinguished in the general test bed overview depicted in Fig. B.10.

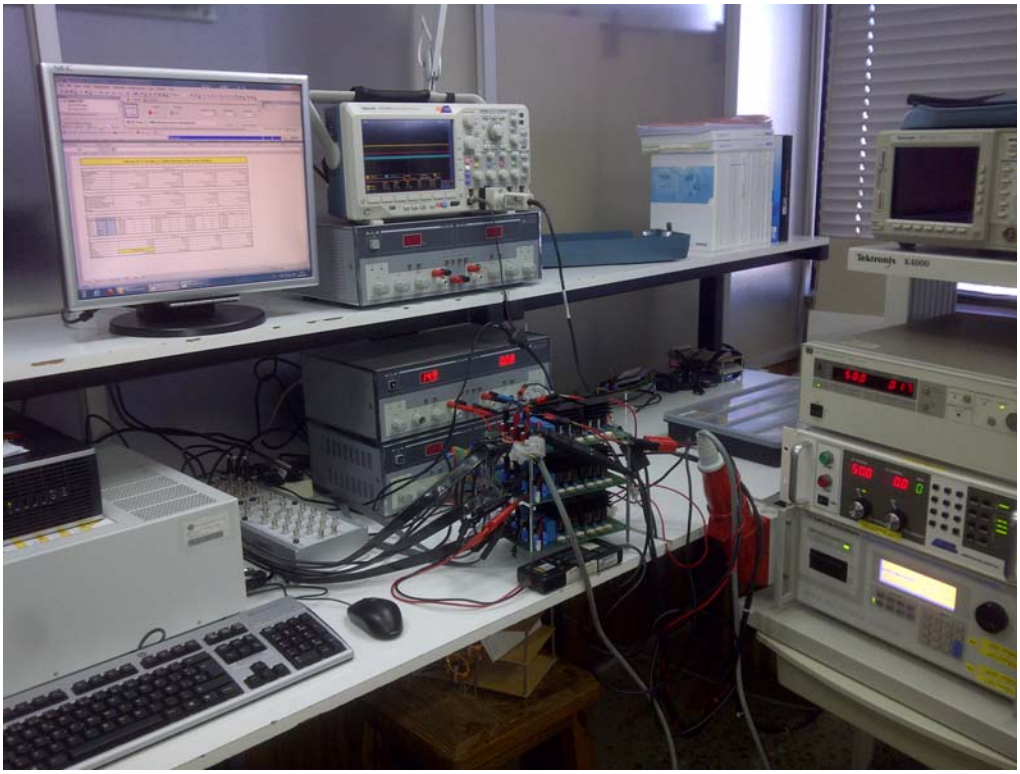


Fig. B.10. General test bed overview.

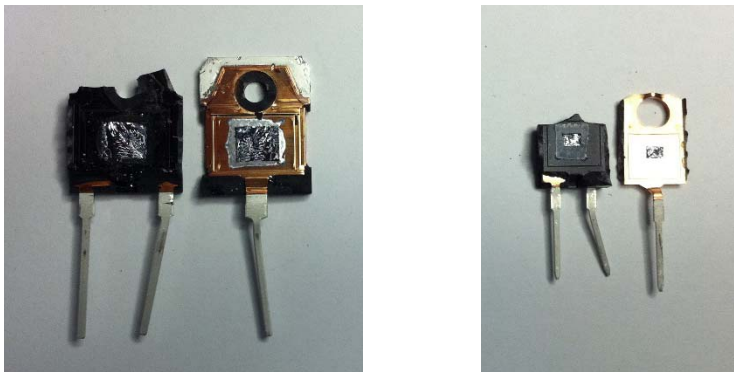
APPENDIX C

THERMAL RESISTANCE VERSUS DEVICE SILICON AREA

Abstract — This appendix contains an analysis carried out to obtain a correlation between the junction-to-sink thermal resistance $R_{th,js}$ and the device silicon area. This correlation is used in Section 3.6.

C.1. Correlation analysis

In order to obtain the correlation between the junction-to-sink thermal resistance $R_{\mathrm{th,js}}$ and the device silicon area A_{S}, some devices have been opened to measure their chip areas. Fig. C.1 presents the pictures of two of them.



(a) (b)

Fig. C.1. Pictures of two opened MOSFETs. (a) MOSFET FDA24N40F. (b) MOSFET FDPF3860T.

Table C.1 shows the measured areas and thermal resistances of all devices analyzed. The values of junction-to-case thermal resistances $R_{\mathrm{th,jc}}$ have been taken from their corresponding datasheets, the values of case-to-sink thermal resistances $R_{\mathrm{th,cs}}$ have been estimated depending on the package, and resistances $R_{\mathrm{th,js}}$ can be equaled from the addition of the previous two resistances.

Device	A_{S} **[mm^2]**	$R_{\mathrm{th,jc}}$ [°C/W]	$R_{\mathrm{th,cs}}$ [°C/W]	$R_{\mathrm{th,js}}$ [°C/W]
FDPF3860T	3.45	3.7	0.5	3.95
IRF3415	22.55	0.75	0.5	1.00
20NF20	10.26	1.38	0.5	1.63
13NM60N	10.64	1.39	0.5	1.64
FDA24N40F	28.8	0.45	0.5	0.95
12N60B3D	16.1	1.2	0.5	1.7
12N60B3D (diode)	7.02	1.9	0.5	2.4

Table C.1. Relevant parameters of devices analyzed.

Fig. C.2 presents the obtained correlation between the junction-to-sink thermal resistance $R_{\mathrm{th,js}}$ and device chip area A_{S}.

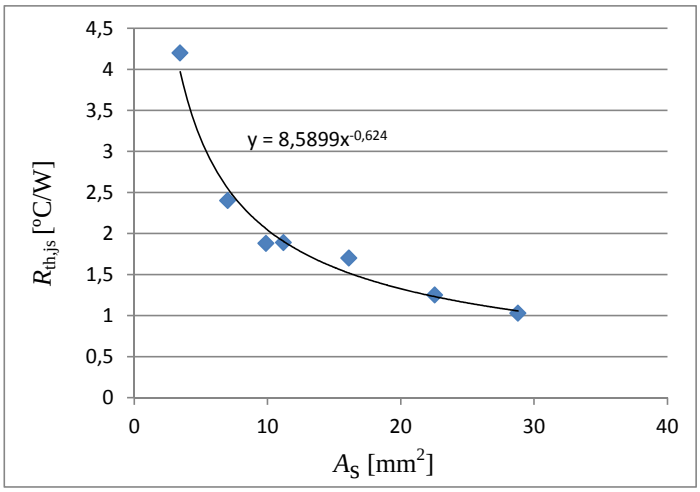


Fig. C.2. Junction-to-sink thermal resistance $R_{th,js}$ as a function of device chip area.

Rounding the obtained correlation, the final expression can be expressed as

$$R_{\mathrm{th,js}}\,(A_{\mathrm{S}}) = 8.5\,\frac{^{\circ}\mathrm{C}}{\mathrm{W}\cdot\mathrm{mm}^2}\cdot {A_{\mathrm{S}}}^{-0.6} \tag{C.1}$$

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