High-Efficiency NPC Multilevel Converter Using Super-Junction MOSFETs

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***Abstract*—Super-junction MOSFETs exhibit low on-state resistances and low switching losses. However, the reverse recovery behavior of their intrinsic diodes and their output capacitance characteristics make their deployment in freewheeling locations challenging. In this paper, a new snubber circuit arrangement has been proposed for a three-level converter to minimize the effect of the output capacitance. This is used in conjunction with diode deactivation circuitry to address the diode recovery behavior. Results are given for a three-phase three-level neutral point clamped converter running from an input voltage of 720 V and supplying a 3-kVA load. The converter operates with no forced cooling and efficiency is estimated at 99.3%. Apart from lower energy consumption, an advantage of high efficiency is a reduced converter mass due to reduced cooling requirements.**

***Index Terms*—Efficiency, MOSFET, multilevel, neutral point clamped, super-junction (SJ).**

I. Introduction

INSULATED-GATE bipolar transistors (IGBTs) and fast-recovery diodes are typically the preferred power devices for use in voltage source converter (VSC) topologies at voltages above approximately 200 V to 300 V. However, super-junction (SJ) technology [1] has made the MOSFET of potential interest here as low $R_{\mathrm{DS(on)}}$ ratings are attainable at these voltages. Advantages are low forward conduction losses, low switching losses and the possibility of implementing synchronous rectification to reduce freewheel diode conduction losses. However, challenges are encountered when deploying SJ devices in VSCs.

- Their intrinsic diodes tend to exhibit adverse behavior and draw a very high reverse recovery charge (Q_{rr}).
- Even with the diode behavior addressed, the output capacitance, C_{oss}, still presents a difficulty. C_{oss} is highly nonlinear [1], increasing with reducing drain-source voltage. This non-linearity is beneficial in single-ended applications [2] as self-discharge losses are low. However, it is problematic in a voltage-sourced bridge-leg at turn-on of the complementary device. For example, as the low-side device begins to turns on, the voltage across it is still high and consequently, the voltage across the other high-side device is low and its C_{oss} is high. The low-side device therefore simultaneously supports a high voltage and sources a large current to supply the charge, Q_{oss}, drawn by the C_{oss} of the high-side device, leading to high switching losses and EMI. Because of these drawbacks, SJ devices cannot readily be used as direct replacements for IGBTs in locations where they have to provide a freewheeling function as well as operating as a forward switch.

Silicon carbide (SiC) MOSFETs draw little reverse recovery charge and have a low C_{oss} [3]. However, commercially-available devices are costlier than silicon counterparts and they exhibit technical challenges when driving their gates due to their lower trans-conductances and lower absolute maximum gate-source voltage limits.

Instead of the VSC, SJ devices can be deployed in a current source converter (CSC) [4]. MOSFETs do not have to freewheel in a CSC and the problems associated with their intrinsic diodes are thus obviated. The CSC has desirable properties, particularly in machine drives, such as reduced winding insulation stresses. However, because of the need to provide a current source instead of a voltage source and the need for output capacitors capable of supporting bipolar voltages, the VSC is normally preferred.

High efficiency ac to dc converters can be realized by deploying SJ MOSFETs with SiC diodes such that the MOSFETs only operate as forward switches and do not freewheel [5]–[7]. Topologically, this becomes more complex in dc to ac converters where the converter has to provide a low-frequency steering function. Combined buck converters can be used here [8], [9] but choke utilization is poor and the technique is not readily suited to machine drives where the machine's series inductance acts as a choke.

Difficulties due to intrinsic diode effects and C_{oss} charging can be addressed with synchronous conducting mode (SCM) [10] operation (also referred to as the triangular conduction mode (TCM) in [11]). With SCM operation the choke current in a converter changes direction twice per switching cycle and soft switching of the MOSFETs at turn-on can be realized. However, RMS currents are higher than when in the continuous conduction mode (CCM) and the converter's switching frequency varies with load and supply voltage conditions. Furthermore, a difficulty is encountered with SCM operation in machine drive

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applications where the machine's series inductance acts as the main choke. This is fixed and therefore cannot be varied for the purpose of optimizing the operation of the power converter circuitry.

Auxiliary bridge-legs [12], [13] can be used in converters for efficient $C_{\rm oss}$ charging. However, additional power devices with lower current ratings but the full supply voltage ratings are required, as are extra drive signals.

Forced commutation [14], [15] techniques can also be used for efficient $C_{\rm oss}$ charging and intrinsic diode deactivation. Again, additional drive signals are required.

Snubber circuitry and the diode deactivation circuitry in [16] was used to address the difficulties presented by the adverse intrinsic diode behavior and $C_{\rm oss}$ in [17] where 600-V SJ MOSFETs were deployed in a two-level converter. However, many applications require a nominal voltage-supporting capability greater than 600 V. SJ MOSFETs are available with 900-V ratings and low $R_{\rm DS(on)}$ values, but a 1200-V rating is often needed. An alternative is to use lower-rated power devices in a multilevel converter. Apart from giving a higher-voltage capability, another advantage of multilevel converters is a more beneficial output voltage harmonic spectrum [18]. This paper presents a three-level VSC with 600-V SJ devices. A novel snubber configuration addresses the effect of the device's output capacitances. This is used in conjunction with circuitry that deactivates the device's intrinsic diodes. The design process used to inform the numbers and locations of the snubber elements and diode deactivation circuits is given. A prototype circuit is presented and experimental results are given.

II. Multilevel Converter Topology Selection and Operation

Various multilevel topologies are available [19], [20], including the neutral point clamped (NPC), flying capacitor-clamped and cascaded H-bridge circuits. A diode-clamped NPC three-level converter is investigated here. Active NPC (ANPC) multilevel converters [21]–[23], have advantages including the ability to balance losses between power devices. However, they have greater complexity, requiring six switches per phase for a three-level converter and the diode-clamped variant is therefore considered in this paper. On the other hand, the focus of this paper is to devise a relatively generalized method to determine how many snubber circuits are required and how to design them in a three-level converter. Therefore, we take a simpler structure, i.e., the conventional NPC converter, as an example as a starting point given the popularity of the NPC structure in various applications. Nevertheless, the devised method can also be applied to the ANPC structure with adjustment. Fig. 1 shows the NPC circuit with SJ MOSFETs (TR1-TR4) and fast-recovery diodes (D5 and D6). D1-4 are the MOSFETs' intrinsic diodes. Tables I and II summarize operation with the output current ($i_{\rm out}$ in Fig. 1), flowing out of, and into the bridge-leg, respectively. The output voltage levels referred to as H, M and L correspond, respectively to V_{ss}, $V_{ss}/2$ and 0 V in Fig. 1. In Tables I and II sequential voltage excursions from H to M, from M to L, from L to M and from M to H are described, arbitrarily starting at H with both TR1 and TR2

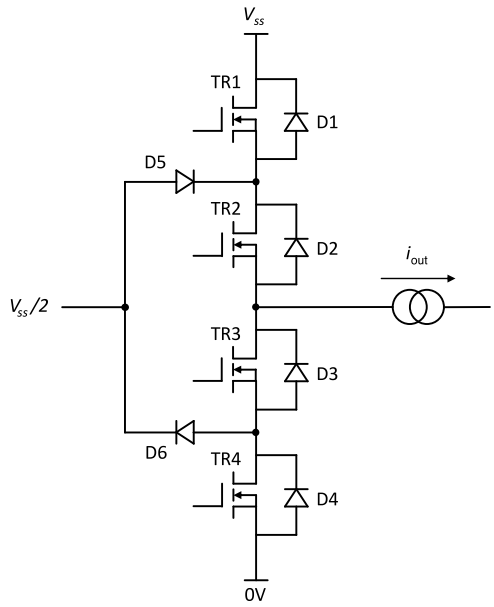

Fig. 1. Three-level NPC converter phase-leg based around MOSFETs.

signaled on. Operation in all four quadrants is thus considered. Simple drive signals with under-lapping are applied in each case. Transient stages during under-lap intervals are shown in grey. Some observations are made with respect to Tables I and II.

1) D5 and D6 are taken as being purpose-designed fast-recovery pn silicon or SiC Schottky diodes. The reverse recovery charge drawn by them is therefore treated as being negligible or much smaller than the $Q_{\rm rr}$ or $Q_{\rm oss}$ drawn by the MOSFETs. The effects of D5 and D6 are therefore neglected in the far right-hand columns in Tables I and II.
2) With the switching sequences given, the intrinsic diodes in either TR1 or TR4 have to recover in reverse during a cycle and deactivating them is desirable.
3) Even if the intrinsic diodes in TR1 and TR4 are deactivated, their output capacitances are still problematic as they draw substantial charging currents.

While the currents in TR2 and TR3 are zero when they are turned off, a voltage change of $V_{ss}/2$ is applied across one of them during each switching cycle. This results in them drawing $C_{\rm oss}$ charging currents to supply $Q_{\rm oss}$. As described in [1], SJ MOSFETs have a highly nonlinear $C_{\rm oss}$. In [17], a simple working rectangular characteristic, Fig. 2, was assumed and this is applied again in this paper. Ideally, $Q_{\rm oss}$ is drawn from a lossless source such as a voltage, v, in series with an inductance, L. The area under the QV curve represents the capacitive co-energy and this is much higher than the capacitive stored electric field energy for low-$R_{\rm DS(on)}$ high-voltage MOSFETs. The straight-line approximation in Fig. 2 yields an overestimate of the co-energy and thus a factor of safety.

In summary, when using SJ MOSFETs in all four quadrants in a diode-clamped three-level converter, the charging of all four device's output capacitances has to be managed. The behavior of the intrinsic diodes of the outer devices (TR1 and TR4 in Fig. 1) also has to be addressed for four-quadrant operation.

TABLE I
OPERATION OF POWER DEVICES WITH CURRENT FLOWING OUT OF BRIDGE-LEG

Stage	**Output voltage level**	**Gate-drive signals** (1 = on, 0 = off)					**States of power devices** • Fwd = conducting in forward direction • Rev = intrinsic diode conducting • SR = acting as synchronous rectifier and conducting in reverse direction • 0 = not conducting						**Devices drawing diode recovery charge, Q_{rr}, or C_{oss} charge, Q_{oss}, when transition into stage is made**	**Charging current routes**
		TR1	TR2	TR3	TR4		TR1	TR2	TR3	TR4	D5	D6		
1	H	1	1	0	0		fwd	fwd	0	0	0	0	D5 (Q_{rr}), TR3 (Q_{oss})	TR1, 2, 3**
2	M	0	1	0	0		0	fwd	0	0	fwd	0	none	none
3	M	0	1	1	0		0	fwd	0	0	fwd	0	none	none
4	L	0	0	1	0		0	0	SR	rev	0	0	none	none
5	L	0	0	1	1		0	0	SR	SR	0	0	none	none
6	L	0	0	1	0		0	0	SR	rev	0	0	none	none
7	M	0	1	1	0		0	fwd	0	0	fwd	0	TR4 (Q_{rr} + Q_{oss})	D5, TR2, 3, 4
8*	M	0	1	0	0		0	fwd	0	0	fwd	0	none	none

*The circuit then transitions back to Stage 1. **The reverse recovery current drawn by D5 is neglected here.

TABLE II
OPERATION OF POWER DEVICES WITH CURRENT FLOWING INTO BRIDGE-LEG

Stage	**Output voltage level**	**Gate-drive signals** (1 = on, 0 = off)					**States of power devices** • Fwd = conducting in forward direction • Rev = intrinsic diode conducting • SR = acting as synchronous rectifier and conducting in reverse direction • 0 = not conducting						**Devices drawing diode recovery charge, Q_{rr}, or C_{oss} charge, Q_{oss}, when transition into stage is made**	**Charging current routes**
		TR1	TR2	TR3	TR4		TR1	TR2	TR3	TR4	D5	D6		
1	H	1	1	0	0		SR	SR	0	0	0	0	none	none
2	H	0	1	0	0		rev	SR	0	0	0	0	none	none
3	M	0	1	1	0		0	0	fwd	0	0	fwd	TR1 (Q_{rr} + Q_{oss})	D6, TR1, 2, 3
4	M	0	0	1	0		0	0	fwd	0	0	fwd	none	none
5	L	0	0	1	1		0	0	fwd	fwd	0	0	D6 (Q_{rr}), TR2 (Q_{oss})	TR2, 3, 4**
6	M	0	0	1	0		0	0	fwd	0	0	fwd	none	none
7	M	0	1	1	0		0	fwd	0	0	0	fwd	none	none
8*	H	0	1	0	0		rev	SR	0	0	0	0	none	none

*The circuit then transitions back to Stage 1. **The reverse recovery current drawn by D6 is neglected here.

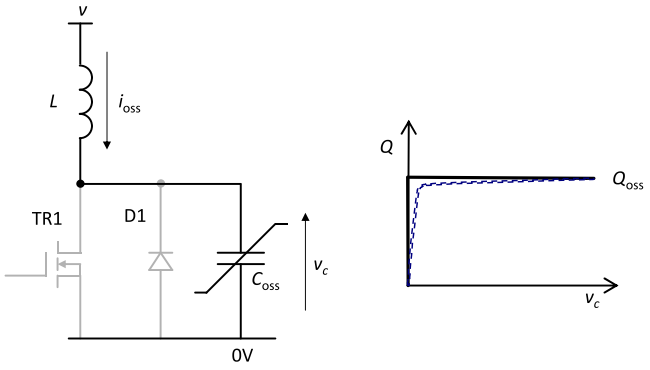

Fig. 2. Rectangular approximation of QV characteristic of output capacitance of super-junction MOSFET.

In low-voltage conversion, a technique for MOSFET intrinsic diode deactivation is to connect a silicon Schottky diode in anti-parallel [24]. However, silicon Schottky diodes do not have sufficient voltage ratings for use at off-line voltages. Those diodes that do, such as the fast recovery silicon P-N diode or the SiC Schottky diode, have a higher forward voltage drop, being comparable to, or greater than, that of the MOSFET's intrinsic diode. The effect of this is that when the MOSFET's channel is turned off, there is insufficient voltage to force current into an external diode.

III. PROPOSED ARRANGEMENT

An objective is to identify the minimum ancillary circuit requirements based on the switching actions listed in Tables I and II, where linear inductors are used to control charging of C_{oss}. Fig. 3 shows the proposed arrangement [25]. As TR1 and TR4 are subjected to intrinsic diode recovery effects, the local intrinsic diode deactivation circuits in [16] are included. By inspecting the far right-hand columns in Tables I and II it is seen that both TR2 and TR3 lie in all the charging current routes. Locating one snubber inductor directly in series with either TR2 or TR3 should therefore suffice to control the C_{oss} charging currents into all four MOSFETs.

However, a difficulty arises with inductor reset. Consider, for example, where the transition from Stage 6 to Stage 7 in Table I is made. TR4 effectively turns off when it has drawn most of its Q_{oss} and its C_{oss} then falls rapidly.

Energy has been stored in the inductor and it is now necessary to reset it but, in Stage 7, TR2, TR3, D6 and D5 would form a zero-volt loop around N, thereby preventing effective

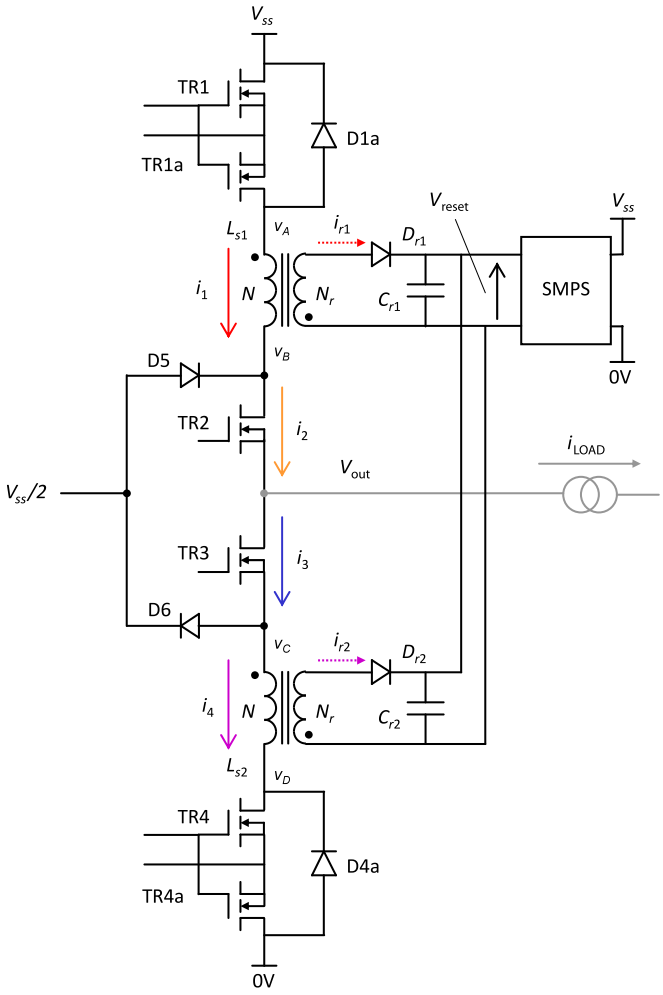

Fig. 3. Proposed phase-leg arrangement.

resetting. For this reason, the circuit with two inductors in Fig. 3 is used as either TR1 or TR4 lie in all the charging routes. Inductor reset is implemented by a secondary winding, N_r, on each inductor that transfers energy into a voltage sink, $V_{\rm reset}$, via a diode, D_r. This energy is returned to the power rails by a switched-mode power supply (SMPS). One SMPS can suffice for recovering the energy from all the inductors in a converter [17]. C_r is a local decoupling capacitor. According to the rectangular QV approximation in Fig. 2, energy, $E_{\rm oss}$, given by

$$E_{\rm oss} = Q_{\rm oss} V_{\rm in} \tag{1}$$

is stored in L_s in the process of charging $C_{\rm oss}$. If $f_{\rm sw}$ is the switching frequency, then the power, W_s, transferred through L_s due to charging any one $C_{\rm oss}$ is given by

$$W_S = f_{\rm sw} Q_{\rm oss} V_{\rm in}. \tag{2}$$

From (2) it is seen that W_s is independent of the load current ($i_{\rm LOAD}$). N_r performs another function once during each switching cycle (assuming transitions are only made between two voltage levels each cycle) apart from allowing the recovery of stored energy associated with the inductor's snubbering

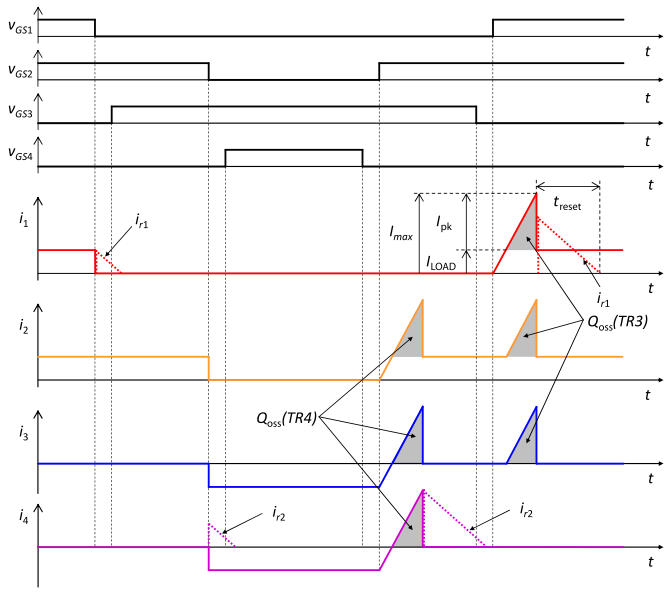

Fig. 4. Waveforms when sourcing current. L_{s2} controls the current into $C_{\rm oss}$(TR4) during the L to M transition. L_{s1} controls the current into $C_{\rm oss}$(TR3) during the M to H transition.

action when charging $C_{\rm oss}$. Depending on the transitions being made (between H and M or between M and L), and the direction of $i_{\rm LOAD}$, it either provides a reflected path for current when current is forced into N or allows commutation of the current in N without the applied mmf undergoing a step change. When current is initially forced into N, if N_r were not present, the inductor would present a high impedance and a large over-voltage would appear across the applicable power device turning off. With N_r present, L_s acts as a voltage transformer until the magnetizing current reaches $i_{\rm LOAD}$. Neglecting leakage inductance effects, the over-voltage across the device is limited to the reflected reset voltage. Similarly, when current in N is commutated, N_r provides a reflected path in parallel with L_s. The power throughput, W_2, due to either a current being forced into N or a current in it being commutated is given by

$$W_2 = \frac{f_{\rm sw} I_{\rm LOAD}^2 L_S}{2}. \tag{3}$$

It is assumed here that $N = N_r$ and the time, t_1, taken for either of these actions is given by

$$T_1 = \frac{L_S I_{\rm LOAD}}{V_{\rm reset}}. \tag{4}$$

Figs. 4 and 5 show idealized waveforms when the converter leg is sourcing current and sinking current, respectively. i_{r1} and i_{r2} are the currents in the secondary windings of L_{s1} and L_{s2}, respectively. The grey areas represent $Q_{\rm oss}$ only, as $Q_{\rm rr}$ is now, ideally, eliminated. The peak current, $I_{\rm pk}$, due to the charging of $C_{\rm oss}$ that flows in L_s is given by

$$I_{\rm pk} = \sqrt{\frac{2VQ_{\rm oss}}{L_S}} \tag{5}$$

where V is $V_{ss}/2$ here. $I_{\rm pk}$ is reached when virtually all of $Q_{\rm oss}$ has been supplied and $C_{\rm oss}$ drops abruptly. Due to the

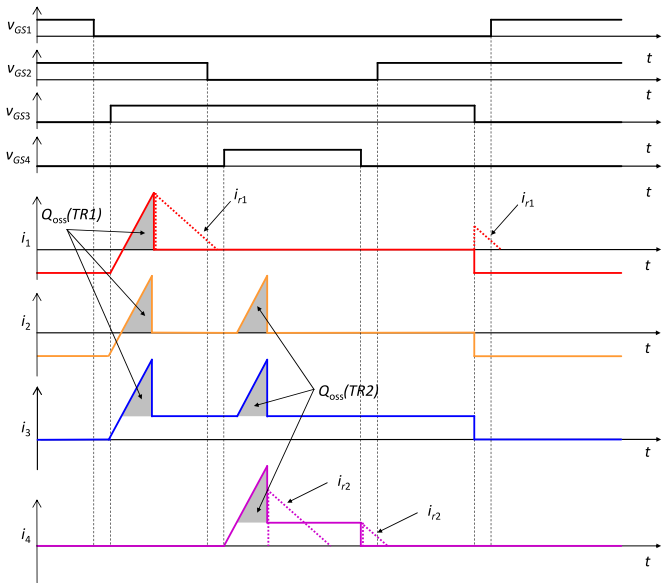

Fig. 5. Waveforms when sinking current. L_{s1} controls the current into C_{oss}(TR1) during the H to M transition. L_{s2} controls the current into C_{oss}(TR2) during the M to L transition.

diode deactivation circuitry, the transient currents drawn by TR1 and TR4 when they become reverse-biased are now (given ideal deactivation) solely C_{oss} charging currents. The charges drawn by them are therefore independent of i_{LOAD} prior to commutation and are the same as those drawn by TR2 and TR3 upon becoming reverse-biased.

However, the peak current in L_s is partially dependent on i_{LOAD} if the current supplying Q_{oss} is superimposed onto it. The energy, E_{sec}, transferred out of N_r into V_{reset} during the reset interval, T_{reset}, is independent of i_{LOAD} and is given by

$$E_{\text{sec}} = \frac{1}{2} I_{\text{pk}}^2 L_s. \tag{6}$$

However, the total energy, ΔE, transferred out of L_s during T_{reset} must be

$$\Delta E = \frac{1}{2}\left[(I_{\text{LOAD}} + I_{\text{pk}})^2 - I_{\text{LOAD}}^2\right] L_S. \tag{7}$$

The difference between ΔE and E_{sec} is accounted for by the primary winding, N, also sourcing energy, E_{pri}, during the reset period, T_{reset}. Subtracting E_{sec} from ΔE gives E_{pri}

$$E_{pri} = \Delta E - E_{\text{sec}}. \tag{8}$$

Putting the results from (6) and (7) into (8) yields

$$E_{pri} = I_{\text{LOAD}} V_{\text{reset}} t_{\text{reset}}. \tag{9}$$

T_{reset} is given by

$$T_{\text{reset}} = \frac{L_S I_{\text{pk}}}{V_{\text{reset}}}. \tag{10}$$

Putting the result from (5) into (10) yields

$$T_{\text{reset}} = \frac{\sqrt{2VQ_{\text{oss}}L_S}}{V_{\text{reset}}}. \tag{11}$$

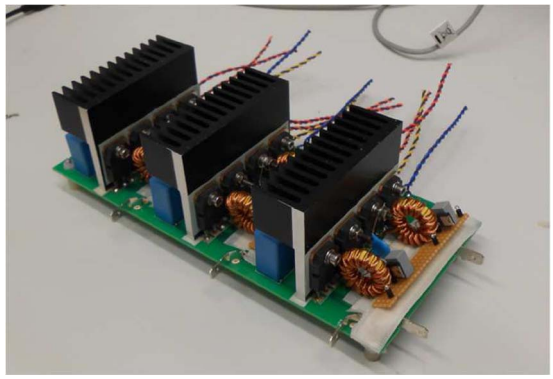

Fig. 6. Experimental hardware. The main MOSFETs are visible on the front surfaces of the heatsinks and the main diodes are located on the rear surfaces.

The flux density change, B_Q, incurred in the core of L_s when sourcing Q_{oss} is given by

$$B_Q = \frac{NI_{\text{pk}}}{SA_e} \tag{12}$$

where S is the core's reluctance. Substituting the result from (5) into (12) yields

$$B_Q = \sqrt{\frac{2\mu_0\mu_r V_{RAIL} Q_{\text{oss}}}{l_e A_e}}. \tag{13}$$

During t_1 and T_{reset}, a reflected over-voltage appears across one of the power devices. Use of an SMPS to recover energy into the dc link has the advantage that the reflected voltage can be small while using a snubber inductor with $N = N_r$, an arrangement with low leakage inductance. An SMPS can attain a high voltage gain without operating at extreme duty cycles and poor efficiency by using an isolated-output topology such as the flyback circuit in [17].

The circuit proposed here uses six fully-rated power devices and four auxiliary devices per phase-leg. An alternative circuit is proposed in [26] where a hybrid arrangement of IGBTs, MOSFETs and diodes is used.

IV. Experimental Hardware Design

A. Main Power Devices and Decoupling Capacitors

The circuit in Fig. 6 was constructed around three of the phase-legs in Fig. 3. V_{RAIL} was 720 V and the output power was 3 kVA at 400 V. f_{sw} was 20 kHz. SJ devices can switch at high frequencies in SMPSs with the consequent benefits of allowing smaller passive components to be used [2]. However, an intended application for the circuitry here is in machine drives where this is not generally advantageous. A frequency of 20 kHz was selected as being suitable for a drive. The devices were: TR1-TR4 = TK40J60U [27], TR1a, TR4a = IPD031N03L G, D1a, D4a = IDD03SG60C [28], D5, D6 = DHG20I600HA [29]. The main devices (TR1-4, D5 and D6) are mounted on the heatsinks shown. TR1a and TR4a only require a low voltage rating and their $R_{\text{DS(on)}}$ for a given area and resultant losses can be very low. They are therefore located in surface-mounted packages on the underside of the PCB. The

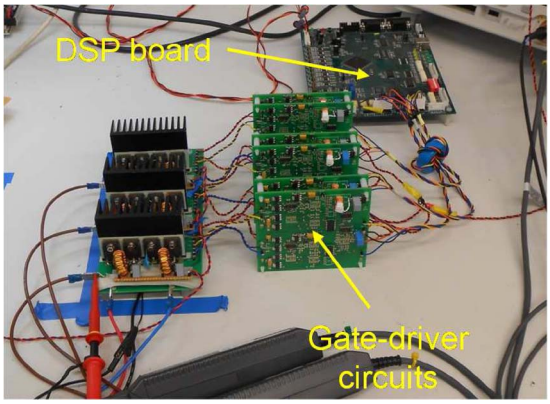

Fig. 7. Test rig. No forced cooling is applied.

power dissipation in D1a and D4a is low due to their operation at low duty cycles, and they are similarly mounted. Three 1-μF, 630-V polypropylene capacitors connected in parallel across each voltage cell provide local supply rail decoupling. The mass of the converter as shown was measured at 0.634 kg. The PCB on which it was built measures 207 mm by 93 mm. The converter was run on the horizontal surface in Fig. 7 with no forced cooling.

B. PWM Generation Circuitry

The three-phase 12-channel PWM signals are generated using a Texas Instrument DSP TMS320F2812. The PWM signals between TR1 and TR3 are generated in a complementary fashion, as are those for TR2 and TR4. The dead-time is 690 ns and the modulation index, M, is 0.9.

C. Snubber Inductor Design and Reset Circuitry

The design of L_s was identical to that in [17]. It was constructed with a Micrometals T80-8/90 toroidal core [30]. $Q_{\rm oss}$ for the TK40J60U device has been measured at 300 nC [17]. Substituting this and data from [30] ($\mu_r = 35$, $l_e = 51.4$ mm, $A_e = 23.1$ mm^2) into (13) gives $B_Q = 94$ mT. N was set at 16. Using the manufacturer's quoted inductance factor this gives an inductance of 4.61 μH. The inductance of one inductor was measured at 4.89 μH in [17]. N_r has the same number of turns as N and each winding was evenly distributed around the core to minimize leakage inductances. N and N_r were as follows:

- N: 22 strands of 0.2-mm diameter copper wire;
- N_r: one strand of 0.315-mm diameter copper wire.

N was formed with stranded wire to mitigate skin-effect losses and ease construction. The flux density, $B_{\rm LOAD}$, attributable to $i_{\rm LOAD}$ flowing in N is given by

$$B_{\rm LOAD} = \frac{N\mu_0\mu_r I_{\rm LOAD}}{l_e}. \tag{14}$$

At 3 kVA and 400 V, the peak $i_{\rm LOAD}$ is 6.15 A. Putting data into (14) yields $B_{\rm LOAD} = 84$ mT. Adding $B_{\rm LOAD}$ to B_Q gives a total flux density excursion of 176 mT. Dividing this by two gives a peak ac flux density change of 88 mT. The worst-case flux density excursion from zero occurs when an inductor is carrying a $C_{\rm oss}$ charging current of a MOSFET superimposed onto the incoming $i_{\rm LOAD}$ when the latter is at its peak value. This occurs, for example, when the converter is sourcing current (Fig. 4) and TR1 turns on and L_{s1} controls the charging current into TR3.

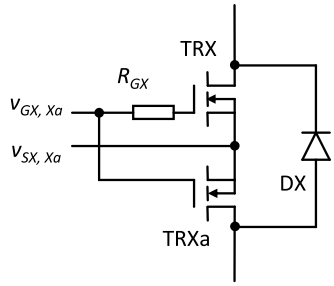

Fig. 8. Local gate driver arrangement with resistor, R_{GX}, to slow the fall in gate-source voltage of TRX relative to that of TRXa.

From the measurements in [17], the resistance, R_w, of N was taken as 10.4 mΩ, when at 60 °C. R_w is small compared to the total $R_{\rm DS(on)}$ value of the MOSFET combination in series with it and the latter dominates. $V_{\rm reset}$ was set at a nominal value of 25 V. D_r was an IDD03SG60C SiC diode and C_r was a 1.5-μF, 50-V polyester type for local decoupling.

D. Gate Driver Circuits

Gate drivers with optical isolation were used between the DSP board and converter. The on-state and off-state gate-source voltages were 12 V and -3 V, respectively. To avoid turning off TR1 and TR4 in Fig. 3 with reverse current in them and activating their intrinsic diodes, the circuitry in Fig. 8 was used. R_{GX} slows the fall in gate-source voltage of TRX relative to that of TRXa. At the penalty of losses in R_{GX} and extra switching losses in TRX, this causes TRXa to turn off and route current out of TRX and into DX before TRX turns off. R_{GX} was 10-Ω.

E. Predicted Losses

Table III shows predicted losses for a phase-leg supplying 1 kVA at unity power factor. Calculations are given in the Appendix. Losses for each row are the total for both components in the description. The following points are noted.

- Switching losses in TR1a and TR4a are neglected.
- Total losses in the components mounted on the heatsink are estimated at 5.59 W.
- The switching-frequency ripple content in $i_{\rm LOAD}$ is neglected.

V. Experimental Results

A. Base Frequency Waveforms

Fig. 9 shows waveforms when supplying 3 kVA into a near unity power factor 400-V load from a 720-V supply voltage.

TABLE III
PREDICTED LOSSES FROM ONE PHASE-LEG

		Description	Loss (W)	Applicable section in Appendix
Loss in components in bridge-leg	Phase-leg components mounted on heatsink	Conduction loss in TR1 and TR4	1.11	*A.*
		Switching loss in main switches (TR1 and TR4)	1.02	*B.*
		Switching loss in main switches (TR2 and TR3)	0	
		Self-discharge loss in TR1 and TR4	0.32	*C.*
		Conduction loss in inner switches (TR2 and TR3)	1.51	*D.*
		Conduction loss in D5 and D6	1.63	*E.*
	Phase-leg components mounted on pcb	Conduction loss in TR1a and TR4a	0.06	*F.*
		Dead-time loss in D1a and D4a	0.14	*G.*
	Snubber inductors	Conduction loss (L_{s1} and L_{s2})	0.15	*H.*
		Core loss (L_{s1} and L_{s2})	0.50	*I.*
Losses in reset circuitry		Reset diode (D_{r1} and D_{r2}) loss	0.16	*J.*
		Losses in SMPS	0.77	*K.*
Total estimated loss			7.37	

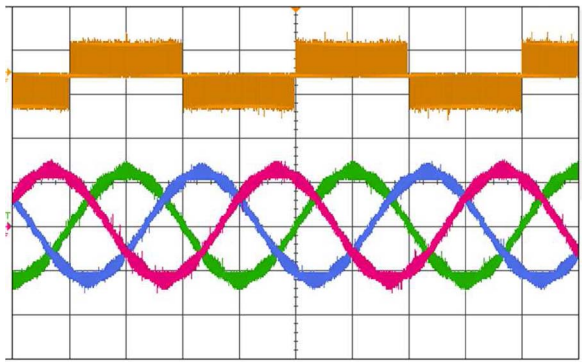

Fig. 9. Base-frequency waveforms showing an output voltage from one phase and the three output currents. The top trace is the voltage. Scales: $v_{\rm out} = 500$ V/div, $i_{\rm LOAD} = 5$ A/div. Time scale $= 5$ ms/div.

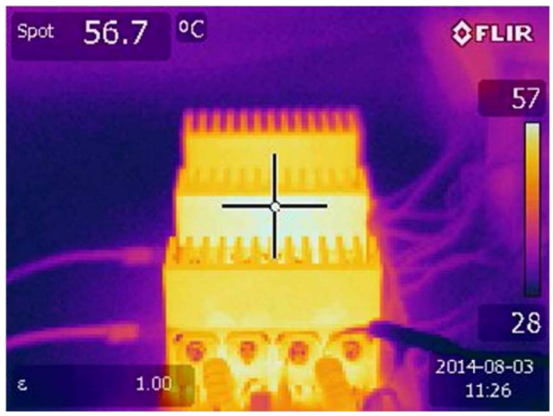

Fig. 10. Thermal photograph of the circuit in Figs. 6 and 7 when supplying 3 kVA into a unity power factor load and in the hard thermal steady-state.

The load was formed with three star-connected series-RL circuits. The inductors were 2-mH laminated steel components. The base frequency was 50 Hz.

B. Power Transferred Into Reset Voltage Sink

The power transferred into $V_{\rm reset}$ is the sum of W_s and W_2, given by (2) and (3), respectively. This is calculated at 3.09 W per phase-leg in the Appendix, giving a total of 9.27 W for all three phases. Instead of commissioning an SMPS, a dump load was used for experimentation. Its resistance (72 Ω) was set so that $V_{\rm reset}$ was close to the nominal value of 25 V. The power dissipation was measured at 8.3 W. This is lower than the 9.27 W predicted, and is expected due to losses in L_s and D_r.

C. Thermal Measurements

Fig. 10 shows a thermal photograph of the circuit running at full load, as in Fig. 9, and in the hard thermal steady-state. Before proceeding with the thermal tests, one of the heatsinks was thermally characterized. A dc current was passed through the path from the source of TR3 to the drain of TR2 and the

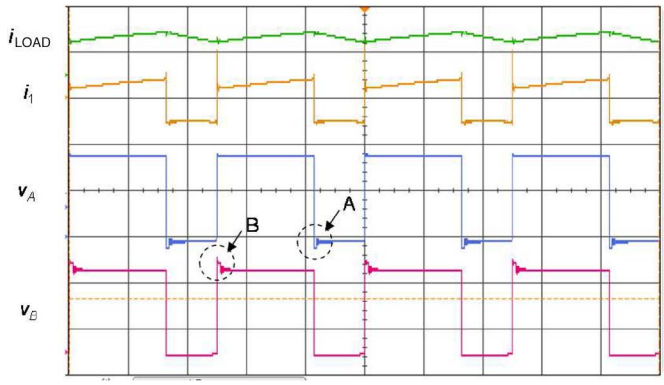

Fig. 11. Switching-frequency waveforms showing complete switching cycles. Scales: i_{LOAD}, $i_1 = 5$ A/div, v_A, $v_B = 200$ V/div. Time scale $= 20$ μs/div.

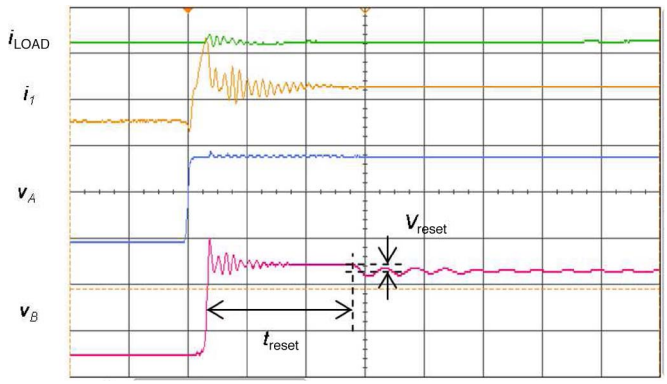

Fig. 12. Waveforms at TR1 turn-on. Scales: i_{LOAD}, $i_1 = 5$ A/div, v_A, $v_B = 200$ V/div. Time scale $= 500$ ns/div.

voltage developed was measured. The thermal resistance was estimated at 4.74 °C/W by recording the heatsink's temperature rise above ambient. The total loss of the components mounted on the heatsinks was estimated at 17.3 W from the average temperature rises of the heatsinks. Due to the proximity of the heatsinks to each other, and the heating effect of losses incurred from circuitry not mounted on the heatsinks, this is expected to be an overestimate. Although the central heatsink is at a higher temperature than the other two, this is only by approximately 2°C and is expected given its physical location.

D. Exemplifying Switching-Frequency Waveforms With Current out of Converter and Positive Output Voltage

Fig. 11 shows switching-frequency waveforms from a phase-leg running under steady-state dc conditions and switching between the "H" and "M" voltage levels so that it outputs a positive voltage. The duty cycle was set so that the average output voltage, v_{out}, is 230 V. An RL load is connected between v_{out} and $V_{ss}/2$. For this test an inductor of 3.9 mH based around ferrite cores was used. i_{LOAD} is 4.35 A. This corresponds to those instances in the ac cycle in Fig. 9 where $\omega t = 0.785$ rads and 2.356 rads. The quantities shown are: i_{LOAD}, the current (i_1) in the primary winding of L_{s1}, the drain voltage of TR1a (v_A) and the drain voltage of TR2 (v_B). For practical purposes v_A is very close to the source voltage of TR1. An overshoot voltage (circle "A") is seen at v_A when current is forced out of L_{s1} at TR1 turn-off. An overshoot voltage (circle "B") is seen at v_B at L_{s1} reset. i_{LOAD} was measured with a high-bandwidth dc current probe. i_1 was measured with a sensor based on a Rogowski coil as this introduces less physical disruption and consequent stray inductance in series with N. The resistance of the dump load substituted for the SMPS was set to give a V_{reset} value close to 25 V. 227 Ω gave $V_{\mathrm{reset}} = 25.6$ V. The power transferred into the resistance was thus calculated at 2.89 W. Figs. 12 and 13 show waveforms at TR1 turn-on. Although no intrinsic diode recovery action is taking place, a C_{oss} charging current is sourced into TR3. It is seen, Fig. 12, that the duration of T_{reset} is in good agreement with the value of 1.30 μs calculated with (10). Fig. 14 shows waveforms at

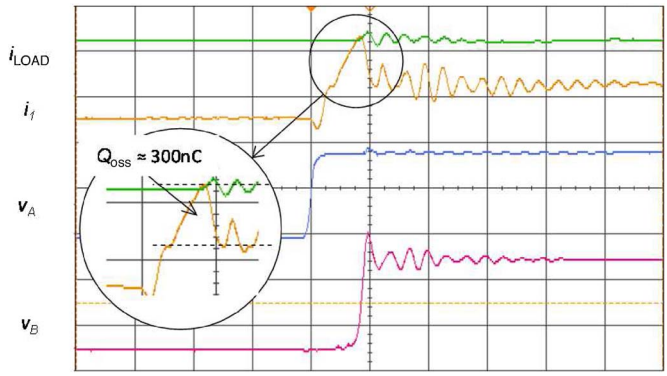

Fig. 13. Expanded view of waveforms at TR1 turn-on. Scales: i_{LOAD}, $i_1 = 5$ A/div, v_A, $v_B = 200$ V/div. Time scale $= 200$ ns/div.

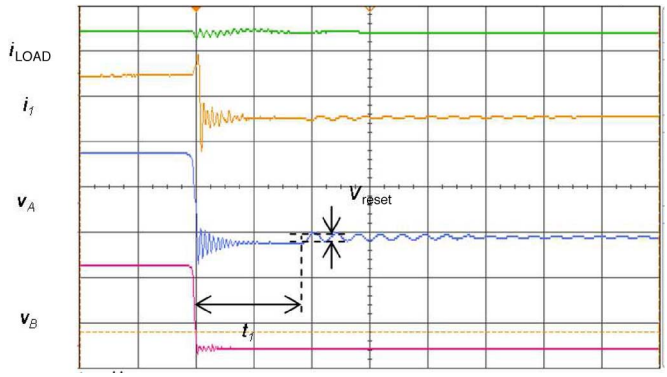

Fig. 14. Waveforms at TR1 turn-off. Scales: i_{LOAD}, $i_1 = 5$ A/div, v_A, $v_B = 200$ V/div. Time scale $= 500$ ns/div.

TR1 turn off where it is also seen that t_1 is in good agreement with the value of 0.85 μs calculated with (4).

E. Exemplifying Switching-Frequency Waveforms With Current out of Converter and Negative Output Voltage

For these tests the RL load was connected between the v_{out} terminal of a phase-leg and 0 V, Fig. 15. Although this is not a standard configuration and the power flow is from the dc supply, an outer device is forced to act as a freewheeling device as is the

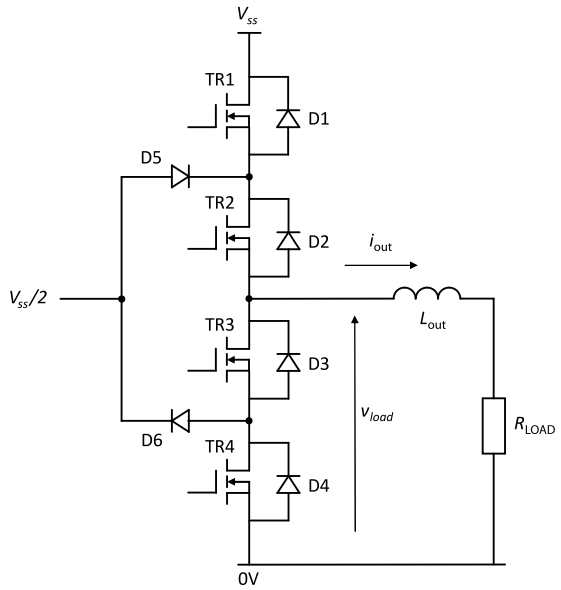

Fig. 15. Connection arrangement with positive output current and negative output voltage (when referenced to mid-point, $V_{ss}/2$). The ancillary circuitry is not shown for clarity.

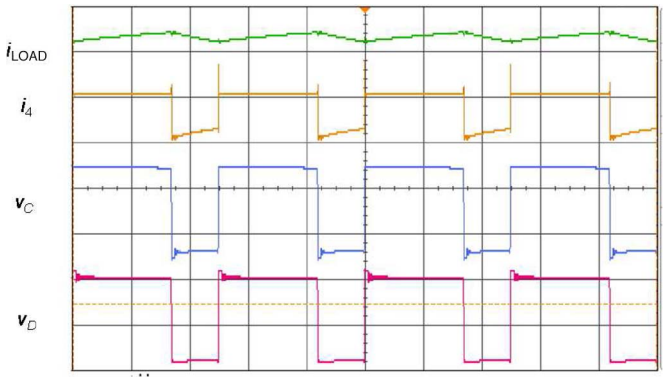

Fig. 16. Switching-frequency waveforms showing complete switching cycles. Scales: i_{LOAD}, $i_4 = 5$ A/div, v_C, $v_D = 200$ V/div. Time scale $= 20$ μs/div.

case with ac to dc (rectifier) operation. In this case the behavior of its intrinsic diode has to be addressed in conjunction with the charging of its C_{oss}, as is the case with the L to M and H to M transitions in Tables I and II, respectively. The switching stresses are thus those encountered with operation as an ac to dc converter. The switching duty factor was set so that the load voltage (not output voltage) is 230 V with an average i_{LOAD} of 4.35 A.

Fig. 16 shows exemplifying switching-frequency waveforms from one of the phase-legs. As in Section D, the phase-leg is running under steady-state dc conditions. In this case it transitions between the "M" and "L" voltage levels to output a negative voltage. Four quantities are shown: i_{LOAD}, the current (i_4) in the primary winding of L_{s2}, the source voltage of TR3 (v_C) and the drain voltage of TR4 (v_D). i_{LOAD} was, again, measured using a high-bandwidth dc current probe. As with i_1, i_4 was measured using a sensor based around a Rogowski coil. V_{reset} was measured at 24.52 V. Given the dump resistance

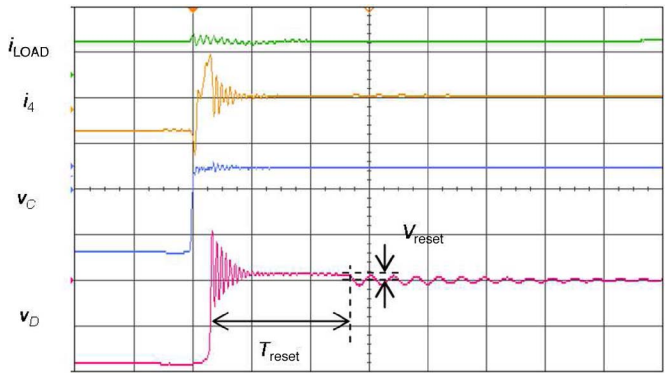

Fig. 17. Waveforms at TR2 turn-on. Scales: i_{LOAD}, $i_4 = 5$ A/div, v_C, $v_D = 200$ V/div. Time scale $= 500$ ns/div.

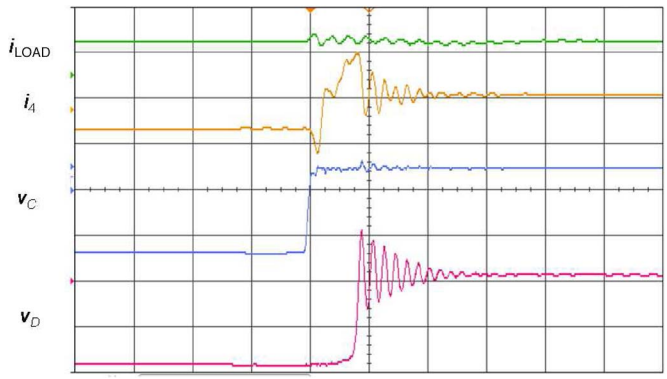

Fig. 18. Expanded view of waveforms at TR2 turn-on. Scales: i_{LOAD}, $i_4 = 5$ A/div, v_C, $v_D = 200$ V/div. Time scale $= 200$ ns/div.

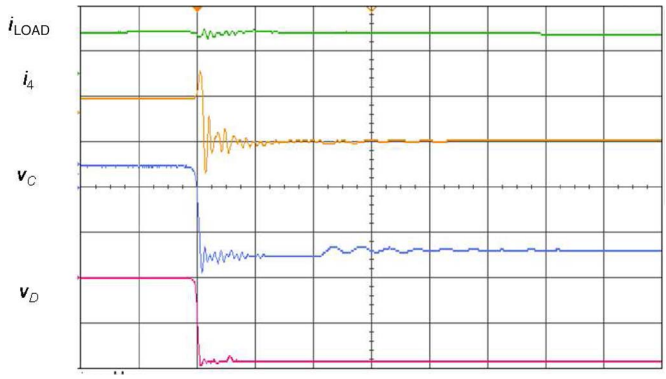

Fig. 19. Waveforms at TR2 turn-off. Scales: i_{LOAD}, $i_4 = 5$ A/div, v_C, $v_D = 200$ V/div. Time scale $= 500$ ns/div.

value of 227 Ω used here, the power transferred into the resistance was calculated at 2.65 W.

Figs. 17 and 18 show waveforms at TR2 turn-on. Fig. 19 shows waveforms at TR2 turn-off. The power transferred into V_{reset} is similar for the two situations where firstly a capacitance has to be charged (2.89 W) and secondly both a C_{oss} has to be charged and an intrinsic diode has to be deactivated (2.65 W). Also, the observed Q_{oss} is approximately 300 nC in both cases. Q_{oss} is taken from the current-time overshoot products in i_1 and i_4 in Figs. 13 and 17, respectively.

It is therefore inferred that intrinsic diode deactivation is effective.

VI. Discussion

Standard gate drive signals with under-lapping were applied. Simple sinusoidal PWM was used, although more sophisticated schemes are available for multilevel conversion [31]–[36]. A 720-V rail was used and a 400-V ac voltage was produced. This gives a headroom voltage of only 35 V at the peak output voltage with simple PWM control. However, harmonic injection can be used in a three-phase inverter control scheme to increase the effective headroom voltage, or space vector modulation with a cell-balancing capability may be used [33].

Although the converter is based around silicon SJ devices, some SiC components are used. These are D1a, D4a, D_{r1} and D_{r2}. However, these are not active switches and the use of SiC MOSFETs or JFETs is avoided. Also, none of these diodes has to be rated for a high steady-state current and their cost is consequently low. D5 and D6 are fast-recovery silicon diodes. The converter has been configured for operation at any power factor. However, during unity power factor operation as a dc to ac converter it only operates in the two quadrants where i_{LOAD} and v_{out} are of the same sign. From Tables I and II it is seen that none of the MOSFET's intrinsic diodes is activated under this condition. At high power factors, operation with diode recovery only occurs when i_{LOAD} is small, thereby reducing the necessity for the deactivation networks around TR1 and TR4. However, in, for example, vehicle charging or V2G applications [37], operation is always or frequently as an ac to dc converter with consequent intrinsic diode recovery.

If L_s is low, this has the advantage that the power transfer given by (3) tends to zero, with a consequent reduction in losses in the inductor energy recovery circuitry. However, a larger peak current (I_{pk}) appears in N at the instant when most of Q_{oss} has been supplied and C_{oss} then rapidly falls. Disadvantages include higher peak voltages across power devices and increased EMI. The snubber inductors introduce leakage inductances into paths that undergo rapid current changes. Although not included here, in [17] the resulting over-voltages across the power devices were effectively clamped using simple low-loss RCD circuits.

The inferred power dissipation of the devices on the heatsinks shows good agreement with the calculated value, although losses in the individual devices have not been experimentally apportioned. Dividing the total loss of devices on the heatsinks (17.3 W) by three gives a loss of 5.77 W, close to the predicted loss of 5.59 W. Individual losses in the inductor cores, windings and reset diodes are not experimentally apportioned. However, aggregate losses are inferred at 0.97 W from the shortfall in the measured power dissipation in the dump resistor when compared to the expected energy transferred through the inductors. We have assumed a modest 75% efficiency for the SMPS stage. Adding the measured losses from the devices on the heatsinks of 17.3 W, the inferred aggregate loss in the inductor cores, windings and reset diodes of 0.97 W, and the expected SMPS loss of 0.77 W yields a total loss of 19.04 W. An efficiency of 99.3% is therefore estimated. However, losses not included here are those in the PCB tracking, those in the auxiliary MOSFETs and diodes, and losses due to ripple current in the decoupling capacitors. Also, other losses, for example, in gate driver circuitry and EMC filter circuitry, would normally be accounted for in a production unit.

The efficiency of an NPC three-level converter using IGBTs switching at 20 kHz is given at approximately 98.8% in [38]. By using SJ devices and increasing efficiency to 99.3% a reduction in losses of 42% is attained. While SJ devices are costlier than IGBTs and ancillary circuitry is required in a VSC application, several system-level benefits result. The lifetime cost in lost energy is reduced. Where forced cooling is dispensed with, the cost of fans or pumps is avoided. Furthermore, the parasitic power consumption of these items is eliminated, as is the need to provide them with a low-voltage power supply. The reliability and servicing costs of forced cooling systems are avoided. In applications where forced cooling is undesirable or impermissible, smaller heatsinks may be used with a consequent reduced overall mass and bulk. This is particularly advantageous in aerospace power systems. High efficiencies are also attainable with SiC devices, but these are costlier than SJ devices and, in the case of SiC MOSFETs, there are concerns over gate oxide behavior [39].

VII. Conclusion

Silicon super-junction MOSFETs can be readily deployed in a three-level neutral point clamped converter provided the behavior of the intrinsic diodes in the outer devices and charging of the output capacitances of all the MOSFETs is addressed. 99.3% efficiency has been estimated in a naturally-cooled converter operating from a 720-V dc rail, switching at 20 kHz, and supplying 3 kVA. Target applications are where forced cooling is undesirable or not possible, and low losses are consequently essential to reduce cooling requirements.

Appendix

Loss formulas for one phase-leg are given in this Appendix. Values are calculated for a 1-kVA unity power factor load.

A. Conduction Loss in Main Outer Switches (TR1 and TR4)

As i_{LOAD} is 4.35 A, its peak value, I_p, is 6.15 A. v_{out} is 230 V (phase) and its peak phase value, V_p, is 325 V. The effective input voltage for calculating duty cycles is half of 720 V, at 360 V. The total on-state loss in TR1 and TR4 is given by

$$w(t) = i^2_{\mathrm{LOAD}}(t) R_{\mathrm{DS(on)}} \delta(t). \tag{A1}$$

$i_{\mathrm{LOAD}}(t)$ is given by

$$i_{\mathrm{LOAD}}(t) = I_p \sin(\omega t - \varphi) \tag{A2}$$

where φ is the phase angle of i_{LOAD}. $\delta(t)$ is given by

$$\delta(t) = \frac{v_{\mathrm{out}}(t)}{V_{\mathrm{in}}} = \frac{V_p}{V_{\mathrm{in}}} \sin \omega t. \tag{A3}$$

The modulation depth, M, is defined as

$$M = \frac{V_p}{V_{\text{in}}}. \tag{A4}$$

Hence, $\delta(t)$ may be expressed as

$$\delta(t) = M \sin \omega t. \tag{A5}$$

The results from (A2) and (A5) are put into (A1) and W_{ave} is then derived as

$$W_{\text{ave}} = \frac{R_{\text{DS(on)}} I_p^2 M}{12\pi} \times [12 + 4\cos 2\varphi]. \tag{A6}$$

$R_{\text{DS(on)}}$ for TR1-4 is taken as 80 mΩ. This was estimated from [26] as being the approximate value at a junction temperature of 60 °C. Putting values into (A6) gives a loss of 1.11 W.

B. Switching Loss in Main Switches (TR1-4)

Each switching cycle a power device is switching i_{LOAD} on and off. Which device switches depends on the direction of i_{LOAD} and whether the transitions are between H and M or between M and L. The total loss is independent of φ and is given by

$$W_{\text{ave}} = \frac{(t_r + t_f) f_{\text{sw}} V_{\text{in}} I_p}{\pi} \tag{A7}$$

where t_r is the rise time and t_f is the fall time. The total switching loss in TR1 and TR4 is given by

$$W_{\text{ave}} = \frac{(t_r + t_f) f_{\text{sw}} V_{\text{in}} I_p}{2\pi} \times (1 + \cos \varphi). \tag{A8}$$

The total switching loss in TR2 and TR3 is given by

$$W_{\text{ave}} = \frac{(t_r + t_f) f_{\text{sw}} V_{\text{in}} I_p}{2\pi} \times (1 - \cos \varphi). \tag{A9}$$

t_f and t_r are each estimated at approximately 40 ns by observation. Putting the values into (A8) and (A9) gives 1.02 W and 0 W, respectively. Due to the self-snubbering action of C_{oss}, turn-off losses may be over-estimated.

C. Self-Discharge Loss in TR1 and TR4

The data in [27] gives C_{oss} for v_{DS} between 0.1 V and 100 V. We have derived a QV curve from this data and linearly extrapolated the curve to 360 V at the gradient (capacitance) observed at 100 V. The stored energy is estimated at 16.1 μJ. Multiplying this by the switching frequency of 20 kHz yields a power dissipation due to self-discharge of 322 mW.

D. Conduction Loss in TR2 and TR3

This is calculated from

$$W_{\text{ave}} = i_{\text{LOAD}}^2 R_{\text{DS(on)}}. \tag{A10}$$

Putting values into (A10) ($R_{\text{DS(on)}} = 80$ mΩ) yields 1.51 W.

E. Conduction Loss in D5 and D6

This is calculated from

$$w(t) = V_f i_{\text{LOAD}}(t)\,(1 - \delta(t))\,. \tag{A11}$$

Putting the results from (A2) and (A5) into (A11) yields

$$w(t) = V_f I_p \sin(\omega t - \varphi) \times (1 - M \sin \omega t). \tag{A12}$$

The average value derived from (A12) is

$$W_{\text{ave}} = \frac{V_f 2 I_p}{\pi} + \frac{V_f I_p M}{4\pi}[(4\varphi - 2\pi)\cos\varphi - 4\sin\varphi]\,. \tag{A13}$$

The diode forward voltage drop, V_f, is estimated at 1.3 V from [29]. Putting this and other values into (A13) yields 1.63 W.

F. Conduction Loss in Auxiliary Switches (TR1a and TR4a)

This was calculated from (A6), but with the $R_{\text{DS(on)}}$ value for the auxiliary MOSFETs entered. This was estimated at 4 mΩ at a junction temperature of 60 °C from the data in [28]. Putting the values at unity power factor into (A6) yields 0.06 W.

G. Dead-Time Loss in D1a and D4a

This is calculated from

$$w(t) = 2 V_f i_{\text{LOAD}}(t) T_{\text{dead}} f_{\text{sw}} \tag{A14}$$

where T_{dead} is the dead-time. Averaging the integral of (A14) between the appropriate limits yields

$$W_{\text{ave}} \frac{4 V_f T_{\text{dead}} f_{\text{sw}} I_p}{\pi}. \tag{A15}$$

Putting $T_{\text{dead}} = 690$ ns and $V_f = 1.3$ V into (A15) gives 0.14 W.

H. Conduction Loss (L_{s1} and L_{s2})

This is given by (A6), but with R_w substituted for $R_{\text{DS(on)}}$

$$W_{\text{ave}} = \frac{R_w I_p^2 M}{12\pi} \times [12 + 4\cos 2\varphi]. \tag{A16}$$

Putting the values into (A16) ($R_w = 10.4$ mΩ) yields 0.15 W.

I. Core Loss (L_{s1} and L_{s2})

The loss density for the -8 material was estimated at 416 mW/cm^3 from the curve-fit formula in [30]. This was then multiplied by the effective volume of the T80-8/90 core (1.19 cm^3) to yield a loss of 495 mW. The peak ac flux density excursion entered was 88 mT, that is, the value when i_{LOAD} is at its peak level. The frequency entered was 20 kHz. However, this is only the frequency of the fundamental component of the flux density excursion and there is a high harmonic content. On the other hand, the peak i_{LOAD} was used.

J. Reset Diode (D_r) Loss

Before calculating reset circuit losses, the energy transferred out of N_r is calculated. Putting the data into (2) gives 2.16 W. The power transferred through L_s due to forcing i_{LOAD} into it or commutating i_{LOAD} is given by (3). Where i_{LOAD} varies sinusoidally, the average power transfer is given by

$$W_{\mathrm{ave}} = \frac{f_{\mathrm{sw}} L_s I_p^2}{2\pi} \int_0^{\pi} (\sin \omega t)^2 d\omega t. \qquad \text{(A17)}$$

Putting the data into (A17) gives 925 mW. Adding the results from (2) and (A17) gives 3.09 W. If this is transferred into V_{reset}, then the average current through D_r into a 25-V reset voltage is 124 mA. If D_r's forward voltage drop is taken as 1.3 V, this gives a loss of 161 mW. Losses in L_s are neglected in estimating the power transferred through D_r.

K. Losses in SMPS

A modest 75% efficiency is assumed for the SMPS. This gives a loss of 773 mW with an input power of 3.09 W. Losses in L_s and D_r are neglected in estimating the power transferred into the SMPS.

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