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High Efficiency Bidirectional 5kW DC-DC Converter with Super-Junction MOSFETs for Electric Vehicle Super-Capacitor Systems

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Abstract—This paper presents a high efficiency 5-kW bidirectional DC-DC converter for use in electric vehicle super-capacitor systems. Super-junction MOSFETs are deployed in the power stage to minimize losses. This is achieved using a snubber inductor and by arranging the gate signal underlap delays in order to control charging current caused by the devices' highly non-linear output capacitance and to deactivate the intrinsic body drain diode respectively. The result is a 5-kW power converter with an estimated efficiency exceeding 99% in the power semiconductor stage and requiring no forced cooling.

I. INTRODUCTION

In electric vehicles, regenerative braking produces significant quantities of energy, which must be stored quickly and efficiently. Typical batteries and fuel cells are unable to satisfy this requirement and therefore super-capacitors are often employed. A DC-DC bi-directional voltage-source converter transfers power between the super-capacitor bank and the high voltage traction drive supply rail [1]-[4].

The optimization of power converter design in order to achieve high efficiencies is very important in automotive applications. High efficiencies bring a number of benefits, which include greater reliability due to reduced power device temperature excursions, a reduction in the size of the converter and lower energy consumption. At voltages greater than 200 V IGBTs have traditionally been the favored devices, however the development of super-junction and wide bandgap technology has made MOSFETs suitable candidates at these higher voltages. Super-junction MOSFETs have a very low $R_{DS(on)}$ and reasonable cost which makes them an attractive alternative if high efficiencies are to be achieved. However, their application in voltage source converters (VSCs) is impeded by two inherent problems. Their body drain diode has an extremely poor reverse recovery behavior and their output capacitance, C_{oss}, is highly non-linear. Both of these issues cause an increase in the overall switching loss for the MOSFETs and must be addressed before they can be deployed in VSCs.

Alternatively, wide bandgap devices have a low C_{oss} and suffer from virtually no reverse recovery, however they are significantly more expensive than silicon devices.

In order to address the challenges of using super-junction MOSFETs in VSCs, additional circuit elements and control strategies must be used. In the literature linear inductive snubbers [5], auxiliary resonant half-bridges [6], maximum efficiency point tracking (MEPT) [7], series MOSFETs for body diode deactivation [8] and MOSFET gate drivers with forced-commutation circuitry [9] incorporated are techniques which can be employed to address these issues. Each has their limitations, for example, the power devices in auxiliary half-bridge legs have to be able to support the whole rail voltage. Additionally the use of series MOSFETs, requires additional switching devices in the power stage. These additional devices cause an increase in cost, converter size and losses.

Maximum efficiency point tracking (MEPT) can be used to optimize dead times and deactivate the intrinsic body drain diode of a MOSFET. MEPT is a software based control method which can reduce the complexity of the hardware but increases that of the control strategy. However, in applications where digital signal processors are required, such as for regulating the currents in the phases of an interleaved converter, this only requires limited additional software to implement both control techniques. Importantly, MEPT alone does not address C_{oss} charging. The C_{oss} characteristic of super-junction devices is considerably more adverse than that of devices designed for lower voltages. In circuitry using super-junction MOSFETs, MEPT must therefore be applied in conjunction with another technique in order to resolve this issue. In this paper a bidirectional DC-DC converter is proposed which uses an inductive snubber to provide data for informing the development of an MEPT control strategy.

II. PROPOSED ARRANGEMENT

Fig. 1 shows the proposed bridge leg arrangement. The snubber inductor L_s controls the flow of intrinsic diode
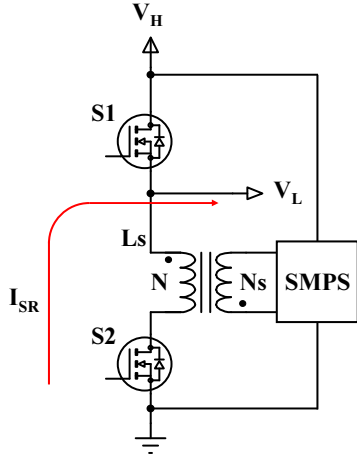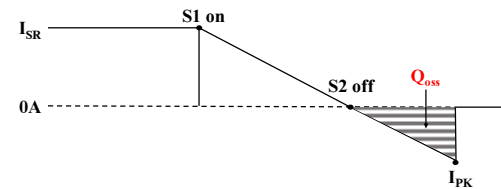
Figure 1. Proposed bridge leg arrangement.

recovery charge (Q_{rr}) or the charge (Q_{oss}) into the output capacitance (C_{oss}) of S1 and S2, depending on the direction of power flow. In doing so, energy is stored in L_s.

This energy can be recovered by means of a secondary winding, N_s, on L_s. The energy thus recovered can then be transferred back to a suitable rail voltage by means of an SMPS. Operation is considered where it is operating in the buck mode and S2 is acting as the synchronous rectifier. As in [5], the QV characteristic of the MOSFET is taken as rectangular. That is, nearly all the charge, Q, is drawn at a very low voltage before C_{oss} collapses abruptly and effectively commutates the current into the device.

Representative waveforms of the current through S2, I_{SR}, are shown in Fig. 2 for four different switching scenarios. As
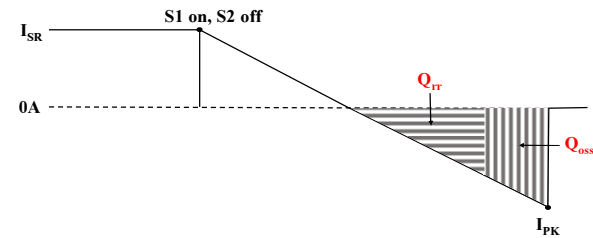
shown, the point at which S2 turns off has a significant effect on the peak current sourced into it at commutation. The magnitude of the peak current, I_{pk}, is important as it determines the power, W, transferred through the snubber inductor and also the peak voltages across the power devices during transients when I_{pk} is commutated. With the exception of the scenario in Fig. 2d, W is calculated from:
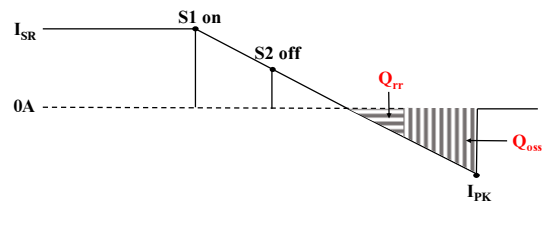
$$W = V_{RAIL} Q_t f \qquad (1)$$

where V_{RAIL} is the supply voltage, Q_t is the combined Q_{rr} and Q_{oss} charges and f is the switching frequency.

The MOSFET's reverse recovery charge is supplied first during the period when the potential across the device is between a negative and a low positive value. Q_{oss} is then supplied after this as the voltage increases.

Fig. 2a shows the effect of switching the SR MOSFET off before the current has reduced (too much dead time) and thus the intrinsic diode conducts the full load current. The full reverse recovery charge must be supplied along with that required to charge the output capacitance, Q_{oss}. If the device is turned off at any point before I_{SR} begins to fall the same quantity of load current will pass through the intrinsic diode and the losses associated with switching therefore will not change significantly. Additional conduction losses will, however, be experienced due to the losses of its intrinsic diode being larger than those when the channel of the device is enhanced.

Fig. 2b shows a reduction in I_{pk}. This is due to the SR MOSFET switching off when the current through it has decreased below the full load current. The underlap has reduced to the point where both devices are conducting at the

a) SR device switches off before I_{SR} has started to drop thus intrinsic diode conducts full load current.

b) SR device switches off after I_{SR} has started to drop and intrinsic diode conducts partial load current.

c) SR device switches off at the optimum point achieving complete diode deactivation thus only Q_{oss} has to be sourced.
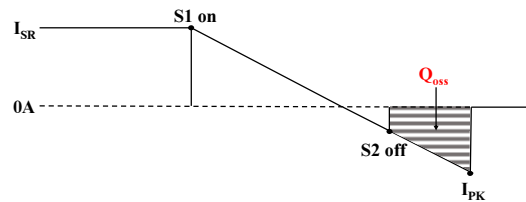
d) SR device switches off after current through it has reversed causing an increase in I_{PK}.

Figure 2. Representative I_{SR} waveforms for four different switching scenarios.

same time, that is, overlap has been introduced. As the current conducted by the intrinsic diode has reduced, the reverse recovery charge has also decreased. The reverse recovery charge required for a given current, I_{SR}, is device specific and this relationship can be expressed by:

$$Q_{rr} = k_{rr}I_{DR} \qquad (2)$$

where k_{rr} is the gradient of a line plotted between Q = zero (at 0 A) and the device's quoted Q_{rr} supplied on the datasheet for a given forward current, I_{DR}, prior to commutation. However, the reverse recovery charge, Q_{rr}, used in datasheets is effectively the combined values of Q_{oss} and Q_{rr} and can be written as:

$$Q_t = Q_{oss} + k_{rr(2)}I_{DR} \qquad (3)$$

where $k_{rr(2)}$ is a modified coefficient to account for the presence of Q_{oss}. The rate of change of current is determined by the inductance of L_s and the supply voltage, and can be determined by:

$$V_{RAIL} = L_s \frac{dI}{dt} \qquad (4)$$

Rearranging (4) in order to find the current flowing through the intrinsic diode of the MOSFET at turn-off gives:

$$I_{SR} = \frac{V_{RAIL}t_u}{L_s} \qquad (5)$$

where t_u is the underlap delay with respect to the 0-A point. Combining (3) and (5) gives:

$$Q_t = Q_{oss} + k_{rr(2)}\frac{V_{RAIL}t_u}{L_s} \qquad (6)$$

I_{pk} can then be calculated using:

$$I_{pk} = \sqrt{\frac{2V_{RAIL}Q_t}{L_s}} \qquad (7)$$

Equating (6) and (7) gives:

$$I_{pk} = \sqrt{\frac{2V_{RAIL}}{L_s}\left(Q_{oss} + k_{rr(2)}\frac{V_{RAIL}t_u}{L_s}\right)} \qquad (8)$$

Fig. 2c shows the effect of switching off the SR MOSFET at the optimum point (at I_{SR} = 0 A). Only the Q_{oss} of the device must be supplied as the intrinsic diode is now deactivated. At this point I_{pk} is at its minimum and this is the circuit's most efficient operating point. If the device is switched off later than this point, Fig. 2d, the peak current is increased as the Q_{oss} must still be charged, but the charging profile becomes trapezoidal as shown as, prior to S2 turn-off, C_{oss} cannot begin to charge. As, ideally diode reverse recovery charge is eliminated, the equation for the region to the right of the 0-A crossing point, is different to (8). I_{pk} when the intrinsic diode has been deactivated is:

$$I_{pk} = \sqrt{\frac{2V_{RAIL}Q_{oss}}{L_s} + \frac{V_{RAIL}^2 t_o^2}{L_s^2}} \qquad (9)$$

where t_o is the overlap time. It is noted that energy is also transferred through L_s when current is initially forced into it. The power, W_2, transferred due to this action has to be added to that determined from (8) or (9) and is given by:

$$W_2 = \frac{fL_s I_{LOAD}^2}{2} \qquad (10)$$

III. EXPERIMENTATION

The experimental converter, Fig. 3, transfers power between a 400-V DC bus, V_H, and a 200-V DC bus, V_L. The current into V_L is 25 A, resulting in 5 kW being transferred. The switching frequency is 25 kHz. Each of the switch positions in the bridge leg is occupied by three super-junction MOSFETs connected in parallel, shown mounted on the heatsink in Fig. 3. The device selection was optimized in order to choose a suitable SJ MOSFET trading off between its $R_{DS(on)}$ and C_{oss} in order to minimize losses based on the use of the snubber inductor and MEPT techniques. Various combinations of paralleled devices and also different MOSFETs were analyzed to determine the optimum combination which will achieve the least losses for an appropriate price. This was done instead of using a traditional figure of merit due to the ability of the snubber to regenerate the losses attributed to charging the devices' C_{oss}. TK62J60W MOSFETs [10] were selected for S1-S6. 8-Ω series gate resistors were used for the six devices in order to achieve suitable switching rise and fall times. The TK62J60W MOSFET has $R_{DS(on)}$ = 33 mΩ. The Enguage Digitiser program [11] was used to calculate Q_{oss} by capturing the QV curves from the manufacturers' capacitance graphs. A Q_{oss} of 1.4 μC is expected for three devices in parallel. From the datasheet a total reverse charge of 7 μC is given when a current of 30.9 A in the intrinsic diode is commutated. Accounting for the inclusion of Q_{oss} in this charge, $k_{rr(2)}$ is estimated at 211 ns.

The snubber inductor, L_s, and reset circuitry are situated in front of the MOSFETS. L_s was constructed from a Micrometals T130-8/90 toroidal core [12]. N and Ns were each of the same number of turns, in this case six, giving a measured inductance of 1.65 μH. The peak AC flux density excursion was calculated to be 77 mT. Stranded wire was used for N to mitigate skin-effect losses and the two
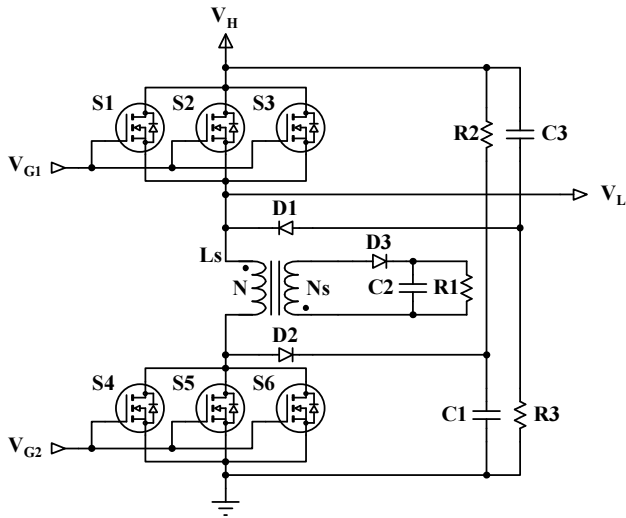
Figure 3. Experimental circuit. Top: schematic diagram. Bottom: Experimental hardware. No forced cooling is required.

windings were evenly distributed around the core to minimize leakage inductances [13]. An SMPS was not commissioned here and, instead, the energy recovered from L_s is dissipated in a 40-Ω dump resistor for experimental purposes. This resistor, R1, is remotely mounted onto another heatsink in order to isolate any thermal effect of the dump losses on the main switching devices. The power dissipated in R1 would typically be returned to the supply via an SMPS as described in [5].

An overvoltage appears across S4-6 at turn off when the reverse charge has been supplied and these devices effectively cut off. Ideally, this overvoltage, V_{os}, is given by:

$$V_{os} = \frac{N}{N_s} V_{reset} \qquad (11)$$

Also, considering buck converter operation only here, an identical overvoltage appears across S1-3 when they turn off and force current into L_s. However, despite its construction, there is inevitably some series leakage inductance between N and Ns. The circuitry formed from R2, R3, C2, C3, D2, and D3 limits the consequent over-voltages.

Fig. 4 shows the calculated voltage across R1 determined using (8), (9) and (10) for varying overlap and underlap. The minimum occurs at the point where diode deactivation occurs without excess shoot-through, Fig. 2c. Losses are lowest here. V was calculated from $V = \sqrt{WR1}$ with W being given by $W = 0.5 \times I_{pk} f + W_2$. It is noted that this assumes all the inductor stored energy is transferred into R1 without losses in, for example, the inductor core being accounted for. Also, above around 100 ns of underlap time, losses are expected to be overestimated as the intrinsic diode current tends to level off, Fig. 2a.
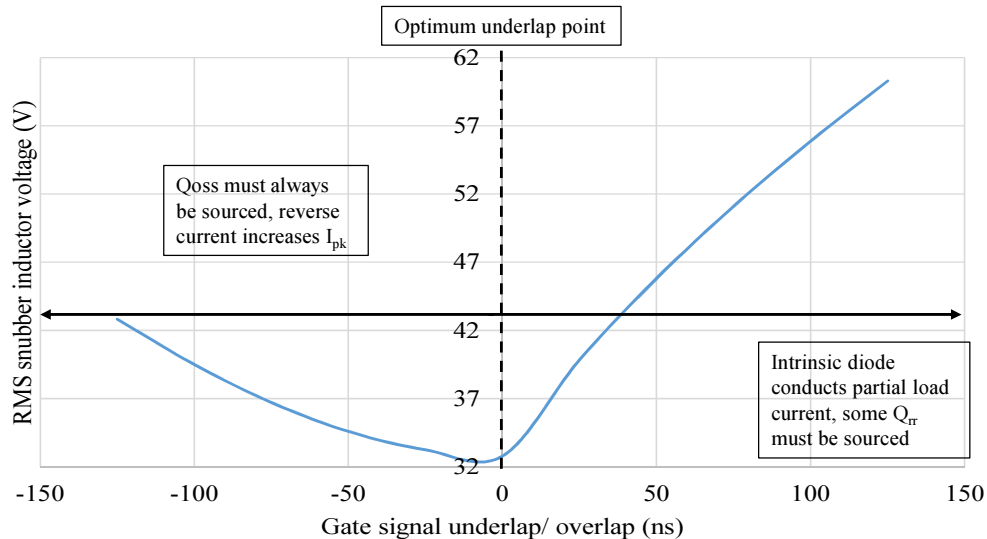

Figure 4. Graph of calculated snubber inductor dump load voltage versus gate signal underlap/overlap (for the S1 on/ S2 off switching transition) showing three of the switching-instance scenarios.
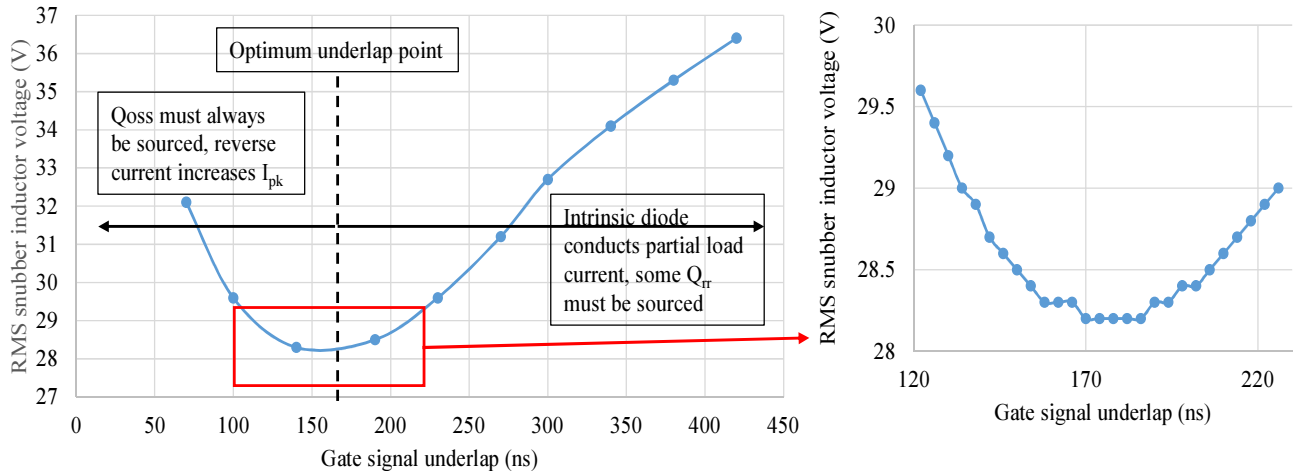
Figure 5. Graph of snubber inductor dump load voltage versus gate signal underlap (for the S1 on/ S2 off switching transition) showing three of the switching-instance scenarios. The inset shows an expanded view of the 0-A I_{SR} cross-over point.

In an open-loop configuration, using a twin channel signal generator, the gate signal delays were adjusted to find the optimum efficiency point. Fig. 5 shows the results of increasing the underlap delay between the control MOSFET turning on and the synchronous rectifier (SR) MOSFET turning off (when operating the bridge leg as a buck converter). The underlap times quoted here are those set on the signal generator and thus the voltage rise and fall times at the device' gate will make the effective values change accordingly. From Fig. 5 the 0-A crossing point of the load current is at approximately 165 ns (the minima in the graphs shown in Fig. 5). At this point the voltage is dependent solely on the energy required to charge the output capacitance, C_{oss}.

The region of the graph below 165 ns shows the effect of decreasing the underlap time past the 0-A crossing point. The voltage increases due to an increase in the current flowing through the primary of the snubber inductor (shoot-though current). The peak current increases as expected and causes additional power to be transferred through the snubber inductor. Shoot-through is normally problematic but the snubber inductor controls this current.

Alternatively, the region above 165 ns up to 420 ns on the graph shows the effect of increasing the underlap time. The voltage rises as the intrinsic diode of the SR MOSFET begins to conduct an increasing quantity of the load current. This in turn draws additional energy from the supply for its reverse recovery and thus causes the increase in voltage measured. Moving to higher values of underlap would cause the graph to plateau once the full load current has been conducted through the intrinsic diode of the SR MOSFET.

The other switching edge delay (between the control MOSFET turning off and the synchronous rectifier (SR) MOSFET turning on) was set to 400 ns. This switching transition is significantly less sensitive to the underlap time applied. This quantity was selected to ensure no shoot-through occurs. As before, shoot-through causes additional losses during this delay period, however when the intrinsic diode conducts there is little effect on the losses. This is due to no reverse recovery being required as the channel of the same device is enhanced after the delay.

Stray inductances are also important. They will prevent instantaneous conduction of the intrinsic diode. This effect is the reason for the U-shape shown in the experimental results compared to the V-shape of those calculated using equations (8) and (9). As the inductance increases, more dead time is required for the diode to start conducting.

The snubber inductor was now modified to achieve lower losses. A second core with the same dimensions as the first, but with a different core material, was used. Higher turns-numbers were used to allow more effective coupling between N and Ns, decreasing leakage inductance and reducing the losses in R2 and R3. The new inductor core was a Micrometals T130-6 toroidal type [14]. N and Ns were, again, each of the same number of turns, in this case 12, giving L_s = 1.38 μH when calculated with the inductance factor of 9.6 nH per turn squared quoted in [14]. The peak AC flux density excursion was calculated to be 45 mT. The modified inductor is shown in Fig. 6 along with the original for comparison.

Figure 6. Photographs of the modified (left) and original (right) snubber inductors.

Fig. 7 and Fig. 8 show the oscilloscope traces of the SR MOSFET drain current waveforms, for the circuit shown in Fig. 3, with and without a snubber inductor respectively. Both figures contain three profiles, one for each of the different quantities of dead time discussed in Fig. 2. To reiterate, these are the cases of where; the delay is too large causing the intrinsic diode of the SJ MOSFET to conduct partial load current, the optimum amount leading to complete diode deactivation and too little leading to shoot-through. A supply voltage of 50 V was used for all six permutations to avoid device destruction in the tests where the snubber inductor was removed. Additionally this voltage gave a clear distinction in the results for the three different quantities of dead time. Note the different time scales and vertical scales used in Fig. 7 and Fig. 8.

The peak current measured, shown in Fig. 7, varies between approximately 35 A and 55 A. The peak occurs within 200 ns which leads to a significant di/dt determined by the stray inductance of the circuit as well as the voltage drop over S1-S3. At the high supply voltage this circuit operates from, this peak would be substantially larger and would be expected to result in device failures along with increased levels of EMI production.

In the results in Fig. 8, the peak current at each dead time is significantly reduced. These current measurements were recorded using a Rogowski coil, which only measures the AC information. The di/dt for this graph is dependent upon the snubber inductance, L_s. The use of a snubber inductor allows these devices to be deployed in high voltage sourced converters.

The circuit with the modified inductor was now run at a supply voltage of 400 V and its full power of 5 kW. The circuit was allowed to reach thermal equilibrium without forced cooling. Fig. 9 shows a thermal image of the circuit where the MOSFET heatsink temperature was recorded at less than 65°C with the converter sourcing maximum power to the load, with an ambient temperature of 29°C.
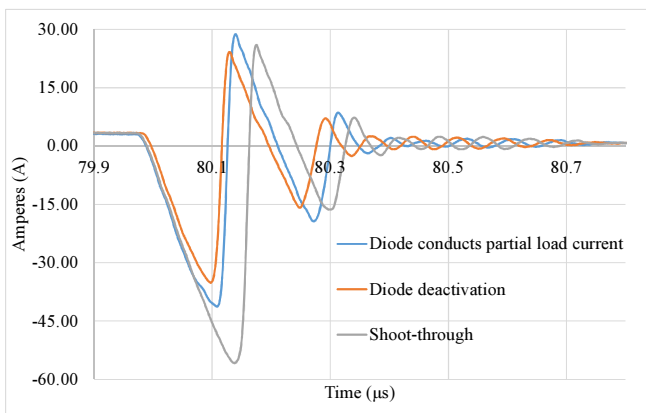

Figure 7. Graph showing the SR drain current measured with a Hall effect current probe. The results for three different quantities of dead time are shown. The circuit operated at a supply voltage of 50-V without a snubber inductor.
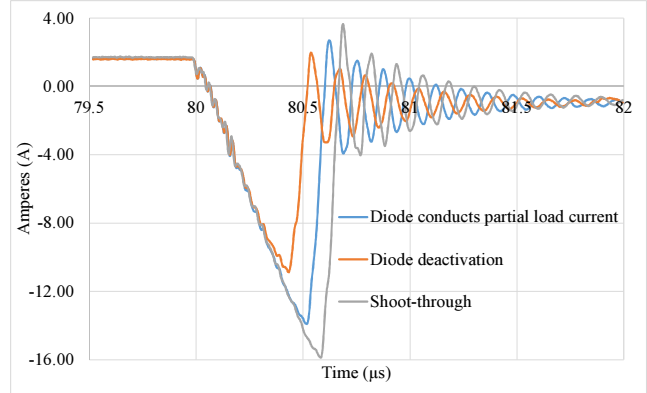

Figure 8. Graphs showing the SR drain current profiles (captured with an oscilloscope using a Rogowski coil) for the circuit with the use of a snubber inductor. Three similar dead times were used and a 50-V supply voltage was applied.

A breakdown of the losses is shown in Table 1. The losses attributed to the MOSFETs were estimated using thermal superposition. Prior to obtaining these results a known power was dissipated into the heatsink to determine its thermal resistance under natural convection. Once thermal equilibrium had been achieved, the thermal resistance was calculated to be 2.22°C/W. The reset losses were calculated using the measured snubber inductor reset voltage and dump resistance value. Losses in the reset diode D1 were estimated from the forward voltage drop obtained from its datasheet. The overvoltage clamp losses were also measured, the variation between the two losses shown in Table 1 for the overvoltage clamp circuits is expected due to the asymmetric nature of their operation here. Finally, the snubber inductor losses were pessimistically estimated at 6.5 W by modelling the snubber inductor volume and its average measured temperature using finite element analysis. The efficiency of the power semiconductor stage is conservatively estimated to be 99.1%. Deploying a modest efficiency SMPS into the snubber inductor reset circuitry would also recover a significant quantity of the 20.02 W dumped in R1.
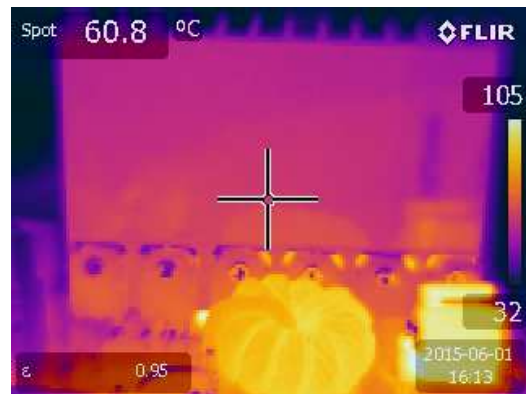

Figure 9. Thermal image of the hardware operating at its rated output power once it has reached thermal equilibrium. The MOSFET heatsink shows a temperature of 60.8°C, the snubber inductor core was measured at 90°C and the ambient temperature was measured at 29°C. The circuit was run on the flat surface in Fig. 3 and no forced cooling was applied.

TABLE I.   ESTIMATED LOSSES FOR THE EXPERIMENTAL HARDWARE.

Device	Loss (W)
Switches S1-S6	14.31
Reset circuit (diode, D1)	1.08
Reset circuit (dump resistor, R1)	20.02
Snubber inductor, L_s	6.5
Over voltage clamp resistor (R3)	0.19
Over voltage clamp resistor (R2)	2.62
Total	**44.72**

IV.   COMPARISON WITH CIRCUIT USING IGBTs

For comparison, a half bridge was constructed using IGBTs with Co-Pack diodes. Six IKW20N60T devices, three in parallel in the upper and lower positions of the bridge leg, were installed on to the same PCB as used in the experiment, outlined above, and attached to the previously characterized heatsink. As forced cooling would be required for these devices, a fan was positioned facing the converter. The circuit and fan positions were marked out in order to ensure repeatability. A second thermal superposition test was carried out and the thermal resistance of the heatsink was recalculated to be 0.552°C/W with forced cooling. Fig. 10 shows a photograph of the circuit and a thermal image under full-load. This was then placed at the same location inside a safety box which had been marked out with tape to ensure accuracy of the results.
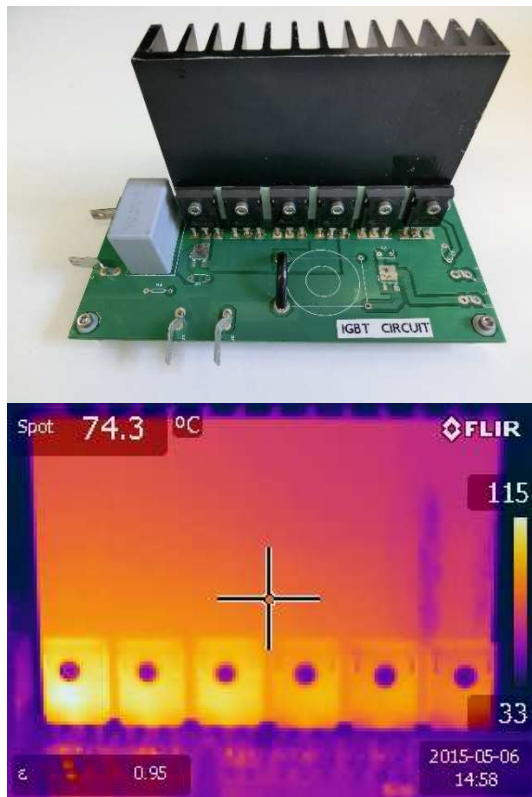

Figure 10. Top: Photograph of the IGBT half bridge constructed using the same PCB and heatsink as that in the previous experiments. Bottom: Thermal image. Forced-cooling is applied.

The dead time was set to 500 ns and the circuit was connected to the 400-V supply. The quantity of dead time does not have any significant effect on the losses here and was simply set to avoid shoot-through. A switching frequency of 25 kHz was used, as in the previous experiment. The duty cycle was again approximately 50% to maintain an output power of 5 kW. The heatsink measured 41ºC above ambient with forced cooling, which equates to a combined switching device loss of 74 W. As shown by the thermal image in Fig. 10, the load sharing is significantly reduced when using IGBTs connected in parallel which is discussed in the literature [15]. For assessing losses, the measurement point selected on the heatsink was the same for both experiments. Comparing the results from the MOSFET and IGBT variants, the efficiency savings are significant.

V.   CONCLUSIONS

A bidirectional DC-DC converter has been constructed and assessed in an open-loop configuration to evaluate the concepts laid out in this paper. Adjusting the overlap between the switching transitions of the two devices in the bridge leg has been shown to have a significant effect on the losses in the circuit. Although additional circuitry is required when using the SJ MOSFETs, important system-level benefits are attained. The heatsink required for the IGBT circuit would be considerably larger than that required by the MOSFETs if natural convection were used. A minimum loss point has been found where the circuit operates at an efficiency greater than 99% and requires no forced cooling. A loss vs. duty function has been experimentally determined that can be used to inform the design of a system with maximum efficiency point tracking.

VI.   ACKNOWLEDGMENT

VII.   REFERENCES

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