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Electric Field Reduction in C-doped AlGaN/GaN on Si High Electron Mobility Transistors

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***Abstract*—It is shown by simulation supported by experiment that a reduced surface field (RESURF) effect, associated with compensated deep acceptors, can occur in carbon doped GaN-on-Si power switching AlGaN/GaN transistors, provided there is a vertical leakage path from the 2DEG to the carbon doped layer. Simulations show that this effect is not present in devices using iron doped GaN buffers explaining the higher voltage capability of carbon doped devices.**

***Index Terms*—Field effect transistors, HEMTs, microwave transistors, power transistors.**

I. Introduction

HEMTs based on the GaN/AlGaN materials system are rapidly becoming the semiconductor device of choice for RF and power switching applications. These devices require a semi-insulating buffer to suppress leakage and punch-through. RF devices frequently make use of iron (Fe) doping to render the GaN insulating, but for the higher voltages required for many power switching applications, it has been found that carbon (C) doping delivers higher breakdown voltage and lower off-state leakage [1, 2]. Unfortunately it has also been found that using carbon can result in a transitory increase in R_{ON}, also known as current-collapse (CC), when switched from the off to the on-state[2, 3]. With field plates now universally used to control surface effects, it is clear that the remaining CC in these devices mostly results from charge storage in deep levels in the buffer. Our previous studies have shown that the difference in CC between Fe and C doping results from their acceptor trap levels pinning the bulk Fermi level in the upper and lower halves of the bandgap respectively [4]. GaN:C is p-type with its low hole density, and hence high resistivity, giving long time constants for charging processes (a hole density of only 10^4cm^{-3} was inferred in [5]). The GaN:C is isolated from the 2DEG by a reverse biased P-N junction, however it has been shown that a non-Ohmic band-to-band leakage path exists through this junction[5, 6], for example by a trap-assisted-tunneling process along dislocations[7] although other mechanisms are also possible. This leakage path allows the potential in the GaN:C layer to roughly follow the 2DEG potential and reduces the back-bias induced CC[8]. However to date, there has been no explanation as to why C conveys an advantage over Fe in breakdown voltage. In this letter, we use simulation, supported by dynamic R_{ON} measurement, to show that another consequence of this vertical leakage path in compensated C-doped GaN is a reduced surface electric field (RESURF) effect [9]. RESURF effects increase breakdown voltage, however their applicability to C-doped GaN-on-Si devices has not been realized before. We also show that this effect is not available in Fe doped buffers, providing a natural explanation for the enhanced breakdown performance of C-doped buffers.

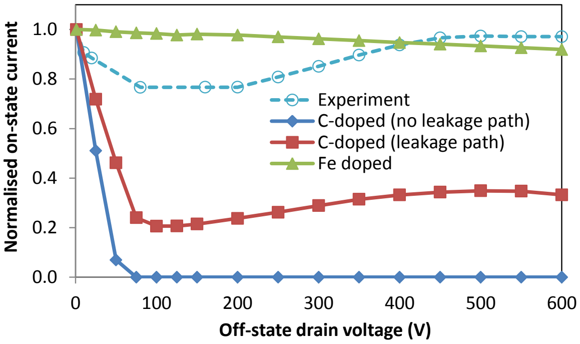

Fig. 1. Dashed line: Normalized current-collapse magnitude for a C-doped AlGaN/GaN device 1s after turn-on following 1000s at the indicated off-state voltage. Solid lines: simulated CC for a similar geometry source-field-plated device with the indicated buffer doping.

II. Experiment

Dynamic on-resistance (CC) measurements were undertaken on AlGaN/GaN-on-Si MISHEMTs fabricated as part of a 650V power device development [10]. These devices have a GaN buffer consisting of an undoped channel region on a carbon doped layer, grown on a semi-insulating strain relief layer on Si. The HEMT tested had a gate-drain spacing of 15µm and V_P=−8V. It was biased in the off-state with V_{GS}=−10V and varying V_{DS} for a time period of 1000s before

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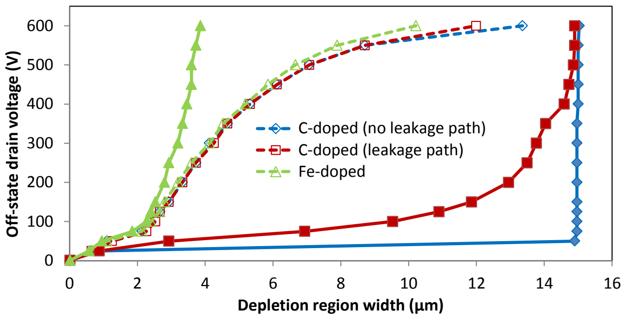

Fig. 2. Simulated length of the off-state depletion region at the drain side of the gate foot as a function of V_{DS} in the off-state. The simulations are shown either 1µs after pulsing from the on-state (dashed) or in equilibrium (full line).

pulsing to the on-state with V_{GS}=0V, V_{DS}=1V. Each on-state current, I_{Don}, was then recorded for 1000s allowing the device to return towards equilibrium. The experimental off-state bias dependence of the normalized initial I_{Don} is shown in Fig. 1. The key observation is that the magnitude of the CC reached a maximum at ~ 100V and then recovered.

Ramped substrate bias measurements were used to extract the vertical I-V characteristics of the layers making up the structure and are reported in [11]. This powerful technique uses the conductivity of the 2DEG as a probe of the electric field in the buffer. Varying the ramp rate and noting any deviation from the prediction of capacitive coupling between Si and 2DEG allows the sign of charge storage to be inferred[5, 6]. Here the important result is that these devices showed hole trapping indicating the presence of a non-Ohmic vertical leakage path between the 2DEG and the C-doped layer, similar to our earlier work [6].

III. Simulation and Discussion

Simulated HEMT devices were modeled using Silvaco ATLAS using the approach described in [4, 5]. They had L_{GD}=15µm and source field plate length 2µm. The buffer had an undoped channel, a doped GaN layer, and the strain relief layer was implemented using undoped AlGaN. The Si was treated as an electrode. For the GaN:C buffer, we used 10^{19}cm^{-3} acceptors 0.92eV above the valence band, and assumed significant auto-compensation by 3x10^{18}cm^{-3} shallow donors [12], giving a free hole density of 4x10^{3}cm^{-3}. The vertical band-to-band leakage path between the 2DEG and the GaN:C is difficult to directly simulate and so was represented using the approach of [5] by providing a narrow heavily doped p-type “short” between the Ohmic metal and the GaN:C located at the outside edge of the source and drain contacts. This approach represents a “worst-case” for CC, and in reality there would be leakage at all points along the channel. Simulations with or without this leakage path were undertaken. For GaN:Fe, acceptors 0.7eV below the conduction band were used[13]. Since the GaN:Fe was n-type, no P-N junction was present and so no leakage path was required. In all cases, cross-sections of 10^{-13} and 10^{-15}cm^{2} for hole and electron capture were used but had essentially no influence since the rate limiting step was transport in the highly resistive layers rather than the trapping process itself.

The simulated drain bias dependences of the CC magnitude are shown in Fig. 1. The Fe doped device showed only a small CC whereas the C-doped device without leakage showed a huge CC consistent with [4], both monotonically increasing with drain bias. By contrast the C-doped device with leakage showed a maximum in the CC exactly like the measurements (Fig. 1) and occurring at a similar voltage of 100V, although with larger magnitude (discussed later). This is consistent with our earlier result that a vertical leakage path is required to simulate C-doped devices[4, 8].

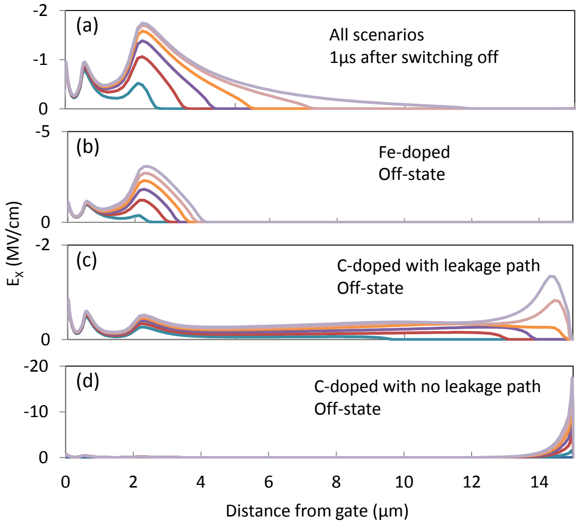

Fig. 3. Channel electric field (E_X) between gate and drain in the off-state for V_{DS} varying from 100 to 600Vin 100V steps. (a) 1µs after switching to off-state (all scenarios were virtually indistinguishable), (b-d) device in equilibrium with the indicated doping.

To help understand the origin of the maximum in CC, Fig. 2 shows the length of the simulated depletion region at the drain side of the gate. Since the resistivity of the doped buffer (Fe or C doped) was so high, 1µs after pulsing from the on-state to the off-state there was very little trapped buffer charge, so the depletion width dependence was essentially independent of dopant (C, Fe) and determined by capacitive coupling. It can be seen that once the depletion region was wider than the source-field plate, it increased in width more quickly than the normally assumed square root of drain bias as a result of Si substrate back-biasing. However once the buffer came into off-state equilibrium (~0.1s for Fe doping and 10^{5}s for C doping), the Fe doped device showed only a small depletion width, whereas the C-doped devices showed rapid depletion across the gate-drain gap.

The consequences for the channel electric field are shown in Fig. 3. Very similar results were seen for all three scenarios 1µs after switching to the off-state (Fig. 3a), a maximum field of 1.7MV/cm was seen, with depletion of the entire gate-drain region starting to occur at 600V as a result of back biasing from the Si substrate. However, in equilibrium the Fe doped device had an increased peak field of 3.1MV/cm at 600V (Fig. 3b). By contrast the leaky C-doped device (Fig. 3c) had a strongly reduced field of mostly ~0.6MV/cm with signs of drain breakdown only close to 600V. If the C-doped device had no leakage (Fig. 3d), the field was very strongly enhanced at the drain terminal reaching 17MV/cm at 600V (although in reality breakdown would have already taken place). It is clear

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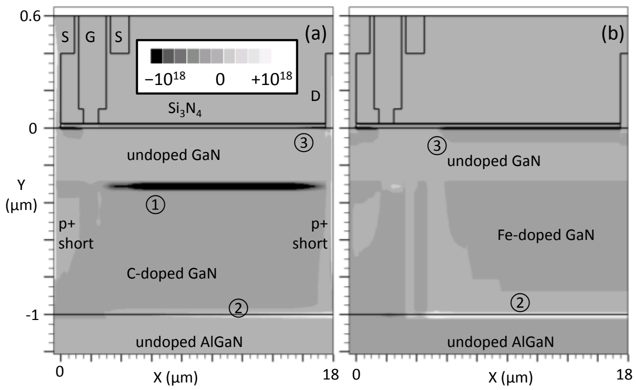

Fig. 4. Net charge density (cm^{-3}) for the GaN buffer region of an off-state source field-plate AlGaN/GaN HEMT with V_{DS}=200V. (a) C-doped buffer with leakage paths, (b) Fe doped device. Black corresponds to negative and white to positive charged regions.

that C-doping, provided there is a vertical leakage path, can dramatically increase lateral breakdown voltage.

The breakdown voltage enhancement in C-doped GaN is primarily due to its ability to spread the voltage drop between gate and drain. A key point is that the GaN:C will act as a back gate and in the simulated case pinches-off the 2DEG at about −40V. As V_{DS} is increased, the resistive GaN:C layer acts as a graded back gate so that at 40V pinch-off will first occur at the gate edge and then move towards the drain. The total negative charge at each point along the channel (ie the 2DEG charge + ionized acceptor charge at the top of the GaN:C) is roughly constant, so in the pinched off region the ionized acceptor density is constant. It is this acceptor charge that causes the reduction in I_{Don} and saturates when most of the channel is pinched off. At the bottom of the GaN:C layer, the field from the Si terminates at exposed positive ionized donors, and their density rises linearly from the gate to the drain, and also increases linearly with increasing V_{DS}. It is this increasing positive charge that causes I_{Don} to rise again at V_{DS}>100V, resulting in the maximum in CC. Fig. 4a shows the ionized dopant charge in off-state at V_{DS}=200V. The GaN:C potential gradient results in a negative acceptor charge ①, a gradient in donor charge ② and a depleted 2DEG ③. The matching ionized charged regions, together with the polarization charge and Si substrate, perform a RESURF function. Unlike the normal RESURF structure[14], there is no need to match positive and negative background doping densities, since electrostatics will ionize the traps to match the required densities. The simulated GaN:C region is isolated from the 2DEG by a reverse biased P-N junction so the potential drops roughly linearly from gate to drain, whereas in reality leakage will occur throughout the gate-drain gap and especially near the drain where the vertical field is highest[6]. This would mean that the actual RESURF region would primarily occur near the gate rather than extending throughout the gap as in Fig. 4a, and giving an explanation for the higher CC magnitude simulated. The exact magnitudes of the CC and RESURF will depend on the balance of these leakage paths.

In the case of the Fe doped device, the buffer is not isolated at all from the 2DEG since it is weakly n-type. This means that the buffer potential will very closely follow the 2DEG potential. In Fig. 4b it can be seen that the 2DEG ③ extends most of the way from drain to gate so there is a lateral equipotential in this part of the buffer, insignificant negative depletion charge, but a uniform positive donor charge ②. All the drain voltage is dropped close to the gate, resulting in the high field of Fig. 3b, and a relatively low lateral breakdown voltage.

IV. CONCLUSION

The carbon doped layer in power AlGaN/GaN transistors is highly resistive p-type which when combined with the leakage via defects such as dislocations, gives long charging or discharging times for acceptor traps. This trapped charge in the buffer results in current-collapse, but can significantly reduce surface electric field and can explain the observed enhanced lateral breakdown voltage.

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