Effect of Load Parasitics on the Losses and Ringing in High Switching Speed SiC MOSFET Based Power Converters

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***Abstract* - In this paper the effect of parasitic elements of the load connected to a power converter are considered. For the case of a high switching speed converter the equivalent parallel capacitance of the load or line inductance will cause a potentially large current overshoot, which will in turn lead to increased switching losses. This paper considers the relation between the operating conditions of the converter, such as switching speed, with the loss due to the parasitic elements. The inclusion of a small output filter inductor to reduce the switching loss and ringing is analyzed and a method for calculating suitable component values to reach a desired target performance is presented.**

Keywords — Silicon Carbide, parasitics, output capacitance, ringing, fast switching

I. Introduction

As the advantages of using wide bandgap technologies such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming better understood the number of applications for high performance converters rapidly increases. However, the high switching speed of these devices presents some new and interesting challenges. The increased switching speed is known to increase both radiated and conducted electromagnetic (EM) issues. In addition to this the high switching speeds cause more pronounced interactions between the switching devices and parasitic circuit elements present in the system, necessitating design optimization to a much higher degree than with previous Silicon based technologies [1]. Of particular interest in this work, the high switching speed will mean that the current overshoot associated with charging the loads parasitic capacitances will be increased.

A. Application induced parasitics

When power switching devices are characterized it is often under lab conditions using optimized circuit layouts. The circuit layout is designed to minimize parasitic inductances, often through the use of short cables and traces. The inductors used as the load can often be designed with an intentionally low equivalent parallel capacitance (EPC) [2]. These conditions do not always fairly represent a realistic application; for example in a rectifier circuit the line inductance will have a significant EPC. Motor drive applications where the converter is connected to the load via a long cable will also tend to present a very high EPC to the converter, which has been shown to reduce the overall converter efficiency [3]. At higher switching speeds other smaller parasitic elements will become more important [4]. Usually, the load of a double pulse test circuit can be modelled by a resistor and an inductor, while in a practical application it will be better modelled with a certain amount of EPC. The output capacitance (C_{out}), along with other parasitic components that will influence the converters performance are indicated in Fig 1.

In the case of high switching speed converters, such as those utilizing wide bandgap devices, many aspects of the system design will affect the performance, such as the interaction of the device output capacitances (C_{oss}) and the PCB trace inductances.

B. Hardware discussion

The work in this paper is centered on results taken from the test rig shown in Fig. 2 and Fig. 3. This can be set up to perform numerous tests including both double pulse tests and continuous operation tests. The switching devices used are the Cree C2M0080120D SiC MOSFET. The circuit allows the driving of the MOSFET gates with voltages between -5 V and 20 V using the Microchip TC4452VOA and control of the switching speed by changing of the gate resistance value. In all cases presented the DC-link voltage used was 600 V.

Current measurements are taken using the Agilent N2783A current probe connected to a wire loop in the drain path of the

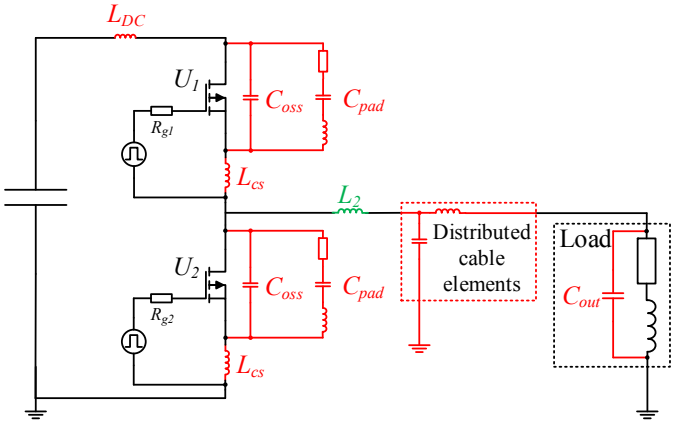

Fig. 1 – Illustration of the location of some of the more critical parasitic elements (Marked red) within a converter phase leg. Including: The DC link inductance (L_{DC}), the device output capacitance (C_{oss}), the common source inductance (L_{cs}), the pad-to-pad capacitance with series inductance and resistance (C_{pad}), the cable elements and the output capacitance (C_{out})

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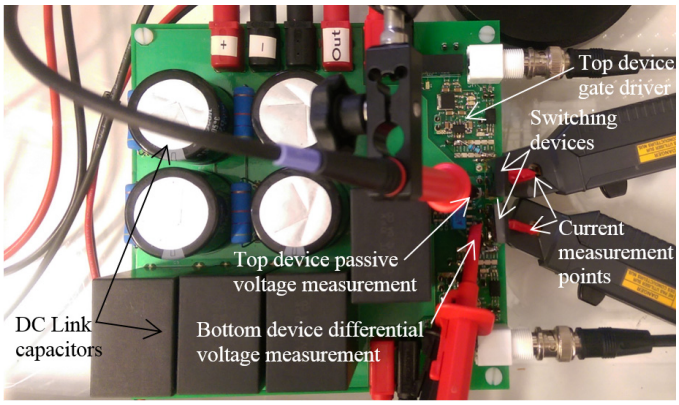

Fig. 2 - Photograph showing the test circuit

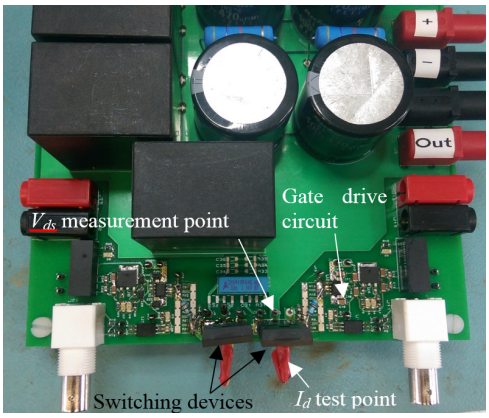

Fig. 3 – Detail view of test circuit – connections removed

device. This is set up with the intention of minimizing the common source inductance by instead introducing the parasitic inductance of the current measurement into the drain path. The design also allows the positive DC link to be grounded which prevents the high side current probe from experiencing a high *dv/dt* during switching which is known to introduce significant measurement noise. The switching speed is controlled by changing the value of the gate resistor. Voltage measurements are taken with a high ratio passive probe (PMK PHV 1000) and a differential voltage probe (PICO TA041) with wires twisted to reduce the noise picked up by the cables.

As the values for motor inductances can vary widely with the motor size, power and design, choosing an inductor which is representative of any general case is difficult. The load used for the experiments is made up of a rheostat and an inductor with values of 10 Ω and 41.7 mH respectively. The equivalent parallel capacitance of the load inductor is 191 pF and that of the resistor is negligible with respect to that of the inductor (<4 pF). The DC resistance of the inductor is 9.73 Ω. In order to allow varying of the inductors EPC provision is made to allow the connection of additional capacitance in parallel with it.

C. *Probe induced parasitics*

When taking measurements in high speed power electronics systems, such as those discussed in this work, it becomes important to consider the effects of the measurement techniques being used to observe the system. Works such as [5] show that a typical oscilloscope probe is far from ideal in its behavior.

In this work three measurement techniques are used; voltage measurement using a passive probe, voltage measurement using a differential voltage probe and current measurement using current probes. Each of these introduces additional elements into the system and also comes with its own set of considerations that will influence the interpretation of the captured waveforms.

The passive voltage probe used introduces a small capacitance across the measurement points. This is quoted as 7.5 pF in the manufacturer's data sheet. The inductance of the ground connection has been minimized as far as possible through the use of a small metal spring which keeps the ground connection very close to the tip.

The differential voltage probe used introduces 7 pF of capacitance between each of its probes and the ground connection. As one of these connections is subjected to a very high *dv/dt* the current admitted by the capacitance will be significant when compared with the current into other capacitive elements.

Finally, the use of current probes in this set up requires two considerations to be made. Firstly the physical dimensions of the probe head are quite large. This forces the use of extended conductors in the critical current loop of the circuit. Each current measurement point is estimated to contribute around 39 nH of inductance to the current path. The second consideration that must be made is that the current probes are not immune to *dv/dt* induced noise. On test, connecting the probe to a stub of conductor and exposing to a high *dv/dt* with no current, a spurious reading of around 1 A was observed.

Clearly when considering the most detailed and small parasitic elements of a converter, taking consideration of the effect of the measurement techniques used is vital. As such these effects are taken into account and their severity is considered in more detail in the simulation.

D. *Simulation model*

To rapidly test multiple circuit conditions an LTspice model has been refined which is capable of performing parametric sweeps. This allows fast and detailed investigation into the effect of the load parasitics. Fig 4 shows waveforms measured from the experimental system alongside some from the simulated system. Though the simulation is not completely faithful to the experimental waveforms it does show the important artifacts and allows for the trends imposed by sweeping parameter values to be investigated.

Modeling of the active devices has been done through the use of the CREE provided spice models.

As this work is concerned with very small parasitic elements of the load it is critical that this model accurately represents the hardware system being tested in as finer detail as possible. Elements such as the main switching loop inductance can have a very significant effect on the switching performance and must be carefully modelled [6]. To this end parasitics such as the gate path inductance, pad to pad capacitance, capacitor ESR, probe capacitance and the commutation path impedance have been analyzed and accounted for.

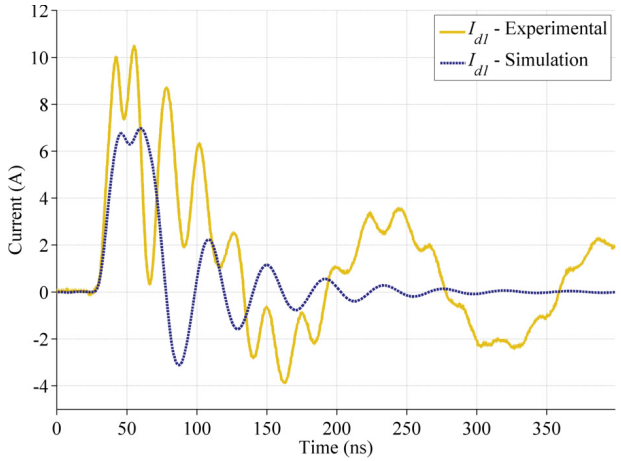

Fig. 4 - Comparison of measured and simulated device currents at turn on (With I_{out} = 0 A, R_g = 6.2 Ω and no filtering inductor [L_2])

II. Current Overshoot And Ringing

One factor that will contribute to the switching losses is the overshoot observed after switching. As the overshoot occurs before the voltage across the switching device falls to zero additional switching losses will occur, it is therefore desirable to remove and control this overshoot. Fig. 5 shows experimental results that demonstrate this current overshoot and Fig. 6 compares the ideal current waveform to one with ringing on it.

There are a few effects that contribute to this current overshoot – firstly any diode reverse recovery current (RRC) will be superimposed upon this current waveform. It has been shown that this effect can be reduced through the use of silicon carbide schottky diodes, hence improving the switching losses [7]. Other aspects of the system that will also contribute to the current overshoot include parasitics of the PCB and parasitics of the load. The current ringing that is evident on the waveform and also illustrated in Fig. 6 will also contribute to electromagnetic (EM) radiation, the suppression of which is important in making a system complaint. To some extent this ringing will be affected by interactions with the load and the capacitance of the device themselves.

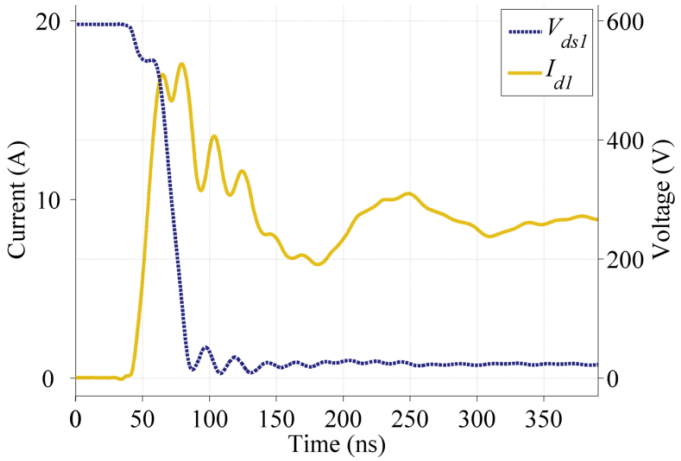

Fig. 5 – Experimental switching waveforms for the top device showing overshoot of the current waveform (R_g = 24 R), initial load current = 10 A

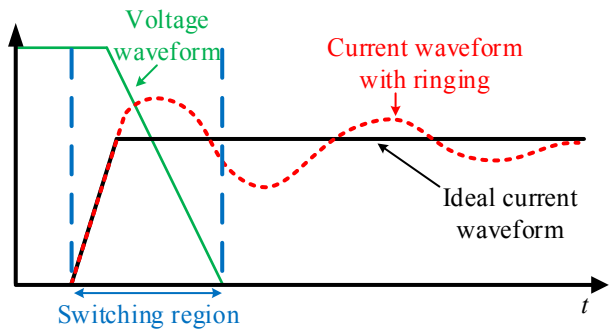

Fig. 6 - Switching waveform with and without current ringing

A. Contributions of the cable and the load

In the case of a motor drive application where the motor is used as the inductive element in the circuit, the parasitic EPC of the motor windings will be a major contributor to this overshoot. As the device switches it will be required to supply current to charge this capacitance, if this occurs during the switching period it will contribute to device losses. The experimental results presented in Fig. 7 demonstrate the impact of having a non-ideal load connected to the output terminals of the converter. It shows the top device drain current (I_{d1}) for the case where the load components (L_2 through to the load as depicted in Fig. 1) are either connected or disconnected from the circuit. It also shows the lower device drain current (I_{d2}) which changes little between the two situations.

In this experiment the inductance is relatively large (45 mH), so the ramp up of the current cannot be seen in the timescale presented, instead only the inrush current is seen. This current is largely made up of that which is charging capacitive elements of the load. Fig. 8 shows the impedance of the load as measured by an impedance analyzer, it can be seen that there is a large equivalent parallel capacitance (145 pF) if the circuit is approximated by that shown in the figure. With the load disconnected from the circuit there is still an inrush current through the top device. Some of this can be seen to be flowing into the lower device which in this instance is turned off and

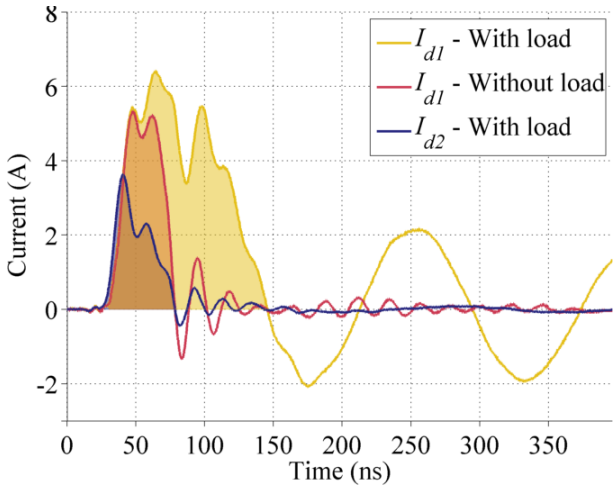

Fig. 7 – Experimental results comparing loaded and unloaded top device switching current during zero current turn on

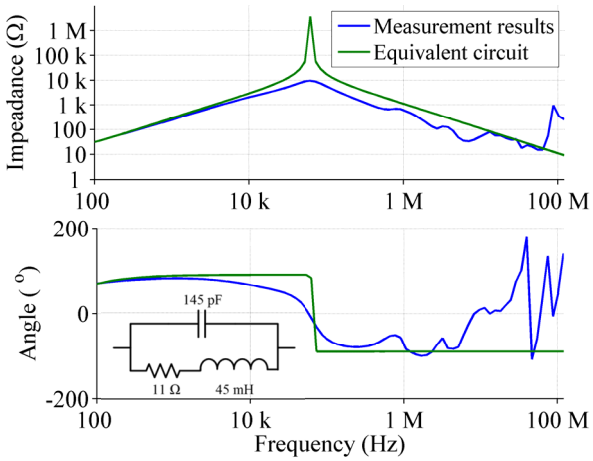

Fig. 8 – Measured impedance of the load components and impedance of the equivalent circuit approximation

appears as a capacitor equal to C_{oss} of the device (80 pF). The rest can be attributed to the need to charge the effective capacitance between planes of the PCB and a small portion to the tip capacitance of the voltage probe that was connected to the circuit's midpoint. It is clear that the effect of the load dominates the overshoot for the case presented.

B. Contributions of PCB pad spacing

It has already been established that the PCB design for a high switching speed converter will be very influential on the performance of the converter. One aspect that begins to play a more significant role at high switching speeds is the impedance between the adjacent pads of the drain and source for each device. Fig. 9 shows the impedance of the PCB measured between the drain and source pads for the top switching device. At high frequencies the impedance becomes very low and as the switching waveforms for high switching speeds will impose high *dv/dt* across this gap a significant current will flow. This makes this a significant parasitic element.

To investigate how the current overshoot is effected by the value of the capacitance between these pads a parametric sweep was performed in the simulation model. As the capacitance

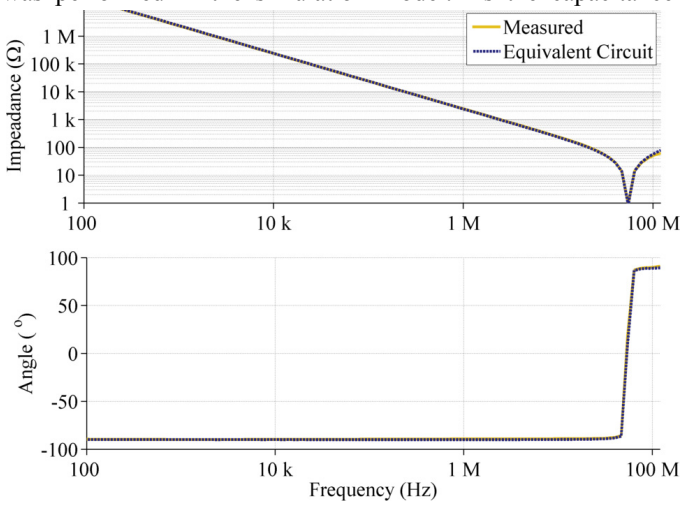

Fig. 9 – Measured and equivalent circuit impedance between drain and source pads on PCB (All circuit components removed)

between two parallel plates is determined by (1) the capacitance (C) will be inversely proportional to the distance (d) between the PCB pads. In the experiment the measured value of capacitance between the pads of the PCB was taken and scaled by various values. Fig. 10 and Fig. 11 show how the current measured at the drain of each device varied as the top device turns on.

$$C = \varepsilon \frac{A}{d} \tag{1}$$

As the value of the capacitance is increased (corresponding to placing the pads closer together) the charge the top switching device has to supply increases. This is because it must supply the charge for the lower C_{pad} as well as the charge to the top C_{pad}, both of which are increasing. The total additional supplied charge will be given by (2). The current overshoot for the lower device is actually reduced with the increase in capacitance. This is because the increased loading on the top device slows down the *dv/dt* at the load connection point of the leg. As the current overshoot into the lower device is limited by the lead inductance a reduced *dv/dt* results in a smaller current spike.

$$Q = 2C_{pad}V \tag{2}$$

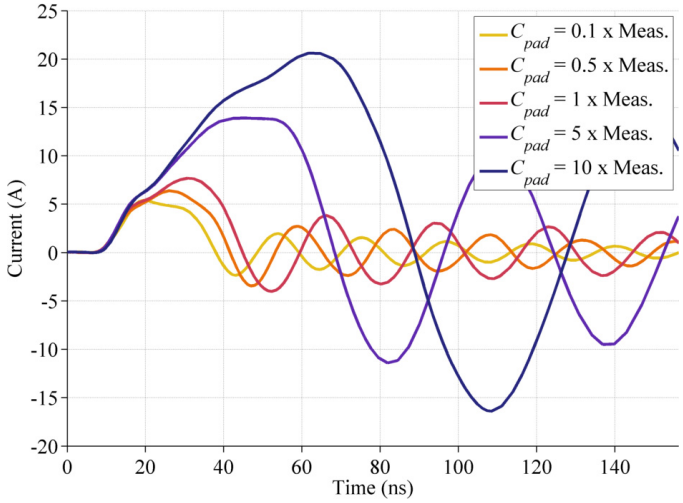

Fig. 10 – Simulated I_{d1} for varying values of C_{pad} (R_g = 6.2 Ω)

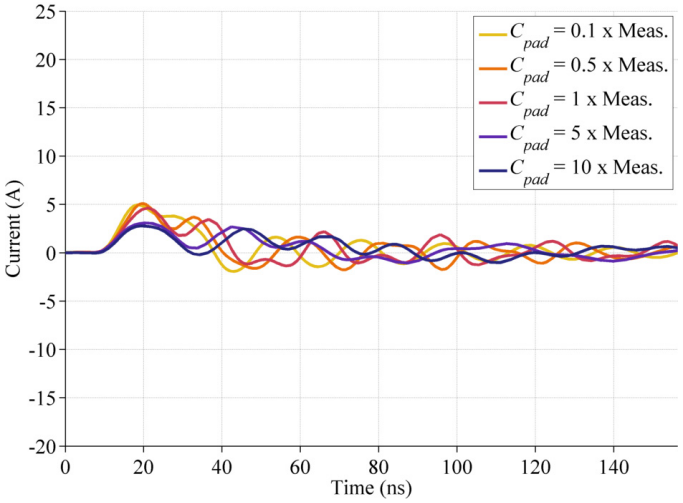

Fig. 11 – Simulated I_{d2} for varying values of C_{pad} (R_g = 6.2 Ω)

As the top device is the more severely affected by this parasitic element during turn on it may be desirable to separate the PCB pads as far as possible to minimize the effect.

C. *Effect of switching speed*

As the current into the parasitic load and cable capacitances will be dependent on the applied *dv/dt* both the switching loss and the overshoot on switching will vary. At very high *dv/dt* a smaller snubber inductance may still present a large enough impedance to reduce the effect of charging the parasitic load capacitance providing its EPC is sufficiently low. Fig. 12 shows how the power dissipated in the top device varies with different gate resistors when the converter is switching on into the load via a 5 m cable. Fig. 13 shows the same set of waveforms for the case where a small inductor (corresponding to L_2 = 13 µH) is placed in series with the cable. It can be seen that for all cases the inclusion of a series snubber inductor reduces the peak power dissipation. Table 1 compares these results numerically and also presents the reduction in switching energy through use of a snubber inductor.

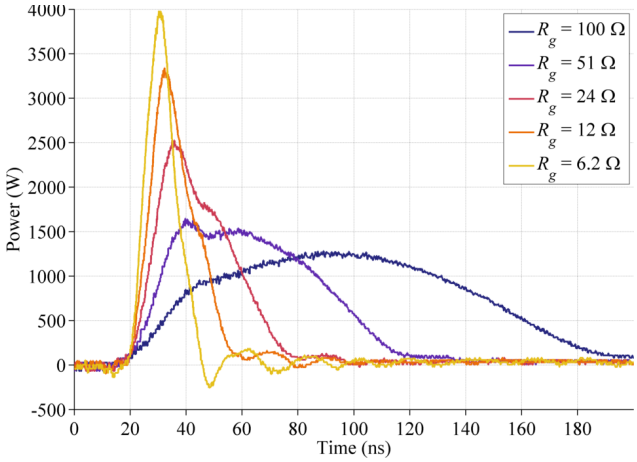

Fig. 12 – Experimental top switching device power dissipation during turn on for load connected via cable

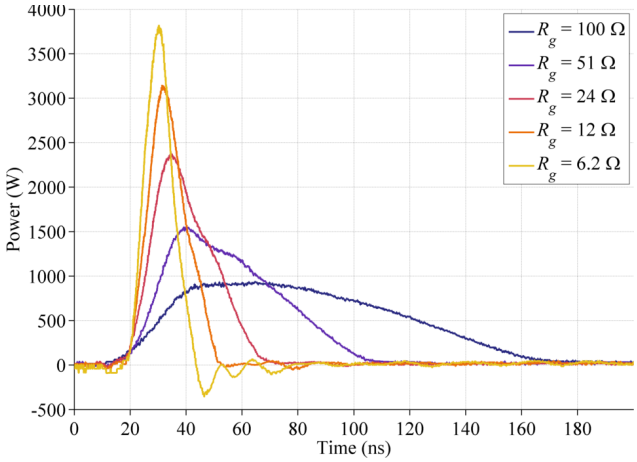

Fig. 13 – Experimental top switching device power dissipation during turn on for load connected via inductor and cable

TABLE 1 VARIATION OF SWITCHING ENERGY WITH SWITCHING SPEED

R_g (Ω)	dv/dt (kV/µs)	Switching energy (µJ)		Energy reduction
		without inductor	*with inductor*	
100	4.9	145	91	37 %
51	8.4	104	73	30 %
24	15.6	74	58	22 %
12	23.7	61	50	18 %
6.2	29.8	50	45	10 %

It is clearly shown that with increased switching speed the switching energy decreases as is expected. It is also interesting to note that as the switching speed is increased the reduction in energy from inclusion of a snubber inductor reduces quite dramatically. This is because the higher switching speeds are able to induce enough current through the EPC of the inductor that its added impedance does not perform as well as desired.

III. REDUCTION OF SWITCHING LOSSES AND RINGING

It is common to place an output filter in series with the load in a motor drive application which is designed to filter the output waveform to some extent, though not all drives make use of this. It is unavoidable with this kind of converter topology that the capacitance associated with the load will have to be charged when a switching action occurs. However, this current will only contribute to switching losses significantly if it is supplied while the device is still in the process of switching. For converters with limited or no output filter the inclusion of a small value inductor with a low EPC can reduce the inrush of current and as such reduce the switching losses. The reset of this inductor is provided during the off period where the voltage drop across the load resistance provides a reset voltage. This idea is illustrated in Fig. 14. The inductance L_2 is chosen to be a low EPC type because this forms a bypass of the inductor for any high frequency current. Such an inductor is shown in Fig. 15, it has only a single layer winding to minimize the inter-winding capacitance.

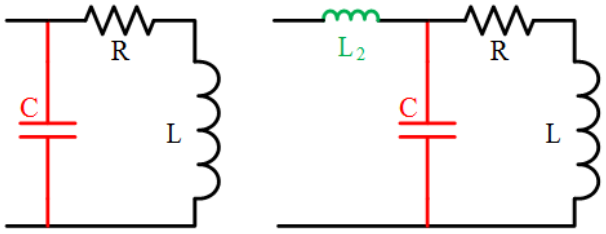

Fig. 14 - Inclusion of a small, low EPC, inductor with the load

Fig. 15 - Small low EPC inductor

At the moment the top device turns on a very high *dv/dt* is applied to the load. If the waveform was assumed to be a step voltage then the current into the load would be defined by the inductance of the connection (the capacitance will take a moment to charge and as such can be treated as a zero voltage source for a brief period). Carrying these assumptions forward it would be possible to reduce the rate of rise, and hence the overshoot, of current into the load at switching time. Of course the situation is significantly more complex, with the poorest assumption being that the applied voltage is a step. However, it is still useful to consider how the system will perform based on this analysis.

It is also possible to reduce the magnitude of the ringing after the switching edge using this snubber inductor. After the switching moment the components that were illustrated in Fig. 1 form a complicated resonate circuit. Analyzing this circuit in an analytical sense that aids a general understanding is very difficult. Simplifying the system by focusing on the impedance of the load and snubber it is possible to get a basic understanding of where the reduction of ringing would be manifested.

Taking the circuit indicated in the right of Fig. 14 to be the load another simplification immediately becomes available. As the large inductance will effectively act as a current source over the timescales of interest it can be disconnected for the purpose of this ac analysis. Then the output circuit becomes simply a capacitor and inductor in series. Analyzing this the magnitude of the outputs impedance, $|Z|$, is found as (3).

$$|Z| = \omega L_2 - \frac{1}{\omega C} \tag{3}$$

It can be seen in (3) that an increase in L_2 will lead to an increases in impedance across all frequencies, suppressing ringing at any frequency. Of course the same could simply be achieved with a resistor in series with the output, however this would lead to unnecessary losses.

To investigate to what extent the utilization of an inductor as described could have on the switching performance of the system, an experiment was carried out in which different combinations of load elements were tested. The load was made up of a multi layered inductor and a wire wound resistor. In addition to this the inductor of Fig. 15 (*inductor*) and a 2 m cable (*cable*) were also included in some of the scenarios. The current and voltage waveforms for the top switching device during zero current turn on are shown in Fig. 16. Fig. 17 shows the power computed for each of the cases along with the switching energy found by integration of the power waveform.

Zero current switching describes the case where no output load current is flowing. It is useful to observe this case as diode reverse recovery will not occur allowing easier analysis of the contributions to the overshoot of other elements of the system.

It can be seen from Fig. 16 that the inclusion of the small inductor reduces the current overshoot quite significantly, particularly in the case where the load is connected via the long cable. Comparing the switching loss shown in Fig. 17 it can be seen that the inclusion of the snubber inductor when the cable is present can bring the switching loss down to a lower level than that of the case where it is just the load connected directly. It can also be seen that the inclusion of the snubber inductor decreases the amplitude of the current ringing.

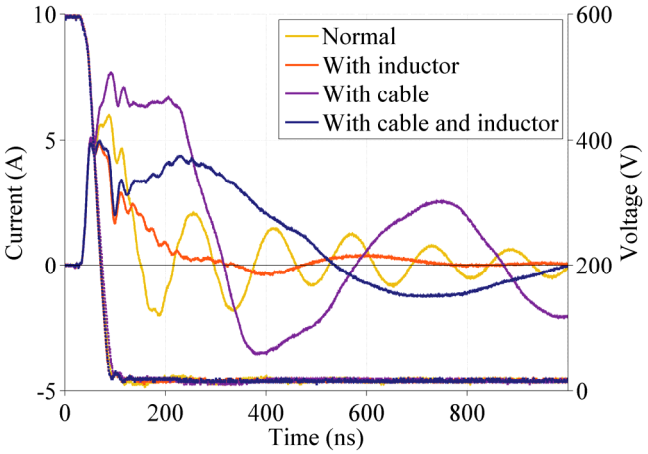

Fig. 16 – Experimental comparison of top device switching waveforms, with both current (solid line) and voltage (dotted line), for different load configurations

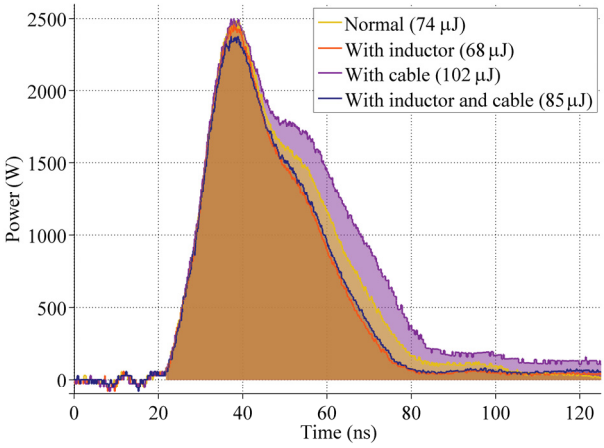

Fig. 17 – Top switching device power for different load configurations

A. *Snubber Size Optimisation*

If using an inductor as a snubber in the way described it will be desirable to minimize its size (physical and inductance). As such, an understanding of how to choose the size of the inductor is necessary. The goal is to damp the overshoot in the current waveform as far as possible, however the degree to which this can be done will be limited by the EPC of the filtering inductor and the parasitics of other circuit elements.

There are several limitations in the use of this snubber. Firstly consider the circuit presented in Fig. 1, placing a snubber inductor in the output path as indicated (L_2) will be able to slow down the rise of current into the output leg. However it will not slow down the current rise associated with charging the lower device capacitance and providing the diode reverse recovery current. Secondly, the EPC of the snubber will provide a path for high frequency current components to flow, limiting its effectiveness.

Analyzing the circuit and all of its relevant parasitics does not provided a solution which is easy to use in an analytical sense. Instead it is proposed that by taking some very severe

approximations a better understanding of the sizing of this inductor can be obtained.

Namely, these assumptions are as follows. The inductance of the cables connecting the load is insignificant. The applied voltage waveform is a ramp with a constant *dv/dt*. The output capacitance does not become charged significantly during the rise of the current. This allows the assumption that the voltage across the inductor will be constant during the transient. The final assumption is a particularly poor one as the output capacitance is relatively small and will charge quickly. The result of this assumption will be that the calculated inductance require for L_2 will be larger than necessary to achieve a particular performance.

To calculate values for L_2 firstly, approximate the expected current that will flow into the output capacitance. This can be done by using the well-known formula describing the relation between current and voltage in a capacitor (4). *dv/dt* is the rate of change of voltage expected at the midpoint of the converter, which will be determined by the switching speed of the devices in use.

$$I = C\frac{dV}{dt} \tag{4}$$

The current calculated with this equation will give the expected peak overshoot (I_{OS}) due to the load capacitance. Now it is possible to specify the value of inductance to use for the snubber. By specifying that the rise time of this current should be somewhat less that the voltage rise-time (in order that the overlap of the current and voltage over the top switching device is reduced) and also taking the voltage over the inductor to be constant during the transient the inductance can be calculated using (5).

$$V = L\frac{dI}{dt} \tag{5}$$

Finally it is necessary to calculate an acceptable value of EPC for the snubber inductance. If the EPC was allowed to be too high then the high frequency components of the current waveform would bypass the inductance entirely and the performance of the snubber would be greatly diminished. To calculate this consider the overshoot current that was previously calculated (I_{OS}). Defining the allowable current through the EPC of the snubber to be one tenth of the current that would have flown through the load inductance EPC is a reasonable performance increase. The allowable capacitance can be calculated using (4). Alternatively, by inspection, it will be one tenth the capacitance of the load EPC.

Simulation results using a snubber inductor specified in this way show a 50% improvement in the turn on losses of the high side device. Fig. 18 shows the simulated current waveform through the top device at turn on with and without a snubber inductor calculated in the described manner.

IV. Effect of Load Capacitance

As any length of cable is added to the output of the converter the effective capacitance of the load is increased. Different motors connected to the output will also have a significant amount of EPC which will have to be handled by the converter. If there is no snubber network at all then the overshoot of the current waveform will increase with this increase of load

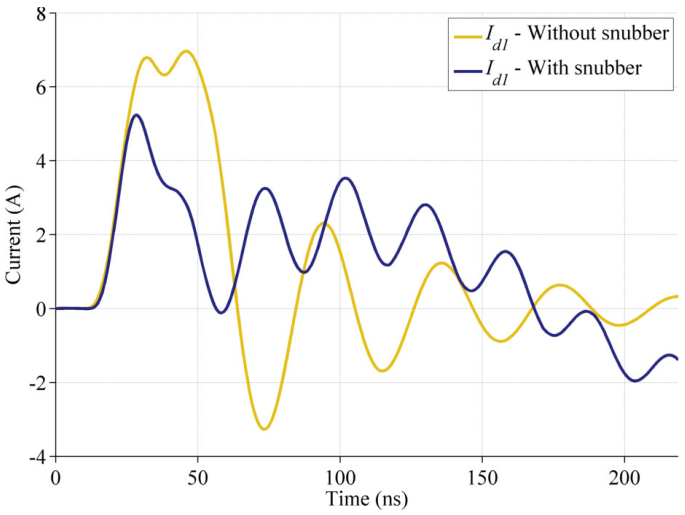

Fig. 18 – Comparison of simulated I_{dI} with and without calculated snubber inductor ($R_g = 24\ \Omega$)

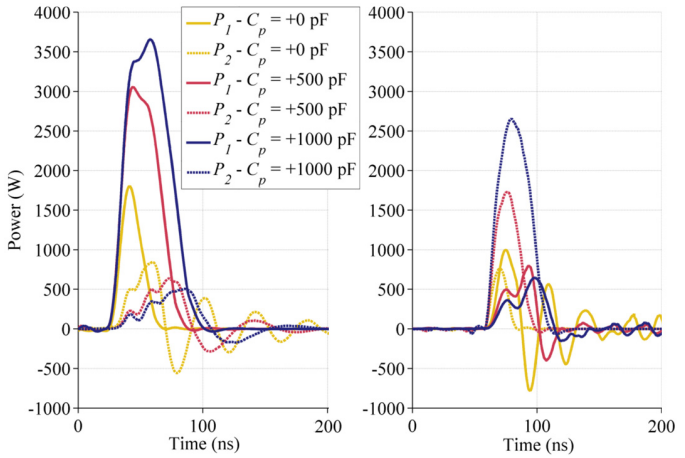

Fig. 19 – Simulated top (P_1) and bottom (P_2) device power dissipation with different values of added output capacitance for: Left – turn on, and Right – Turn off

capacitance. As such the power dissipated in the top device during turn on will be increased. Fig. 19 displays simulation results which show how the power waveforms for the top switching device vary with a range of additional capacitance connected in parallel with the load.

Investigating the energy dissipated in each case the results of Table II are obtained.

TABLE II SWITCHING ENERGY UNDER VARYING LOAD CONDITIONS

Added Capacitance (pF)	**On (µJ)**			**Off (µJ)**		
	Top	***Bottom***	***Total***	***Top***	***Bottom***	***Total***
+ 0	28	16	**44**	12	11	**23**
+ 500	104	17	**121**	14	38	**52**
+ 1000	161	18	**179**	15	78	**93**

To investigate these waveforms under real converter conditions an experiment was carried out in which different capacitances were connected in parallel with the experimental load. Given that the capacitance of a motor can vary in a wide

range the capacitance added in series with the load inductor in the experiments was varied between 0 pF and 1000 pF [8]. It is expected from the simulation results that the energy dissipated in the turn on waveform will be increased with increasing capacitance. Fig. 20 shows experimental waveforms for the top switching device with varying additional capacitance in parallel with the load inductance.

The inductance of the output connection remains constant through these tests, as the capacitance is increasing the overshoot current would be expected to increase as shown by (4). Indeed this is what is seen in the results presented. If the snubber inductor shown in Fig. 14 were also included in the circuit it would be expected that it would have an increasingly beneficial effect in the case of a larger capacitance.

V. Conclusions

Parasitics present in the load of an industrial drive or converter will lead to the losses in the switching devices being more than that which is measured under laboratory conditions. It has been shown that the overshoot due to the loads EPC can be reduced considerably through use of a snubber inductor. This can significantly reduce turn on switching loss as well as reducing ringing. A method for calculating the size of this inductor has also been presented. Consideration of switching speed has shown how even relatively minor parasitic elements can have a significant impact on the performance of the converter.

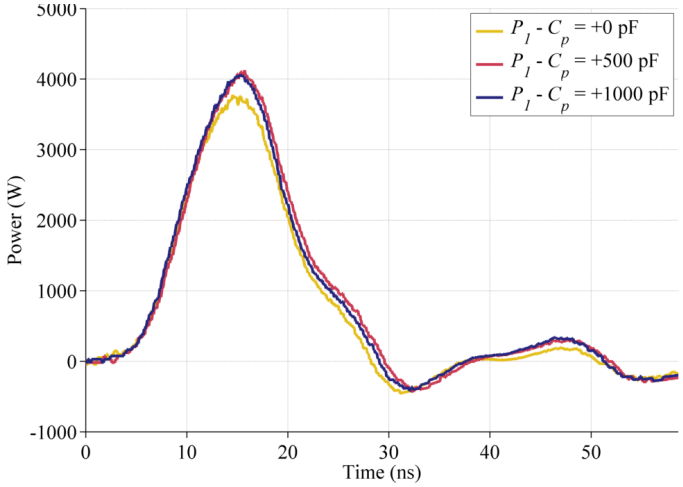

Fig. 20 - Experimental results showing top device power dissipation (P_1) with a range of added load capacitance

VI. Further Work

The work presented here leaves several aspects open to further investigation. Clearly the development of a more accurate simulation model developed using 3D analysis of the PCB parasitics will allow further, more accurate scrutiny, of the PCB parasitics. This will also enable the separation of the contributions to the total loss, allowing the more severe contributors to be identified. In addition to this the impact on radiated and conducted electromagnetic interference of the reduced ringing will be of interest. Further analysis of the parasitic elements behaviors during switching will provide a clear understanding of the mechanisms that define the ringing. Finally, the creation of an experimental system that allows the results regarding the closeness of the device pads will be able to validate the results shown here.

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