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Contactless Thermal Boundary Resistance Measurement of GaN-on-diamond Wafers

J.W. Pomeroy, R. B. Simon, H. Sun, D. Francis, F. Faili, D.J. Twitchen, M. Kuball

Abstract—**Low thermal resistance GaN-on-diamond wafers offer enhanced thermal management with respect to GaN-on-SiC devices. The GaN/diamond interfacial thermal resistance can contribute significantly to the total device thermal resistance and must therefore be minimized to gain the maximum benefit from GaN-on-diamond. A contactless thermoreflectance measurement technique has been developed, which can be used after wafer growth and before device fabrication, enabling rapid feedback about the influence of growth parameters on interfacial thermal resistance. A measured 2× reduction in the GaN/diamond interfacial resistance is achieved by reducing the dielectric thickness between the GaN and diamond from 90 nm to 50 nm, enabling a potential 25% increase in transistor power dissipation for GaN-on-diamond.**

***Index Terms*—AlGaN/GaN, HEMTs, diamond, thermal management, thermal resistance, thermoreflectance.**

I. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have greatly contributed to the high-power RF amplifier field [1]. However, managing waste heat is an increasingly important consideration when extending GaN RF HEMT operation to ultra-high-power densities. The heteroepitaxial integration of GaN devices with diamond grown by chemical vapor deposition (CVD), to form GaN-on-diamond, takes advantage of very high thermal conductivity diamond within ~1 μm of where heat is generated in the transistor channel [2]. GaN-on-diamond wafers have been made in diameters up to 100 mm, suitable for commercial wafer processing [2]. Excellent electrical and thermal performance has already been demonstrated for RF transistors on GaN-on-diamond wafers [3, 4], and 3× higher power densities have been obtained with respect to GaN-on-SiC devices [5]. However, an effective thermal boundary resistance (TBR_{eff}), including contributions from crystalline defects close to interfaces and low thermal conductivity interfacial layers, contributes to the total device thermal resistance in any heteroepitaxial GaN device. For example, in GaN-on-SiC wafers the TBR_{eff} is attributed to the high defect density within the AlN nucleation layer, which is used for GaN epitaxy on SiC. In GaN-on-SiC the TBR_{eff} can account for up to 20-30% of the total transistor thermal resistance [6]. Similarly, a TBR_{eff} exists at the GaN/diamond interface, associated with the dielectric layer and diamond nucleation layer [4, 7]. TBR_{eff} must be minimized in order to gain the full benefit of high thermal conductivity diamond substrates and therefore measurement of this parameter is needed. Existing TBR_{eff} measurement techniques are either destructive or require long feedback times. For example, time domain thermoreflectance (TDTR) requires the sample to be coated with a metal transducer [7], whereas Raman thermography requires device fabrication [4, 6]. In this letter, we demonstrate a rapid, contactless laser reflectance technique for mapping the GaN-on-diamond TBR_{eff} on as-grown wafers prior to device fabrication. The benefit of using this technique to optimize thermal resistance is illustrated by measuring the TBR_{eff} of GaN-on-diamond wafers with different dielectric layer thicknesses and assessing the improvement in transistor thermal resistance based on a validated thermal simulation.

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II. Measurement and Analysis

The GaN-on-diamond wafers measured here originate from GaN growth on silicon substrates, following the material preparation method described in Ref. [3]: GaN-on-Si wafers were temporarily mounted upside down on handle wafers, the silicon substrate and nitride transitions layers were removed, after which diamond was grown on the GaN backside after the deposition of a thin dielectric layer. The resulting layer structure consists of a standard AlGaN/GaN HEMT heterostructure, a 700 nm-thick GaN layer and a thin dielectric on a 110 μm-thick CVD grown polycrystalline diamond substrate. Two wafers were investigated having dielectric layer thicknesses of 50 nm and 90 nm, but otherwise using the same diamond synthesis conditions and are therefore assumed to have the same diamond microstructure and thermal properties. A schematic of the GaN-on-diamond layer structure is shown as an inset of Fig. 1.

The thermoreflectance measurement technique presented here for GaN-on-diamond does not require any modification of the wafer surface, such as a metal deposition. A nanosecond above-bandgap pump laser is used to heat the GaN surface directly, while the GaN surface temperature is probed by the surface reflectivity, modulated by the highly temperature-dependent refractive index (n); e.g. the thermo-optic coefficient dn/dT of GaN at room temperature is 1×10^{-4} K^{-1} at 532 nm [8]. The reflectivity at each interface is dependent on the refractive index contrast and is determined by the Fresnel

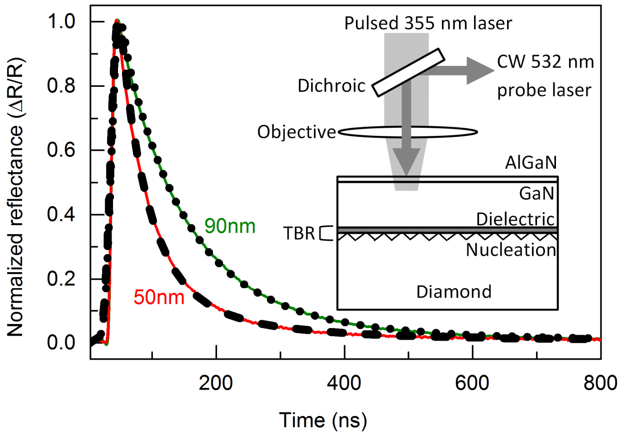

Fig. 1. (a) Thermoreflectance signal measured on two GaN-on-diamond wafers with 90 nm and 50 nm-thick dielectric layers. Best fit model results including TBR_{eff} values of 1.7×10^{-8} m^2K/W (50 nm layer) and 4.1×10^{-8} m^2K/W (90 nm layer) are overlaid. The GaN-on-diamond layer structure and thermoreflectance optical setup are shown schematically as an inset.

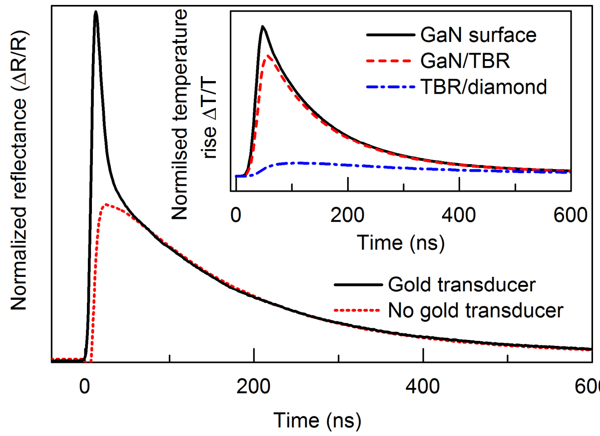

Fig. 2. Thermoreflectance signal measured for a GaN-on-diamond wafer with a 90 nm adhesion layer, with and without gold transducer, normalized at the 75 ns value to aid visual comparison. AS INSET: Modeled transient temperature rise at the GaN surface, GaN/TBR interface and TBR/diamond interface, using a GaN/diamond $TBR_{eff} = 4.0\times10^{-8}$ m^2K/W.

equations. In the case of GaN-on-diamond the dominant reflection is at the air/AlGaN-GaN interface where the refractive index contrast is large (n_{air}=1, n_{GaN}=2.4 and $n_{diamond}$=2.4 at 532 nm): At normal incidence, 15% of the light is reflected at this interface. The thermoreflectance measurement configuration is shown schematically as an inset of Fig. 1. Measurements were performed using a 15× 0.3 N.A. quartz objective (maximum 17° angle of incidence). The GaN surface is heated by a 70 µm FWHM Gaussian profile, 10 ns laser pulse produced by a 355 nm (3.49 eV) frequency-tripled Nd:YAG laser, with a 30 kHz repetition rate and ~2.3 µJ pulse energy incident at the sample surface; at this wavelength the absorption depth in GaN is ~100 nm [9]. The sample reflectivity, probing the surface temperature rise, was monitored using a below bandgap continuous wave (CW) 532 nm laser, focused to a 2 µm-diameter spot at the sample surface, coaxial with the pump beam. A beam splitter is used to sample the reflected beam intensity, measured using a silicon photodiode, transimpedence amplifier (2.3 ns rise time) and a digital oscilloscope. A long pass filter is used to ensure that no residual light from the pump beam was detected.

Fig. 1 shows the thermoreflectance signal measured for the GaN-on-diamond wafers at an ambient temperature of 25°C, normalized to the peak reflectivity modulation. Only a few seconds is needed to record each trace, enabling fast wafer mapping. On each sample, repeat measurements at five locations produced indistinguishable results. A clear decrease in the thermal relaxation time constant is observed for the sample with a 50 nm-thick dielectric layer with respect to the sample with a 90 nm-thick layer, indicating a reduction in thermal resistance. To accurately interpret this result, it is important to verify that the modulated reflectivity signal originates from the sample surface. To do this, TDTR measurements were performed on each wafer after coating the surface with a 100 nm-thick gold transducer, using a thin titanium adhesion layer. Fig. 2 shows the result of the TDTR for the wafer with a 90 nm dielectric interlayer, overlaid with the thermoreflectance measurement performed without a gold transducer. An initial deviation (<35 ns) between the reflectivity transients recorded with and without metal transducer is due to the thermal response time of the gold transducer following the heating pulse. After 35 ns, once the gold layer reaches thermal equilibrium with the semiconductor surface, excellent agreement is found between the temperature transients measured with and without the gold transducer for each wafer (50 nm layer trace not shown), verifying that the surface temperature is measured using the contactless technique presented here.

A 3-D time domain finite element (FE) thermal model was used to analyze the temperature transients measured for the GaN-on-diamond layer structure shown in Fig. 1, omitting the thin AlGaN layer which had no effect on the modeling results. The TBR_{eff} is represented by a contact resistance between the GaN and diamond, including contributions from low thermal conductivity dielectric layer and the diamond nucleation layer in the first <100 nm of growth. The measured temporal and spatial profiles of the heating laser pulse were used in the model. A typical epitaxial GaN thermal conductivity (κ) value of 160 W/mK was used [4,6]. An effective diamond thermal conductivity of 1200 W/mK was used, which is lower than bulk values due to grain boundary scattering in the initial growth layer of the diamond [4]; this value was determined by measuring the temperature rise within the first few microns of a CVD polycrystalline diamond substrate beneath an active AlGaN/GaN transistor [4]. Reported densities and heat capacities were used for the GaN [10] and diamond [11]. The inset of Fig. 2 shows the modeled temperature transient, for illustration assuming a TBR_{eff} value of 4×10^{-8} m^2K/W. The vertical temperature gradient generated across the GaN layer relaxes after 75 ns and only a small temperature difference (ΔT) is observed across the diamond substrate. After 75 ns the remaining ΔT is predominantly across the TBR_{eff} layer only. Consequently, the TBR_{eff} value is the only sensitive parameter in fitting the temperature decay in the >100 ns region; This was verified by adjusting the GaN and diamond thermal conductivity by ±25%, which had no discernable effect on the

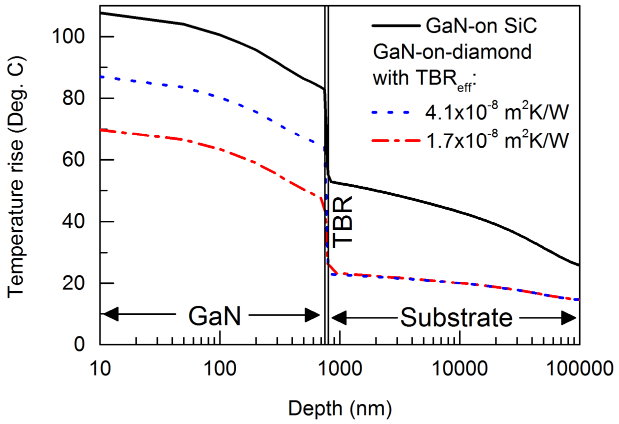

Fig. 3. Thermal simulation of the vertical temperature profile beneath the central finger of an 8 finger AlGaN/GaN-on-diamond HEMT at a power dissipation of 5W/mm. Temperature profiles are calculated using the TBR_{eff} values determined in this work and for comparison a GaN-on-SiC transistor.

simulated temperature transient during this timescale. By fitting the thermal model to the traces shown in Fig. 1 as described (>100 ns), TBR_{eff} values were determined as 4.1×10^{-8} m^2K/W and 1.7×10^{-8} m^2K/W for the wafers with 90 nm and 50 nm-thick dielectric layers, respectively. These TBR_{eff} values are consistent with the range of reported values measured by TDTR (1.7-4.2$\times10^{-8}$ m^2K/W) [7] and Raman thermography (2.7-3.6$\times10^{-8}$ m^2K/W) [4]. The observed ~2× reduction in TBR_{eff} with decreasing dielectric layer thickness highlights that this layer is responsible for a significant proportion of the total interface thermal resistance and that its thickness should be reduced as far as possible. The limiting factor for reducing the dielectric layer thickness is the requirement that the correct conditions for diamond nucleation and growth are maintained at this interface.

An experimentally validated 3D FE GaN HEMT on diamond model was used to assess the benefit of measured the TBR_{eff} reduction [4], using the layer structure shown in Fig. 1 and considering a typical GaN multi-finger cell geometry: 8×125 µm, 30 µm gate pitch, on a 3×3 mm die with a power dissipation of 5 W/mm. The die is mounted on a 1 mm-thick CuW heat spreader (200 W/mK) with a 25 µm-thick AuSn die attach (56 W/mK). Fig. 3 illustrates the simulated vertical temperature profile beneath the central gate finger; A GaN-on-SiC device with the same geometry is shown for comparison, assuming κ_{SiC} = 450 W/mK and a representative TBR_{eff} value of 2×10^{-8} m^2K/W [6]. Based on the modeled temperature rises, power dissipation can be increased 25% for the GaN-on-diamond wafer with the 50 nm dielectric (TBR_{eff} = 1.7×10^{-8} m^2K/W), with respect to the thicker 90 nm dielectric layer (TBR_{eff} = 4.1×10^{-8} m^2K/W), highlighting the benefit of growth optimization based on measurement results. At the same channel temperature rise, power dissipation can be increased 50% for the GaN-on-diamond wafer with improved TBR_{eff} with respect to GaN-on-SiC. An even further reduction in GaN-on-diamond thermal resistance is anticipated by reducing the dielectric layer thickness further. Combined with gate pitches optimized specifically for GaN-on-diamond [5], total output power >3× greater than GaN-on-SiC will be achievable [5].

III. Conclusion

A rapid contactless interfacial thermal resistance measurement technique has been demonstrated for GaN-on-diamond wafers. This technique can be applied after wafer growth, enabling mapping and screening of interfacial thermal resistance before device fabrication. Furthermore, TBR_{eff} values can be reduced by to tuning growth parameters, with an associated improvement in transistor thermal resistance.

References

[1] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-Based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, pp. 287-305, Feb. 2008.

[2] D. Francis, F. Faili, D. Babic, F. Ejeckam, A. Nurmikko, and H. Maris, "Formation and characterization of 4-inch GaN-on-diamond substrates," *Diamond and Related Materials*, vol. 19, pp. 229-233, Feb. 2010.

[3] D. C. Dumka, T. M. Chou, F. Faili, D. Francis, and F. Ejeckam, "AlGaN/GaN HEMTs on diamond substrate with over 7W/mm output power density at 10 GHz," *Electronics Letters*, vol. 49, pp. 1298-1299, Sep. 2013.

[4] J. W. Pomeroy, M. Bernardoni, D. C. Dumka, D. M. Fanning, and M. Kuball, "Low thermal resistance GaN-on-diamond transistors characterized by three-dimensional Raman thermography mapping," *Applied Physics Letters*, vol. 104, pp. 083513-1-5, Feb. 2014.

[5] J.D. Blevins, G.D. Via, K. Sutherlin, S. Tetlak, B. Poling, R. Gilbert et al. "Recent Progress in GaN-on-Diamond Device Technology", in *CS Mantech Conference*, pp. 105-108, May 2014.

[6] A. Manoi, J. W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of Thermal Boundary Resistance in AlGaN/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure," *IEEE Electron Device Letters*, vol. 31, pp. 1395-1397, Dec 2010.

[7] J. W. Cho, Z. J. Li, E. Bozorg-Grayeli, T. Kodama, D. Francis, F. Ejeckam, *et al.*, "Improved Thermal Interfaces of GaN-Diamond Composite Substrates for HEMT Applications," *IEEE Transactions on Components Packaging and Manufacturing Technology,* vol. 3, pp. 79-85, Jan 2013.

[8] N. Watanabe, T. Kimoto, and J. Suda, "The temperature dependence of the refractive indices of GaN and AlN from room temperature up to 515 degrees C," *Journal of Applied Physics,* vol. 104, pp. 106101-1-3, Nov. 2008.

[9] J. F. Muth, J. H. Lee, I. K. Shmagin, R. M. Kolbas, H. C. Casey, B. P. Keller, et al., "Absorption coefficient, energy gap, exciton binding energy, and recombination lifetime of GaN obtained from transmission measurements," *Applied Physics Letters*, vol. 71, pp. 2572-2574, Nov. 1997.

[10] J. Leitner, A. Strejc, D. Sedmidubsky, and K. Ruzicka, "High temperature enthalpy and heat capacity of GaN," *Thermochimica Acta*, vol. 401, pp. 169-173, May 2003.

[11] A. C. Victor, "Heat Capacity of Diamond at High Temperatures," *Journal of Chemical Physics*, vol. 36, pp. 1903-1911, April 1962.