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Performance Comparison of Multi Input Capacitor Converter Circuits

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ABSTRACT

This paper analyze the operation of a multi input switched capacitor (MIC) converters using a couple of switches, diodes and capacitors for several levels. With two input sources it is possible to obtain 8 output voltage levels. Here, 5 topologies of switched capacitor circuits namely summation, subtraction, inverting, double and half circuits are simulated and their performances are analyzed. Multi Input Converters have a high regard for multiple renewable energy sources used in smart grid systems, especially for distributed generators. The effects on output voltage with variation in load for different frequencies are also analyzed. Hardware implementation of summation and subtraction circuit is carried out and the results are compared with the simulated results

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1. INTRODUCTION

Inductors and capacitors are the main energy storage for the switched-mode power supplies (SMPS). The sizes are usually dominated by the inductor and transformer [1]. DC-DC converters play a vital role in renewable energy based applications [2], [3]. Resonant converters based on this SMPS can operate at high switching frequencies to decrease the size of the converters, however, their switching frequencies are not constant and hence the electromagnetic interference (EMI) filter cannot be optimized. Extended period quasiresonant converters have been introduced in [4], [5]. These converters are able to operate at constant switching frequencies and all the switching devices are switched at zero-current or zero-voltage. The requirement of magnetic components restricts the application and increases the difficulty in designing the converters. These difficulties were replaced with switched capacitor circuits. Switched-capacitor (SC) DC-DC power converters [6] are a subset of DC-DC power converters, using only switches and capacitors that can efficiently convert one voltage to another. Since SC converters does not have any inductors, they are ideal for integrated implementations, as common integrated inductors are not suitable for power electronic applications. The main advantage of this kind of converter is that no magnetic component is required for storing energy, making it possible to fabricate a smaller size and lighter weight converter in an integrated circuit [7]. There are very mature theories and techniques to design variety of DC–DC converters with single-input. Buck converter can for lower voltage than input [8], boost converter output higher voltage [9], boost-buck converter and Cuk converter can obtain the output voltage with step up or down ratio [10] In addition, Half-mode, Double-mode [11], step-up and step-down converter based on switched-capacitor can output half, twice and multiple and fractional voltage ratios [12], [13]. In recent years, with the continuous development

of new energy technologies and the production of complex electrical equipment, multi-input DC–DC converter has aroused significant attention. A few topologies of multi input converters (MICs) have been presented in [14]-[21]. Due to the advantages of multiport converter, recently there have been extensive researches that resulted in a wide variety of topologies. One simple approach is to interface several converter stages to a common dc bus with independent control for each converter stage. A multi input boost-type converter [22] was designed for hybrid electric vehicles using such loose structure.

2. MULTILEVEL CONVERSION CIRCUITS

Figure 1 shows the diagram of a multilevel dc conversion from two different voltage levels. Two voltage levels as input, it is anticipated that the two voltage levels can be converted to other voltage levels in order to suit different voltage needs for other electronic appliances. With these five conversion circuits namely summation circuit, subtraction circuit, double circuit, half circuit, inverting circuit it is possible to convert two input voltages into eight levels of voltage. With only one input source Vs , the family of switched-capacitor converter can transform it into 0.5VS , −Vs, or 2Vs . With two input supplies Vs1 and Vs2, it can transform them into Vs1 + Vs2 or Vs1–Vs2. So, using the switched-capacitor converter and three distribution lines, two voltage levels can be converted into eight voltage levels. It includes Vs1+Vs2 (Summation) , Vs1-Vs2 (Subtraction), 2Vs1 (Double) , 2Vs2 (Double) , 0.5Vs1 (Half), 0.5Vs2 (Half), -Vs1 (Inverting) and –Vs2 (Inverting). Each of the circuits uses only two switches, two diodes and two capacitors. Therefore, the size of the circuits is very small and simple enough to handle. A pair of complementary pulses is given to two switches with fixed duty ratio of 0.5 for all the five circuits.

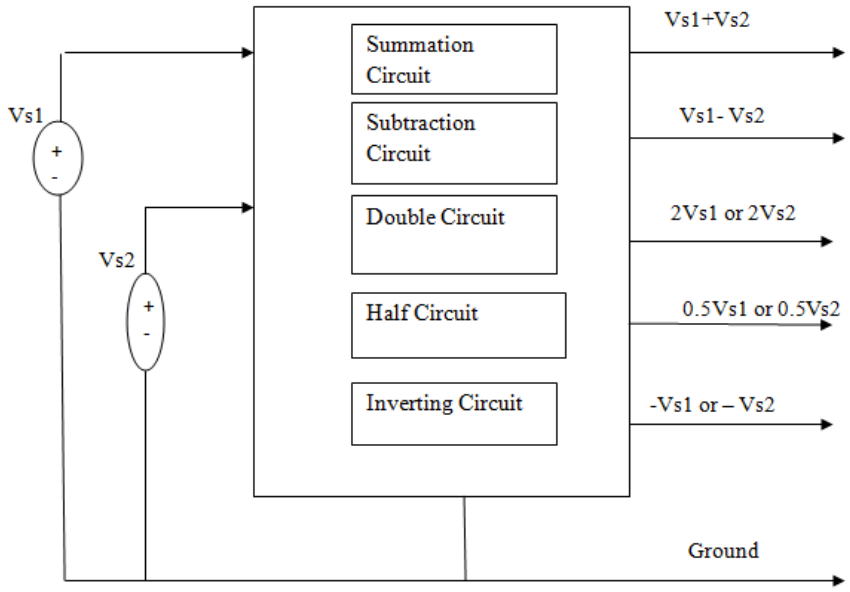


Figure 1. Multilevel converter

2.1. Summation circuit

The basic circuit diagram of a summation circuit is shown in Figure 2. Here, when Q1 is turned ON and Q2 is turned OFF, diode D1 is forward biased and D2 is reverse biased. Vs1, C1, Q1, and D1 forms a closed loop. Vs1 charges C1 and the voltage across C1 is the same voltage as Vs1, i.e., Vc1 = Vs1. When, Q1 is turned OFF and Q2 is turned ON, D2 is forward biased and D1 is reverse biased, Vs2, C1, Q2, D2, and C2 form a closed loop. C1 is connected in series with Vs2 and delivers the total voltage to C2, so the voltage across C2 is Vs2 + Vc1. As Vc1 = Vs1, the output voltage Vo = Vs1 + Vs2. Figure 3 shows the output voltage of summation circuit. Here Vs1 and Vs2 are 24V and 12 V respectively, the output voltage across load is 33.87V.

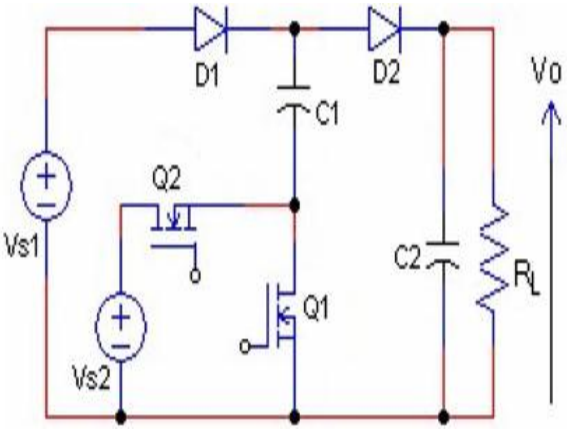


Figure 2. Summation Circuit

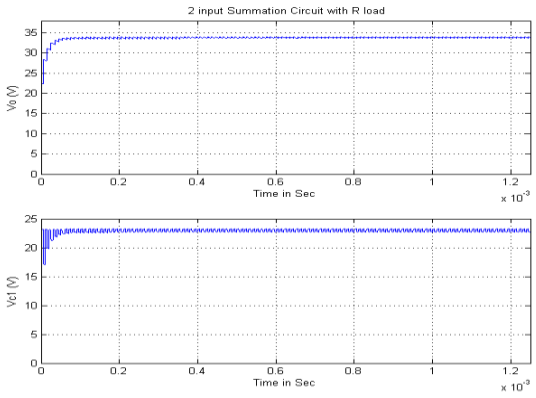


Figure 3. Output voltage and capacitor voltage of Summation Circuit

2.2. Subtraction circuit

The circuit diagram of a subtraction circuit is shown in Figure 4. When Q1 is turned ON and Q2 is turned OFF, D1 is forward biased and D2 is reverse biased. Vs1, Vs2, C1, Q1, and D1 form a closed loop, and Vs1 is connected in series with –Vs2 and charges C1, so the voltage across C1 is Vs1-Vs2. Next, when Q1 is turned OFF and Q2 is turned ON, D2 is forward biased and D1 is reverse biased, C1, Q2, D2, and C2 form a closed loop. C1 is connected in series with C2, so the voltage across C2 is equal to Vc1. The output voltage Vo = Vs-Vs. Figure 5 shows the output of a subtraction circuit. Here Vs1 and Vs2 are 24V and 12 V respectively, Vo = 12.27V.

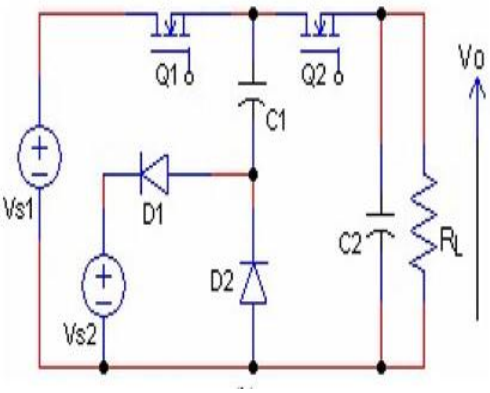


Figure 4. Subtraction circuit

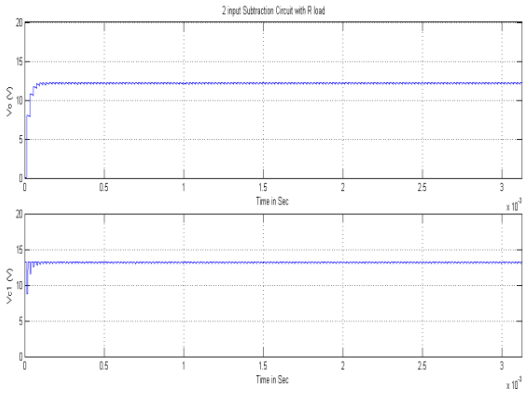


Figure 5. Output voltage and capacitor voltage of Subtraction circuit

2.3. Double circuit

The circuit diagram of double circuit is shown in Figure 6. During mode 1, when Q1 is ON, Q2 is OFF, D1 is forward biased and D2 is reverse biased, Vs1, D1,C1,Q1 forms a closed loop and capacitor C1 charges to voltage Vs. This is known as charging state. In mode 2 Q2 is ON, Q1 is OFF, D2 is forward biased and D1 is reverse biased, Vs, Q2, C1, D2, RL forms a closed loop. Capacitor C1 discharges now and capacitor C2 is now charging to voltage Vc1+Vs.This is known as discharging state. The output of double circuit becomes Vo = 2Vs. Figure 7 shows the output of double circuit. Here Vs1 and Vs2 are 24V and 12 V respectively, the output voltage Vo = 45.67V.

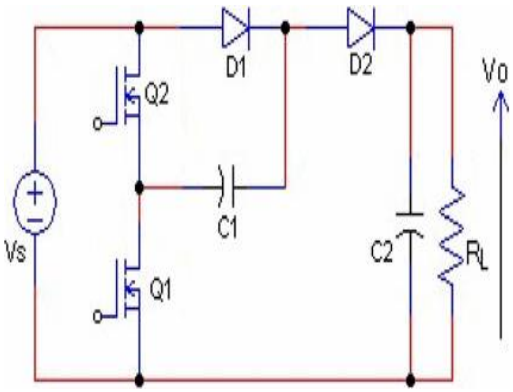


Figure 6. Double circuit

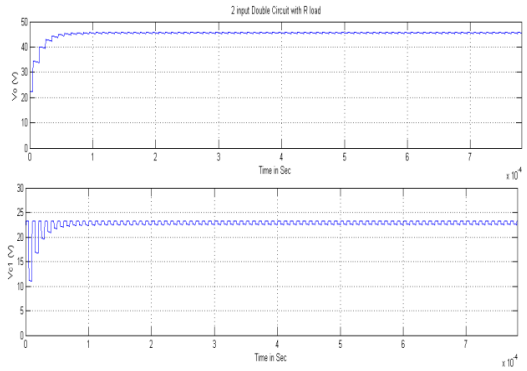


Figure 7. Output voltage and capacitor voltage of double circuit

2.4. Half circuit

The diagram of half circuit is shown in Figure 8. In mode 1 Q1 is ON, Q2 is OFF, D1 is forward biased and D2 is reverse biased, Vs, Q1, C1, D1, C2 forms a closed loop. Capacitor C1and capacitor C2 equally charges to voltage 0.5Vs. In mode 2 Q2 is ON, Q1 is OFF, D2 is forward biased and D1 is reverse biased. The voltage across capacitor C2 remains constant. The output of half circuit is Vo = 0.5Vs2. Figure 9 shows the output of half circuit. Here Vs2 is 24V, the output voltage Vo = 11.14V.

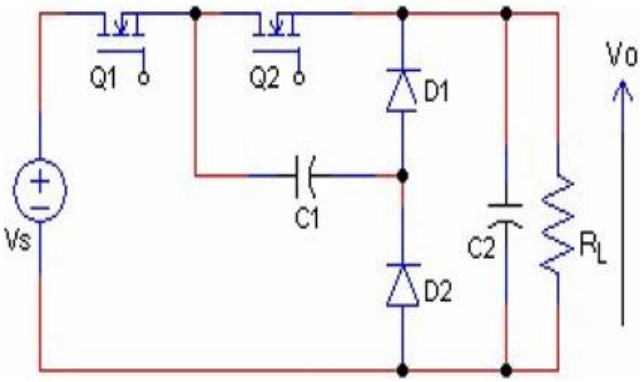


Figure 8. Half circuit

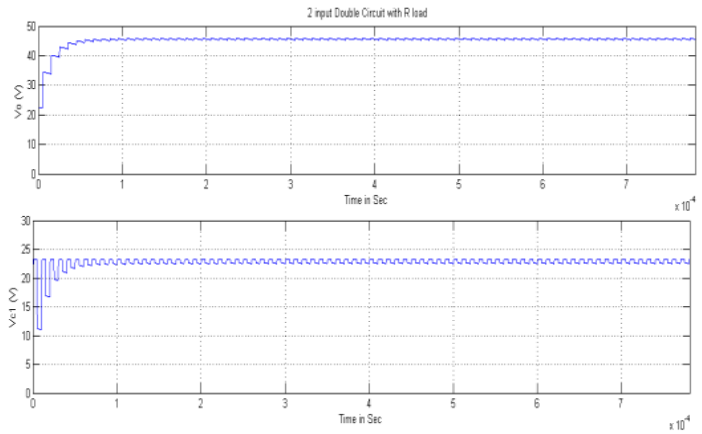


Figure 9. Output voltage and capacitor voltage of half circuit

2.5. Inverting circuit

The inverting circuit is shown in Figure 10. In mode 1 Q1 is ON, Q2 is OFF, D1 is forward biased and D2 is reverse biased,Vs,Q1,C1,D1 forms a closed loop and capacitor C1 charges to voltage Vs .This is known as charging state. In mode 2 Q2 is ON, Q1 is OFF, D2 is forward biased and D1 is reverse biased, Q2, C1, D2, C2 forms a closed loop and capacitor C1 starts discharging. Capacitor C2 is now charging to voltage Vs with reverse polarity. This is known as discharging state. The output of inverting circuit Vo = -Vs. The output voltage of an inverter circuit is shown in Figure 11. The input voltage is 12V and output voltage is -12V.

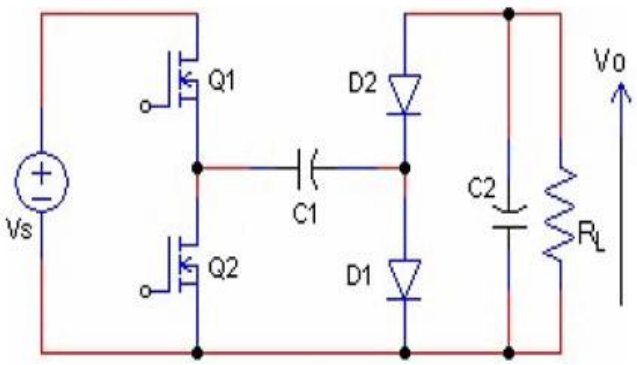


Figure 10. Inverting circuit

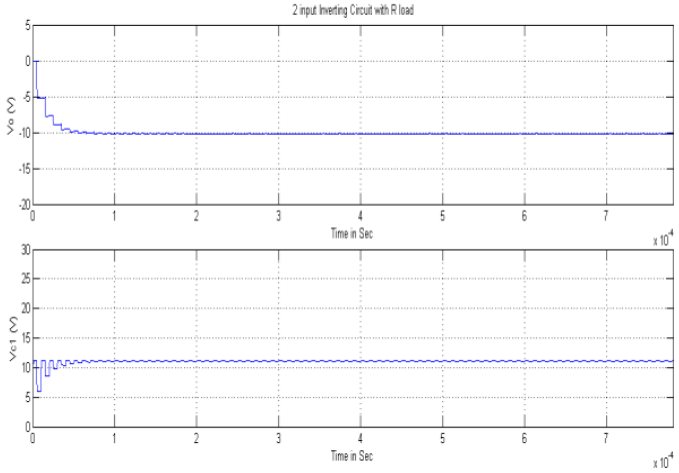
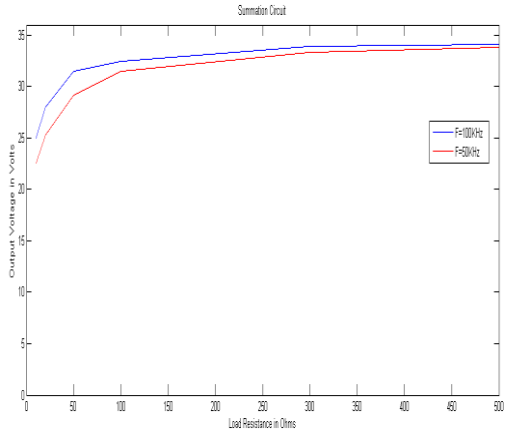


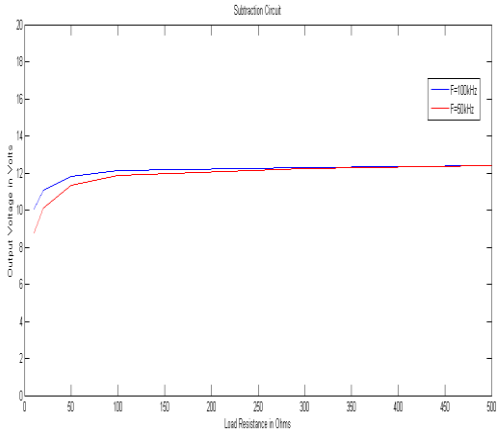
Figure 11. Output voltage and capacitor voltage of inverting circuit

3. VARIATION OF LOAD AND FREQUENCY ON CONVERSION CIRCUITS

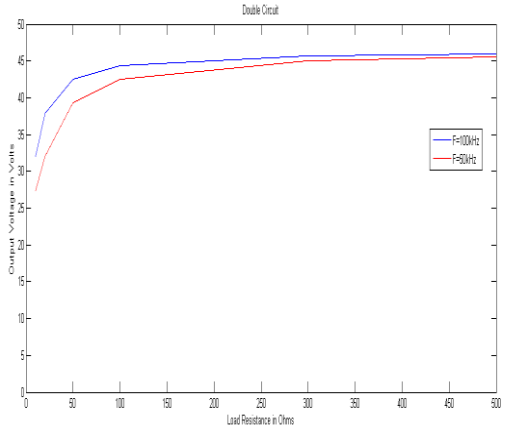
The performance of the above said circuits are analyzed under different loads and frequencies. The results obtained are shown in Figure 11 (a) to Figure 11(e). The input voltages considered are 24V and 12V. The frequency chosen are 50 kHz and 100 kHz. The load is varied from 1 to 500Ω. It is clear that, the performance of the circuit is independent of the switching frequency. The initial voltage shoot increases with frequency, finally settle down to a constant value.



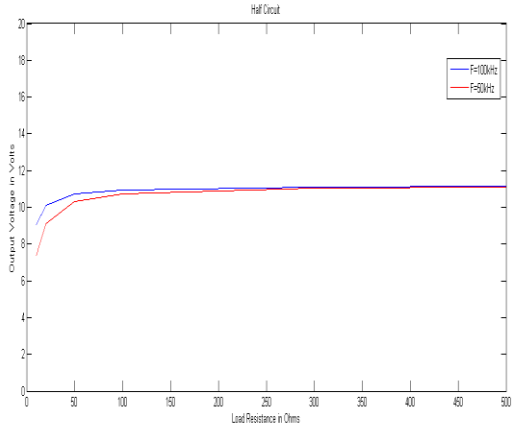
(a)



(b)



(c)



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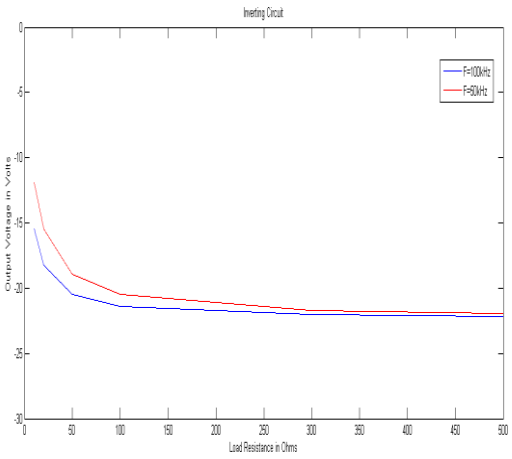


(e)

Figure 12. (a) Summing circuit under variable load and frequency, (b) subtracting circuit under variable load and frequency, (c) double Circuit under variable load and frequency, (d) half circuit under variable load and frequency, (e) inverting circuit under variable load and frequency

4. HARDWARE REULTS AND DISCUSSION

To validate the simulation findings a hardware prototype for summation and subtraction circuit are fabricated. The circuit is tested for the frequencies of 50 kHz, 100 kHz and loads of 100Ω and 330 Ω.

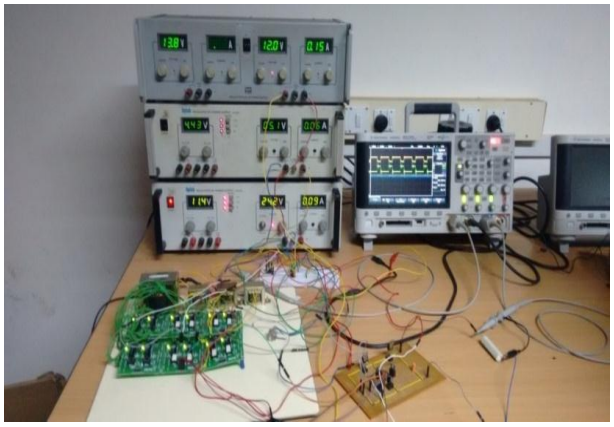


Figure 13. Hardware set up for summation circuit

Figure 13 shows the experimental setup for summation circuit. For a load of 330Ω and switching frequency of 100 kHz, the input voltages given to the summation converter are 24V and 12 V respectively. The output voltage obtained is 32.1V and is shown in Figure 14. This is similar to the values obtained in simulation.

Table 1. Summation Circuit Results for 100 kHz

Load (Ω)	Calculated output voltage (V)	Simulated output voltage (V)	Experimental output voltage(V)
100	33.09	31.52	30.3
330	34.1	33.46	32.1
430	34.23	33.67	32.4

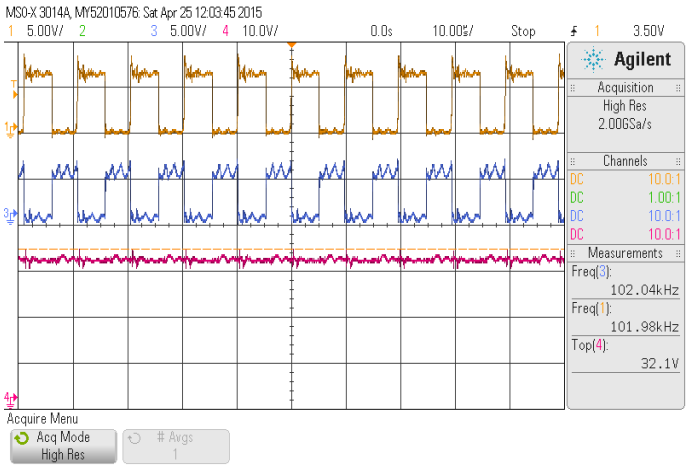
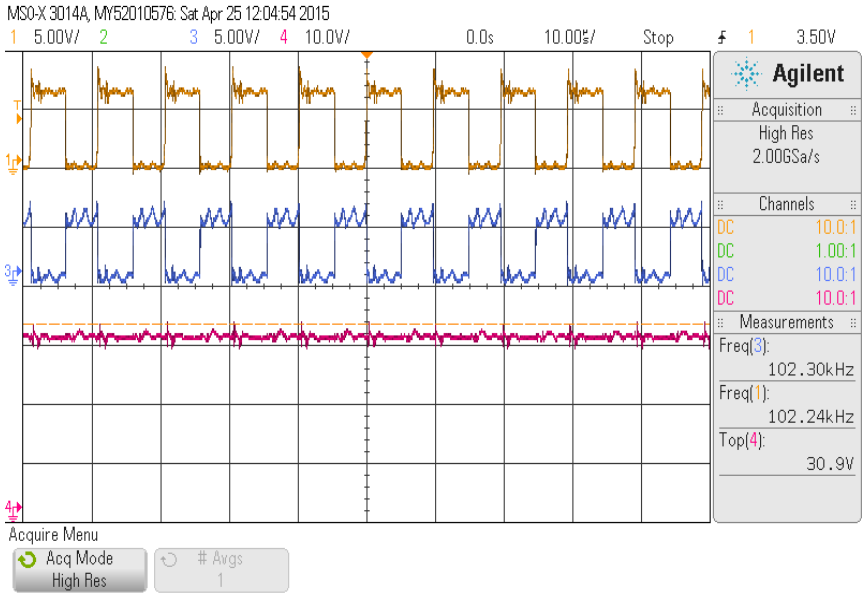


Figure 14. Output voltage for summation circuit

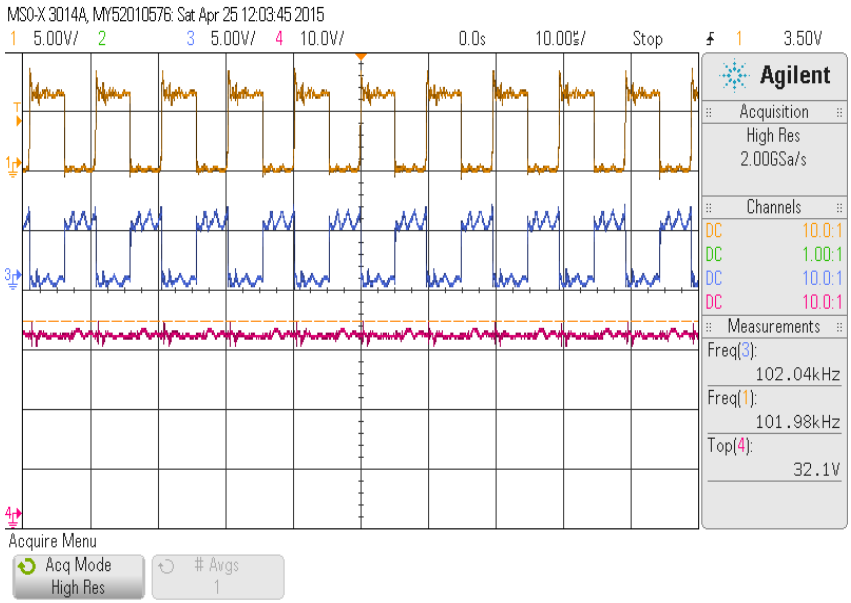
4.1. Variable load with fixed frequency of 100 kHz

When C1 and f are fixed, the variation in frequency is shown in Figure 15(a) and Figure 15(b). indicates the influence of a varying load on Vo. The output voltages for resistances of 100Ω and 330 Ω are shown. It is clear that, the output voltage changes with variation in load resistance. The comparison between

simulated and hardware results are furnished in Table 2.



(a)



(b)

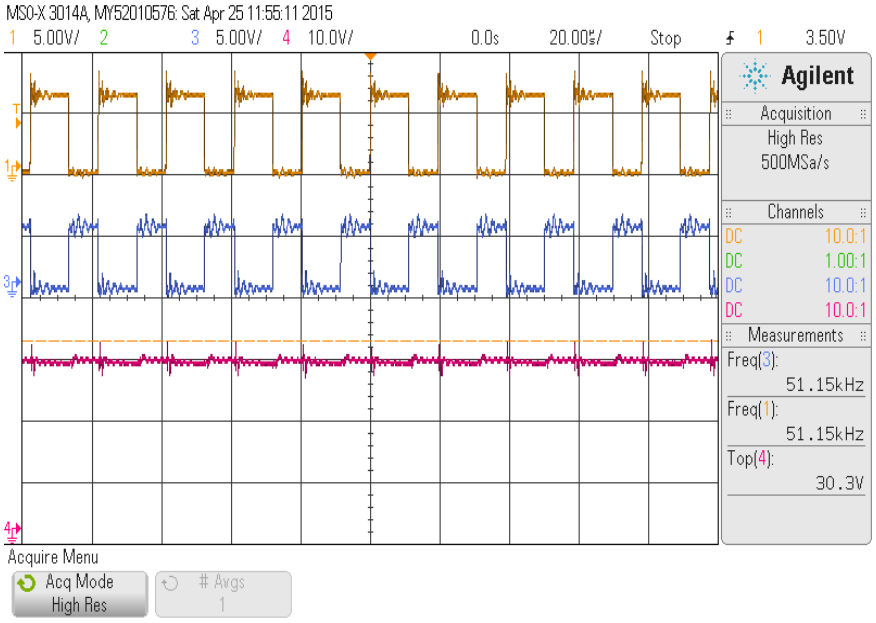
Figure 15. (a) Output voltage for 100Ω, (b) Output voltage for 330Ω

Table 2. Summation Circuit Results for Variable Load

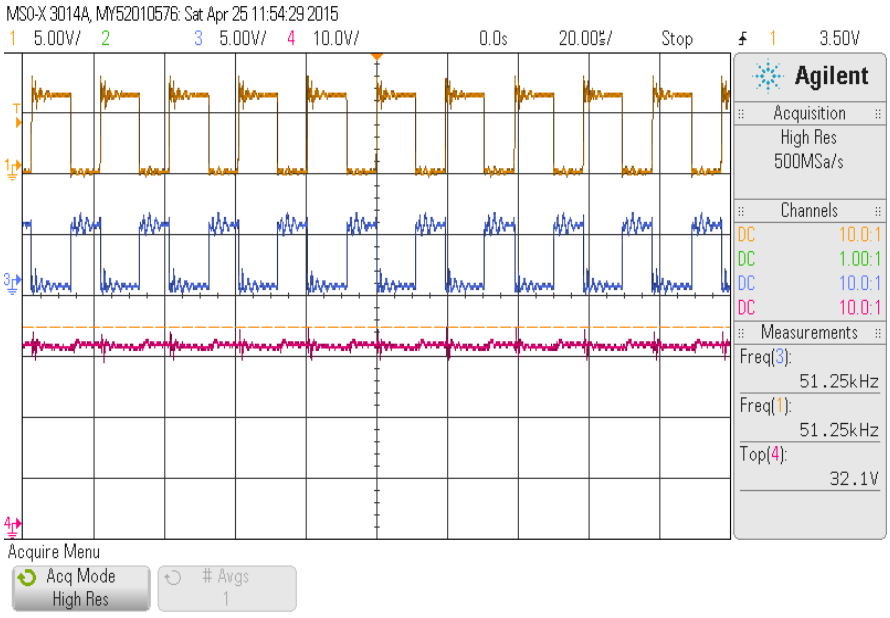
Load (Ω)	Calculated output voltage (V)	Simulated output voltage(V)	Experimental output voltage(V)
100	33.83	32.88	30.9
330	34.36	33.91	32.1
430	34.4	34.02	32.6

4.2. Variable load with fixed frequency of 50 kHz

The hardware output for 50 kHz for variable resistance is shown in Figure 16(a) and Figure 16(b). The output varies with the change in load resistance.



(a)

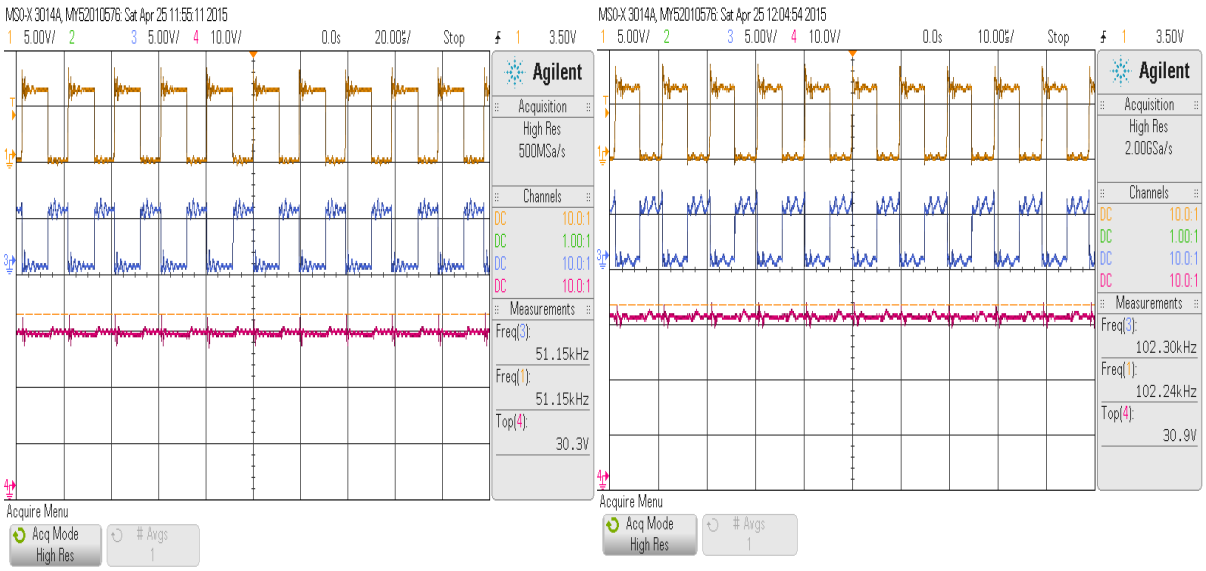


(b)

Figure 16. (a.) Output voltage for 100Ω, (b) output voltage for 330Ω

4.3. Variable frequency with fixed of load 100 Ω

For a fixed load of 100 Ω, the switching frequency is varied for 50 kHz and 100 kHz and the results obtained are shown in fig 17.a and 17.b. The simulated and hardware results are furnished in Table 3. It is clear that, the output depends on both load resistance and frequency.



(a) (a)

Figure 17. (a) Output voltage for 50 kHz, (b) output voltage for 100 kHz

Table 3. Summation Circuit Results for Variable Frequencies

Frequency (kHz)	Calculated output voltage (V)	Simulated output voltage (V)	Experimental output voltage (V)
50	33.09	31.52	30.3
100	33.83	32.88	30.9

4.4. Subtraction circuit

For a load of 330Ω and switching frequency of 100 kHz, the input voltages given to the subtraction converter are 24V and 10 V respectively. The output voltage obtained is 12.2V and is shown in Figure 18.

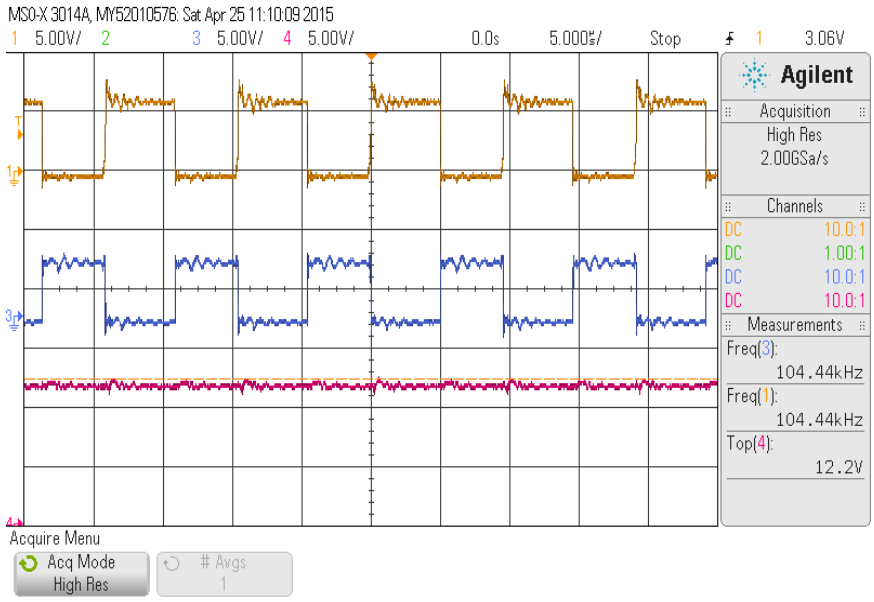


Figure 18. Output voltage for subtraction circuit

Figure 19(a) to Figure 19(b) shows the output voltage at 100 kHz and100Ω, output voltage at 100 kHz and 330Ω, output voltage at 50 kHz and 100Ω, and the output voltage at 50 kHz and 330Ω. Table 4 shows the subtraction circuit results for variable frequencies.

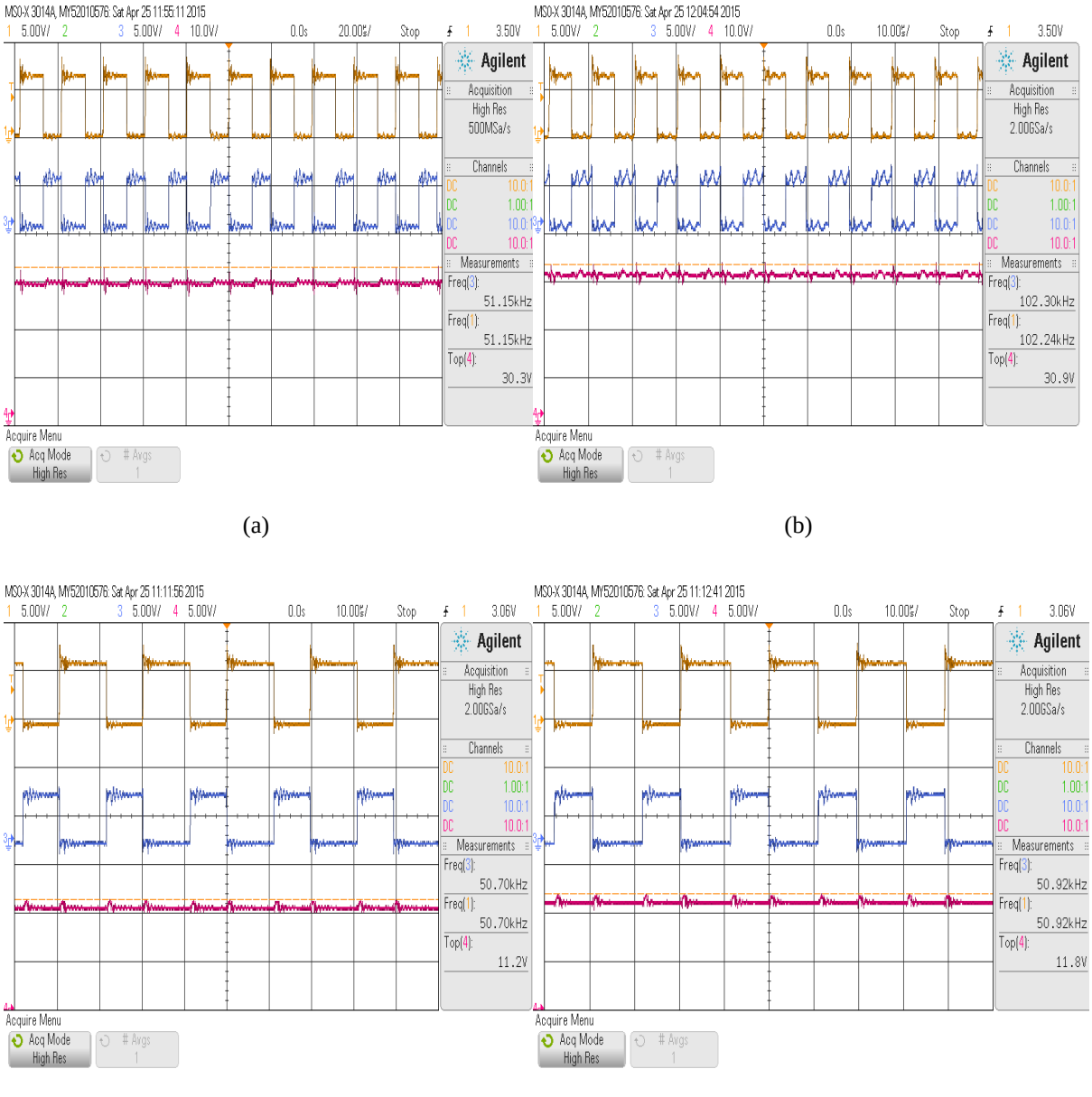


Figure 19. (a) Output voltage at 100 kHz and100Ω, (b) Output voltage at 100 kHz and 330Ω, (c) Output voltage at 50 kHz and 100Ω, (d) Output voltage at 50 kHz and 330Ω

Table 4. Subtraction Circuit Results for Variable Frequencies

Load (Ω)	Frequency = 100 kHz			Frequency = 50 kHz		
	Calculated output voltage (V)	Simulated output voltage (V)	Experimental output voltage (V)	Calculated output voltage (V)	Simulated output voltage (V)	Experimental output voltage (V)
100	12.32	12.11	11.6	12.02	11.85	11.2
330	12.5	12.32	12.2	12.42	12.26	11.8
430	12.53	12.36	12.2	12.46	12.33	12.2

5. CONCLUSION

The performance of various multi input switched capacitor converters are analyzed in this paper. Various topologies namely summation, subtraction, inverting, double and half circuits are simulated under variable load and variable frequencies. The variation in outputs with variable load and frequencies are illustrated. With different switched capacitors topologies mentioned here a multi converter can convert two input voltages can be used to obtain 7 different voltage levels. The results have been experimentally verified for summation and subtraction converters for different loads under different frequencies. These results have been compared with the theoretical and simulated value. This can be extended to three input converters also.

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