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A Unified Codec Scheme for reduction of Area and Crosstalk in RC and RLC Modeled Interconnects using both Bus Encoding and Shielding Insertion Technique

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ABSTRACT

This paper presents a unified codec scheme for reduction of area and crosstalk in RC and RLC modeled interconnects using both bus encoding and shielding insertion technique. It is based upon bus invert method and focuses on 4 bit coupled lines. Previously used codec scheme focused independently on either RC or RLC models and they considered coupling between 5 bit coupled lines i.e. 4 bit data lines and 1 bit control line. However, our proposed codec scheme focuses on all types of couplings i.e. Type-0 to Type-4 and demonstrates an overall reduction in area as well as crosstalk considering coupling between 4 bit coupled lines and isolating the control signal using redundant shielding thus reducing the cases of coupling drastically. The proposed work has been implemented using both Semi Custom and Full Custom design approaches. The model has been described, synthesized and simulated in hardware description language VHDL along with its FPGA implementation. The power consumption has been calculated using Xpower tool of Xilinx. Same model has also been implemented using Cadence Virtuoso Analog Design Suite in 0.18um CMOS technology and the corresponding power, delay and area has been computed. The proposed scheme demonstrates an overall reduction of 76.68% in crosstalk delay and 56.33% in chip area and transistor count. 79.58% power reduction is achieved in full-custom design implementation as compared to semi-custom design implementation.

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1. INTRODUCTION

Interconnects are used to connect different macro cells in a VLSI chip and are also used to distribute clock/ground and other signals within a VLSI Chip. According to International Technology Roadmaps for Semiconductor (ITRS-2011), the circuits to be manufactured in the nanometer scale will contain more than a billion transistors and shall operate at clock frequencies greater than 10 GHz. Therefore, at such higher frequencies we cannot be restricted to RC modeled interconnects only. The effect of inductance comes into existence which cannot be ignored for the proper and accurate operation of the circuit. Mutual inductance if not considered may lead to signal-integrity issues. One of the signal-integrity issues of much concern is Crosstalk. Crosstalk is the coupling of energy from one line to another either through Mutual Capacitance (Electric Field) or Mutual Inductance (Magnetic Field). In the RC Modeled interconnects, the worst case crosstalk occurs when the adjacent wires have an opposite transition. On the contrary, this worst case pattern

is the best case for RLC Modeled Interconnects [1]. A few common methods to reduce crosstalk and subsequently the power consumption are insertion of repeaters in between the interconnect length, insertion of shielding between adjacent wires, minimizing spacing between signal and ground lines, isolating critical signals from the other signal lines, terminating signal lines into their characteristic impedance and bus encoding methods [2].

Based upon the study investigations, a unified encoding method has been proposed and implemented at both full-custom and semi-custom level which deals with both RC and RLC modeled interconnects. It aims at reducing all the types of crosstalk couplings (Type-0, Type-1, Type-2, Type-3 and Type-4) by reducing the switching and coupling activity and thus causing a reduction in the power consumption.

The rest of the paper is organized as follows: Section II describes the various types and cases of crosstalk couplings and power dissipation in RC and RLC modeled interconnects. Working and implementation of the proposed work has been explained in Section III. Simulation Results have been discussed in Section IV. Section V compares the proposed design with previous work and Section VI concludes the paper.

2. CROSSTALK COUPLINGS AND POWER DISSIPATION IN VLSI INTERCONNECTS

Coupling between the groups of three wires may be classified into 5 categories namely, Type-0, Type-1, Type-2, Type-3 and Type-4. Type-0 and Type-1 are the worst cases of crosstalk that occur in RLC modeled Interconnects. Here capacitive coupling is almost negligible. Type-3 and Type-4 are the worst cases of crosstalk in RC modeled interconnect and inductive coupling here is almost negligible [1&2].

Table 1. Different types of crosstalk couplings

TYPE-0	TYPE-1	TYPE-2	TYPE-3	TYPE-4
- - -	- -↑	- ↑ -	- ↑↓	↑↓↑
↑↑↑	-↑↑	↑↑ -	- ↓↑	↓↑↓
↓↓↓	↑- -	↑ - ↓	↑↓ -	
	↑↑-	↑↑↓	↓↑ -	
	- -↓	↑↓↓		
	-↓↓	- ↓ -		
	- -↓	↓ - ↓		
	↓↓ -	↓ - ↑		
		↓↓↑		
		↓↑↑		

↑: transition from 0 to 1; ↓: transition from 1 to 0; -: no transition

In CMOS circuits power dissipation is mainly due to two components, Static Dissipation and Dynamic Dissipation. Power dissipation is VLSI interconnects can be given by the expression [1&2]

$$P = \alpha V_{DD}^2 f C_L \quad (1)$$

Where, C_L is the load capacitance, V_{dd} is the power supply voltage, f is the clock frequency and α is the switching activity whose value lies between 0 and 1. Thus for low power consumption any one of the parameter in given expressions has to be reduced. In this work focus has been on reducing the number of signal transitions (α).

3. PROPOSED WORK IMPLEMENTATION

The figure 2 shows the implementation of a unified scheme proposed in this works for both RC and RLC modeled interconnects. Model consists of a transition detector, separate type-0, type-1, type-2, type-3 and type-4 crosstalk coupling detectors. XOR gates are used at both the transmitter and receiver side for accurate and reliable encoding and encoding of the transmitted 4 bit data. Transition Detector acts as a comparator and compares the 4 bit present input with the previously transmitted 4 bit data. 8 bit output of the transition detector acts as an input to the type-0, type-1, type-2, type-3 and type-4 coupling detectors which detect that whether the transitions detected by the transition detector cause crosstalk or not. The output of the

coupling detectors will go 'High' if any of the cases shown in table 1 is encountered. OR Logic is used to generate the control signal. XOR Stack1 is used to transmit the encoded data along with the control signal to the output side**.** Shielding is used to transmit the control signal. At the output side XOR Stack2 is used to decode the received encoded data depending upon the status of the control signal.

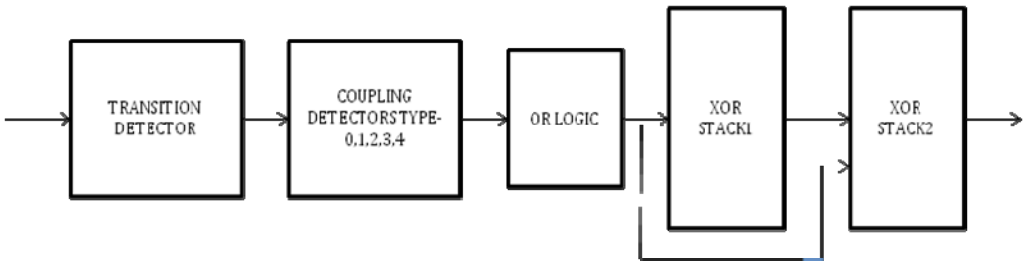

Figure 2. Block Diagram of the proposed codec scheme implementation

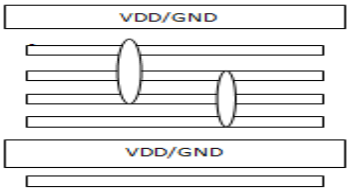

Figure 3. Interconnect routing for a 4 bit bus

Figure 3 shows the interconnect routing approach followed for proposed work. Control bit line is isolated from the 4 bit interconnect model by using the shielding approach thus, reducing the cases of the possible couplings that could occur.

4. SIMULATION RESULTS

The codec scheme has first been described in VHDL and simulated using Model Sim simulator. FPGA implementation has been done using Xilinx Spartan3 FPGA family, XC3S200 device and PQ208 package. The whole design is synthesized using Xilinx Synthesis Tool (XST). The power consumption results are computed using Xpower tool of Xilinx ISE suite. Then it has been implemented and simulated using Cadence Virtuoso Analog Design Suite. Simulation Results have been computed for 16 combinations of input data. Pre-layout and post-layout simulations were performed to verify the proposed codec scheme. The power consumption and propagation delay results have been computed at 0.18µm technology node.

4.1. HDL Implemetation Simulation Results

Figure 4 shows the simulation waveform of the Transition Detector. It compares the present data with the previously transmitted data stream. Its output ***Sa*** to ***Sd*** goes high when low to high transition occurs and ***Sh*** goes high when high to low transition occurs and ***Si*** to ***Sl*** when no transition occurs.

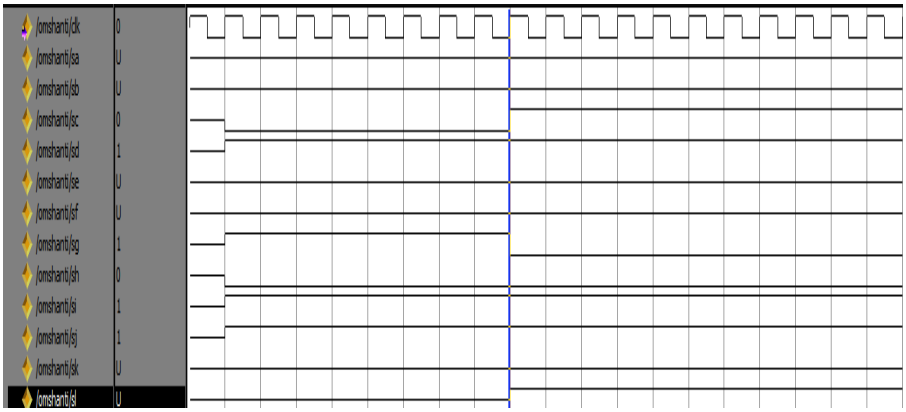

Figure 4. Simulation Waveforms of Transition Detector

Depending upon the output of the Transition Detector, Type-0, Type-1, Type-2, Type-3 and Type-4 coupling detectors output may go 'high' if any of the crosstalk couplings as shown in figure 5.

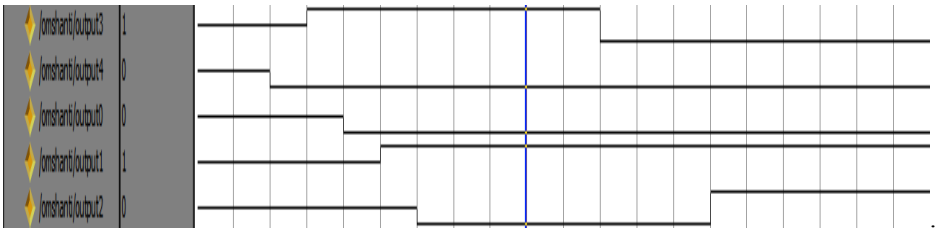

Figure 5. Simulation Waveforms of Crosstalk Couplings

OR logic output is given by signal ***rb1***.If ***rb1*** is of 'low' logic then original input data stream is send through the interconnect model along with the shielded control bit. If the output of OR logic is 'high' then the inverted input data along with the shielded control bit is send to the output side, therefore reducing the switching activity and thus the coupling activity. Final output of the implemented codec scheme is shown in Figure 6.

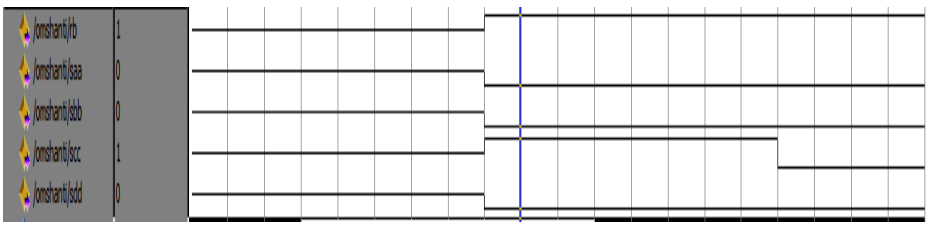

Figure 6. Output Simulation Waveforms of the Implemented Codec Scheme

Table 2 shows the total power consumption by the implemented codec scheme as per the semi-custom design approach.

Table 2. Power Analysis Summary

Power summary:	I(mA)	P(mW)
Total estimated power consumption		24
Quiescent Vccint 1.20V	5	6
Quiescent Vccaux 2.50V	7	18

According to the timing summary, the maximum output required time after clock is 4.770ns, clock period and delay computed is 5.518ns (frequency: 181.225MHz) and 5.518ns (Levels of Logic = 2)

4.2. Analog Schematic and Layout Generation and Simulation Results.

Out of the 16 implemented cases when 4 bit input data 1000 was compared with the previously transmitted data 0111 the power consumed was maximum. Figure 7 to Figure 13 shows the simulation waveforms of the individual blocks.

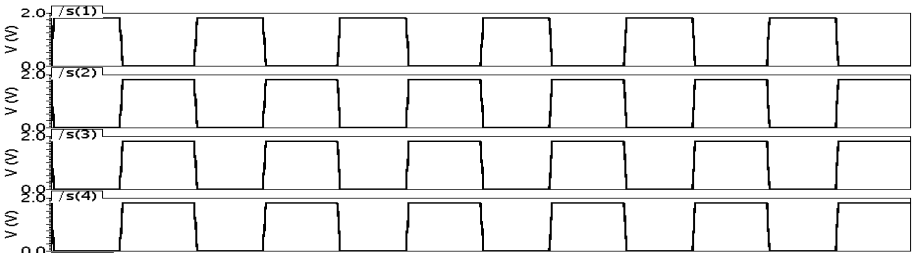

Figure 7. Present data input 1000

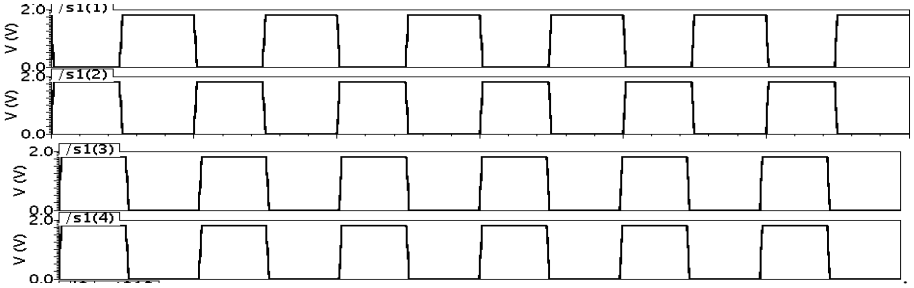

Figure 8. Previous data input 0111

Transition Detector compares the present data with the previously transmitted data as shown in figure 9. ***Sa*** to ***Sd*** are the outputs of the transition detector used to detect low to high transitions. ***Se*** to ***Sh*** are the outputs of the transition detector used to detect high to low transitions.

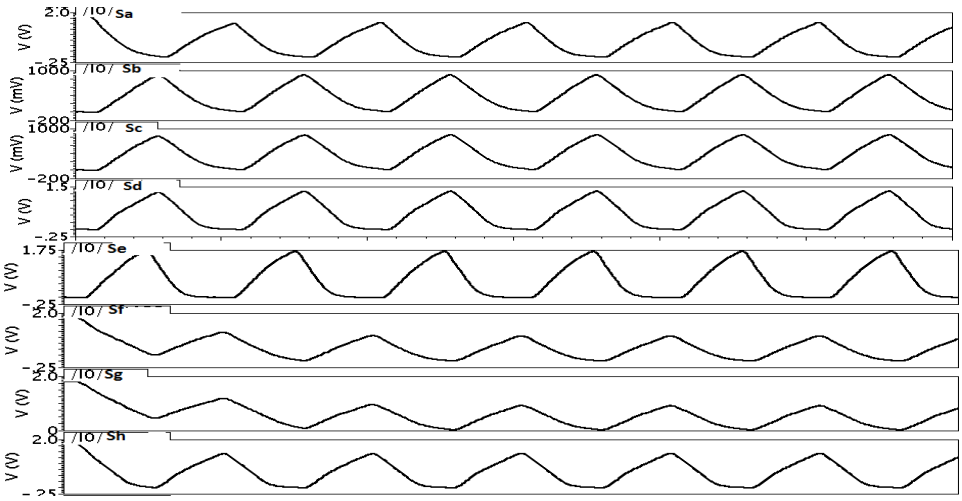

Figure 9. Transition Detector outputs ***Sa*** to ***Sh***

Outputs of the transition detector acts as an input to the various coupling detectors which detect whether the transitions detected by the transition detector result in any of the cases of crosstalk couplings as shown in Table 1. Figure 10 shows ***Out 0*** to ***Out 4*** outputs of the coupling detectors.

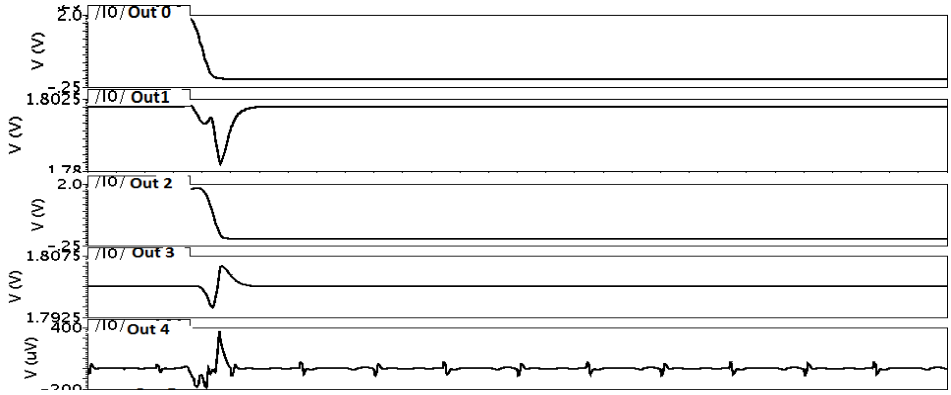

Figure 10. Type 0, Type 1, Type 2, Type 3, Type 4 Coupling Detector outputs

OR logic is used to generate the 1 bit control signal ***Out5*** by ORing the outputs of the coupling detectors as shown in figure 11. It is also transmitted to the output side via shielding.

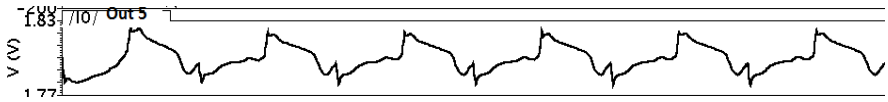

Figure 11. Control Signal

Input data along with the control signal is input to the XOR Stack which encodes the data ***X1*** TO ***X4*** and transmits it through the 4 bit interconnect lines to the output side as shown in figure 12.

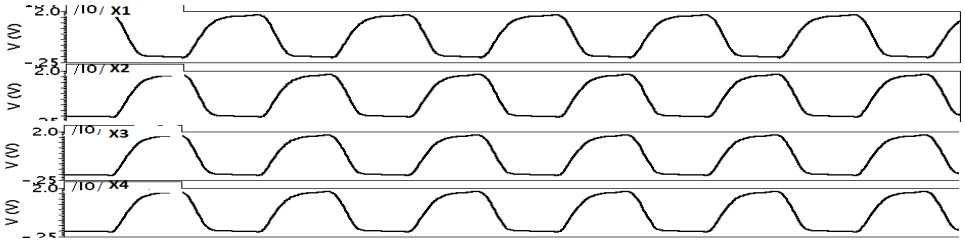

Figure 12. Encoded data at the output of XOR Stack1

O1 to ***O4*** are the outputs of the XOR Stack2. XOR Stack is used at the Output Side so as to decode the transmitted data transmitted data.

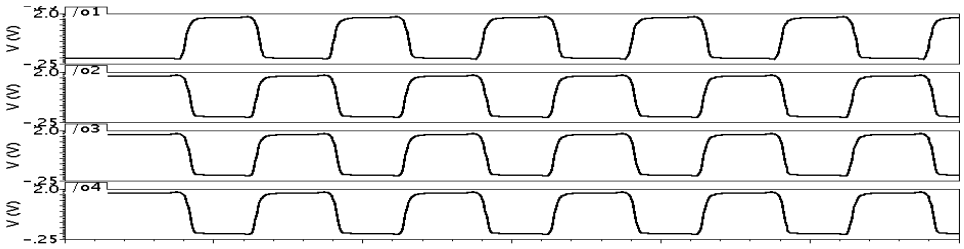

Figure 13. Decoded Data at the output of XOR Stack2

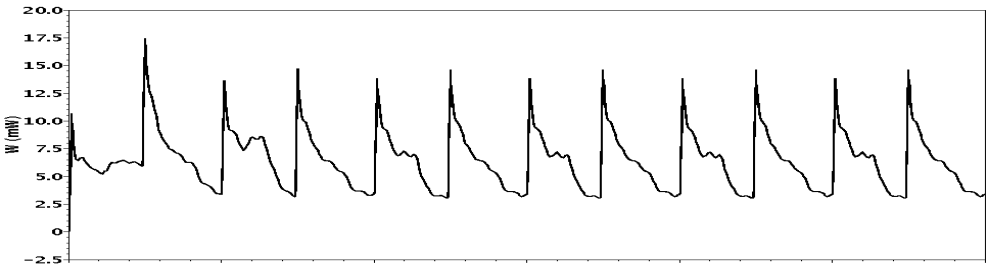

Figure 14. Total Power Plot

Figure14 shows the power plot of the total codec scheme.
Layout of the implemented codec scheme is shown in figure15 where different circles represent different blocks
CIRCLE1: Layout of the Transition Detector
CIRCLE2: Layout of the Type-0 Coupling Detector
CIRCLE3: Layout of the Type-1 Coupling Detector
CIRCLE4: Layout of the Type-2 Coupling Detector
CIRCLE5: Layout of the Type-3 Coupling Detector
CIRCLE6: Layout of the Type-4 Coupling Detector
CIRCLE7: Layout of the OR Logic
CIRCLE8: Layout of the XOR Stack1
CIRCLE9: Layout of the XOR Stack2

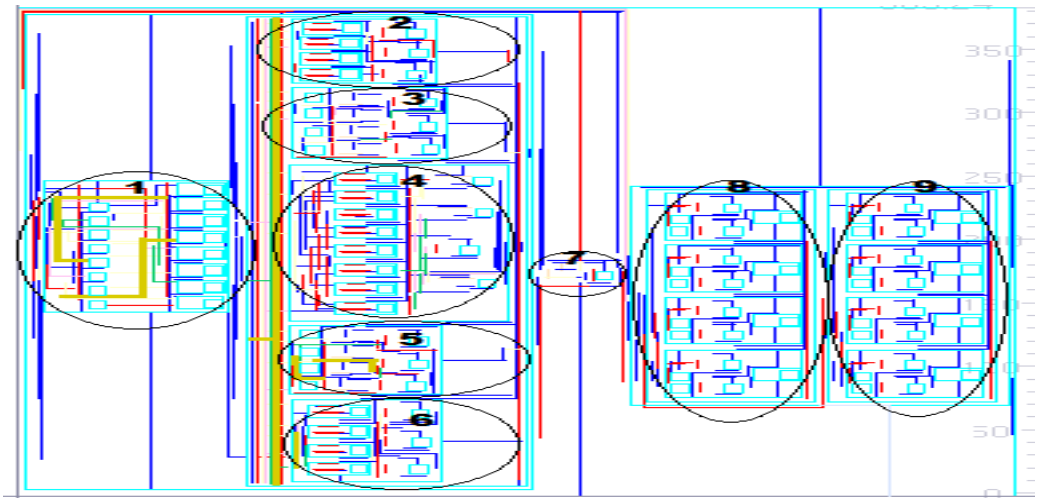

Figure 15. Complete Layout of the Implemented Codec Scheme

Table 2 shows the pre and post layout power and delay results.

Table 2. Power and Delay Summary

Parameter	Pre-Layout	Post-Layout
Power (mW)	4. 083	4.686
Delay (ps)	414.7	722.7

Table 3 compares the Semi-Custom and Full-Custom power and delay results**.**

Table 3. Full-Custom and Semi-Custom Power and Delay Comparison

Parameter	Semi-Custom	Full-Custom
Power (mW)	20	4. 083
Delay (ps)	5518	414.7

Table 4 compares the present work with the previous work

Table 4. Comparison of present and previous work

BLOCK	[1]	[2]	PROPOSED WORK
Transition Detector(gates)	20	--	16
Type-0 Detector(gates)	--	15	7
Type-1 Detector(gates)	--	15	11
Type-2 Detector(gates)	--	--	12
Type-3 Detector(gates)	15	--	11
Type-4 Detector(gates)	15	--	7
XOR Stack (gates)	8	8	8
Number of Transistors	284	284	268
Propagation Delay(ps)	296	1779	414.7

5. CONCLUSION

This work demonstrated a unified method to detect the various types of crosstalk couplings with the semi-custom and full-custom design implementations. All the possible cases of crosstalk were implemented and tested using Spartan3 FPGA kit and Cadence Analog Virtuoso Design Suite. Power analysis was done using the Xpower tool of Xilinx ISE Suite for semi-custom design. The power & time delay calculations are performed for same codec scheme using Visualization & Analysis XL Calculator provided in Cadence Spectre tool for full custom design in 0.18µm CMOS technology.

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