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A 5.9 GHz Low Power and Wide Tuning Range CMOS Current-controlled Ring Oscillator

PraptoNugroho*/*, Ramesh K. Pokharel**, HaruichiKanaya*, KeijiYoshida***
* Graduate School of Information Science and Electrical Engineering, Kyushu University
** Center for Japan Egypt Cooperation in Science and Technology, Kyushu University
*** Departement of Electrical Engineering and Information Technology, UniversitasGadjahMada

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ABSTRACT

Designing low power, low noise, wide tuning range and small size circuit in one single chip is very challenging. This paper describes alow power, wide tuning range three-stage current-controlled ring oscillator (CCO) which has been designedon 0.18µm CMOS technology. The CCO circuit has tuning range from 251 MHz to 5.5 GHz or it has tuning width 183%. Using 1.8V supply voltage, the CCO circuit consumes current from144 µA to 9.76mA. Phase noise is -104 dBc /Hz at 5.5 GHz and 4Mhz offset frequency. FoM is -154.4 dBc /Hz which is the best among published counterpart papers. The size of the core oscillator circuits without bonding pads is only 0.0003 mm^2.

Corresponding Author:

PraptoNugroho,
*Graduate School of Information Science and Electrical Engineering, Kyushu University,
Motooka 744, Nishi-ku, Fukuoka 819-0395, Japan.
***Departement of Electrical Engineering and Information Technology,Faculty of Engineering,
UniversitasGadjahMada,JalanGrafika No 2, Yogyakarta 55281, Indonesia.
Email: tatok@ugm.ac.id

1. INTRODUCTION

Oscillator is a crucial component in phase-locked loop (PLL) and phase locked loop is one of the key elements in many communication devices and circuits. According on its controlling input, oscillator can be classified into two groups, voltage-controlled oscillator (VCO) and current-controlled oscillator (CCO) as shown in Fig. 1(a) and 1(b).Among the oscillator types, LC oscillator is widely used because it has better phase noise. However, LC oscillators have narrow tuning range and need large die area. Ring oscillatorsin the other hand provide wide tuning range, relatively constant voltage swing and low voltage operation [1], [2], [7]. These oscillators also require less die area compared with LC counterpart and can be built in any standard CMOS processes.

Various topologies of ring oscillator circuits have been reported in the literatures. Among them, three-stage ring oscillator topology has been reported successfully in [8], [11] and [12]. This success makes three-stage topology very attractive.

This paper presents the analysis and design of 5.5 GHz controlled oscillator in which its frequency varies linearly with its load current source or it can be written as a current controlled oscillator (CCO). Circuit architecture is described in Section II along with a simplified analysis for its frequency of oscillation. Section III presents oscillator design and post layout simulation results. Finally, Section IV concludes the paper.

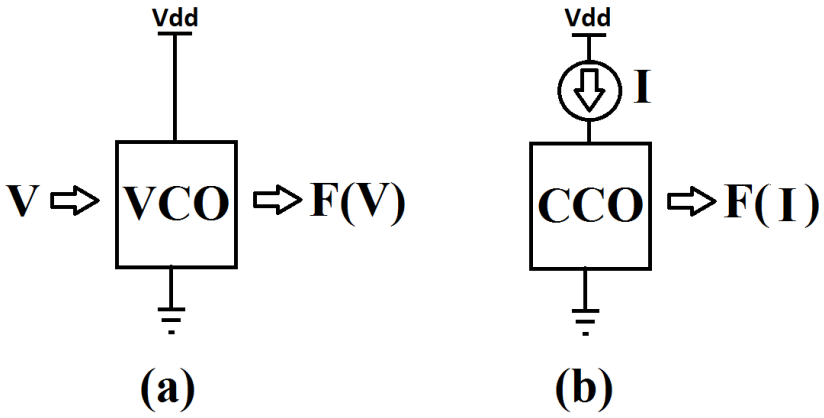

Figure 1.A block diagram of a VCO (a) and CCO (b).

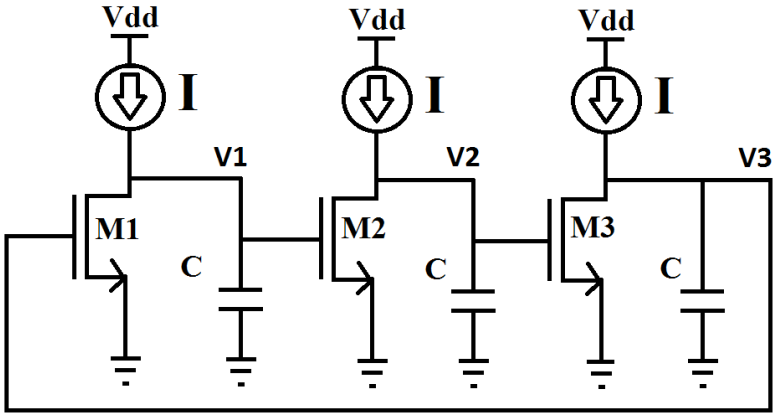

Figure 2.Circuit of the proposed three-stage ring oscillator with current load.

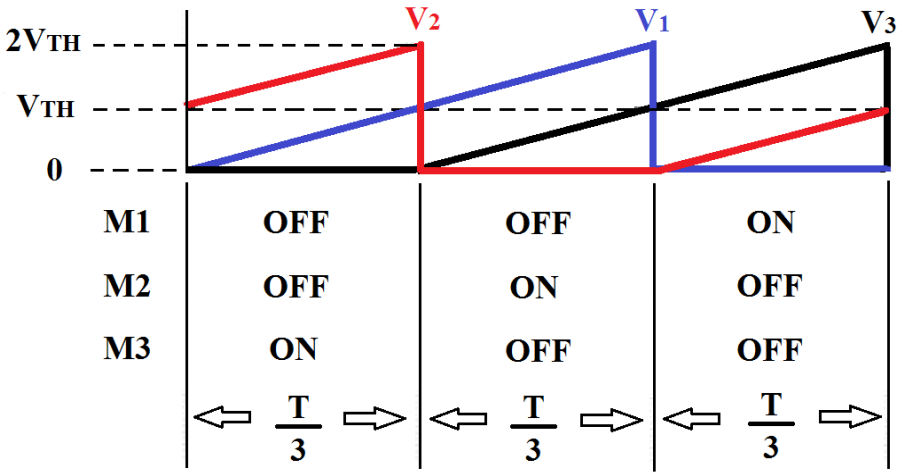

Figure3.Simplified steady state oscillating waveforms.

2. CIRCUIT ARCHITECTURE

Fig. 2 shows general topology of the proposedcurrent-controlled ring oscillator. It is based on a three-stage inverting ring oscillator [2]. Inverting stage consist of NMOS inverters driving a current source. Current source can be implemented by using resistive load circuit.

A simplified analysis of this circuit by using a switch model of NMOSis provided by [5]. The NMOS assumed becomes short circuit when its gate-source voltage V_{GS} exceeds its threshold voltage V_{TH}. By this assumption,only one NMOS can turn on at any given time. Assumed the three NMOS devices are identical or in other word they have same V_{TH}, the total period T can be divided equally by the ON duration of each transistor as shown in Fig. 3.

It can be seen from the picture thatone NMOS can turnon for T/3period and turn off for another 2T/3when the charging process in the capacitor is taking place. An NMOS is ON when its gate voltage reach threshold voltage (V_{TH}) and OFF when its gate voltage reach $2V_{TH}$. Voltage rises from $V_{TH}$to $2V_{TH}$in T/3 period. Thus NMOS is ON in T/3 period. For example, in the first T/3 periode when the output of M1 (V1) rises from zero to some point before V_{TH}, the next transistor (M2) is still turned off. M2 is turned on when V1 reach some point above V_{TH}.M2 is turned onuntilV1 reach $2V_{TH}$in T/3 period. When M2 turn on, its output (V2) goes to ground. Thus, because V2 supply the gate of M3, M3 change its state from turning on to turning off which then the charging process of C2 is taking place. Each transistor is turned on for T/3when its output is zero and it is turned off for another T/3 during charging time of output capacitor byI.Thus,the output rises from zero at a slope of I/C and then turn on the next transistor in the ring. Therefore,based on this mechanism, we can derive formulae to obtain the period of the oscillation as follows

$$T = \frac{3C}{I} V_{TH} \quad (1)$$

Thus

$$f = \frac{I}{3CV_{TH}} \quad (2)$$

It shows that frequency varies linearly with current which is a desirable property for phase-locked applications. The minimum supply voltage can be calculated by looking at the maximum output voltage $2V_{TH}$ added by the minimum operating voltage of the current source as below

$$V_{DD}(\min) = 2V_{TH} + V_I \quad (3)$$

where$V_I$is the minimum operating voltage of the current source that can be minimized by the use of PMOS device as current source. It can be as low as PMOS overdrive voltage.

In practice, steady state oscillating waveform cannot behave as ideal as shown in Fig. 3 because the circuit needs a small duration (δ) for discharging each output capacitor since an NMOS cannot have zero resistance when turn on. Fig.4 illustrates this behavior.

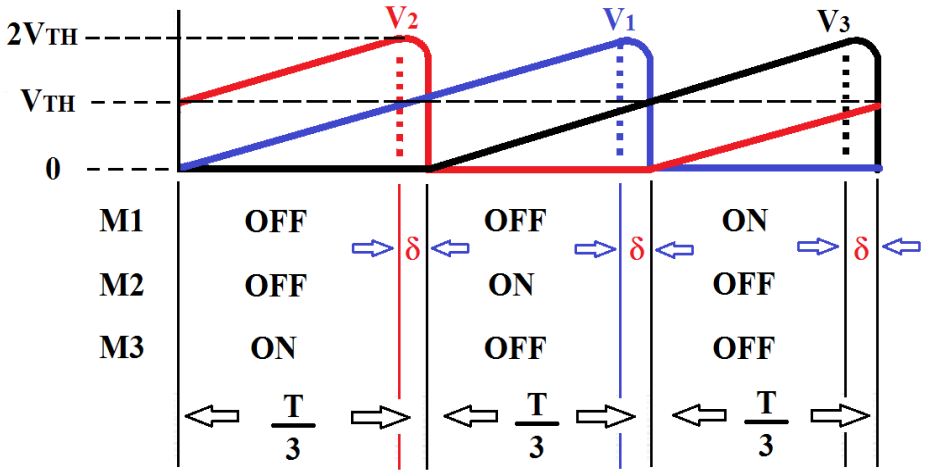

Figure4. Steady state waveforms when each NMOS has finite W and L.

This behavior has an increasing effect on its period of oscillation (T), which is derived as follows.

$$V_{TH} = V_L + \frac{\left(\frac{IT}{3} - I\delta\right)}{C} \quad (4)$$

$$V_H = V_{TH} + \frac{IT}{3C} \quad (5)$$

where VL≈ 0 is the minimum drain voltage of an NMOS to carry current. The dynamic equation during this duration is derived as

$$C\frac{dv}{dt} = I - \frac{I^2 t^2 \beta}{2C} \quad (6)$$

where voltage at t = 0 to δ is V_H and V_{TH}, while $\beta = \mu_n C_{ox} \frac{W}{L}$

By doing some integration and algebraic manipulation at the above equations, we can come up with an exact formulae to determining T as given by

$$T = \frac{3C\left((V_{TH} - V_L) + 3\sqrt{\frac{n}{2} + \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}} + 3\sqrt{\frac{n}{2} - \sqrt{\frac{n^2}{4} + \frac{m^3}{27}}}\right)}{I} \quad (7)$$

3. CIRCUITS DESIGN AND POST LAYOUT SIMULATION RESULTS

Fig.5 shows the core circuit of the proposed current-controlled oscillator circuit. M1, M2, M3 are the main inverting stage, while M4, M5, M6 are the resistive load circuits. However, resistive load devices that commonly formed using NMOS static inverters are now replaced by PMOS resistive load so that power consumption depends directly on the current. Hence, spike that is caused by voltage supply which is typically found in a static inverter has been removed. Using PMOS as current source made V_{DS} can be as low as overdrive voltage that increases output voltage swing. PMOS load gate is operated in saturation region by connecting the gate to ground to obtain maximum current load. There is no capacitance used in order to get high frequency output, but there are parasitic capacitances at the output nodes that cannot be eliminated which can reduce frequency output.

The chip is implemented in 0.18μm CMOS technology. Picture of the chip layout is shown in Fig. 6. The size of the core oscillator and digital control circuits include bonding pads is 0.09 mm^2 (0.0003 mm^2 without bonding pads). This is noted as the smallest chip area compared to the published papers.

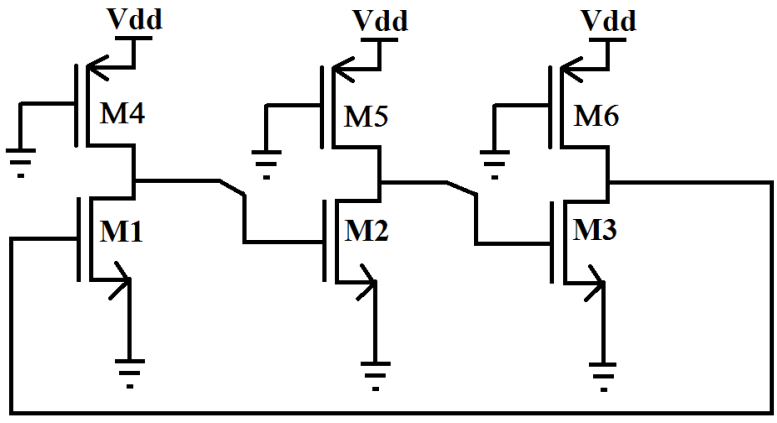

Figure 5.Schematic of the designed circuit.

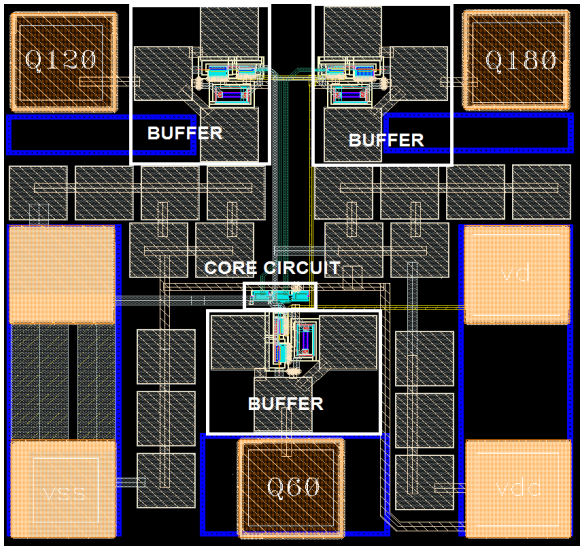

Figure 6. Chip layout of the proposed CCO

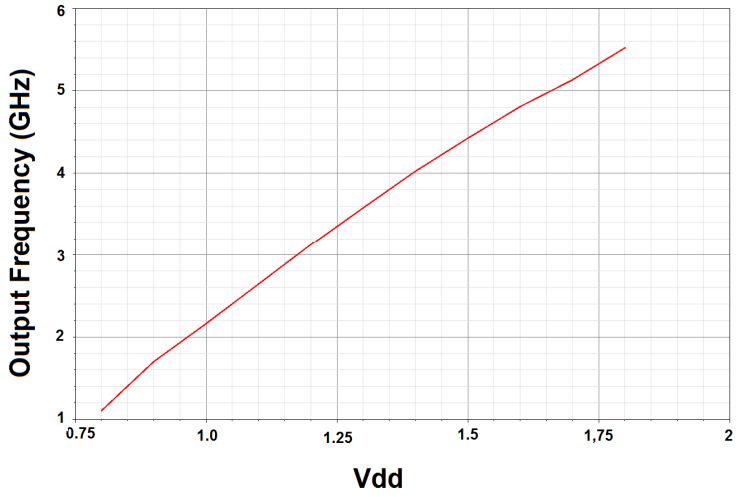

Figure 7. Tuning curve of the proposed CCO.

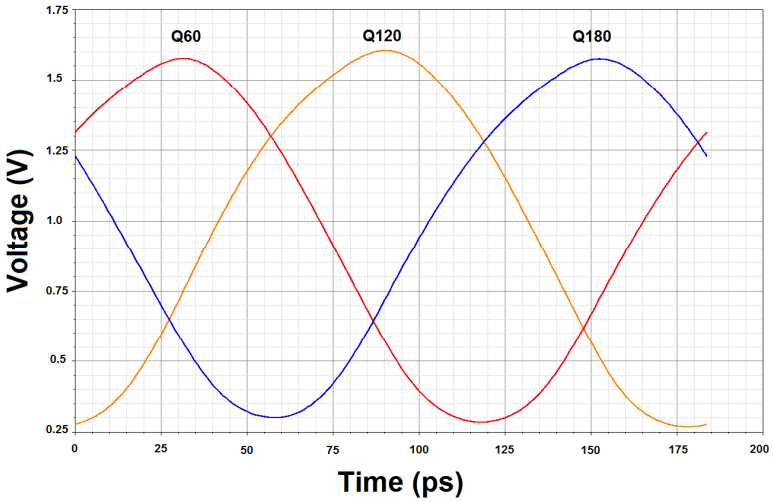

Figure 8. Output waveform at 5.5 GHz.

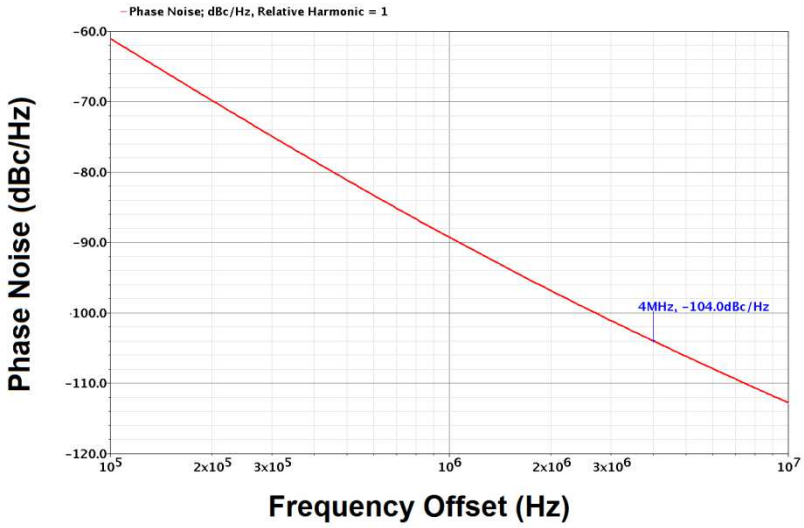

Figure 9. Phase noiseofthe proposed current-controlled oscillator at 5.5 GHz

Table 1.Performance Comparison.

Ref.	Freq. (GHz)	Technology	Pdc (mW)	Area (mm2)	Tuning range	PN (dBc/Hz)	Offset (MHz)	FoM (dBc/Hz)
[8]	2	BiCMOS 0.6 µm	17	0.023	19%	-75	1	-140.2
[9]	2.2	BiCMOS 0.5 µm	100	0.5	84%	-106	2	-146.8
[3]	3.6	CMOS 0.18 µm	17	0.24	70%	-90.1	1	-148.9
[10]	2.2	BiCMOS 0.6 µm	11.8	-	-	-94	1	-150.3
[4]	11.5	BiCMOS 0.5 µm	75	0.13	16%	-94.3	2	-150.7
[12]	3.5	CMOS 0.18 µm	16.2	-	189%	-106	4	-152.7
[11]	10	inP HBT	250	0.85	-	-97	1	-153
[6]	1.8	Bipolar	22.5	-	32%	-82	1	-153.6
This work	**5.5**	**CMOS 0.18 µm**	**17.5**	**0.0003**	**183%**	**-104**	**4**	**-154.4**

----- Not Available

Fig. 7 shows the measured CCO tuning range. It shows a linear tuning curve. Tuning range is obtained by varying its voltage supply from 0.8V to 1.8V resulting output frequencies from 251 MHz to 5.5 GHz or about 183% wide.Output waveform in 5.5 GHz is shown in Fig. 8 which shows voltage swing more than 1.5 Volt. Phase noise -104 dBc/Hz at 4 MHz offset frequency from 5.5 GHz carrier frequency is shown in simulation result in Fig. 9. Current consumption noted as low as 9.76 mA at 1.8V supply voltage. At 251 MHz, phase noise and power consumption is -79 dBc/Hz and 68.4 mW respectively.

Table I summarize and compare the performance of the proposed current-controlled oscillator (CCO) to the recently published papers on the same technology. It can be seen that the proposed (CCO) has the best FoM performance. It has also wider tuning range. The proposed CCO also exhibits a low power for high frequency output with adequate phase noise. Figure of merit (FoM) of the proposed CCO is -154.4 dBc/Hz, by using FoM definition as

$$FoM = -20\log\left(\frac{f_o}{\Delta f}\right) + L(\Delta f) + 10\log P_{dissp(mW)} \quad (9)$$

withf_{osc}, 1/*f*, L (1/*f*), and $P_{\text{dissp(mW)}}$ denoting oscillation frequency, offset frequency, phase noise in dBc/Hz and power consumption in mW, respectively.

4. CONCLUSIONS

In conclusion, a CMOS three-stage current controlled ring oscillator based on an inverting NMOS with current load is analyzed and designed. The post layout simulation shows that the proposedcurrent-controlled oscillator (CCO)circuit consumes small current to produce high frequency output. The proposed CCO has better performance compared to the published referred papers. FoM comparison result shows proposed CCO to be the best among published results. It has linear and wide tuning range and has very small chip area which makes it suitable for PLL and clock generation.

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BIOGRAPHY OF AUTHORS

PraptoNugroho
receivedB.Eng degree in Electrical Engineering from GadjahMada University, Yogyakarta, Indonesia in 2000 and M.Eng Degree in Electrical Engineering from Chulalongkorn University, Bangkok, Thailand in 2007. From 2000-2005 he was with semiconductor packaging and testing companies, Yoshikawa Electronics Bintan and Omedata Electronics as a Product and a Test Engineer respectively. Then from 2005-Now, he joined Dept. of Electrical Engineering and Information Technology (JTETI), GadjahMada University as faculty member. He is currently a Ph.D student in the Dept. of Electronics, Kyushu University, Fukuoka, Japan.

Ramesh K. Pokharel
received the M. E. and Doctorate degrees from the University of Tokyo, Japan in 2000 and 2003, respectively all in electrical engineering. He had short academic and industrial experiences in Nepal before he joined the University of Tokyo in 1997 as a research student. He had been a post-doctoral research fellow with the Department of Electrical Engineering and Electronics, Aoyama Gakuin University, Japan from April 2003 to March 2005. In April 2005, he joined the Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, and since September 2010, he has been a Professor at the Center for Japan-Egypt Cooperation in Science and Technology, Kyushu University. His current research interests include the low cost RFIC and analog circuits for microwave and millimeter wave wireless communications, on-chip signal integrity issues, and on-chip meta-materials in CMOS. He is a member of the IEEE. Dr. Pokharel was a recipient of the Monbu-Kagakusho Scholarship of the Japanese Government from 1997-2003, and an excellent COE research presentation award from the University of Tokyo in 2003.

HaruichiKanaya
was born in Yamaguchi, Japan, in 1967.He received the B.S. (Physics) degree from Yamaguchi University in 1990, and the M.E. (Applied Physics) and D.E. degrees from Kyushu University in 1992 and 1994, respectively. In 1994, he became a Research Fellow (PD) of the Japan Society for the Promotion of Science. In 1998, he was a visiting scholar at the Massachusetts Institute of Technology (MIT), USA. He is currently engaged in the study and design of RF CMOS System LSI and superconducting microwave devices, as an Associate Professor in the Department of Electronics, Graduate School of Information Science and Electrical Engineering, and also System LSI Research center, Kyushu University. Dr. Kanaya is a member of the Institute of Electrical and Electronics Engineers (IEEE).

Keiji Yoshida
was born in Fukuoka, Japan, in 1948. He received the B.E., M.E. and Dr. Eng. degrees from Kyushu University in 1971, 1973 and 1978, respectively. He is currently engaged in the study of applications of superconducting thin films to microwave and optical devices and design of RF-LSI chips for SoC, as a Professor in the Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University. Dr. Yoshida is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the Japan Society of Applied Physics.