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Full on-chip low dropout voltage regulator with an enhanced transient response for low power systems

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ABSTRACT

A full on chip low dropout voltage regulator (LDO) with fast transient response and small capacitor compensation circuit is proposed. The novel technique is implemented to detect the variation voltage at the output of LDO and enable the proposed fast detector amplifier (FDA) to improve load transient response of 50mA load step. The large external capacitor used in Conventional LDO Regulators is removed allowing for greater power system integration for system-on-chip (SoC) applications. The 1.6-V Full On-Chip LDO voltage regulator with a power supply of 1.8 V was designed and simulated in the 0.18µm CMOS technology, consuming only 14 µA of ground current with a fast settling-time LNR(Line Regulation) and LOR(Load regulation) of 928ns and 883ns respectively while the rise and fall times in LNR and LOR is 500ns.

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1. INTRODUCTION

In the past few decades, the low dropout voltage regulator (LDO) has been generally needed in System on Chip (SoC) devices. This LDO involves providing accurate features such as fast transient response and low quiescent current. These challenges involve an increasing demand for higher levels of integration on the chip. Using multiple local on-chip voltage regulators is an advantageous method in the SoC development [1, 2]. Especially, where the reduction of power consumption is required, the latest generation of LDOs offers the optimal solution for powering circuitry in many of the embedded system applications. In fact, they can deliver accurate and regulated supply voltages for noise-sensitive analog blocks [3, 4]. These advantages make LDOs extensively required in power management of the embedded systems between the switching power converters (SWPC) and the other- analog circuitries to eventually increase the battery lifetime.

In [4], an additional feedback path guarantees the stability at the expense of the quiescent current of 65 µA. In conventional LDOs [5-7], adding a large output capacitor (up to 4.7µF) is necessary to locate the dominant pole at low frequencies so that achieves good frequency compensation. The large output capacitor occupies a large chip-area. In order to design a full on-chip LDO regulator, the number of compensating capacitors must be reduced [7]. Several LDO regulators suitable for on-chip integration have recently been designed [8–19]. However, existing solutions only partially address previously mentioned issues.

The compensation technique of the damping factor in [9] offers a high power supply rejection ratio (PSRR) (-30 dB at 1 MHz), but the regulator is not stable at a low load current. In [10], a symmetric single

ended-cascade-compensation technique is applied to stabilize the regulator over the full range of transient load current, thereby removing any additional circuitry [4] at the price of large active area occupations by the MOSFET capacitors integrated on the system. To achieve a full on-chip LDO in [8, 12, 14], the technique of nested Miller compensation (NMC) is used in [8], to reduce the required Miller capacitance and control the damping frequency simultaneously. The full on-chip LDO architecture scheme with adaptive frequency compensation in [12], which guarantees stability over the full range of transient and alternating load current, at the expense of gain and system rapidity.

In [20], a push-pull error amplifier was used to inject more current to quickly charge and discharge the the power transistor gate capacitors during load transient variations as well as to generate a considerable current into the load but only at the condition if a large input voltage is applied, in addition the stability of the LDO goes down at low load conditions causing output voltage variations. In [21], the subthreshold slew-rate enhancement technique (SSE) was proposed, in which all transistors of BIAS work in the subthreshold region. An important enhancement response time is improved at the cost of a large area, which is unsuitable for SoC solutions. In [22] a Slew-rate Enhancement (SRE) circuit was proposed, with a bandwidth less than 50 hertz under full voltage swing, which is not recommended for high frequency system.

In this paper, a Full on-chip LDO for low power embedded systems is proposed. The key features are to guarantee the system stability and eliminate the need of any large passive devices and any off-chip capacitor which is not recommended in the SoC designs as the case presented in [5-7] and [23] shows. The solution presented in this work pursues the same objective presented in [20-22], which is enhancing the response time with a fast settling-time without deteriorating the gain bandwidth to address the mentioned issue in [20-22]. By using a simple fast detector amplifier and small on-chip compensation capacitors, the proposed circuit achieved a low quiescent current and minimum under/over-shoots over the full range of transient load current, therefore, making it suitable for low power applications and presenting a solution of the problems shown in [4, 8], while guaranteeing stability under all operating conditions. Morever, an optimized on-chip active area is achieved due to the low number of poles and zeros. The circuit implementation of the proposed LDO is organized as follows:

2. PROPOSED LDO STRUCTURE

The circuit implementation of the proposed LDO is shown in Figure 1, M_1-M_{17}, M_{b1}-M_{b2} and R_1-R_2 form the source driven current operational error amplifier (EA). M_{18}-M_{21}, R_3-R_5 and C_f form the proposed Fast Detector Amplifier, The symmetrical operational amplifier, M_{22}-M_{29} and M_{b3} form the voltage buffer stage, it serves technically to isolate the loading effects as well as isolates the input which is the gate of the transistor M_{26} from the output which is the feedback network adjustment so that provide an amount of current to the current operational EA [24]. PT is the Power Transistor PMOSFET forming the output stage. The class-AB push-pull EA scheme should offer low power dissipation, and its bias current should be as low as possible, in order to drive the PT gate and to achieve a good corrective feedback action [20].

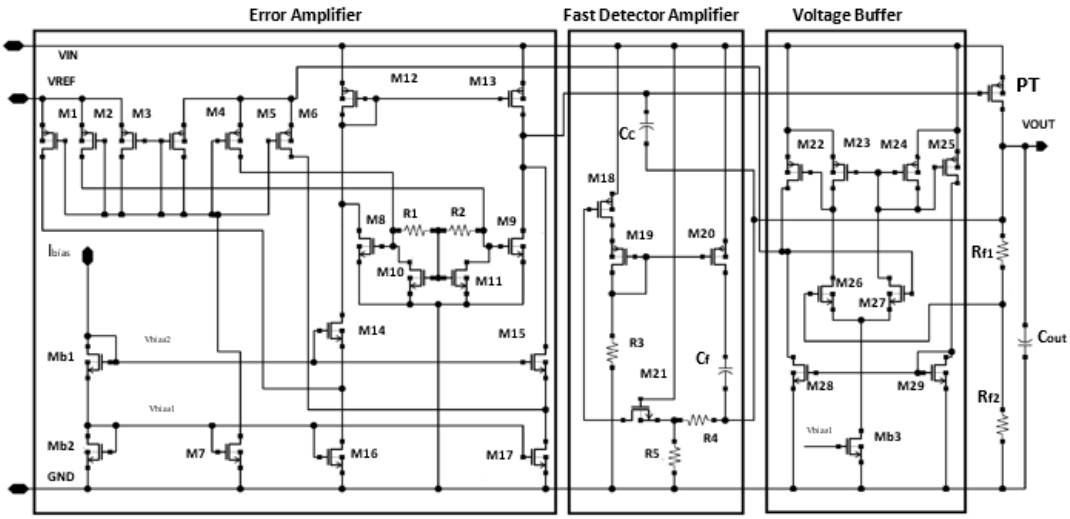


Figure 1. Circuit implementation of the proposed LDO

2.1. Proposed fast detector amplifier (FDA)

To enhance the transient response, a novel technique is implemented in this proposed structure as shown in Figure 2. The M21 transistor is used to transmit the output voltage variation due to the variation of the load current to activate the Fast Detector Amplifier block (FDA). The control signal through M21 is converted to current and amplified by the current mirror M19-M20 that allows more current direct to the load through the C_f capacitor afterwards.

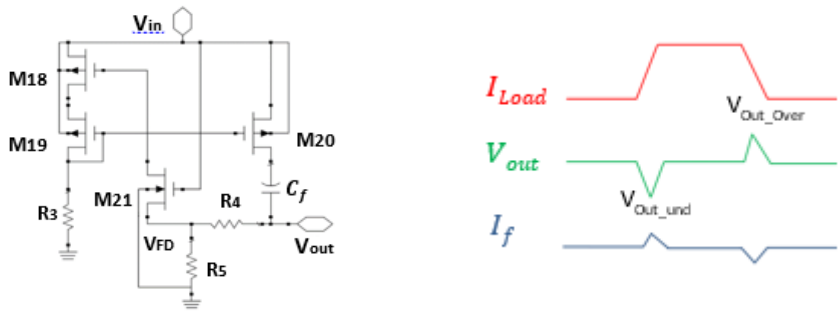


Figure 2. Schematic of the fast detector amplifier (FDA)

When the load demands more current and the EA is incapable to correctly drive the gate of the power transistor to provide the load current demanded, the capacitor C_f functions as a current provider path to the load that assists the regulation system to recover the nominal value of output voltage with a very short settling time as detailed in Figure 2. Where, I_{load}, V_{out}, I_f, V_{out_under} and V_{out_over} are respectively the load current, the nominal output voltage, the current injected by the FDA, the output voltage when I_{load} steps from low to high load current and the output voltage when I_{load} steps from high to low load current.

The variation of the output voltage activates the fast detector amplifier. In the case of a drop of output voltage, an amount of current is injected to the load through C_f capacitor. In the case of overload, the sense of current through C_f will be changed and tied to the LDO ground across the network resistors. This variation is given by:

$$\Delta V_{Cf} = \Delta(V_{out} - V_{D20}) = \frac{1-g_{m18}g_{m20}r_{18}r_{20}\beta}{1-Sr_{20}C_f}\Delta V_{out} \quad (1)$$

With $\beta = \frac{R_5}{R_5+R_4}$

When $$I_{f\,(s)} = C_f\frac{\Delta V_{cf}}{\Delta t} = \frac{1-g_{m18}g_{m20}r_{18}r_{20}\beta}{1-Sr_{20}C_f}\cdot C_f\cdot\frac{\Delta V_{out}}{\Delta t} \quad (2)$$

Where gm18, gm19, gm20, r18, r19 and r20 are the transconductance and the resistance of transistors M18, M19 and M20 respectively, VD20 is the drain voltage of transistor M20, and β is the ratio of voltage divider circuit as shown in Figure 2. There are three cases to consider.

Case 1: Low to high load current: the output voltage drops ($\Delta V_{out} < 0$); gm18 and gm20 increase and fulfill the condition $g_{m18}g_{m20}r_{18}r_{20}\beta \gg 1$. Thus, more current from the FDA block being directed towards the output system through C_f when the power transistor (PT) is not able to provide the current demanded. The current I_f injected to the output of LDO through the capacitor C_f is controlled by the FDA gain. In fact, the drop of V_{out} decreases the gate voltage of M18 through dropout voltage in resistance R5 and creates current in transistor M19. As result, the current provided by M19 is amplified by current mirror M19 - M20. Consequently, more current is injected to the load through C_f and the output voltage of LDO recovers its nominal value with a small Undershoot.

Case 2: when V_{out} recovers the nominal value, the current through M18 and M19 takes its minimum value and $g_{m18}g_{m20}r_{18}r_{20}\beta \approx 1$. Thus, the voltage variation across C_f become negligible and the current flowing to the output of the system is also negligible. Consequently, the LDO operates in normal conditions.

Case 3: high to low load current: the output voltage becomes greater (ΔV_{out} >0), both gm18 and gm20 decrease and the condition $g_{m18}g_{m20}r_{18}r_{20}\beta \leq 1$ is satisfied. In this case, the current through C_f changes direction and follow to the ground through FDA instead of the system output and a large part of overload current directed towards the compensation capacitor C_C to the gate of the power transistor. Consequently, the overload current redirected to the gate of the PT through capacitor Cc, that helps the main loop to recover the control of the power transistor PT. as a result, the PT stops providing the current to the load that not demanded.

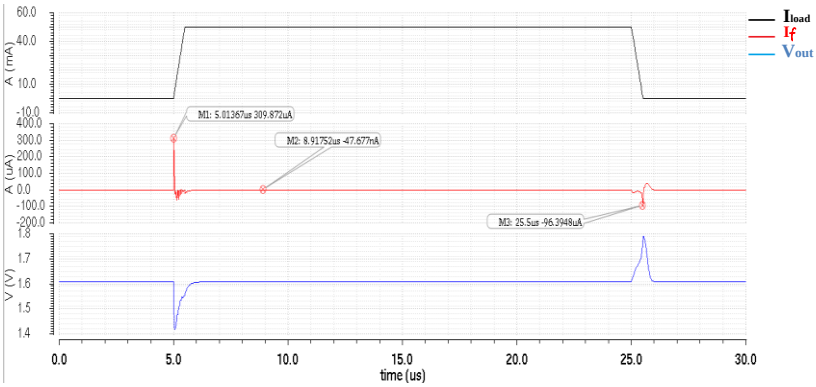


Figure 3. Simulation of the current injection by the proposed fast detector amplifier

For example, when I_{Load}steps from low to high load with capacitance $C_{out}$of 100pF at the system output, only I_f=10µA produced by the proposed FDA circuit is enough to compensate the current drawn from capacitor C_{out} to the load, with an undershoot of 100mV within less than 1µs settling time. In the other case, when I_{Load} steps from high to low load, and with a small resistance at the output of the second stage of EA, the discharge of capacitor at the PT gate is being faster. As a consequent, the system recovers the nominal value of the output voltage. Figure 3 demonstrates the current injection I_f of the FDA at the full load current range.

2.2. Transient response compensation

The simplified block diagram of this proposed LDO is presented in Figure 4, and the parasitic gate capacitors C_{GS} and C_{GD} are taken into consideration. C_{oa1}, C_{oa2}, C_c and C_{out} are the equivalent output capacitances of the EA, voltage buffer, the compensation capacitor and the load capacitance respectively. R_{oa1}, R_{oa2}, r_p and R_L are the equivalent output resistances of the EA, the voltage buffer,the PT and the equivalent load of the LDO respectively. The parasitic capacitances of the fast-detector-amplifier are much smaller than those of the PT.

The large output capacitor C_{out} is used to ensure stability at all operation conditions, which causes a problem of integration on a SoC due to its large ocupied area. However, the dominant-pole must be located inside the loop of the feedback network, and the transient control signal must propagate at the PT gate, since the gate capacitance of the PT $C_G \approx C_{GS} + C_{oa2} + (C_c + C_{GD})A_{Pass}$.The equivalent resistance at the output of the error amplifier R_{oa2} acts as a current-voltage-converter. Consequently, this converter causes a propagation-delay proportional to $R_{oa2}C_G$. When the gate capacitor of the PT becomes enlarged, the propagation-delay will be longer.

When the load current I_{Load}increases, the PT can provide the required load current only when the gate voltage V_G moves close enough to its steady-state within a delay-time t_p, which is related to EA's parasitic poles. The rapidity of the LDO is typically associated to the PT propagation-delay and can be written as g_{m2} /C_G, where g_{m2} is the error amplifier transconductance of the second stage in small signal representation, the value of $g_{m2}$is technically limited. Therefore, the implementation of an auxiliary circuit is involved to charge quickly the gate capacitor of the PT.

The Fast Detector Amplifier (FDA) proposed in this work presents the core of the compensation circuit, as shown in Figure 4. The voltage variations at the Full-on-Chip LDO output are sensed and then eventually converted into an amount of current I_f by the FDA. When the PT is uncapable to supply

the required load current, at this moment I_f will be supplied into the Full-on-Chip LDO output. When a load step current ΔI_{LOAD} is demanded, an output voltage ripple ΔV_{OUT} is produced; the extracted current from PT gate capacitors flows through C_c and C_f until the PT's drain current ΔI_{DS-PM} recompenses ΔI_{LOAD}, allowing the output voltage V_{out} to return quickly back to the steady state.

Using the Conceptual structure circuit in Figure 4, the current flowing in the feedback resistors $R_{F1}$and R_{F2} is considering neglected due to their large parametres, the gate variation of the PT to recompensate the variation of ΔI_{LOAD} corresponds to:

$$\Delta I_{LOAD} \cong \Delta I_{DS-PM} \cong g_{mp} * \Delta V_g \cong g_{mp} \frac{C_c}{C_G} \Delta V_{VOUT} \quad (3)$$

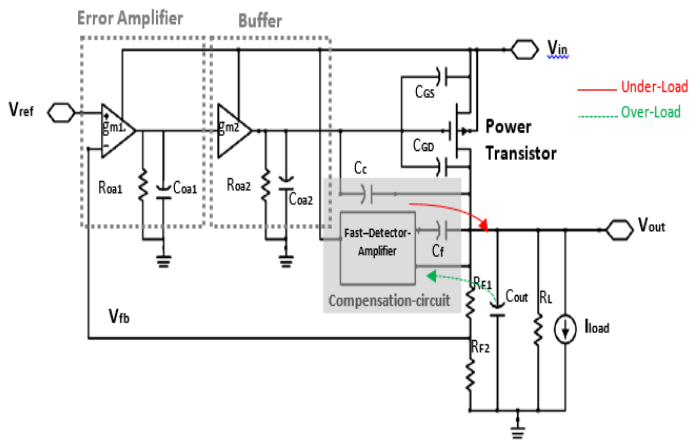


Figure 4. Conceptual structure of the proposed full-on-chip LDO

For example, when Iload steps from 0 to 50 mA with a maximum output ripple of 100 mV and using the values of g_{mp}=5 mA/V (no load) and C_G=50 pF, the compensating capacitance C_c is in the order of 5nF. The worst-case scenario when the transient operation goes from low to high load current, PT requires a large coupling capacitance. Thus, the required coupling capacitor is too large to be integrated. The proposed technique is used to decrease the size of C_c while maintaining the stability and improving the transient response, the parasitic capacitances of the FDA are neglected, and the current flowing through Rf1 and Rf2 is neglected, the current load variation ΔI_{LOAD}corresponds to:

$$\Delta I_{LOAD} = g_{mp}\Delta V_g + \Delta I_f + \Delta I_{Cout} \cong g_{mp} * \frac{C_c}{C_G}\Delta V_{out} + (1 - g_{m18}g_{m20}r_{18}r_{20}\beta)C_f\Delta V_{out} + C_{out}\Delta V_{out} \quad (4)$$

ΔI_{Cout} Correspond to the current variation via the output-capacitor.

For the analysis of the proposed circuit, considering the simplified open-loop characteristic of the LDO's compensation scheme shown in Figure 4. The current injected through C_f is increased by factor $(1 - g_{m18}g_{m20}r_{18}r_{20}\beta)$, where A_d is the FDA gain. This allows us to reduce the value of the capacitor C_f. Besides, g_{m20} and r_{20} are not too large to affect the stability. Accordingly, the FDA effects in the full-On-Chip LDO are active either in over-load or under-load variations. Figure 11(b) shows the improvement of the transient response at full load using the proposed FDA compensation, which yields reduction in undershoots with capacitor value of C_f is 30 pF and of C_c is 10 pF.

2.3. Frequency response of the proposed LDO

The internal loop of the full on-chip LDO voltage regulator is comprised of several embedded poles, which have detrimental effects on the stability. Considering the same conceptual structure in Figure 4 and without using the compensation-circuit, the LDO will have three located poles; P_1: at the output of the error-amplifier,P_2 : pole at the gate of the power transistor and P_3:pole at the output of the LDO voltage regulator:

$$P_1 = {}^{1}/_{R_{oa1}C_{oa1}}$$

$$P_2 = {}^{1}/_{R_{oa2}(C_{oa2} + C_{GS} + A_{pass}C_{GD})} \quad (5)$$
$$P_3 \cong {}^{1}/_{R_{out}(C_{out} + C_{GD})}$$

The equivalent output resistance can be written as $R_{out} \cong r_p//(R_{F1} + R_{F2})//R_L$

Where r_p and $A_{pass}$are the total resistance between the drain and source of the PT and its voltage gain respectively. When r_p and A_{pass} increase and decrease due to the load current variations, the two poles P_2 and P_3 move to the LDO output to low frequencies thus significantly affecting the system's stability, since these poles are very sensitive to the output load conditions.

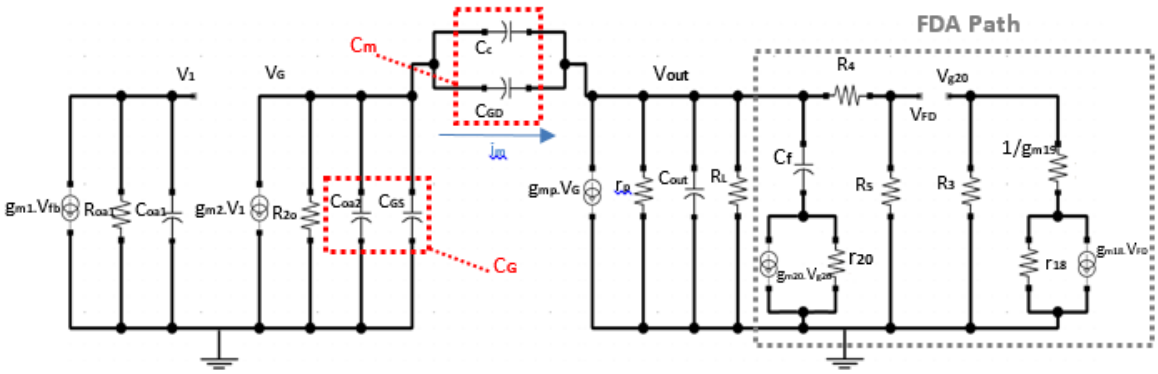


Figure 5. Equivalent small-signal model of the proposed voltage regulator, including the FDA path

At low load conditions, the equivalent output resistance increases, and consequently the pole p_2 will be pushed to the low frequencies because of the undesired parasitic poles, since the parasitic capacitor C_{GD} generates the right-half plane (RHP) zero Z_1 ($\cong G_{mp}/C_{GD}$), which reduces the loop phase margin of the frequency response. Therefore, the LDO system without using the compensation-circuit may not be stable especially at no load condition

The topology's transfer function can be obtained by using the equivalent small-signal model representation of the proposed structure shown in Figure 5. The Miller capacitance is accounted for $C_G \approx C_{GS} + A_{pass}(C_{oa2} + C_C + C_{GD})$.

The continuity of the current at the PT gate and output nodes proves that:

$$\begin{cases} -g_{m2}V_1 = \frac{V_G}{R_{oa2}} + S(C_{GS} + C_{oa2})V_G + S(C_c + C_{GD})(V_G - V_{OUT}) \\ -g_{mp}V_G = \frac{V_{OUT}}{r_p} + SC_{out}V_{OUT} + S(C_c + C_{GD})(V_{OUT} - V_G) + \frac{V_{OUT}}{Z_{FD}} \end{cases} \quad (6)$$

Where:

$$V_1 = -g_{m1}Z_1V_{ref},\ Z_{FD} = \frac{R_{FD}(1+Sr_{20}C_f)}{1+(R_{FD}+r_{20})C_f},\ Z_1 = \frac{R_{oa1}}{1+SR_{oa1}C_{oa1}},\ C_m = C_{GD} + C_c,\ C_G = C_{GS} + C_{oa2}$$

$$H(s) = \frac{g_{m1}g_{m2}g_{mp}R_{oa1}R_{oa2}r_p\left(1-S\frac{C_m}{g_{mp}}\right)(1+Sr_{20}C_f)}{(1+SR_{oa1}C_{oa1})(1+Sg_{mp}R_{oa2}r_pC_m)[1+aS+bS^2]} \quad (7)$$

Where:

$$a = \left(\frac{1}{g_{mp}C_m}\left[\frac{r_{20}}{R_{oa2}}(C_{out} + C_m)C_f + C_{out}(C_G + C_m) + \frac{r_{20}(C_G+C_m)C_f}{r_p}\right] + r_{20}C_f\right)$$

$$b = \frac{1}{g_{mp}C_m}\left[(C_{out}C_f)(C_G + C_m)r_{20} + r_{20}C_GC_fC_m\right]$$

The (7) sheds light on the important effect of the FDA circuit and the use of Miller compensation. The negative effect of the RHP zero (g_{mp}/C_m) on the stability of the system will be canceled easily by the LHP ($1/r_{20}C_f$). In this case the both RHP and LHP zeros are placed at very high frequencies (>2.5 GHz). To analyze the transfer function in (7), with two orders at denominator ($1+aS+bS^2$), there are two cases to consider.

Case 1: low to high output current: g_{mp} increases and with the circuit structure and parameters transistors (g_{mp}≈551mA/V (at full-load), r_p=3.8Ω, r_{20}=208Ω, R_{oa2}≈380KΩ, C_f=30pF, C_c=10pF, C_{GD}=8pF, C_{GS}=2pF and C_{out}=100pf).

To simplify the ($1+aS+bS^2$) expression, considering the two following approximations: $R_{oa2} >> r_p$ And $\frac{C_f r_{20}}{r_p} >> C_{out}$. The factors of two orders at denominator become as follows:

$$a=\left(\frac{r_{20}}{r_p g_{mp} C_m}\left[(C_G+C_m)C_f+r_p g_{mp} C_m C_f\right]\right) \text{ and } b=\frac{r_{20}}{g_{mp}C_m}\left[C_{out}C_G C_f+C_G C_f C_m\right]$$

The condition $\Delta = a^2-4b>0$ will be verified and can be expressed as follows:

$$g_{mp}C_f+\left(\frac{C_G+C_m}{r_p}\right)-2\sqrt{\left(\frac{C_{out}(C_G+C_m)}{r_{20}C_f}\right)}>0 \tag{8}$$

At this condition, the system poles are given by:

$$P_1=-\frac{1}{R_{oa1}C_{oa1}}, \qquad P_d=\frac{1}{g_{mp}r_p R_{oa2}C_m}$$

$$P_{3,4}=\frac{-\left(\frac{r_{20}}{r_p g_{mp}C_m}\left[(C_G+C_m)C_f+r_p g_{mp}C_m C_f\right]\right)\pm\sqrt{g_{mp}C_f+\left(\frac{C_G+C_m}{r_p}\right)-2\sqrt{\left(\frac{C_{out}(C_G+C_m)}{r_{20}C_f}\right)}}}{\frac{2}{g_{mp}C_m}\left[r_{20}C_{out}C_G C_f+r_{20}C_G C_f C_m\right]} \tag{9}$$

The denominator of the transfer function in (7) contains a first pole P_1 occurs at the output of the EA placed at high frequency C_{oa1} (≈ a few fF),, a dominant pole P_d due to the compensation capacitor placed at low frequencies, the third and fourth poles are located much after the Transition frequency at high frequencies and have no effect on the LDO stability which justify that the presented FDA implementation operates only when the over and under load with guarantees the stability in all output load conditions.

The fast-detector-amplifier operates in the transient regime to reduce the spikes at the output of the LDO when the current load switches either from its maximum to the minimum or vice versa, unlike in the normal operating conditions, the FDA becomes inactive and the current at the PT gate becomes:

$$\begin{cases} i_m=SC_m(C_G-C_{OUT})=g_{mp}V_G+\frac{V_{OUT}}{Z_{OUT}} \\ SC_m(C_G-C_{OUT})=-g_{m2}V_1-\frac{V_G}{Z_2} \end{cases} \tag{10}$$

Where $Z_{OUT}\simeq\frac{r_p}{1+Sr_pC_{OUT}}$ $Z_2=\frac{R_{oa2}}{1+SR_{oa2}C_G}$.

The open-loop transfer function in this case is expressed as follows:

$$H(s)\simeq \frac{g_{m1}g_{m2}g_{mp}R_{oa1}R_{oa2}r_p\left(1-S\frac{C_m}{g_{mp}}\right)}{(1+SR_{oa1}C_{oa1})\left[1+S\left(R_{oa2}(C_m+C_G)+r_p(C_m+C_{OUT})+R_{oa2}r_p g_{mp}C_m\right)+S^2\left(R_{oa2}r_p(C_mC_{OUT}+C_mC_G+C_{OUT}C_G)\right)\right]} \tag{11}$$

The poles obtained can be expressed by:

$$P_1=\frac{1}{R_{oa1}C_{oa1}}, \qquad P_d=\frac{-1}{\left(R_{oa2}(C_m+C_G)+r_p(C_m+C_{OUT})+R_{oa2}r_p g_{mp}C_m\right)}$$

$$P_2 = \frac{-(R_{oa2}(C_m+C_G)+r_p(C_m+C_{OUT})+R_{oa2}r_p g_{mp}C_m)}{(R_{oa2}r_p(C_mC_{OUT}+C_mC_G+C_{OUT}C_G)} \quad (12)$$

As illustrated in (11), and with a small capacitor C_{oa1}, the pole P_1 is located at high frequency; its effect on stability is neglected. The dominant pole at the EA output is the only pole located before the UGF, which explains its influence on the open loop frequency response. Due to the EA architecture depicted, the dominant pole P_d is pushed to higher part of the frequency axis when R_{oa2} decreases. On the contrary, when g_{mp} decreases at the low load current, the displacement of P_d towards the left part of the frequency axis caused by the increase of r_p remains very small. From (12), the stability is not affected because of the presence of the PT resistor $r_p$at the numerator and denominator, the location of the pole P_2 at high frequencies stays nearly the same, regardless of the load current conditions.

3. SIMULATION RESULTS

3.1. Open loop frequency response

The loop-gain simulation has been performed, without using the Off-chip output capacitor. The proposed LDO is stable with a good phase margin of approximately 74° at full load as shown in Figure 6. The simulation of the proposed LDO was performed with Spectre.

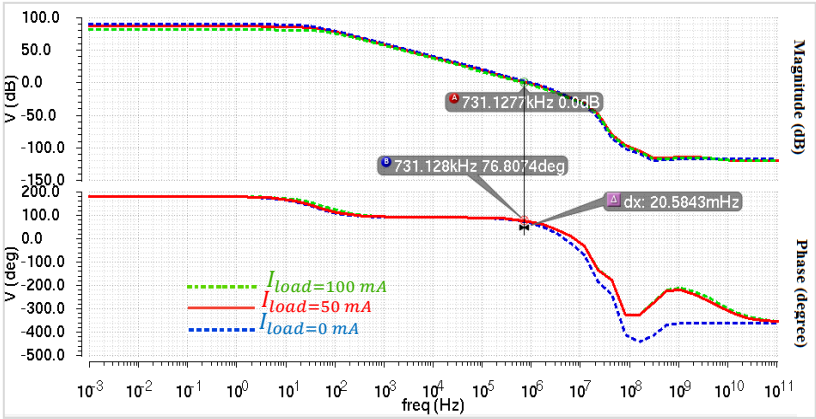


Figure 6. The open loop frequency response of proposed LDO (I_{load}= 0mA/60mA/100mA)

3.2. DC line regulation

The dc-line regulation is one of the important characteristics. The simulation of the DC line regulation at full load current is shown in Figure 7 in the range of the supply voltage [1.8V; 2.5V]. The variation of the DC line regulation is measured to be 93.17 uV/V at $I_{Load} = 50$mA.

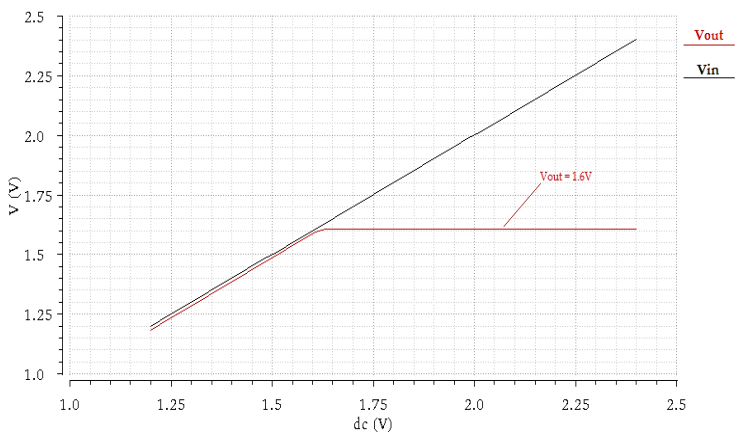


Figure 7. DC line regulation Simulated V_{in} changes from 1.2V to 2.5 V and V_{out} = 1.6 V at full load

3.3. DC load regulation

Figure 8 shows the simulation result of dc-load regulation, when I_{Load}, changes from 0A to 50 mA, the variations of the output voltage equals 0.196 mV.

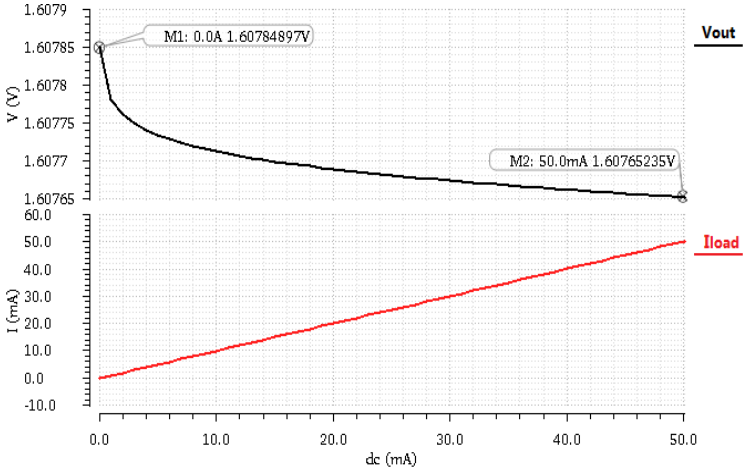


Figure 8. Simulation of DC load regulation when V_{in}=1.8V and I_{load} changes from 0A to 50 mA

3.4. Power supply rejection

Power supply rejection is the ability of the voltage regulator to suppress the output noise. Figure 9 shows the simulation of the PSR at 50 mA load current. The value of -72 dB is obtained in only the range of [0-55Hz] without using the FDA while with the present of the FDA, the same PSR of 72 dB in the range of [0-300Hz]. At 1 MHz the PSR ≈ 0dB without the FDA while the PSR achieves about 6.35dB with using the FDA. These simulation results confirm that the proposed FDA in the Full-On-Chip regulator obtains perfect improvements.

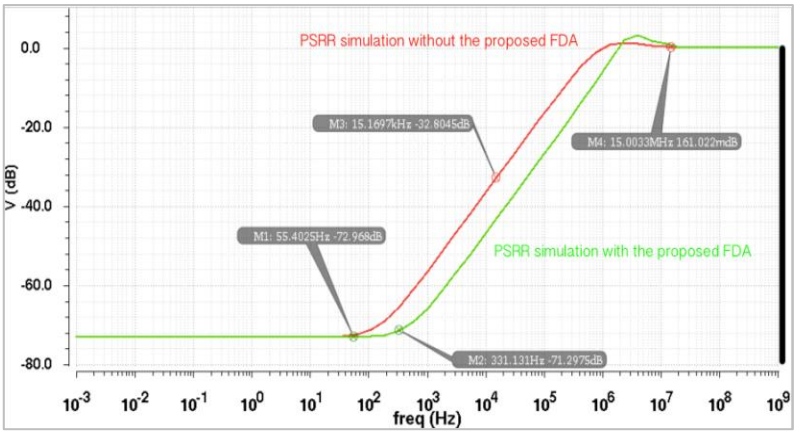


Figure 9. PSR Simulation performance for $\boldsymbol{I_{load}}$= 50 mA when $\boldsymbol{V_{in}}$=1.8 V and $\boldsymbol{V_{out}}$=1.6 V

3.5. Line transient response

Figure 10, shows the line transient response of the proposed LDO for supply voltage changes from 1.8 to 2.2 V with a maximum variation of output 100.65 mV and a settling time of Line Regulation (LNR) equals 928.42ns.

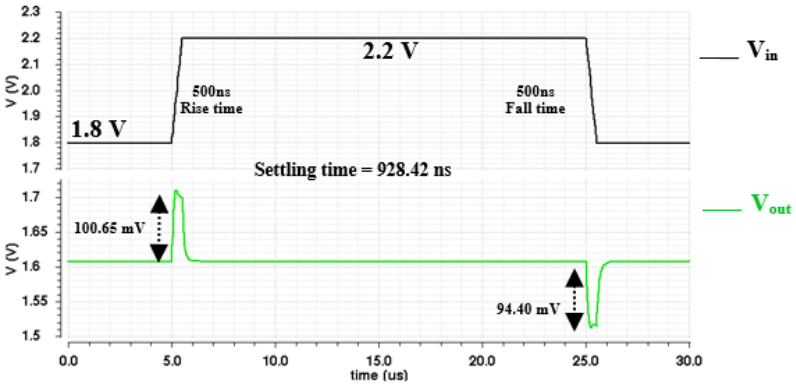
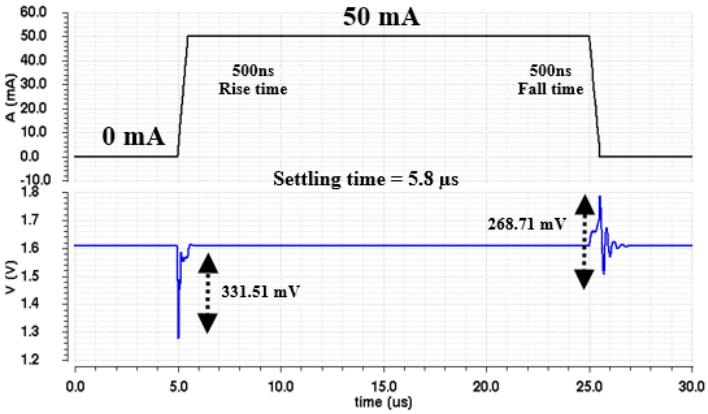


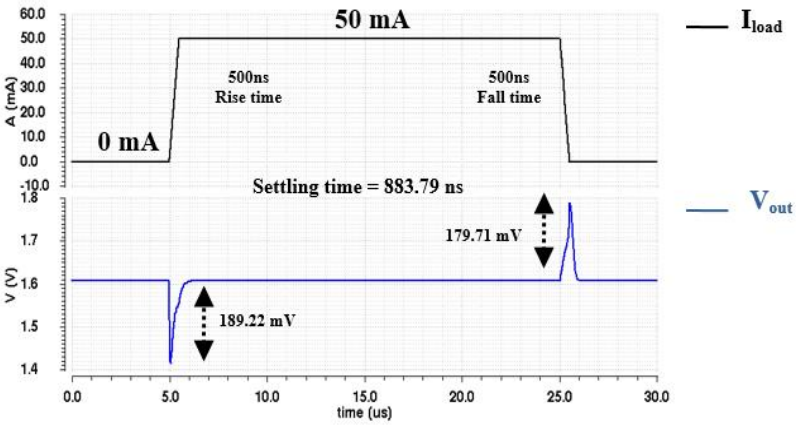
Figure 10. Simulation of line transient response, when V_{in}changes from 1.8 V to 2.2 V including the FDA

3.6. Load transient response

To confirm the above analyses of the proposed technique, two load transient simulations are shown in Figure 11. When load current is switching between 0 mA and 50mA with 500 ns rise/fall time, the maximum variations (undershoot and overshoot) with proposed technique are 189.22 mV and 179.71 mV, respectively with a maximum Load regulation (LOR) settling time of 883.79 ns, without FDA block the output variation (undershoot and overshoot) up to 331.51 mV and 268.71mV, respectively which means that both the undershoot and overshoot are significantly reduced.



(a)



(b)

Figure 11. Load transient, when I_{Load} changes from 0 mA to 50 mA
(a) Without fast detector amplifier, (b) with the fast detector amplifier

3.7. Full-on-chip layout

The proposed LDO regulator has been designed in 0.18 µm CMOS technology. The layout of the IC LDO is shown in Figure 12, with an active chip area of 0.0568 mm^2, this is dominated by Power PMOS transistor, of which the control stage composed by: the error amplifier, the fast-detector-amplifier, and the voltage buffer. The on-chip MOS capacitors occupy a small area on chip.

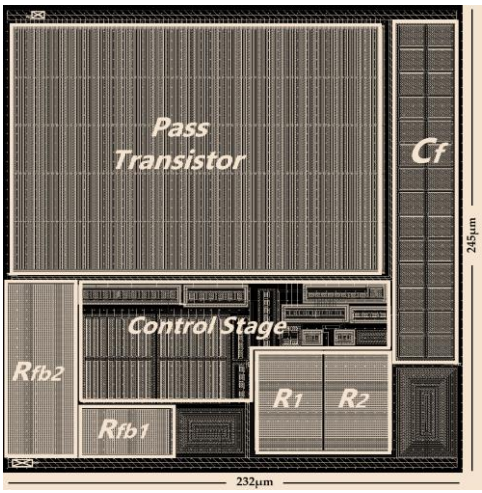


Figure 12. Layout of the proposed full on-chip CMOS LDO

To evaluate the performance designs of the proposed full on-chip LDO, a figure of merit (FOM) used in [11] has been analyzed: $FOM = \frac{\Delta V_{out} C_{out} I_Q}{I^2_{Load\_max}}$. I_Q, ΔV_{out} and I_{LOAD_max} are the quiescent current, the maximum output voltage variation and the highest output current respectively. A lower FOM implies a better performance. In this case, the FOM equal 31.79 fs (femto second). The summary of the performance comparison with previous published works of proposed LDO regulator is shown in Table 1.

Table 1. Summary of performances and comparison with other works.

	[18]	[19]	[21]	[22]	[24]	This work
Technology (µm)	0.11	0.065	0.18	0.35	0.18	0.18
Iload (mA)	200	200	100	100	100	50
Vin (V)	1.8-3.8	1.5-3.7	1.4-1.8	1.2-2	1.2-1.8	1.2-1.8
Vout (V)	2.25	1.2	1.2	1.8	1	1.6
VDO (mV)	200	200	200	200	200	200
Cout (pF)	5000	0-30	100	free	100000	30
IQ(mA)	0.046	0.0088	0.046	0.015	0.135	0.014 (full load)
Settling time(µs)	0.067 (1ns rise time)	0.8	7	2	0.01	0.9284 (LNR[1]) 0.8837 (LOR[2])
Active chip area (mm^2)	N/A	N/A	N/A	0.043	0.024	0.0568
FOM (ns)	0.11	0.035	N/A	0.105	N/A	0,00003178

1 Line Regulation (500ns rise/fall time) N/A: Not Available
2 Load Regulation (500ns rise/fall time)

4. CONCLUSION

In this paper, a full on chip CMOS LDO with a dynamic derivative feedback control is proposed. The FDA path can detect fast-changing voltage spikes at the output of full on-chip LDO providing an additional charging/discharging path momentarily. The regulator circuit design features an active compensation technique, which guarantees the stability through the full load current range of 0 mA to 50mA. The new technique implemented in this work proves a better transient response without degrading the power consumption of the LDO. The detailed analysis of the proposed structure is revealed to justify the performance of the technique utilized. The simulations prove the theory results. A comparison with other reported regulators shows that the proposed full on-chip LDO achieved low voltage transient variations, low quiescent-current, and fast settling-time, simultaneously.

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