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An efficient design approach of ROI based DWT using vedic and wallace tree multiplier on FPGA platform

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ABSTRACT

In digital image processing, the compression mechanism is utilized to enhance the visual perception and storage cost. By using hardware architectures, reconstruction of medical images especially Region of interest (ROI) part using Lossy image compression is a challenging task. In this paper, the ROI Based Discrete wavelet transformation (DWT) using separate Wallace- tree multiplier (WM) and modified Vedic Multiplier (VM) methods are designed. The Lifting based DWT method is used for the ROI compression and reconstruction. The 9/7 filter coefficients are multiplied in DWT using Wallace- tree multiplier (WM) and modified Vedic Multiplier (VM). The designed Wallace tree multiplier works with the parallel mechanism using pipeline architecture results with optimized hardware resources, and 8x8 Vedic multiplier designs improves the ROI reconstruction image quality and fast computation. To evaluate the performance metrics between ROI Based DWT-WM and DWT-VM on FPGA platform. The PSNR and MSE are calculated for different Brain MRI images, and also hardware constraints include Area, Delay, maximum operating frequency and power results are tabulated. The proposed model is designed using Xilinx platform using Verilog-HDL and simulated using ModelSim and Implemented on Artix-7 FPGA device.

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1. INTRODUCTION

Medical imaging place critical role in today's health care of patients for entire treatment process from diagnostics to surgical operations. Medical image processing has to face a lot of challenges in image management, data mining, Medical visualization for Virtual Reality (VR) bio-imaging and Neuro-imaging. The amount of medical image data is increasing from kilo to terabyte storage due to Image resolution and visualization, and it is costly [1]. Image compression techniques are established to reduce the number of bits which is required to transmit or store images without loss of data information. Compressed image minimizes the expense bandwidth and cost-effective during image transmission. In today's world, the application fields for such compressions include Mobiles, TV, Video broadcasting with High Definition (HD), digital video recording and so on [2]. The fundamental components of image compression are redundancy reduction which removes the image duplication while irrelevancy reduction removes unwanted partsfrom the image, which is not observed in receiver section [3].

The extensively used image compression techniques can be categorizing into two parts lossless and Lossy compression. Lossless compression which recovers the input image after decompression from the compressed image. In Lossy compression, An image must be reconstructed after decompression with the acceptable loss of quality. Many compression algorithms are developed by researchers to compress and

rebuild the image with high quality. The image compression techniques like Discrete Wavelet Transformation (DWT), Fast Fourier transformation (FFT), DCT (Discrete cosine transformation), Sparse based Wavelet, Singular Value Decomposition (SVD) and Block Truncation Coding (BTC) are used for enhancement of image quality and compression ratio [4-6]. The effective lossless compression techniques include Huffman Encoding (HE), Run Length Encoding (RLE), Arthematic Encoding and Dictionary Techniques (LZ77, LZ78, LZW) and bit plane coding [7].To improve the compression ratio, Quality of the image, hybrid algorithms are designed which are the combination of two or more compression techniques. Hybrid compression technique [8] introduces to enhance the standard of the reconstructed image with high PSNR value which includes the combination of Principal Component Analysis (Also known as Karhunen-LoeveTransform (KLW)), DCT followed by SPIHT technique (Set-Partitioning-In-Hierarchical-Trees) and results to minimize the encoding time.

ROI Based hybrid compression algorithms to improve the PSNR, CR, Space saving and time-consuming compared to conventional approaches. The ROI based lossless image compression with Embedded Zero-tree Wavelet (EZW) Algorithm [9] is designed for better diagnosis and compared with other techniques like Haar Wavelet (HW) [10] and Daubechies wavelet (DbW) Transformation with better image quality. The Burrows-Wheeler (BW) Transform and Move to Front(MTF) transform with Huffman encoding and hybrid fractal encoding [11] and DWT followed by SPHIT technique [12] are ROI based hybrid compression approach applicable to medical MRI images with CR improvements. The ROI of radiological Image applied to Vedic compression algorithm [13] on software approach with improvement in computation speed, compression ratio and visual quality outcomes with different image database over conventional DCT approach. The FPGA based approach with 2D-DWT using modified Vedic Multiplier [14] with less number of Half and full adder in adder- tree module which results in less resource but the output image quality is not up to the standards.

Most of the Research work towards on ROI-Based image compression with Lossy or lossless techniques are software-based approaches. Very few works on hardware-based procedures for Medical image processing with optimization problems, Hardware complexity, and Performance degradation with constraints. Our proposed design towards ROI Based Lifting scheme DWT approach using Vedic Multiplier to improve the computation speed with image quality image and Wallace tree multiplier enhances the hardware complexity with optimization using pipelining architectures on FPGA. Section 1 has discussed the existing approaches using ROI image compression, FPGA based DWT methods with Vedic multiplier and Wallace tree multipliers. In Section 3, Overview of the methodology which deals with the proposed design. The ROI Based DWT-WM and VM design methods explained in detail in section 4 followed by the results and discussion with performance tabulation in section 5, and section 6 gives the conclusion of the overall work.

This section discusses the methods adopted for ROI based image compression for different medical images, DWT Approaches, Vedic and Wallace multiplier during recent years. Hamzah et al. [15] have presented the Four-dimensional- ROI Image compression and used non-separable Double Lifting integer wavelet transform (IWT) to reduce the rounding noise, and the number of rounding operators along with increasing coding performance and the architecture is compatible to JPEG-2000 conventional approach. The Blocked ROI compressive sensing (CS) of THEMIS images and its reconstruction of images with improvement in image quality and CR has presented by Srija et al. [16]. Amit et al. [17] have given a Polygonal ROI based image compression of DICOM images for telemedicine applications using zero padding, Lossy, and lossless wavelet compression. For Better Portable Graphics (BPG), David et al. [18] have presented an ROI based image compression techniques which include video coding algorithms and results 25 % improvement in CR over traditional image compression techniques. The cloud-based solutions for histopathological images using ROI based compression are presented by Aparna et al. [19] with great CR with optimized storage to and from the cloud.

To perform the ROI compressions from the current survey, suitable hardware based transformations are selected to show the image compression. Kiranmaye et al. [20] have presented a 2D-DWT lifting approach having overlapped-stripe based scanning method which reduces the temporary memory in the process and predicts, updates and addition models are incorporated in architecture and results with less area and power consumption than previous approaches, but lags with image quality and computation speed. For error tolerant applications, the 2D-DWT method followed by a smooth Gaussian filter is designed by Nayna et al. [21] which results in the average image quality output which is acceptable to human eyes. Shweta et al. [22] have presented DWT for image compression using Mallat algorithm structure on Xilinx system generator and which results from right reconstruct image and lags with an area and power consumption on FPGA.

To improve the computation speed, multipliers place critical role to maintain the compression and quality of reconstructed images. Gadakh et al. [23] have presented Ancient 16 X 16 Vedic Multiplier (VM)includes Urdhva-Tiryagbhyam (UT) sutra and results with path delay and memory consumption,

but it is same as conventional approaches. The 8x8 Vedic multiplier with modified Full adders presented by Bandi et al. [24] with performance analysis of Area resource. Kahar et al. [25] show a 64 X64 Vedic multiplier with conventional approaches and performance include area and path delay are tabulated. This multiplier uses the same traditional approaches without novelty. The Xuan et al. [26] has presented an unsigned 32-bit multiplier using Wallace multiplier and booth encoder. The Carry-lookahead adder and modified Wallace tree adder used as adder-tree and which gives fast results with more area utilization. Asif et al. [27] present a Wallace-tree (WM) multiplier includes high-speed counters. Lucas et al. [28] and Ram et al. [29] presents Wallace multipliers using Carry select adder with an area and delay comparison.

Sunaina et al. [30] and Suma et al. [31] presents the Vedic multiplier based image compression using DWT method which includes conventional Vedic approach and traditional DWT approaches and results from the area and delays utilization tabulation with no improvement in image quality. The work of Na'am et al. [32] have concentrated on medical image processing of fundus image and introduced an automatic ROI mechanims that adopts threshold method of segmentation. Further, an work of Lakshminarayana and Sarvagya [33], presented an compresive sensing based medical image compression by considering ROI with lossless compression. The perfromance of [33] is analyzed by considering MSE, PSNR and compression ratio.

There is a lot of study towards Image compression using Transformation and other methods as software approaches and fewer hardware approaches in medical image applications. Very few works on ROI based criteria for Medical images using the Vedic multiplier based on FPGA with lagging in performance matrices includes PSNR, MSE and resource optimization. These problems are overcome in proposed techniques with the following section.

2. PROPOSED METHODOLOGY

The proposed design includes ROI Based Lifting scheme of discrete wavelet Transformation (DWT) using area efficient Wallace- tree multiplier (WM) and modified Vedic Multiplier (VM). The Wallace tree multiplier works with parallel processing using pipelined architecture results in an optimized area with high speed. The modified Vedic Multiplier is used to enhance the execution speed of the proposed design. The Figure 1 represents the architectural model of the proposed plan.

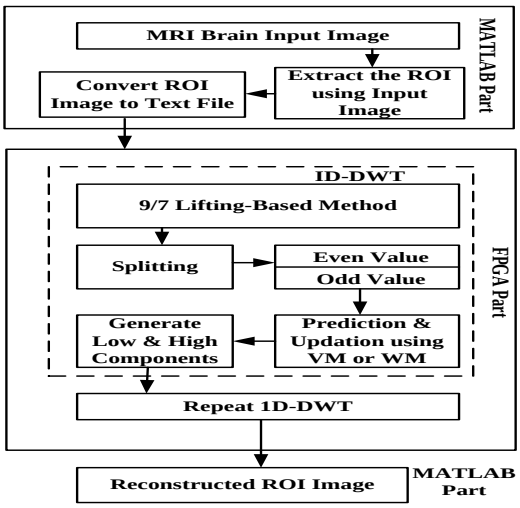

Figure 1. Proposed methodology

Consider the MRI-Brain Input image, extract the ROI part from the input image, and convert the ROI Image part to text file format using Matlab. The proposed design is applicable only to ROI image part and not to complete MRI-brain image. The 9/7 lifting scheme based DWT receives the text file through test-cases. Split the ROI image pixels to even and odd components. The prediction followed by updating is performing along with Multiplication of 9/7 lifting coefficients using Wallace-tree or Vedic Multiplier. The low and high pass components are generated and repeat the same process to reconstruct the ROI image. In the next section, a detailed discussion of the Design and working is elaborated.

3. PROPOSED DESIGN

The proposed design is to perform the ROI image compression using Wallace-tree and Vedic Multiplier. The following Figure 2, indicates the hardware representation of proposedlifting scheme based 1D-DWT using WM or VM. Compare to complete MRI-Brian image, ROI portion image compression has an enormous advantage with fast computation, less resource utilization, and less hardware complexity over FPGA scenario.

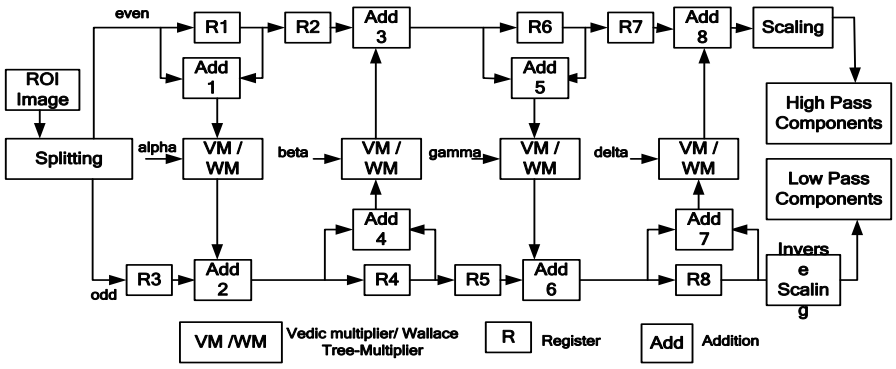

Figure 2. The hardware representation of proposed lifting scheme based 1D-DWT using WM or VM

The ROI image pixels are stored in memory locations based on sizes as a text format. Extract the pixels serially and split to even and odd components-based clock. The design uses 8-Registers, 8- addition units and 4- multiplication unit using WM or VM which are part of the prediction and update operation followed by scaling and inverse scaling. The prediction operation includes the even components are added (Add1) with delayed register (R1), the outcomes are multiplied (WM/VM) with one of the Daubechies 9/7 "alpha" filter coefficients. The updating operation includes the odd components after added with predicated output, perform the addition with odd delayed components, then multiply the "beta" coefficient the process repeats for “gamma” and “delta" coefficients as a prediction and updates operations respectively. Similarly, Scaling and inverse scaling modules are performed using prediction and update activities with scaling and inverse scaling factors to generate the high and low pass components respectively. The 1D-DWT outputs include low and high pass components are fed to the DWT process again, to create the 2D- DWT output components, which are used to recover back and reconstruct the ROI Image. The Filter coefficient multiplication is done using WM and VM separately in DWT module are explained in detail with following architectures. The proposed Design ROI Based DWT Architecture uses two different Multiplier methods namely Wallace tree multiplier and Vedic Multiplier. The practical operation of both the multipliers is explained below.

3.1. Wallace tree multiplier

The pipeline architecture of Wallace- tree Multiplier is designed and shown in Figure 3. It mainly includes Booth encoder using Radix-4 Booth recording table, Partial product generation, Compressors, and adder- tree Module. The booth encoder uses the 8-bit multiplier input for booth compression using radix-4booth recording is tabulated in Table-1. Based on Multiplier input, the encoded record includes 0,1, -1, 2 and -2 is multiplied with 8-bit multiplicand for partial product formation. The partial product generates the output and complements based on multiplicand.

Table 1. Radix-4 booth recording

B(Multiplier)	Recording	Partial Product (PP)
000	0	0
001	1	1XMultiplicand
010	1	1XMultiplicand
011	2	2XMultiplicand
100	-2	-2XMultiplicand
101	-1	-1XMultiplicand
110	-1	-1XMultiplicand
111	0	0

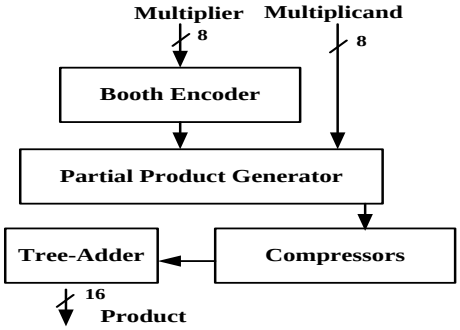

Figure 3. Wallace-tree Multiplier Design

The partial product outputs used in four compressors to reduce the number of stages of multiplication operations to boost the computation process and inputs to the Wallace tree adder. The Wallace tree adder includes the half adder (HA), the full adder (FA), FA with carrying generation along with one-inverted and two- inverted inputs. The prevention of sign extension also included in the design of Wallace-tree adder option. The tree-adder results from the 16-bit product as a final output.

3.2. Vedic multiplier

The proposed 8x8 modified Vedic multiplier operates multiply two decimal or binary number in less time according to the Urdhva Tiryakbhyam sutra. This sutra manages the inputs vertically and crosswise. Firstly, design 2x2 Vedic multiplier using two half-adder concerning vertical and crosswise operations. To design the 4x4 Vedic multiplier, four 2x2 Vedic multipliers along with 4-bit adder and two 6-bit adders used. Similarly, to develop 8X8 Vedic Multiplier, four 4X4 Vedic Multiplier, one 8-bit adder and two 12-bit adders are used which is as shown in Figure 4.

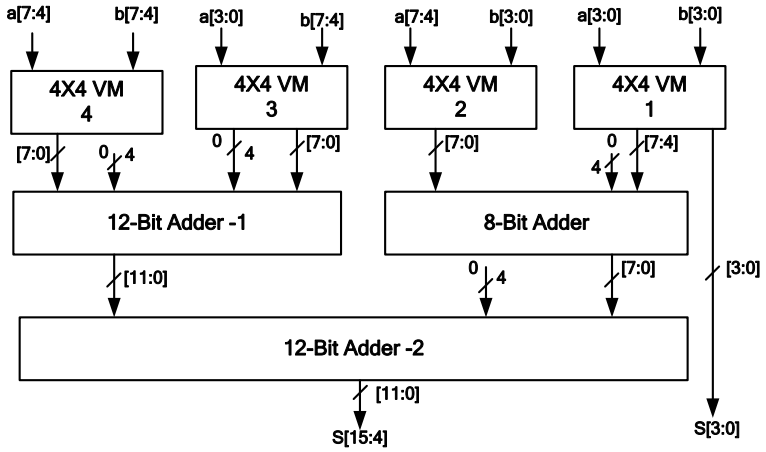

Figure 4. Proposed 8X8 Vedic multiplier

Apply the two 8-bit inputs (a7: a0, b7: b0) to four 4x4 Vedic multipliers vertical and cross-wisely. The first 4x4 VM results from LSB 4-bit as a final sum of first 4-bits (s [3:0]). For 8-bit adder receives second 4x4 VM as first 8-bit input and first 4x4 VM's MSB 4-bits [7:4] along with four zeros' as a second 8-bit input. Similarly, for the 12-bit adder, third 4x4 VM 8-bit output along with four zeros (LSB side) as first 12-bit input and forth 4x4 VM 8-bit output along with four zeros (MSB side) as second 12-bit input results 12-bit adder output. Further, final 12-bit adder requires 8-bit adder output along with four zero's (MSB side) as 12-bit input and first 12-bit adder output as the second input after addition, Results from the 12-bit output which considered as final output (s [15:4]).

4. RESULTS AND ANALYSIS

The proposed Lifting based DWT using Wallace-tree Multiplier (DWT-WM) and Vedic Multiplier (DWT-VM) results analyzed in the below section. The entire model is designed over Xilinx ISE 14.7 Platform using Verilog-HDL and simulated using Modelsim 6.5 simulator and prototyped on FPGA includes Artix-7 family, XC7A100T-3 device, with package CSG324.

The obtained results from the proposed modelover the FPGA platform represented in igure 5. By using Matlab, convert the 256x 256 Brain MRI-Input image-5(a) into text file format. Apply Text file through test case of the proposed design and simulate using a ModelSim simulator, store the low and high pass components in output text file, convert back image format using Matlab to generate the 1D-DWT output image. Compare to DWT-WM, DWT-VM gives better image resolution and quality shown in Figure 5(b) and 5(c) respectively.

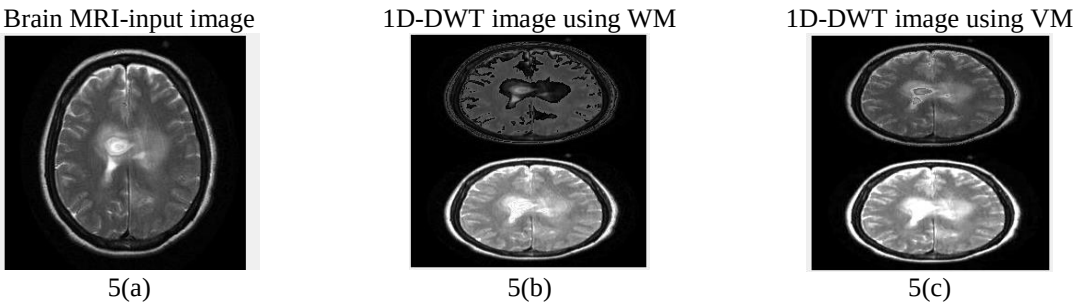

Figure 5. 5(a) Brain MRI-input image, 5(b) 1D- DWT using Wallace-tree Multiplier (WM), 5(c) 1D- DWT using Vedic Multiplier (VM) Results on FPGA Platform

The ROI- Based DWT Design using WM and VM simulation results are shown in Figure 6 and Figure 7 respectively. For both the simulation, 90 x 86 size of ROI Image is considered. Once clock (Clk) activated with active low asynchronous reset (rst) signal, the process starts, and the ROI image includes 8-bit pixel information stored in allocated 7740 memory locations. The memory location (mem_adrs) divides into 3870 address for even and odd inputs after splitting. Perform DWT operation, the 8-bit low (lout) and high (hout) pass components generated.

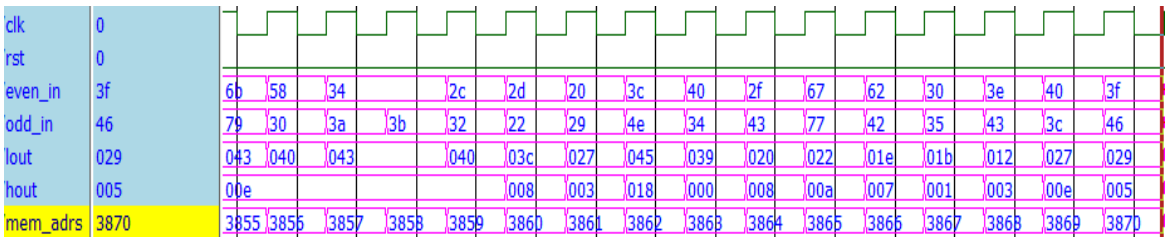

Figure 6. Simulation Results of ROI-Based DWT Design using Wallace-Tree Multiplier

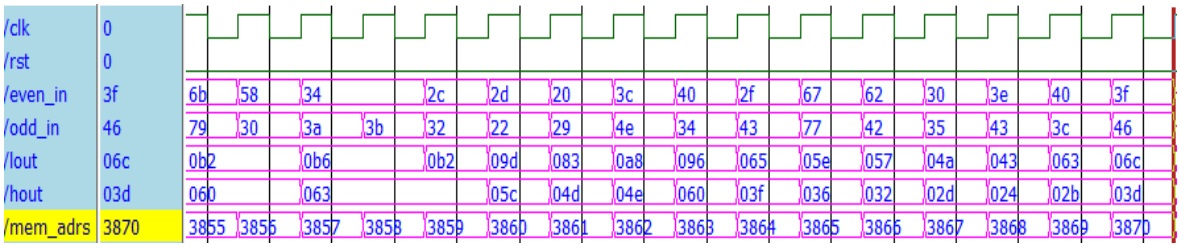

Figure 7. Simulation Results of ROI-Based DWT Design using Vedic Multiplier

The ROI- Based DWT-WM and DWT-VM Results on FPGA are represented in Figure 8. The different 256x256 input MRI brain images (8a) is considered, select the ROI part of image1 with size 86x90, image2 with size 90x90 and image3 with size 90x86 from the input images (8b) perform the DWT operation using WM and VM, recover the output ROI images, which is same as input ROI image shown in 8(c) and 8(d) respectively. To investigate the performance metrics of the recovered ROI image quality, PSNR and MSE taken into considerations.

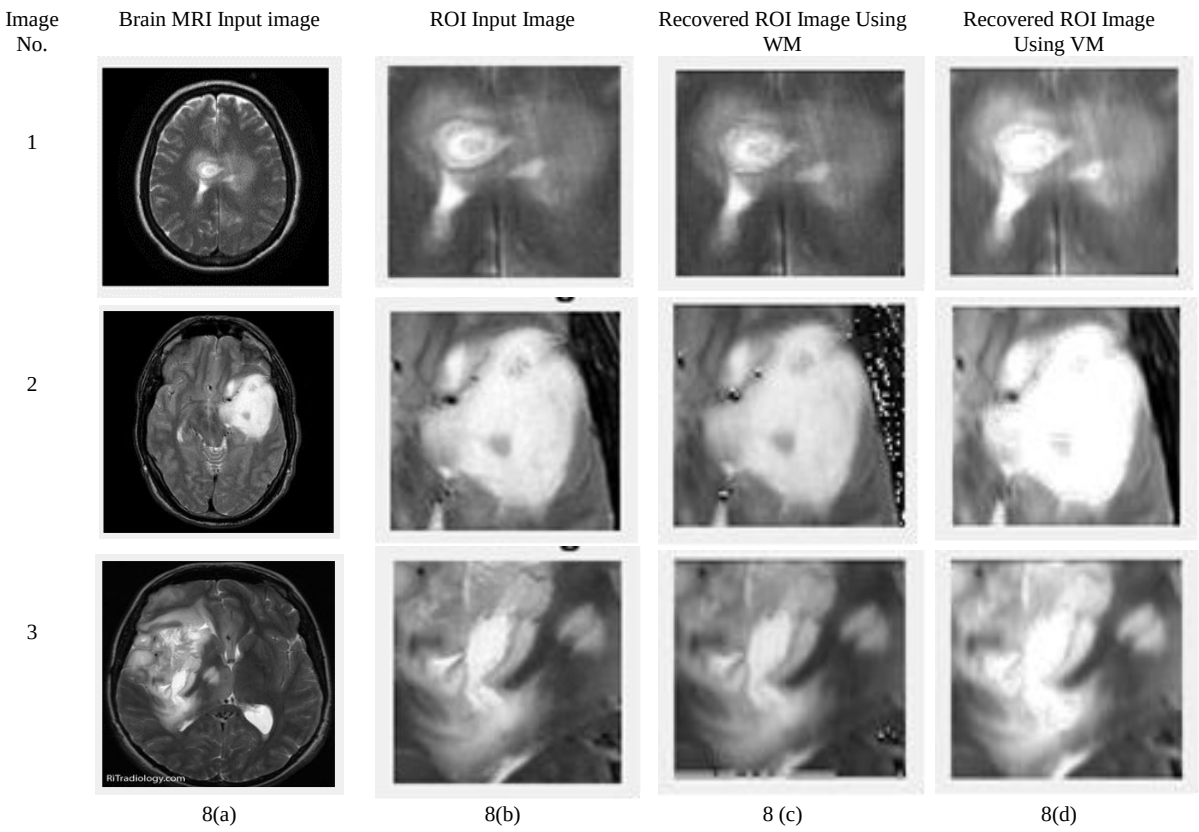

Figure 8. ROI- Based DWT using Wallace-tree Multiplier (WM) and Vedic Multiplier (VM) Results on FPGA Platform: 8(a) Different Brain-MRI input images, 8(b) ROI input image, 8(c) Recovered ROI Image using WM, 8(d) Recovered ROI Image using VM

Table 2 shows the PSNR and MSR of both ROI Based DWT-WM and VM after recovery. The image-2 of DWT-VM with ROI size 90x90 gives better PSNR with 31.491dB and MSE ratio of 46.12 concerning DWT-WM method includes the PSNR of 27.91 and MSE of 105.2.

Table 2. Observation of PSNR and MSE for ROI based DWT-WMand DWT-VM after compression and reconstruction

Brain MRI Input-Images	ROI-Image Size	ROI-DWT-WM		ROI-DWT-VM	
		PSNR (dB)	MSE	PSNR (dB)	MSE
1	86x90	27.156	125.64	28.506	91.7
2	90x90	27.91	105.2	31.491	46.12
3	90x86	27.23	122.9	30.024	64.65

Figure 9 shows the comparative graph of both ROI-Based DWT-WM and VM methods of three brain images for PSNR and MSE respectively. The ROI-Based DWT-VM gives on an average PSNR of 30.007 dB than DWT-WM with average PSNR of 27.43 concerning three brain images with an improvement of 8.58%. Similarly, The ROI-Based DWT-VM gives on an average MSE of 67.49 than DWT-WM with average MSE of 117.91 concerning three brain images with an improvement of 42.76% and which is quite acceptable as lossless image quality.

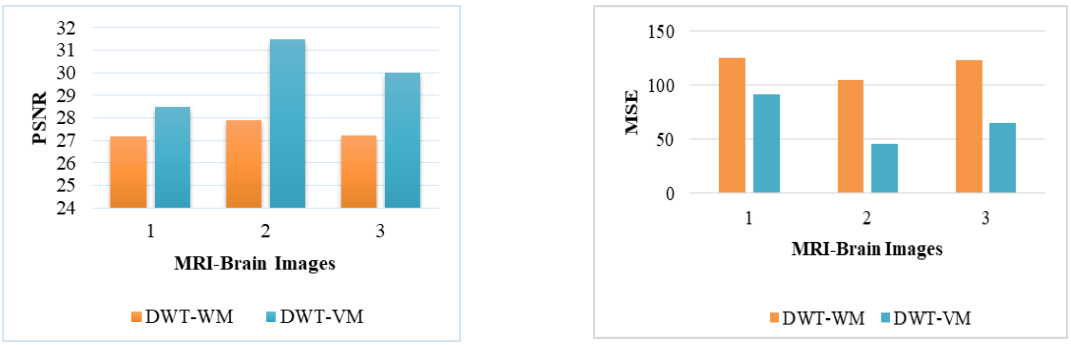

Figure 9. Comparative results of PSNR and MSR for Three different Brain-MRI images using ROI-based DWT-WM and DWT-VM.

The area resource of the Wallace tree multiplier uses 87 slice LUT's which less than the Vedic Multiplier of 109 slice LUT's. The Vedic multiplier consumes the 7.519nsec for path delay and is less than the Wallace tree multiplier of 9.009nsec as tabulated in Table 3.

Table 3. Resource and delay obtained of Wallace-tree Multiplier (WM) and Vedic Multiplier (VM) on FPGA

Area and Delay utilization	Vedic Multiplier	Wallace-Tree Multiplier
Number of Slice LUTs	109	87
Path Delay (ns)	7.519	9.009

The resource utilization (Area), timing and power consumption of ROI-based DWT-WM and DWT-VM on FPGA platform is tabulated in Table 4 and Table 5 respectively. It shows that the DWT-WM consumes fewer area resources includes slice registers, LUT's, LUT-FF pairs than DWT-VM. Similarly, for timing and power utilization, ROI-based DWT-WM is better than DWT-VM. The ROI-based DWT-WM method works high speed of 175.199MHz and utilizes less power of 0.099Wover DWT-VM Method.

Table 4. Resource utilization of ROI-based DWT-WM and DWT-VM on FPGA

Logic Utilization	Available	DWT-WM	DWT-VM
Number of Slice Registers	126800	115	141
Number of Slice LUTs	63400	243	276
LUT-Flip-flop (FF) pairs	363	66	54

Table 5. Timing and power consumption of ROI-based DWT-WM and DWT-VM on FPGA

Timing Utilization	DWT-WM	DWT-VM
Minimum period (ns)	5.708	6.016
Maximum Frequency (MHz)	175.199	166.21

Power Utilization	DWT-WM	DWT-VM
Total Power(W)	0.099	0.103
Dynamic Power (W)	0.017	0.023

5. CONCLUSION

This research paper has presented a cost-effective technique for image compression of MRI-Brain images. The proposed design includes ROI- Based DWT using Wallace-tree multiplier and Vedic multiplier. The 9/7 Lifting scheme used for the DWT method, 8X8 Vedic multiplier is constructed using 4x4 Vedic multiplier and adders. The Wallace-tree (WM) Multiplier is designed using booth encoding and compressors along with adder-tree modules. The 1D-DWT results and ROI image Reconstruction hardware Results using DWT-WM and DWT-VM presented in the results section. For image quality and resolution, DWT-VM method gives better PSNR and MSE with an improvement of 8.58% and 42.76% respectively over DWT-WM method with promising lossless image compression characteristics. Concerning Chip hardware constraints, the DWT-WM method utilizes less resource Area, high operating frequency, and less power consumption than DWT-VM Method with optimal fast computation on FPGA.

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