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A test architecture design for SoCs using atam method

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ABSTRACT

Test arranging is a basic issue in structure on-a-chip (S.O.C) experiment mechanization. Capable investigation designs constrain the general organization check request time, keep away from analysis reserve conflicts, in addition to purpose of restriction control disseminating in the midst of examination manner. In this broadsheet, we absent a fused method to manage a couple of test arranging issues. We first present a system to choose perfect timetables for sensibly evaluated SOC's among need associations, i.e., plans that spare alluring orderings among tests. This furthermore acquaints a capable heuristic estimation with plan examinations designed for enormous S.O.Cs through need necessities in polynomial occasion. We portray a narrative figuring with the purpose of uses pre-emption of tests to secure capable date-books in favour of SOCs. Exploratory marks on behalf of an educational S-O-C plus a cutting edge SOC exhibit with the aim of capable investigation timetables be able to subsist gained in sensible CPU occasion.

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1. INTRODUCTION

This work contracts through the arrangement of check models for specific S/O/C difficult. These structures contain wrapping along with ATAMs. For a specified S-O-C, among showed limitations of components also their assessments, we structure plans which restrain the necessary A.T.E vector reminiscence significance along amid test request occasion. In this broadsheet, we figure the issues of test building plan together for components in the company of settled with versatile distance end to end look at manacles. Along these lines, we decide a meaning of a plan self-governing test time cuts down set out toward SOCs and summary the lower set out characteristics toward the 'ITC'O3 SOC Test Benchmarks'. We absent a book building self-sufficient heuristic count to facilitate successfully redesigns the analysis plan for a prearranged S.O.C [1]. The computation beneficially chooses the amount of A_TAMS furthermore their sizes, the errand of elements to TAMs, moreover the wrapper structure per section. We demonstrate how thus figuring container he second-hand on behalf of streamlining together Test motor vehicle plus Test Rail Architectures among consecutive moreover similar examination designs. Exploratory marks in favour of the 'I.T.C'O3 SOC Test Benchmarks' exhibit to facilitate stood out from in advance dispersed figuring's, we show signs of improvement test times at insignificant figure time [2, 3]. The usage of test traditions, tree-creating figuring's for power-obliged booking, and composed TAM plan and test arranging are different starting late.

Modular test developments

Isolated test enhancement is logically used for SOCs. Non-method of reasoning modules, for instance, embedded straightforward equipment along with reminiscences necessitate stay lone taxing unpaid to their 'unpredictable' route organization. Dim boxed outcast jogs, for instance, hard (plan) focuses and mixed focuses, for which no utilization purposes of intrigue are identified, ought to be attempted beside the investigations as given through their supplier, in addition to thusly furthermore necessitate stay lone taxing. Regardless, despite intended for justification sections of which the utilization unpretentious components are recognized, specific test progression is an engaging option [4-6]. At this point, a specific 'segment and-vanquish' check enhancement move towards lessens the test age enrol occasion with related information quantity. Ultimately, a deliberate check come near engages ordeal recycle, which particularly fulfills if a middle or else element is worn in various S.O.C structures. With the true objective to facilitate estimated examination enhancement, an entrenched element have to be inaccessible beginning it's incorporating equipment also electrical experiment get towards ought to exist given. Zorian et al. [1] introduce a traditional connected experiment get to building permitting confined trying of S.O.C.s including 3 parts for each module-under-test: (1)a analysis configuration basis along with descend, (2) a investigation get the opportunity to instrument (T.A.M), furthermore (3) a covering. The binding container withdraws the element beginning its condition moreover gives trading helpfulness flanked by utilitarian right of entry to the element plus test admission from side to side the T.A.M. The examination configuration have a far reaching crash together on the necessary vector reminiscence significance for each A.T.E canal, and under the analysis request instance of the S.O.C, 2 inputs parameter in the general SOC examination costs. In whatever is left of this newspaper, we unreservedly insinuate these II limitations as assessment time'.

This broadsheet watches out for the subject of organizing convincing as well as capable check get to structures including packaging furthermore T.A.M's. The broadsheet points of interest the official issue implications of assessment plan upgrade concerning compulsory A.T.E vector recollection significance also analysis submission instance, together on behalf of sections through settled extent check handcuffs and furthermore intended for At last, we there exploratory marks designed for the ITC'O2 S-O-C Test yardsticks, which demonstrate to facilitate TRARCHITECT give way centered investigation point in time grades in superfluous enlist instance [6-8].

a. The continuation of this document is dealt with as seeks after. Fragment
b. Reviews previous labour in this space. Territory
c. Describe the issues of experiment building structure mutually on behalf of elements among settled moreover versatile duration channel manacles, tolerating the vital limitations of sections along with a maximal S-o-C T-A-M thickness are demonstrated.
d. In sector underneath we decide an enhanced subordinate set out toward the analysis instance of a agreed S.o.C. Finally this displays our building independent heuristic progression figuring TR-ARCHITECT.
e. Section 3 presents execution purposes of enthusiasm of building specific portions meant for TR-ARCHITECT pro the examination motor vehicle along with Test_Rail Architectures. At end encloses test results for twelve yardstick SOCs. We take a gander at ordeal instance marks for TR-ARCHITECT in addition to those gained beside various systems to the theoretical inferior bounce. Zone 8 completes this manuscript.

2. EXISTED WORK

Different assessment models contain be portrayed in writing. Aerts plus Marinissen [41 portrayed the 3 sweep base analysis designs delineated in Figure 1 (a) the Multiplexing building, (b) the Daisychain Architecture, also (c) the Distribution Architecture.

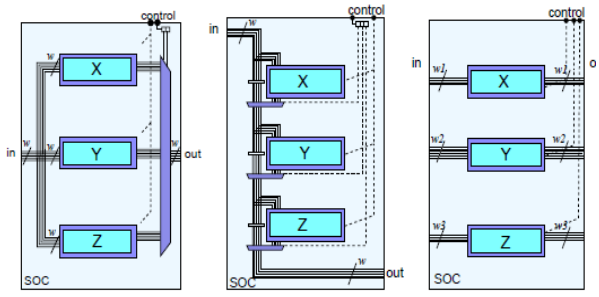


Figure 1. (a) Multiplexing architecture;(b) Daisy_chain arch;(b) Distribution arch

In the Multiplexing furthermore Daisy sequence Architectures, every elements gain induction to the occupied open T.A.M breadth. In the Multiplexing planning, only a solitary unit container be gotten to without a moment's delay. This recommends the total check moment is the entire of the personage component examination periods, yet, additional basically, in like manner with the intention of module-external difficult (i.e., hard the utensils plus cabling amidst the element) is ungainly before still incredible. This is a result of the way with the aim of merely a solitary element wrapper container be gotten to on the double, although designed for module-outside difficult the bindings of somewhere around two elements require to he got to in the meantime. In view of its bypass framework, the Daisychain construction does not contain this control [9]. In the sharing planning, the sum open T.A-M breadth is scattered more than the parts. This empowers sections to be attempted at the same time, and along these lines the total SOC test period is the most extraordinary of the separate unit test periods. With the ultimate objective to constrain the S.C.K investigation point in time, the breadth of an character T.A.M have to be promotional to the proportion of investigation information to facilitate ought to be elated to in addition to starting a unit related with the T-A-M. The analysis means of transport construction shown through Varma moreover Bhatia is a mix of the Multiplexing also Allocation Architectures.

A singular analysis transport is on a very basic level the proportional as what is portrayed by the Multiplexing structural design: elements related with a comparative test transport must be attempted successively. The Test Bus Architecture considers various test transports on 1 S-O*C, which work uninhibitedly, seeing that in the Distribution Building. Element linked to a periodic test shipment meet the negative effects of vague drawback from either the architecture of multiplexing, i.e. Difficult external module is troubling or unusual. The design Test Bus Architecture [10-14] is shown in Figure 2(a). The SOC includes six components, called A by F. This Test Bus Architecture starting point involves 3 experiment transportations. Modules An as well as B are associated with either the three-width Test Bus 1; modules C, D also E are associated with the four-width Test Bus 2; module F is associated with two-width Test Bus 3. Figure 2(b) demonstrates that the test plan can be examined. The three test transports be capable of be worked uninhibitedly. The modules related with an average test transport are attempted in a self-decisive anyway progressive demand.

We call this timetable successive, in light of the fact that per T-A-M the components are (a) (b) Figure2 Example Test motor vehicle construction (an) as well as a possible looking at consecutive test plan (h). The analysis Rail Architecture obtainable by Marinissen et al. [6] is a mix of the Daisy chain with Allotment Architectures. A solitary assessment railing is for the most part the equal as what is portrayed through the Daisy chain Architecture: modules related with the proportional Test Rail can be attempted in the meantime and furthermore progressively. A Test Rail Architecture thinks about various Test rails on one SOC that works without reservation, as in the Architecture of Production. The advantage of Test Rail Architecture over Test Bus Design is that it simultaneously enables access to different or all wrappers, supporting subsystem-external testing. Figure 3 shows a model Test-Rail Architecture. Test Rail Architectures support various sorts of test designs. Figure 2 (b) as well as (c) demonstrate II probable looking at test designs. The timetable in Figure 2(b) is a consecutive timetable; the elements related with a run of the mill Test-Rail are attempted in a self-confident anyway progressive demand [15-17]. The timetable in Figure 2(c) is a parallel date-book. In this timetable, we detail to test all modules related with a common Test-Rail in similar.

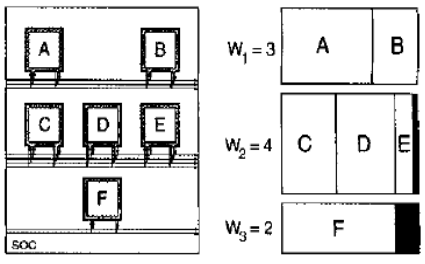


Figure 2. (a) Example Test Bus Architecture and (b) a possible corresponding serial test schedule

2.1. Problems in Existed Method

To plan a trial building in support of a specified plan of element along with a known figure of experiment sticks, a S.O-C integrator needs to choose (1) the check designing make, (2) the amount of TAMs, (3) the breadths of these TAMs, (4) the undertaking of modules to T.A.Ms, furthermore (5) the covering structure for each module.

2.1.1. Issue 1 [Fixed-duration Module-inner Scan handcuffs]

A game plan of elements M, furthermore for every section m E.M the amount of analysis structures p,the amount of practical data incurable I, the amount of utilitarian yield workstation om.the amount of helpful bidirectional incurable b,, the amount of range manacles s,, along with in favour of every yield series k, the extent of the yield sequence in flip disappointments l, m,k. In addition is agreed a numeral W max that addresses the most extraordinary amount of S.O.C-level TAM ropes with the aspire of can be worn. Choose a T_A_M designing and a wrapper plan for each module with the true objective that the general SOC-level test time (in clock cycles) is restricted also W max isn't outperformed.

2.1.2. Issue 2 [Flexible-distance end to end Module-domestic Scan Chains]

All limitations as demonstrated in trouble 1, anyway as opposed to the amount of compass chains entire furthermore the span l,h in support of every yield series k, the whole integer of breadth flip disappointments is known. Choose a T-A-M building moreover a wrapper plan for each one element with the true objective to facilitate the general SOC-level test time (in clock cycles) is constrained as well as W max isn't outperformed [18-19].

3. PROPOSED METHOD AND PROBLEMS SOLUTION

3.1. Problem 1 [fixed-length module-interior scrutinize cuffs]

A plan of sections M, along with aimed at every one Module m E-M the amount of check structures p. the amount of pragmatic data incurable I, the amount of utilitarian yield mortal om. the amount of valuable bidirectional fatals b,, the amount of scope chains s, moreover for all yield chain k, the piece of the range sequence in turn over disappointments l, m,k. Also is given a digit W max that addresses the most extraordinary integer of SOC-level TAM supports to facilitate container be use. Choose a T_A_M building and a wrapper structure for each module with the true objective that the general SOC-level test time (in clock cycles) is restricted in addition to W max isn't outperformed.

3.2. Problem 2 [flexible-length module-internal scan chains]

All constraints as decided in trouble 1, yet as opposed to the amount of compass chains add up to along with the extent l,h on behalf of every yield chain k, the whole amount of range flip disappointments fm is specified. Choose a T.A.M designing in addition to a wrapping plan for each one module with the ultimate objective that the general SOC-level test time (in clock cycles) is constrained plus W max isn't out performed [20].

3.3. Sequential circuit testing

In successive circuits the underlying state (enlist's qualities) isn't of course known. Subsequently, the refinement of flaws and the proliferation of the relating incorrect reactions may swing to be a hard undertaking. An answer is to utilize strategies for the correct instatement of the circuit state to known qualities. Use of appropriate test vector successions as well as the utilization of Set/Reset signs to setup the required state. Improvement of productive systems to set the underlying state and watch the consequent state after the reaction of the circuit.

The memory components (locks or Flip-Flops) in a structure are legitimately associated with frame a brought together move enlist (filter enlist or chain). Along these lines the inside condition of the circuit is resolved (controlled) by moving in (examine in) to the sweep enlist the required test information to be connected to the combinational rationale. Besides, the current inward state (past rationale reaction) can be seen by moving out (examine out) the information put away into the sweep enlist. Figure 3 is testing related to scan sequentially. Figure 4 expalins about scaning regarding ting general test.

Figure 5 expalins about output way of testing here d-flip lemon assumes an imperative job so we are utilizing this strategy got issue 1 arrangement. Figure 6 expalins that output applications in the test procedure here we got high precision contrasted with existed strategies A center test wrapper called TestShell has remained projected through Marinissen et al. [3] similarly is right now exploited privileged Philips. The TestShell includes of the complementary segments. Figure 6 showns that application of scanning procedure [21-22].

A mortal test cell with each quarry. The test cell provides both transient response and discernibility. A (discretionary) bypass record allowing a TAM to sidestep center as well as packaging, throughthe ultimate goal of testing an extra center connected with a comparable TAM. A block of test controls (TCB). The TCB has a bit-cut environment along with encompass of a move in addition to a revive enlist. The TCB is principally future to manage the task of the Test Shell, throughout a little obligatory piece cuts. Additional customer branded bit cuts can be incorporated for manage of centre inner test manner.

Figure 7 is the path delay model regarding to chain of flipflops [23-24]. Figure 8 is the Flip flop chain reording with the help of scan test.

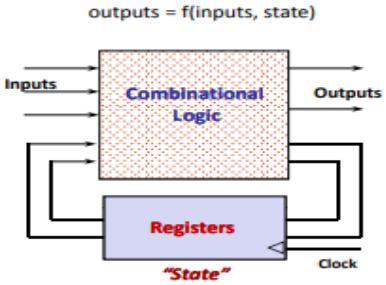


Figure 3. Sequential scan testing

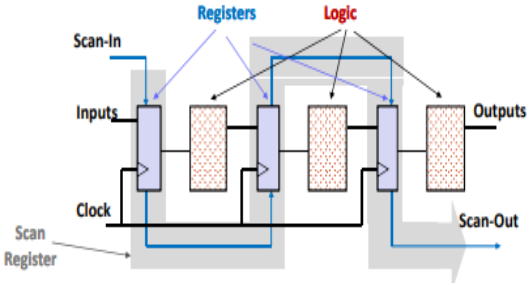


Figure 4. General scan test

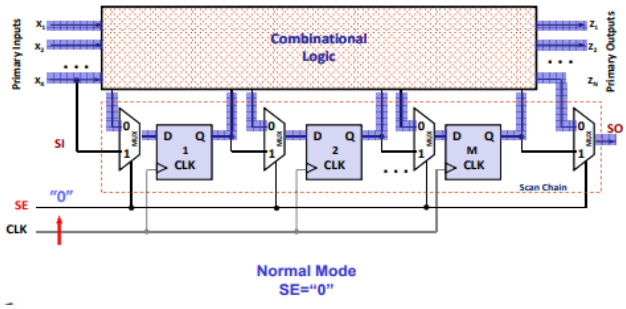


Figure 5. Scan path design

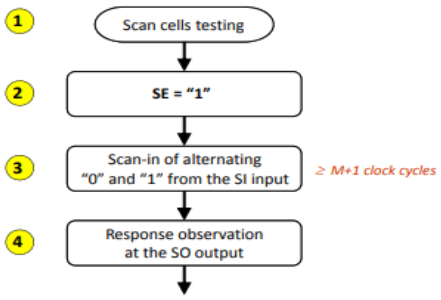


Figure 6. Scan applications

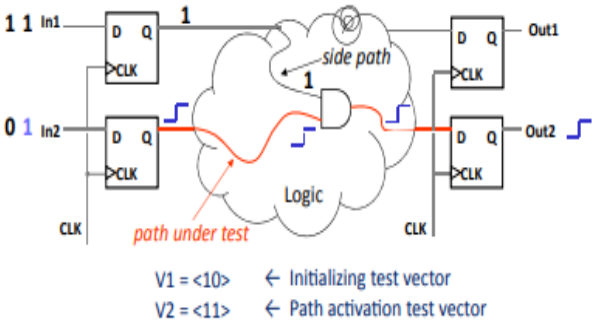


Figure 7. Delay fault testing

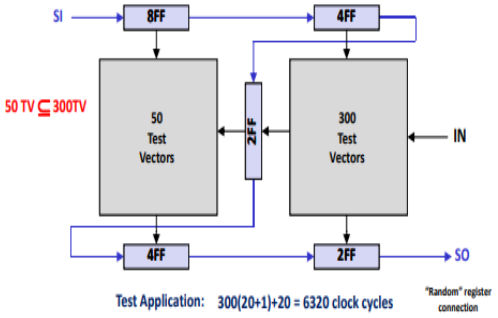


Figure 8. Reordering of scan chain Flip Flop

We have just examined various deformities that can cause postpone shortcomings:

a. GOS deserts
b. Resistive shorting deserts among hubs plus to the supply rails
c. Scrounging transistor spillages, inadequate on intersections as well as wrong otherwise moved limit voltages
d. Certain kinds of releases
e. Procedure variety container similarly make gadget switch at a speed lesser than the particular.

Sweep chain reordering is a procedure utilized in the plan and testing of processing gadgets that empowers the streamlining of setting and sewing flip slump registers with an output chain. It is utilized to streamline and reorder the sweep chain process in the event that it gets isolates, ceased or congested.

4. HAZARDS

2 vector succession is ABC = (111), (101)

a. Gate G 1 presents an extra postponement of 1 unit.
b. Production E of entryway G 3 is headed to a rationale 1, once component following D - > 0.
c. Produce a malfunction on F

Figure 9 is the gate delays which are cicled in Figure 10 explains about time line vector ahen ABC=101 is applied. Figure 11 expalins that dyanamic hazards related to test path which is showed in Figure 12 shows that time loine starting when AB=11 applied Figure 13 is the static hazards processing with the help of dynamic hazards test generation.

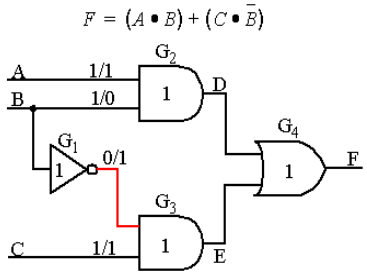


Figure 9. Gate delays are circled

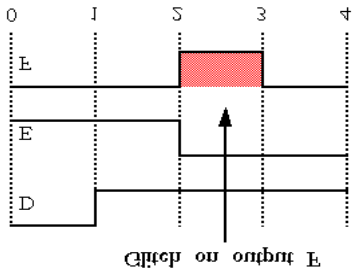


Figure 10. Time line starting when vector ABC=101 is applied

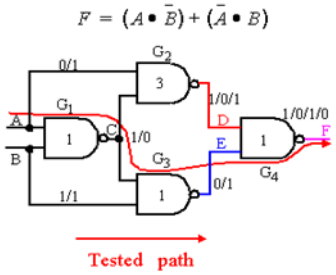


Figure 11. Dynamic Hazards

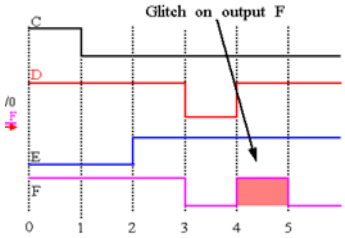


Figure 12. Time Line Starting When Vector AB= (11)Is Applied

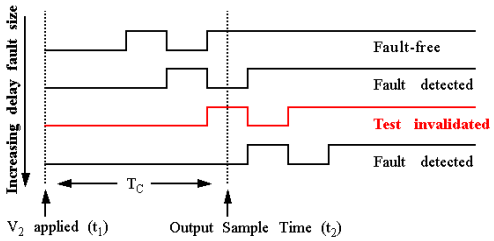


Figure 13. Static hazards can create dynamic hazards along tested paths and need to be considered during test generation

Two vector arrangement is AB = (01), (11).

Entryway G 2 has a defer estimation of 3 time units, owing whichever to an imperfection or an alternate physical execution of the NAND door. Note, in contrast to the past precedent, the anomaly happens previous to the planned change for this situation, also be able to nullify the test (e.g. blame isn't identified). Figure 14 explains that critical paths at 6 time uniuts shown in below [25-26].

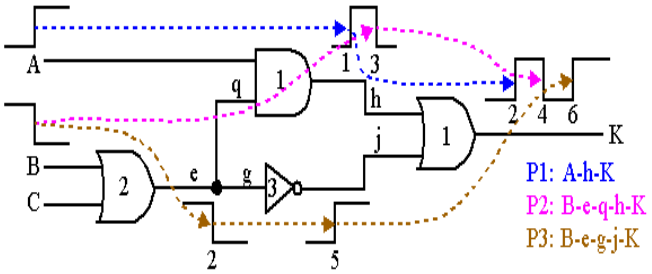


Figure 14. The critical path(s) of this circuit is 6 time units

Let's set the clock period T = 7
Assume only one faulty path.
No delay mistake is detected if path stoppage the length of P3 is less than 7 units.
This experiment will not notice single wait faults the length of paths P1 or P2.
Assume there can be multiple faulty paths.
Assume P2 moreover P3 are defective with P2 extend the "static glitch" at the production beyond 7 units, after that it mask P3's delay error.
This test is called a non-robust test for delay fault P3.

Algorithm 1 [TR-ARCHITECT]
1 CREATE START SOLUTION
2 OPTIMIZE- BOTTOM UP;
3 OPTIMIZE- TOP DOWN;
4 RESHUFFLE

Algorithm 2 [CREATE START SOLUTION]
do
{
item = 10;
value = value + item;
} while(value<100);
Item = 10;
do
{
value = value + item;
} while(value<100);

Figure .15 is the model of conceptual test shell using this test model ezily and fix problems in a simple manner [27]. All methods and techniques are reduces the problems 1 and 2 respectively and they give better quality design.

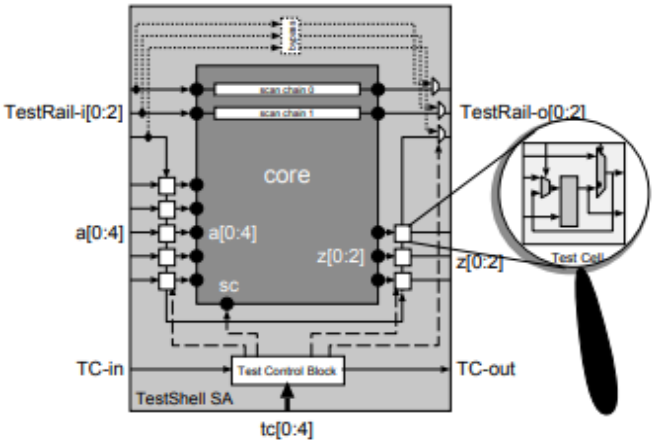
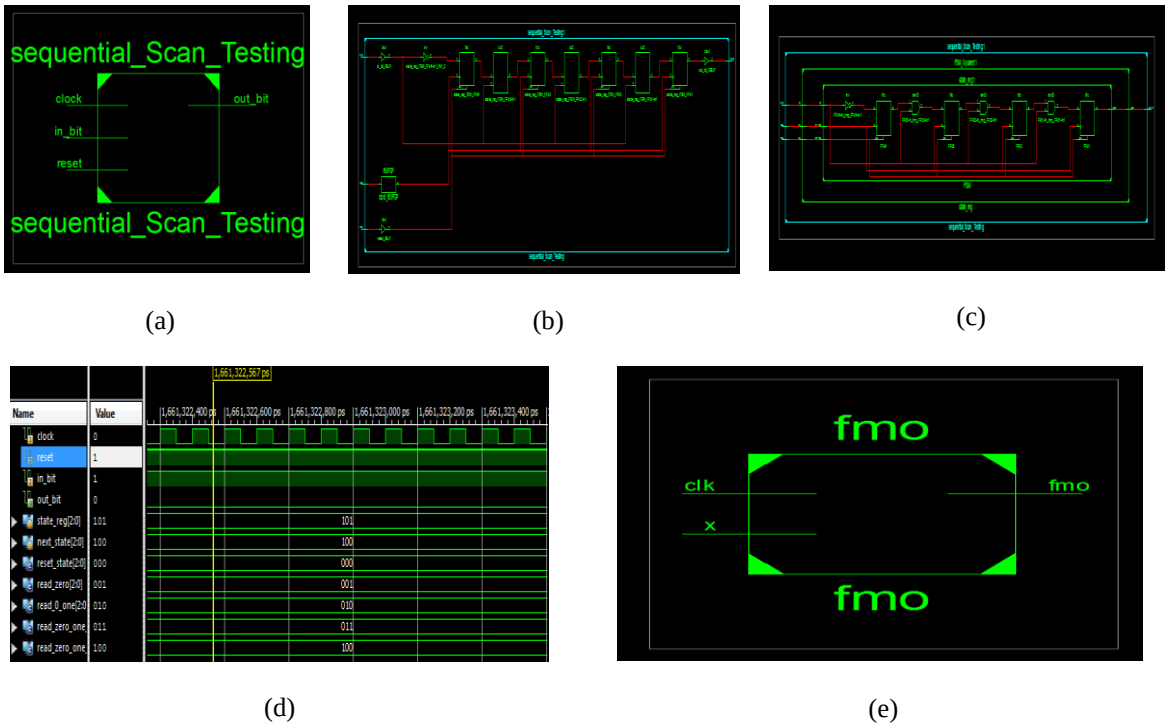


Figure 15. Conceptual view of Philips' Test Shell

5. RESULTS

Figure 16 (a-e) is the block diagram of test cell and Figure 17 shows the internal block diagram of test cell and Figure 18 shows that the output waveforms of test cell. Table 1 explains about comparison of parameters at TAM and ATAM models here efficiency of existed is 80% but proposed method have 99.8% this is good achievement. P(E) is less compared to existed method



(a) (b) (c)

(d) (e)

Figure 16. (a) Aseq_scan_test, (b). Technological schematic of seq_scan, (c). RTL schematic of seq_scaning_test, (d). Output waveforms of seq_scan_test, (e). Test cell

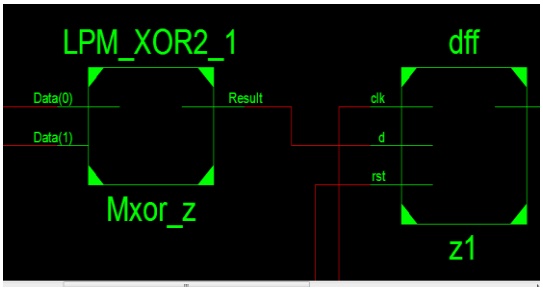


Figure 17. Internal block of test cell

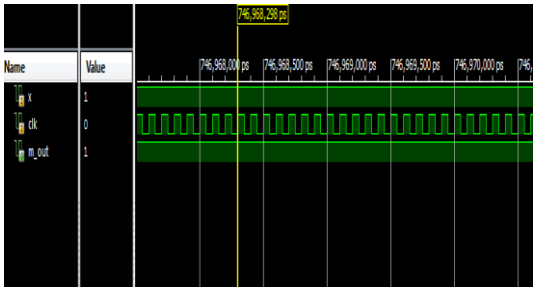


Figure 18. Simulation result of test cell

Table 1. Comparions with ATAM

PARAMETERS	TAM	ATAM
Efficiency	80%	99.8%
Probability of error	0.1	0.01

6. CONCLUSION

At long last utilizing the above test cells like powerful perils, ATAM and reordering testing and postpone blame test squares we showed signs of improvement productivity and less likelihood of blunder. So contrasted with TAM, ATAM gives the better outcomes. Proficiency increments by 19.8% and likelihood of mistake is 0.01 this is great accomplishment contrasted with existed techniques.

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