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Modular multilevel inverter for renewable energy applications

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ABSTRACT

This paper proposes a Multilevel Inverter (MLI) which focuses on two objective, minimal voltage sources and lesser switching component. The proposed Asymmetrical Cascaded Multilevel Inverter (ACMLI) is able to achieve the objective by selectively opting the voltage level of DC sources chosen and implementing the mathematical operation of addition and subtraction on the DC sources. This system also utilizes multiple carrier sinusoidal pulse width modulation technique (MCS-PWM) for operating the switches. It is found that the number of switches required for proposed modular bridge ACMLI and modified H bridge ACMLI was lesser than the traditional Cascaded H bridge Multilevel Inverter (CHB-MLI). It is also evident that the number of DC voltage sources and filter required for smoothing the output waveform is reduced compared to the traditional MLI. The Total Harmonic Distortion (THD) for the proposed circuit was simulated and analyzed in MATLAB Simulink environment and the results are found to be very less and satisfactory. The proposed circuit can find its application in integrating Renewable Energy Sources (RES) to the utility grid, Electrical Vehicle (EV), harmonic reduction and so on. The simulation results of the proposed circuits are tabulated and compared with the traditional cascaded MLI

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1. INTRODUCTION

In power generation sector the percentage of power generated by renewable energy is on increasing mode in recent years and it is forecasted that in future the renewable energy would play a major role in power sector. To cater the growth in renewable energy sector abundant research work are carried out in the broad areas of harvesting maximum power, energy conversion, power electronics components, storage components, grid integration etc.

Inverter is a circuit which transforms constant DC component to varying AC component. The basic traditional inverter is of two level in nature and to make it a sinusoidal AC waveform huge amount of filter is required. The above process leads to huge amount of losses, to reduce the loss of energy during conversion Multilevel Level Inverter (MLI) are considered as one of the wise option. MLI is a type of inverter in which the required output voltage waveform is constructed with several DC input sources [1-4]. The output waveform is of staircase structure in nature, with the increase in DC input source the quality of the output waveform increases [5]. In general there are three basic types on MLI they are Diode clamped MLI, Flying Capacitor MLI and Cascaded H bridge MLI.

Cascaded H Bridge topology is gaining popularity due to its simple structure [6-8]. The absence of diodes and capacitor in the circuit adds more attraction. The cascaded H Bridge MLI is controlled by various control techniques. The cascaded H bridge MLI also have some drawback like a) the increase in the staircase

increases the number of DC input voltage sources. b) Increase in the in the staircase also increases the number of power electronics components. The above mentioned drawbacks increase the size and cost of the MLI.

The cascaded H Bridge MLI further divided in to symmetrical and asymmetrical type [9, 10]. In the first type all the DC input voltage source used has the same amplitude. The number of steps in the staircase is equal to the number of DC sources. If the number of steps increases more the required DC sources also increases, due to the above discussed fact it is not an effective method. In the second type all the DC input voltage sources used has different amplitude, due to the unequal voltage sources this method eliminates the disadvantage of symmetric type and it is more flexible and modular in structure and operation. The cascaded H bridge MLI are widely used in PV systems, UPS systems etc. In asymmetric type proper selection the value of the DC sources the quality of the output voltage waveform, the number of DC sources required and the requirement of power electronics components is managed in an effective manner [11-17]. For selecting the amplitude of the DC sources various method are adopted.

All types of MLI discussed so far requires a control signal for operating the power electronics components present in the circuit. There are various control techniques available to effectively operate the power electronics components in order to achieve quality staircase output waveform [18-24]. In recent years Pulse Width Modulation (PWM) based control techniques are widely used due to various reasons like less switching losses and less stress on power electronics components. The various PWM control method available are sinusoidal PWM, multiple PWM, selective harmonic PWM, space vector modulation, multiple carrier sinusoidal PWM etc. In this paper two modular ACMLI is proposed with minimal power electronics components and input DC sources. Both the circuit implements the same control scheme for obtaining the required staircase output. The two circuits proposed are simulated in MATLAB Simulink environment.

2. PROPOSED MULTILEVEL INVERTER

The proposed two MLI circuits in this paper use four different DC source for obtaining fourty nine level stepped output in the resistive load with the output obtained is further filtered by a LC filter to generate a pure sine waveform. The filter required for the above design is very less compared to the conventional inverter in practice. Both the circuits discussed here use the basic mathematical operation of addition and subtraction between the voltage sources available in the input side. Modular 49 level ACMLI using the proposed methodology is shown below in Figure 1.

This circuit consists of totally five bridges where the four bridges are connected to the input voltage sources separately and the fifth bridge is connected to the load as shown in the Figure 1. Each bridge has four power devices and there are totally 20 power devices available for converting the DC voltage available in the input side to AC voltage available at the load. The bridges I, II, III and IV are capable of providing positive or negative voltage depending on the power device operated.

The operation of the bridges for obtaining some voltage steps is discussed below in Figure 3 with necessary circuit diagram. Bridge – I has power devices B_{11}, B_{12}, B_{13}, B_{14} and voltage input V_1 similarly bridge II, III and IV has devices B_{21}, B_{22}, B_{23}, $B_{24,}$ B_{31}, B_{32}, B_{33}, $B_{34}B_{41}$, B_{42}, B_{43}, B_{44} andvoltage inputs V_2, V_3 and V_4 respectively. The bridge V acts as the main bridge with power devices M_1, M_2, M_3, M_4 and load. Some of the voltage levels possible by the MLI circuit I is tabulated in Table 1. Where 1 refers that the switch in ON state and 0 refers that the switch is in OFF state. As shown in Table 1, if the voltage inputs are of different values the number of voltage level increases.

The operation of the circuit for the generation of required stepped waveform in the load is described in Figure 3. The second circuit is a modular 49 level modified H bridge ACMLI with asymmetrical voltage inputs as shown in Figure 2. This circuit consists of four DC voltage inputs V_1, V_2, V_3, V_4 and sixteen power devices they are S_1, S_2, S_3, S_4, S_{R1}, S_{R2}, S_{L1}, S_{L2}, etc. Here all the DC voltage sources V_1, V_2, V_3 and V_4 has a power device in series and a power device in parallel with it. If the DC voltage source is required the series connected switch is operated otherwise the parallel connected switch is operated to bypass the DC voltage source, But care should be taken such that both the series and parallel switch is not operated at the same time to avoid short circuit of the DC voltage source. Some of the sample voltage levels possible by the proposed ACMLI circuit shown in Figure 2 are tabulated in Table 2. The operation of the circuit for the generation of required stepped waveform in the load is described in Figure 9. As seen in the Figure 2, it is also noted that short circuit condition in the circuit is eliminated by not operating both the switches on the same leg at the same time.

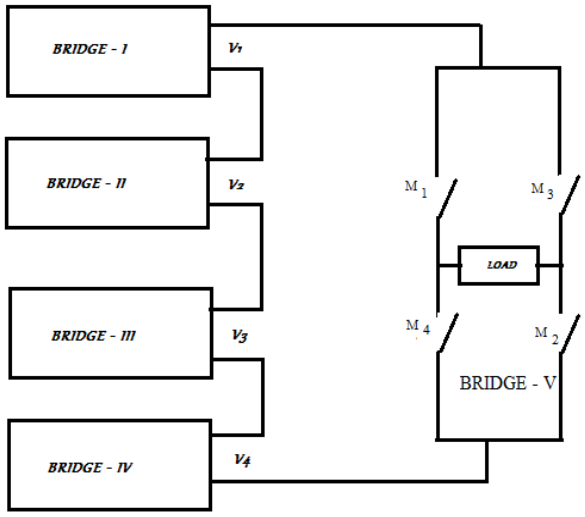

Figure 1. Proposed modular 49 level bridge type ACMLI

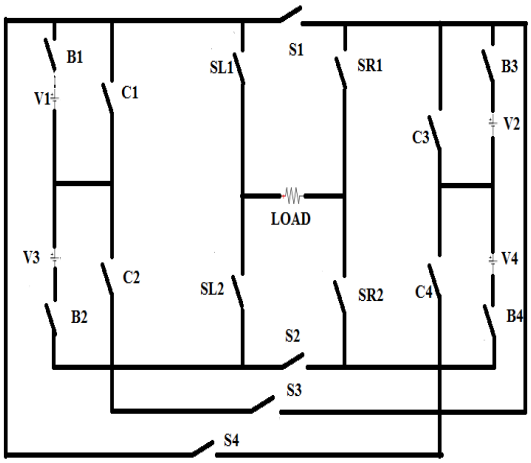

Figure 2. Proposed modular 49 level modified H bridge type ACMLI

3. PRINCIPLE OF OPERATION

The principle of operation of the two circuits shown in Figure 1 and Figure 2 are discussed in this section. In the circuit proposed below asymmetric method is adopted. The Figure 1 and Figure 2 shows the structure of the proposed circuits both the circuit uses the same DC voltage input. The mathematical expression governing the circuits are discussed are given below

Consider there are N bridges available in Modular 49 level bridge type ACMLI with an individual source present in each bridge. The value of input DC sources are governed by the following equations:

$$V_1 = V_{dc} \quad (1)$$

$$V_2 = 3V_1 \quad (2)$$

$$V_n = 5V_{(n-2)} \quad (3)$$

The (1), (2) and (3) should be satisfied to achieve uniform and proper voltage steps. The number of steps in the generated output voltage waveform with respect to the number of input voltage source is:

$$L_{level} = \frac{\sum_{k=0}^{n} V_k}{V_1} x\ 2 + 1 \quad (4)$$

The number of power electronic components required for switching purpose with respect to the number of input voltage source is given by:

$$\text{Total switches required} = 4\ (n + 1) \quad (5)$$

Where n is the number of DC input voltage source.

The maximum output voltage possible is given by

$$V_{o\ max} = \sum_{k=0}^{n} V_k\ x\ 2 + 1 \quad (6)$$

The switching pattern implemented for Modular 49 level bridge type ACMLI using the above expression is shown in Table 1. The analysis of Modular 49 level bridge type ACMLI is done with four input voltage sources. The input voltage value for Modular 49 level bridge type ACMLI is calculated using (1), (2) and (3). The DC voltages in the input sides are chosen in such a manner that the basic mathematical addition and subtraction can be implemented for achieving more number of steps in the output waveform. The voltage steps obtainable for this Modular bridge type ACMLI is 49 steps at the output waveform. The details of

switch operation applicable for Modular 49 level bridge type ACMLI is given in the Table 1. For analysis purpose following levels are considered V_1, V_2-V_1, V_2, (V_1+V_2), V_3 and (V_1+V_3) respectively.

Level 1: In this step the output voltage across the load is $V_o = V_1$.To achieve this step output the power devices B_{11}, B_{12}, B_{21}, B_{23}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated .In this step only one source is delivering the power to the load through power devices as shown in Figure 3(a).

Level 2: In this step the output voltage across the load is $V_o = V_2 - V_1$. To achieve this step output the power devices B_{13}, B_{14}, B_{21}, B_{22}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step two sources take part in delivering the required power to the load through power devices as shown in Figure 3(b).

Level 3: In this step the output voltage across the load is $V_o = V_2$. To achieve this step output the power devices B_{11}, B_{13}, B_{21}, B_{22}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices as shown in Figure 3(c).

Level 4: In this step the output voltage across the load is $V_o = V_2 + V_1$. To achieve this step output the power devices B_{11}, B_{12}, B_{21}, B_{22}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In step two sources take part in delivering the required power to the load through power devices as shown in Figure 3(d).

Level 5: In this step the output voltage across the load is $V_o = V_3$. To achieve this step output the power devices B_{13}, B_{14}, B_{21}, B_{23}, B_{31}, B_{32}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices as shown in Figure 3(e).

Level 6: In this step the output voltage across the load is $V_o = V_3 + V_1$. To achieve this step output the power devices B_{11}, B_{13}, B_{21}, B_{23}, B_{31}, B_{32}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices as shown in Figure 3(f).

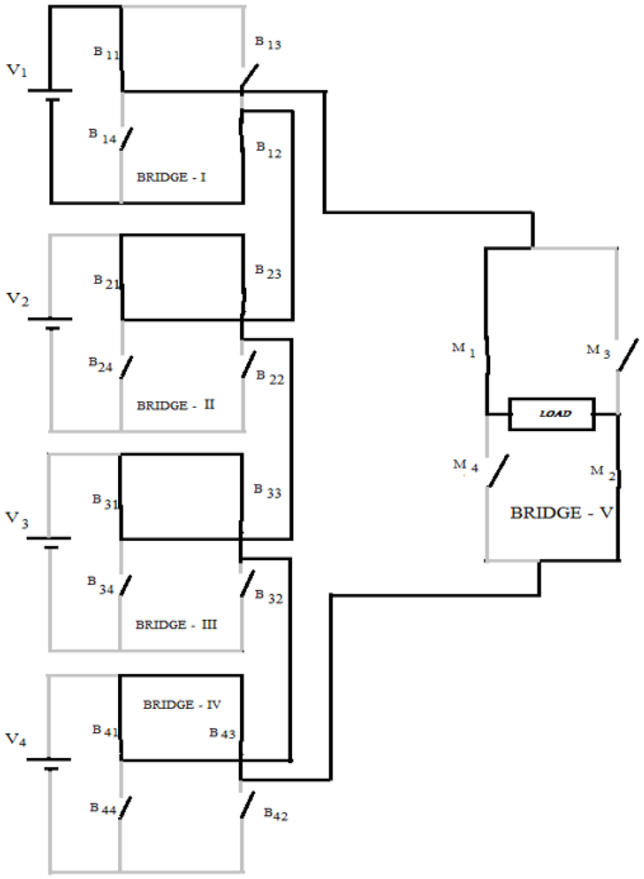

Figure 3(a). Level 1 ($V_o = V_1$)

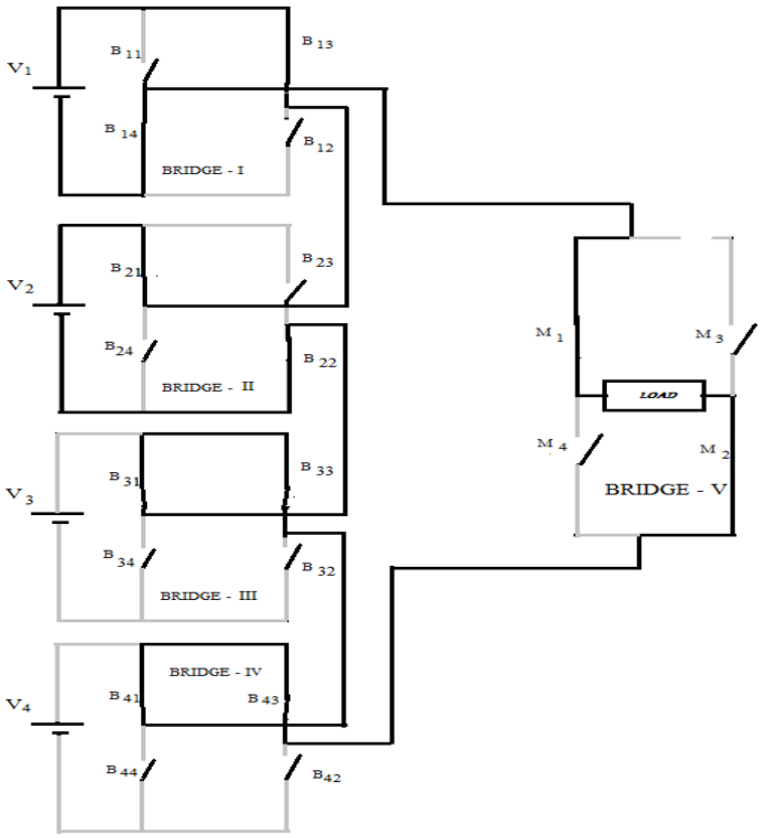

Figure 3(b). Level 2 ($V_o = V_2 - V_1$)

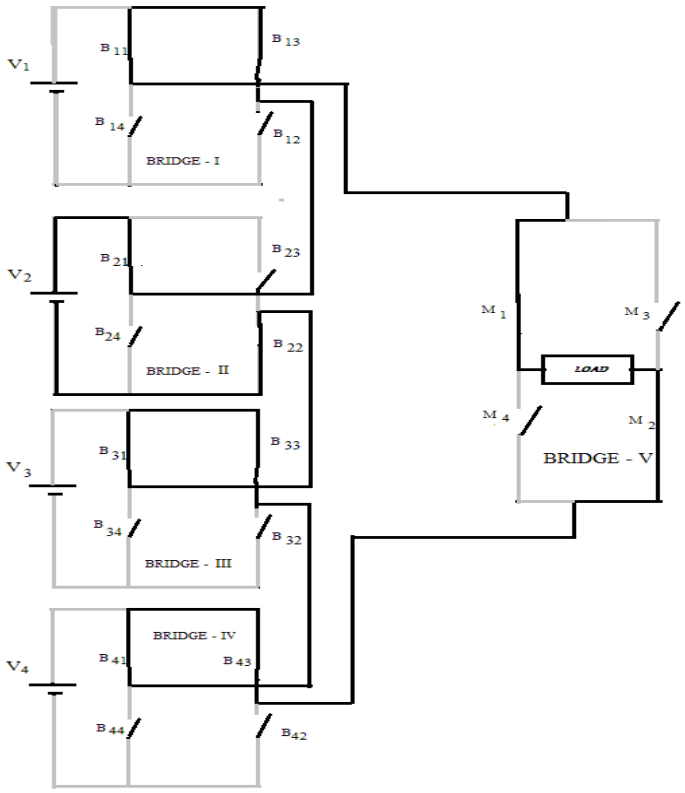

Figure 3(c). Level 3 ($V_o = V_2$)

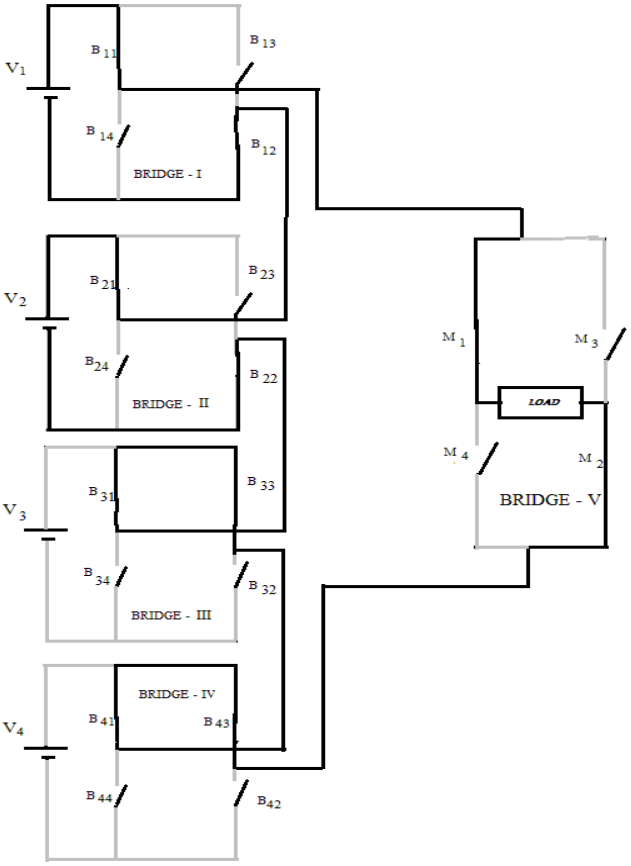

Figure 3(d). Level 4 ($V_o = V_2 + V_1$)

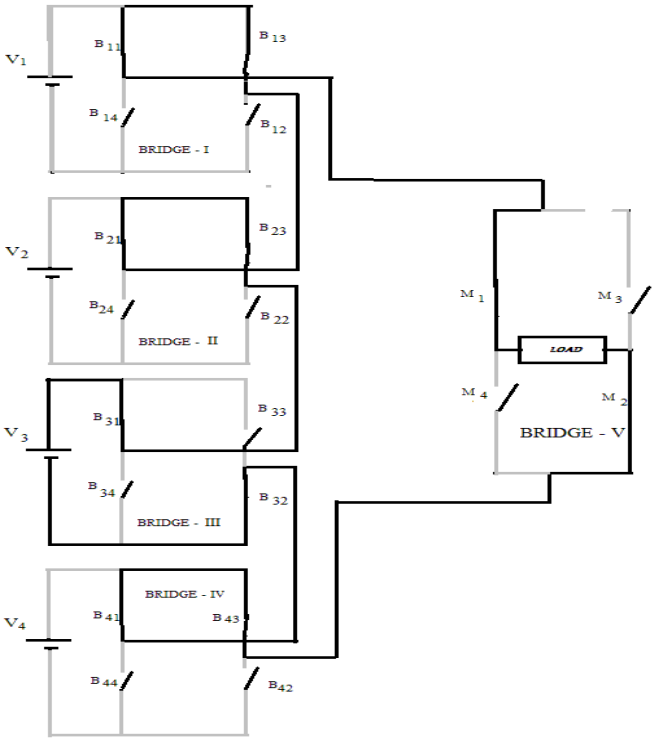

Figure 3(e). Level 5 (Vo = V3)

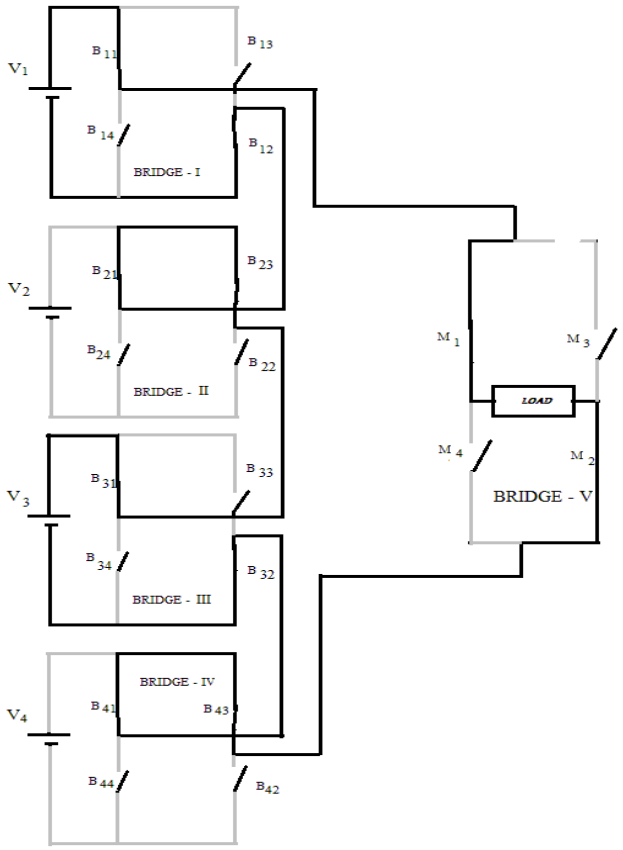

Figure 3(f). Level 6 ($V_o = V_3 + V_1$)

Table 1. Switching sequence for circuit i

Step	Switching Sequence for Modular 49 level bridge type ACMLI																			
	Bridge - I				Bridge–II				Bridge–III				Bridge-IV				Main Bridge			
	B11	B12	B13	B14	B21	B22	B23	B24	B31	B32	B33	B34	B41	B42	B43	B44	M1	M2	M3	M4
1	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0
2	0	0	1	1	1	1	0	0	1	0	1	0	1	0	1	0	1	1	0	0
3	1	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0	1	1	0	0
4	1	1	0	0	1	1	0	0	1	0	1	0	1	0	1	0	1	1	0	0
5	1	0	1	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	0
6	1	1	0	0	1	0	1	0	1	1	0	0	1	0	1	0	1	1	0	0

The Modular 49 level Modified H bridge type ACMLI follows the same mathematical expressions for the values of DC voltage sources, Number of stepsgenerates and maximum output voltage (ie) (1), (2), (3) and (4) is satisfied by the Modular 49 level Modified H bridge type ACMLI also, for this circuit the number of power electronic components required is governed by different equation and is given below.

$$Total\ number\ of\ switches = 8n - \frac{(2n-2)(2n-4)}{(n-1)} \quad (7)$$

In the above case the numbers of sources are considered even for effective utilization. The switching pattern for the proposed Modular 49 level Modified H bridge type ACMLI is shown in Table 2 and the operation of the circuit for the above mentioned pattern is discussed below. The input voltage source value of proposed Modular 49 level Modified H bridge type ACMLI also determined by (1), (2) and (3) respectively.

Level 1: In this step the output voltage across the load is $V_o = V_1$. To achieve this step output the power devices B_1, SL_1, SR_2, S_2 and C_2 are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices as shown in Figure 4(a).

Level 2: In this step the output voltage across the load is $V_o = V_2 - V_1$. To achieve this step output the power devices B_{13}, B_{14}, B_{21}, B_{22}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step two sources take part in delivering the required power to the load through power devices as shown in Figure 4(b).

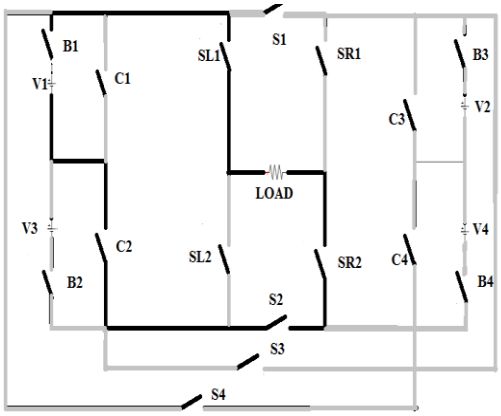

Figure 4(a). Level 1 (V0 = V1)

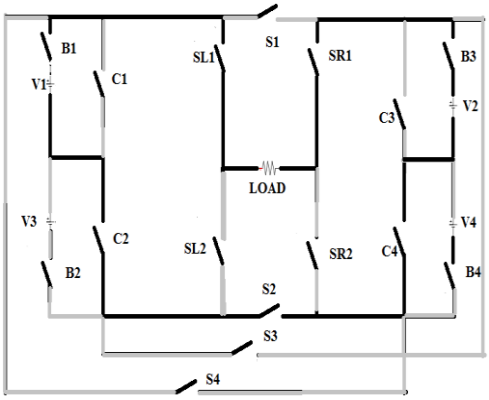

Figure 4(b). Level 2 (Vo= V2 –V1)

Table 2. Switching sequence for circuit ii

Step	Switching Sequence for Modular 49 level Modified H bridge type ACMLI															
	B1	B2	B3	B4	C1	C2	C3	C4	S1	S2	S3	S4	SL1	SL2	SR1	SR2
1	1	0	0	0	0	1	0	0	0	1	0	0	1	0	0	1
2	1	0	1	0	0	1	0	1	1	0	0	0	0	1	0	1
3	0	0	1	0	0	0	0	1	1	0	0	0	1	0	0	1
4	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1
5	0	1	0	0	1	0	0	0	0	1	0	0	1	0	0	1
6	1	1	0	0	0	0	0	0	0	1	0	0	1	0	0	1

Level 3: In this step the output voltage across the load is $V_o = V_2$. To achieve this step output the power devices B_{11}, B_{13}, B_{21}, B_{22}, B_{31}, B_{33}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices as shown in Figure 4(c).

Level 4: In this step the output voltage across the load is $V_o = V_2 + V_1$. To achieve this step output the power devices B_{11}, B_{12}, B_{21}, B_{22}, B_{31}, B_{33},B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step two sources take part in delivering the required power to the load through power devices.

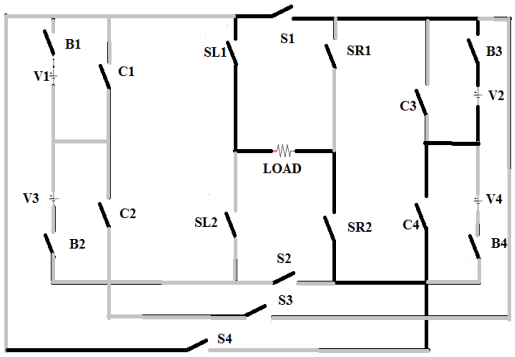

Figure. 4c. Level 3 ($V_0 = V_2$)

Level 5: In this step the output voltage across the load is $V_o = V_3$. To achieve this step output the power devices B_{13}, B_{14}, B_{21}, B_{23}, B_{31}, B_{32}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step only one source is delivering the power to the load through power devices.

Level 6: In this step the output voltage across the load is $V_o = V_3 + V_1$. To achieve this step output the power devices B_{11}, B_{13}, B_{21}, B_{23}, B_{31}, B_{32}, B_{41} and B_{43} are in ON condition and all the other power devices are not operated. In this step two sources take part in delivering the required power to the load through power devices.

In order to reduce the stress and count of power semiconductor components additive and subtractive concept is implemented with few input voltage sources. The selection of input voltage sources are made such that maximum output voltage is generated with small steps and with minimal number of voltage sources. The proposed circuit consists of four DC sources V_1, V_2, V_3, V_4 and sixteen power switches (S_1, S_2, S_3, S_4, S_{R1}, S_{R2}, S_{L1}, S_{L2}, etc.). As shown in the Figure 1, it should be noted that at the same time both the switches in the same leg should not be operated to eliminate short circuit issues. Similarly the switch S_1 and S_2 are not ON at the same time.

The modular topology proposed in this paper is operated by a high frequency sinusoidal multiple carrier PWM signal. In this scheme of the control twenty four high frequency triangular wave of same phase is compared with reference sinusoidal signal, the resultant signal developed is given as the firing pulse for the power electronic components after further processing and manipulation.

4. SIMULATION OUTPUTS

The developed fourty nine level ACMLI circuit is simulated with the help of MATLAB Simulink and the Simulink model is shown in Figure 5 and Figure 6. The input DC voltage sources V_1, V_2 , V_3 and V_4 for both the model are considered as 10 V, 30V, 50 V and 150 V respectively, the MOSFET is chosen as the power electronics components and the load is assumed as RL load with required filter circuit. The control method opted here is multi carrier sinusoidal PWM [25].The design of filter component is done in order to get pure sine waveform at the output [26]. The MATLAB model of the proposed circuit is shown in Figure 5 and Figure 6. The output voltage waveform for the total fourty nine-level ACMLI and Total harmonics distortion (THD) analysis is for both the circuit is shown in Figures 7-13 respectively.

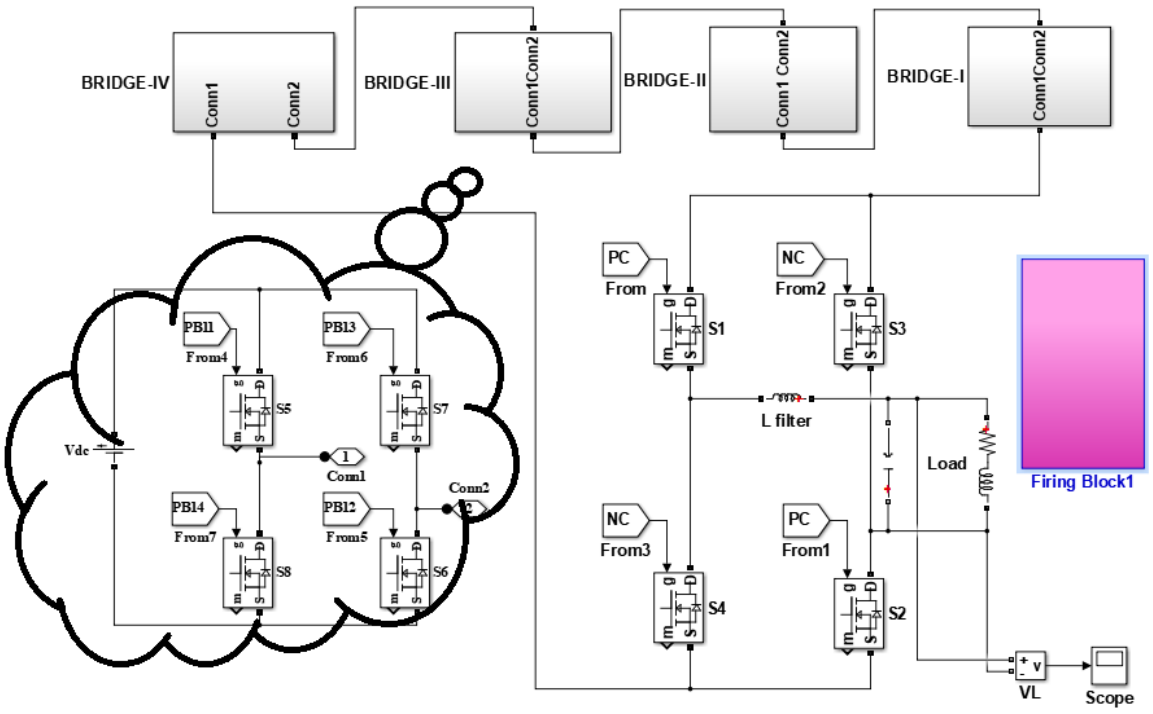

Figure 5. Simulink circuit for the proposed modular 49 level ACMLI

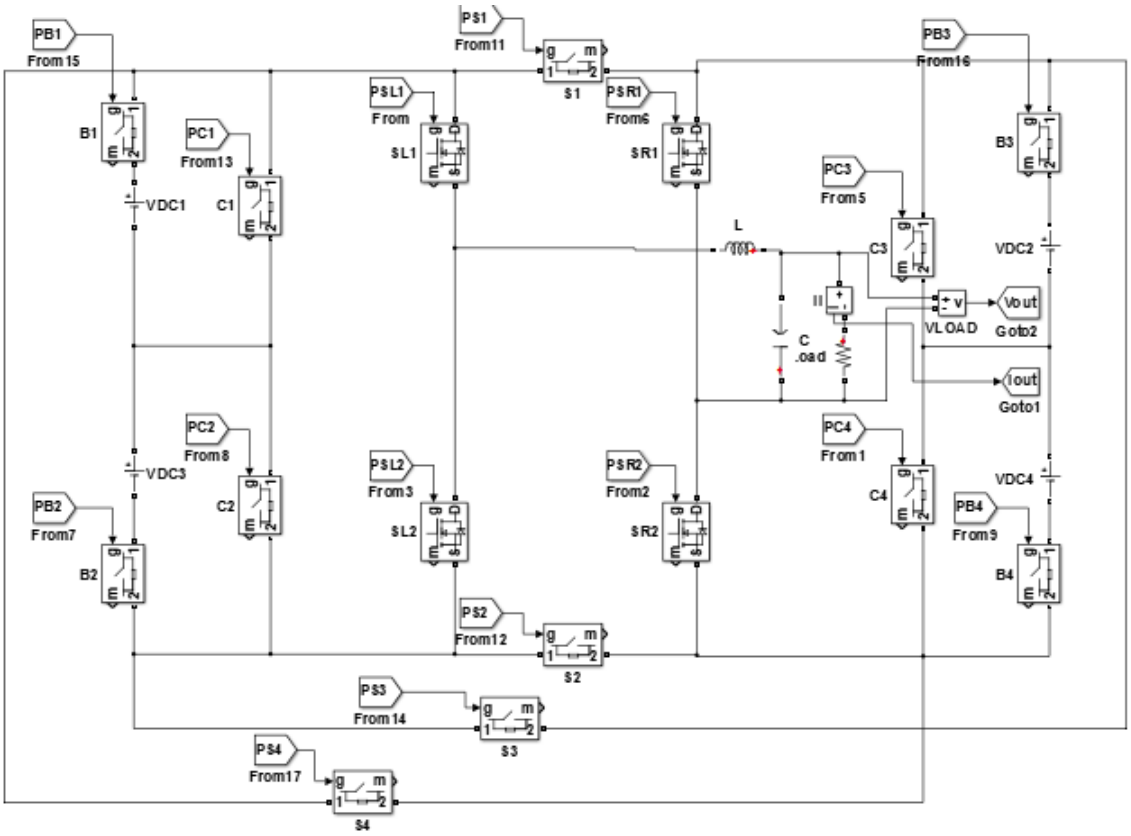

Figure 6. Simulink circuit for the proposed modular 49 level modified H bridge ACMLI

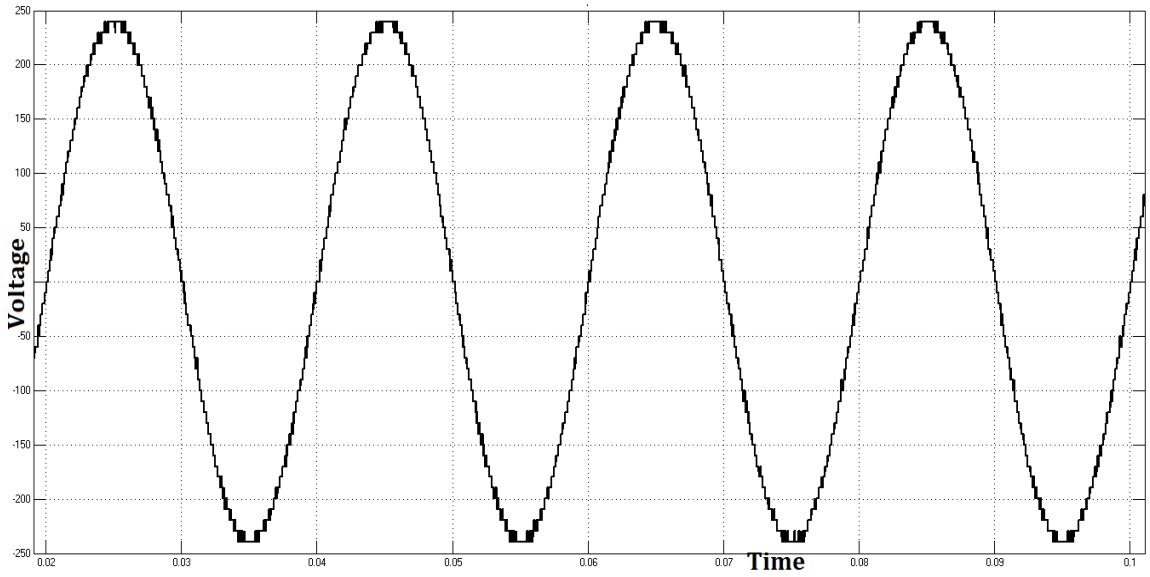

Figure 7. Output staircase waveform of voltage for proposed modular 49 level bridge type ACMLI without filter

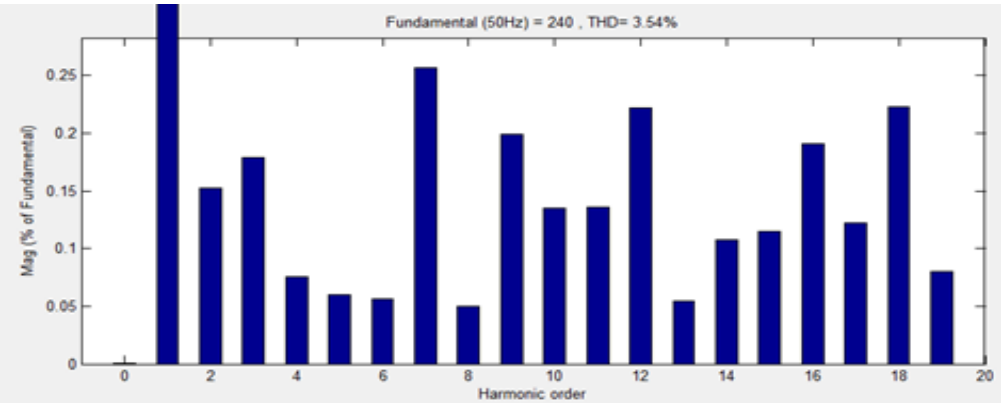

Figure 8. THD for proposed modular 49 level bridge ACMLI without filter

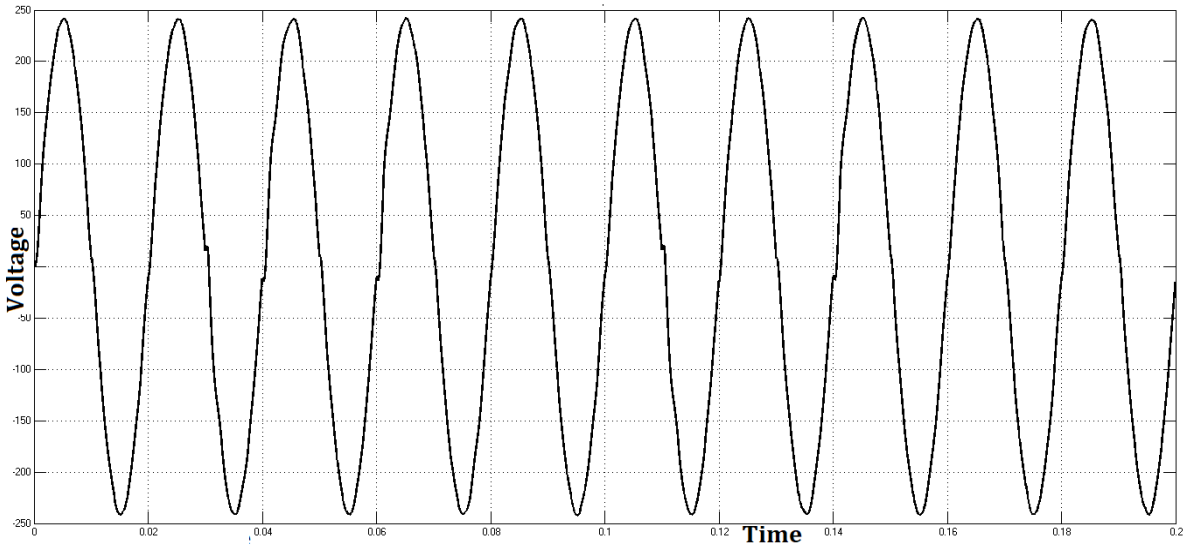

Figure 9. Output staircase waveform of voltage for proposed modular 49 level bridge type ACMLI with filter

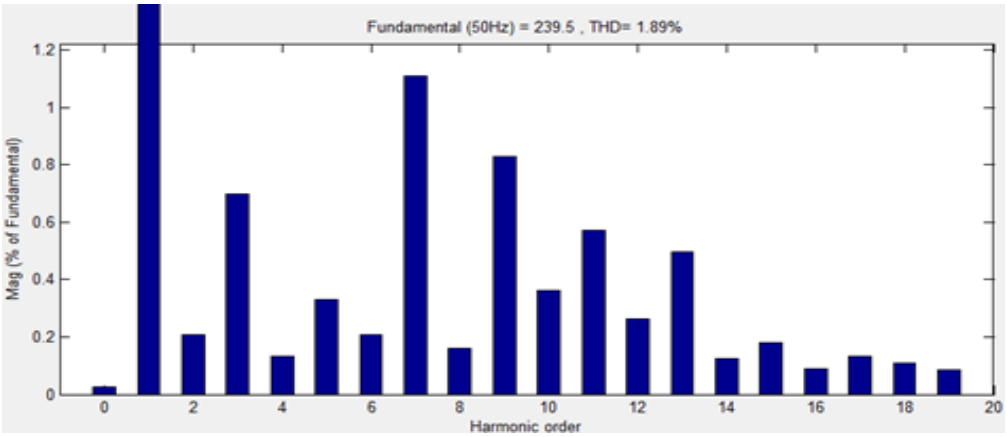

Figure 10. THD for proposed modular 49 level bridge ACMLI with filter

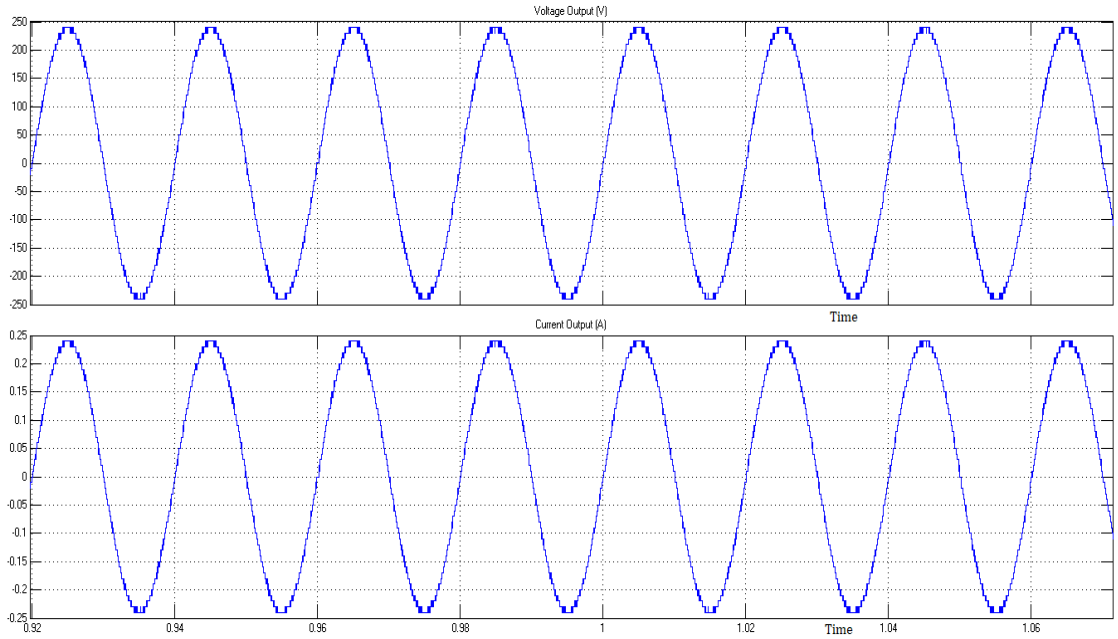

Figure 11. Output staircase waveform of voltage and current for proposed modified 49 level H bridge type ACMLI without filter

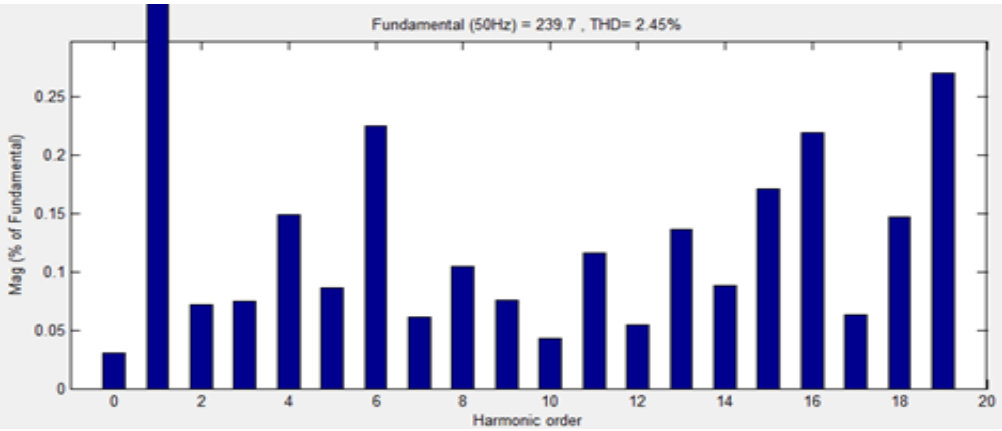

Figure 12. THD for proposed modified 49 level H bridge type ACMLI without filter

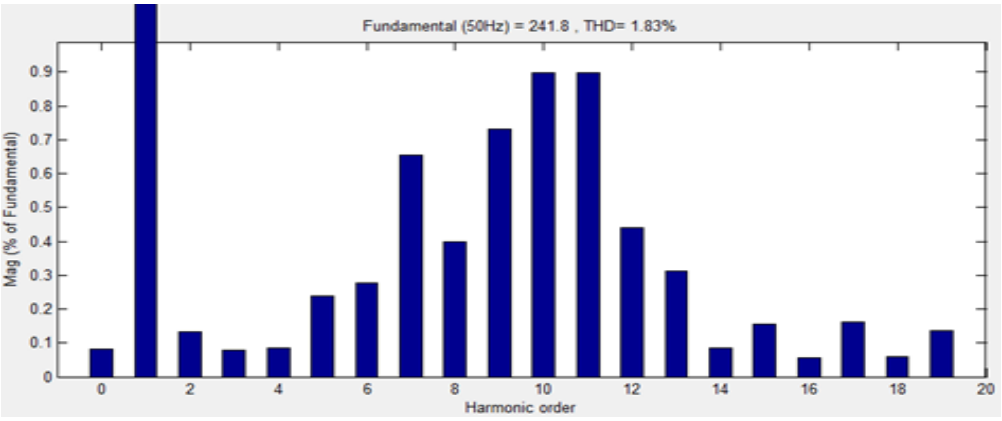

Figure 13. THD for proposed modified 49 level H bridge type ACMLI with filter

5. COMPARISON

The simulation results for the proposed MLI circuits are compared with existing MLI configuration with respect to the required sources, required switches and THD. From the result comparison shown in Table 3, it is found that the required sources by both the MLI circuit proposed is minimum compared to traditional bridge type and other MLI circuit refered. Modified H bridge ACMLI circuit requires the least number of switches compared to other MLI circuits for generating 49 levels and the THD is also minimum in modified H bridge ACMLI (1.83 %) compared to a all circuits

Table 3. Result comparison

Configuration	Required Sources	Required Switches	THD %
Basic bridge type	24	120	>3
Modular 49 level bridge type ACMLI	4	20	1.89
Modular 49 level modified H bridge ACMLI	4	16	1.83
Reference [15]	12	50	-
Reference [16] (27 level)	5	14	4.28

6. CONCLUSION

A modular multilevel inverter circuits are developed and proposed in this paper with the main objective to reduce the number of power electronics components. The working and sequence of operation of the proposed circuit is discussed and simulated. To generate the control pulse for the power electronics components an advanced multiple carrier control scheme is implemented. A detail control scheme for both the circuit is tabulated and the results were compared with basic MLI circuit with respect number of voltage sources and power electronics components. The developed circuit is analyzed with the help of MATLAB circuit in Simulink environment and the various analysis for single phase MLI were shown.

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