International Journal of Electrical and Computer Engineering (IJECE) Vol. 5, No. 5, October 2015, pp. 957~966 ISSN: 2088-8708

957

An Interleaved Boost Converter Based PFC Control Strategy for **BLDC** motor

V. Ramesh, Y. Kusuma Latha

Department of Electrical and Electronics Engineering, K L University, Vaddeswaram, India

Article Info	ABSTRACT
<i>Article history:</i> Received Apr 28, 2015 Revised Aug 6, 2015 Accepted Aug 21, 2015	In this paper, interleaved power factor correction (PFC) boost converter based control strategy for BLDC motor has been proposed. The converter exhibits the characteristics of voltage doubler for duty greater than 0.5. The switching losses and losses during reverse recovery operation are considerably reduced in this proposed topology. The due reduction in switching voltages due to voltage doubler mode. The proposed topology has
<i>Keyword:</i> BLDC Motor Four switch VSI Interleaved boost converter	high efficiency compared to conventional counterpart due to slight increase in conduction losses. In this paper, the proposed PFC control strategy has been applied to six switch and four switch VSI fed BLDC Motor drive for effective torque ripple minimization. A comparison is also made between the six switch and Four Switch VSI fed PMBLDC Motor drive.
Power factor correction Six switch VSI	Copyright © 2015 Institute of Advanced Engineering and Science. All rights reserved.
Company on line Arathan	

Corresponding Author:

V. Ramesh, Departement of Electrical and Electronics Engineering, K L University, Vaddeswaram, Guntur Dt, Andhra Pradesh, India - 522502. Email: rameshvaddi6013@kluniversity.in

1. **INTRODUCTION**

The evolution of power rating drives for domestic applications ranging from a sample fans, mixers to water and efficiency as the major concern. The inherent advantages of BLDC motor like high efficiency higher flux density less maintaince low cost and less problems of electromagnetic interference [1]-[2]. In addition to domestic applications they are extensively used in motion control medical and transportation fields and numerous industrial applications where torque ripple is of primary concern. The increase in the number of switches implies high switching losses and also increased cost [3]. In order to over come this problem a new topology is proposed which reduces the number of switches (instead of 6,'4'switches are used) [4].

The presence of two interleaved boost converter channels achieves natural self balancing of currents in order to present current sharing. This further reduces the number of current sensing components and further reduces the total number of components causing increase in power density [5]. The efficiency of the proposed converter at high line voltage is slightly decreases due to slight increase in conduction losses [6]-[7]. However, high line voltage has negligible impact efficiency [8]. The characteristics of converter the heat sinks and thermal design aspects are decided by efficiency at full load and lower line voltage is increased with the help of proposed converter topology [9]-[10].

In this paper proposed topology six switch and Four switch based VSI fed BLDC motor. With interleaved PFC converter is presented. A comparison is made between two schemes. The proposed control strategy reduces the losses due to switching and ripples in the toque output of BLDC motor. The inter leaved boost converter with the special characteristic of voltage doubler mode is used to control the DC linkvoltage The reduction of the power electronics of switches by '2' enhances the reliability of the system, reduces the sizes of inverter which in turn reduces the makes the system economical for usage.

2. DESCRIPTION OF PROPOSED INTERLEAVED PFC BOOST CONVERTER WITH VOLTAGE DOUBLER CHARACTERISTICS

The proposed power factor corrected interleaved converter voltage incorporating voltage doubler nature is presented in section Figure1 shows simple block diagram of the proposed topology of interleaved PFC boot converter based BLDC motor drive. Figure 2 shows the simplified circuit diagram of the proposed topology.

It is assumed that the switching are ideal the ripple the capacitor voltage C_B and C_F negligible. Therfore, the capacitors one represented as voltage sources.

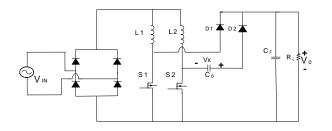


Figure 1. Proposed topology of interleaved PFC boost converter

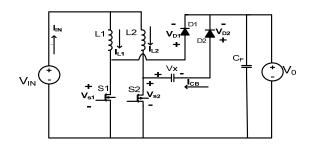
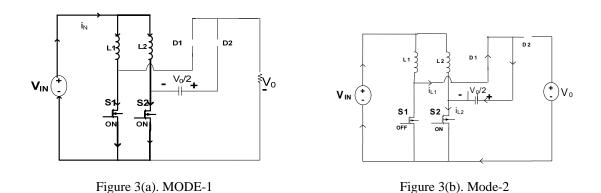


Figure 2. Simplified circuit diagram of the proposed topology

MODE OF OPERATION:

Mode1:

In mode I, during the time interval T_0 - T_1 , both switches S_1 and S_2 are conducting on. Here, inductor currents i_{L1} and i_{L2} are increasing at the same rate. Figure 3 (a) represents the equivalent circuit diagram of the converter during the time interval T_0 - T_1 and the timing wave form are represented in Figure 4



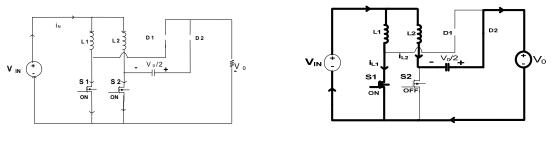


Figure 3(c). Mode-3

Figure 3(d). Mode-4

$$V_{IN} = L_1 \frac{diL1}{dt} = L_2 = \frac{diL2}{dt}$$
(1)

It is assumed that the inductance are identical $L1 = L_2 = L$. During this mode D_1 and D_2 are non conducting, hence C_F supplies the load current.

$$\frac{\mathrm{di}\mathrm{L1}}{\mathrm{dt}} = \frac{\mathrm{di}\mathrm{L2}}{\mathrm{dt}} = \frac{\mathrm{V}_{\mathrm{IN}}}{\mathrm{L}} \tag{2}$$

MODE-2

At time instant T_1 , S_1 is switched off current through inductor L_1 passed through S_1 as shown figure 3(b) is diverted from the switch to rectifier D₁, as shown in Figure 3(b), The C_B dischanges the energy stored in the inductor L₁

The rate of decrease is given by

$$V_{IN} = L1 \frac{diL1}{dt} + \frac{Vo}{2} \tag{3}$$

From (3), identical inductances L=L1

$$\frac{diL1}{dt} = \frac{1}{L} \left(V_{IN} - \frac{V0}{2} \right)$$
(4)

MODE-3

In mode 3, CB is charged At time instant T₂ operation is same as mode 1

MODE-4

In mode 4, at time instant T₃ switched off and current in the inductor is diverted to corresponding Diode D_2 . At t=T₃, When switch S₂ is switched off the current through inductor i_{L2} is commutated from switch S_2 into rectifier D_2 . In this stage energy stored in L_2 dischrege into C_F as shown in Figure 3 (d).

The rate of drecease in current is given by

$$V_{IN} = L1 \frac{diL2}{dt} - \frac{Vo}{2} + V_0$$
(5)

$$\frac{diL2}{dt} = \frac{1}{L} \left(V_{IN} - \frac{V0}{2} \right)$$
(6)

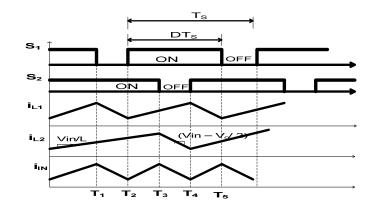


Figure 4. Timing diagrams (0.5<D <1)

After mode 4 the switching cycle is repeated and switch S1 switched on. The duty cycle given by

$$V_{IN} = \left(\frac{Vo}{2} - V_{IN}\right) \cdot (1 - D)T_S \tag{7}$$

So that

$$\frac{Vo}{VIN} = \frac{2}{1-D} (0.5 \le D < 1)$$
(8)

The voltage doubler characteristic is observed for duty cycle greater than 0.5 and the PFC boost converter is operating at lower line voltage (typically 85V) and greater than 0.5. The voltage ratio of the proposed converter twice that of conventional converter .The rms value of switch current is smaller than that conventional converter part.

The ratio of the RMS switch currents during a switching cycle is

$$\frac{iRMS, interleaved_doubler}{iRMS, interleaved_boost} = \sqrt{\frac{M-2}{M-1}} \quad (0.5 \le D < 1)$$
(9)

Where, $M=V_0/V_{in}$ and typically 'M' is always greater than as equal to '4'. The switch conduction loss of the proposed rectifier at M=4 is the switching losses of the proposed converter M=4 is 67% of the losses in case of the losses in case of conventional one. Also conduction losses are less for proposed converter.

3. PROPOSED INTERLEAVED PFC BOOST CONVERTER FOR VSI FED BLDC MOTOR

The interleaved PFC boost converter based BLDC motor drive system with two configurations preented in the following section. The closed loop control of BLDC motor drive system is shown in Figure 5. The topology shows some draw back s like bulky current sensors which increase the cost and more ripple in torque content.



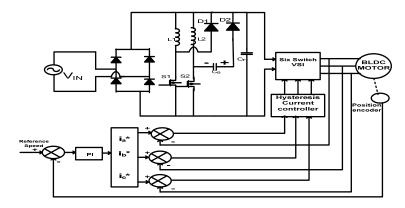


Figure 5. Six Switch VSI fed BLDC drive with interleaved PFC boost converter

The closed loop control four switch as fed BLDC motor drive system with interleaved boost converter is shown in figure 6. This schems is more advantageous with 2 current sensors 4 power electronic switches reduces as well as cost and switching losses, enhancing the performance of the system in terms of lower voltage stress and faster dynamic response. In view of all the above, the proposed converter has added advantages compared to the conventional counterpart for BLDC motor.

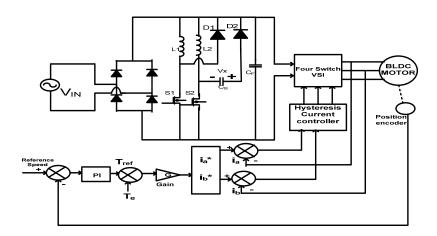
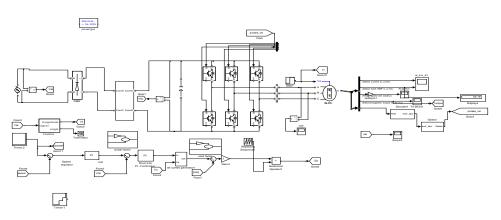
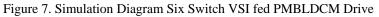


Figure 6. Four Switch VSI fed BLDC drive with interleaved PFC boost converter

4. RESULTS AND DISCUSSION

4.1 Six Switch VSI fed PMBLDCM Drive:





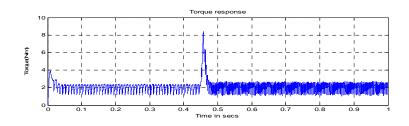


Figure 8. Torque wave form under variable Speed Condition

The performance of the three leg inverter fed PMBLDCM drive with interleaved boost converter under constant torque with variable speed is evaluated with speed variation from 300 rpm to 750 rpm at rated torque of 3 Nm. Figure 7 shows the performance of PMBLDCM drive using Six switch VSI fed PMBLDCM drive with interleaved boost converter at constant torque with variable speed condition. Figure 8 shows the torque response of Six Switch Three Phase Inverter fed PMBLDCM drive with interleaved boost converter. It is observed that the toque rises initially at t=0.01 sec from 0 N-m to 3.8 -m and later it fluctuates between 2.5N-m and 2.8N-m there onwords. During the t=0.45sec speed transition from 350rpm to 750rpm the torque momentarily rises to 8.5N-m.

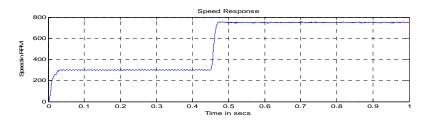


Figure 9. Speed wave form of the drive at constant load torque and variable speed condition

Figure 9 shows the speed wave form of BLDC motor in comparision with reference speed. The speed raises from 200rpm at t=0.01sec and suddenly falls to 300rpm .Further, the speed raises to 300rpm at t=0.03sec the speed is maintained around 300rpm from t=0.03sec. At t=0.45 sec the speed raises from 300 to 750 rpm and gradually settles down at t=1 sec to a steady state value of 750rpm .

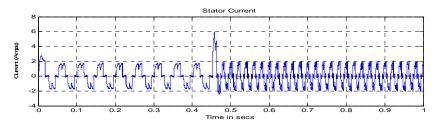


Figure 10. Stator current response at constant Torque with variable speed condition

Figure 10 shows the stator current waveform of one of the phase of BLDC motor drive system. The stator current at t=0.01 sec is maintained at constant value of 2.8Amps. During the abrupt change in speed from 300rpm to 700rpm at t=0.45 sec the stator current raises to 6.0Amps and reaches to previous value of the current wave form.

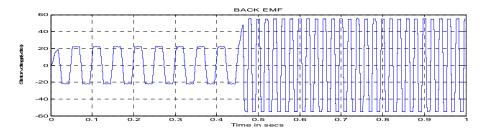


Figure 11. Back EMF at constant torque with variable speed condition

Figure 11 shows the Back EMF response at constant torque with variable speed. As we know that back EMF is proportional to the speed, at t=0.02sec, the set speed is 300rpm and motor reaches to set 300rpm and the magnitude of back emf is 20V, and motor reaches to set speed of 750 rpm at t=0.45sec and the magnitude of back emf is 55V.

4.2 Four Switch VSI fed PMBLDCM Drive

The performance of Four Switch VSI fed PMBLDCM drive with interleaved boost converter under constant torque with variable speed is evaluated with a speed variation from 300 rpm to 750 rpm at rated torque of 3 Nm. Figure 6 shows the torque response of Four Switch VSI fed PMBLDCM drive with interleaved boost converter. Figure 13 shows the toque output of BLCD motor with proposed drive model of BLDC motor. It is observed that the toque rises initially at t=0.01 sec from 0 N-m to 2N-m and later it fluctuates between 2.5N-m and 3.8N-m there onwords. During the t=0.45sec speed transition from 350rpm to 750rpm the momentarily raises to 15N-m.Torque ripple content is less when compared with Six Switch Three Phase Inverter fed PMBLDCM Drive. But at starting motor rotates with very high speed.

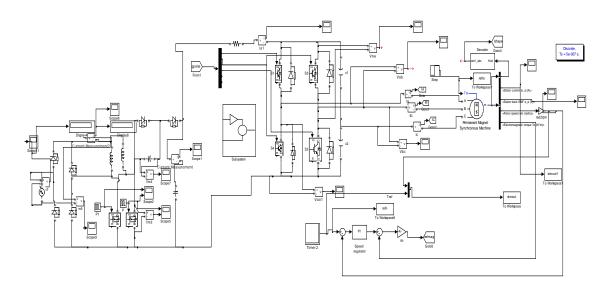


Figure 12. Simulation Diagram Four Switch VSI fed PMBLDCM Drive



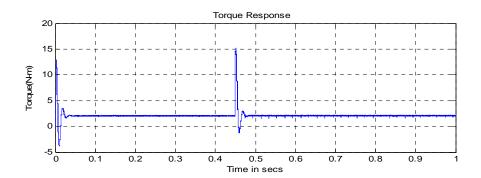


Figure 13. Torque waveform under variable speed condition

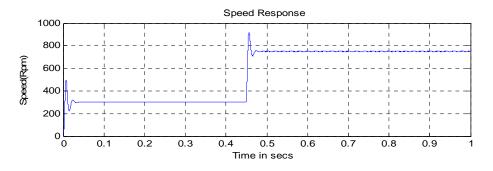


Figure 14. Speed wave form of the drive at constant load torque and variable speed condition

Figure 14 shows the speed dynamic response of the BLDC drive initially, the speed gradually settles down to 300 rpm at t = 0.45 sec the speed is altered from 300rpm to 750 rpm. The motor reaches to final steady speed 750 rpm with in 1sec.

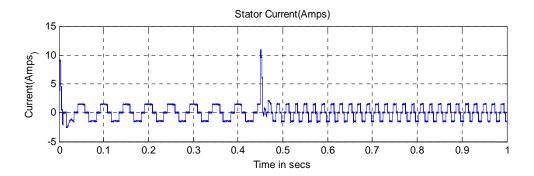


Figure 15. Stator current response at constant Torque with variable speed condition

Figure 15 Shows the stator current response one of the phase of BLDC motor. The stastor current in 9 Amps at the time starting (i.e t=0.01 sec) and reaches a steady value of 1.6 Amps. During the dynamic response of BLDC motor drive system at (t=0.45 sec change in speed from 350rpm to 750 rpm) the reaches 11 Amps at t=0.45 sec. The stator current finally reached its perious steady state values of 1.6 Amps at the t=0.45 sec

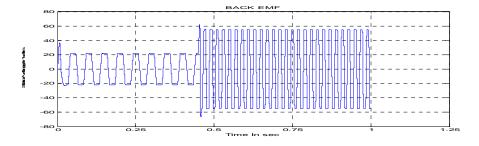


Figure 16. Back EMF at constant torque with variable speed condition Four Switch VSI

Figure 16.shows the Back EMF waveform at constant torque with variable speed. As we know that back EMF is proportional to the speed, at t=0.02sec, the set speed is 300rpm and motor reaches to set speed 300rpm and the magnitude of back emf is 38V, and motor reaches to set speed of 750 rpm at t=0.45sec and the magnitude of back emf is 55V.

Table 1. Comparison of Toque ripple		
Type of Scheme	Torque Ripple	
Six Switch VSI fed BLDC Motor drive	1.18 N-m	
Four Switch VSI fed BLDC Motor drive	0.198N-m	

Table 1 shows the torque comparison between six switch VSI and Four switch VSI fed PMBLDC Motor drive. It is observed that torque ripple in six switch VSI fed PMBLDC Motor drive is 1.18 N-m and for four switch VSI fed PMBLDC Motor drive it is 0.198 N-m.

5. CONCLUSION

In this paper two configuration of BLDC motor drive topologies namely four switch and six switch VSI is presented along with interleaved PFC boost converter. The proposed converter has improved efficiency at low lines voltage due to reduction in conduction as well as switching losses. The reduction in conduction losses is attributed to the voltage doubler characteristics of interleaved PFC converter reduces the currents through the switches. This paper presents comparative analysis of four switch and six switch voltage source fed BLDC motor. The results inferred that toque ripple as well on the losses during switching are reduced in case of four switch topology when compared with six switch topology BLDC drive. Therefore four switch VSI fed BLDC drive system with interleaved PFC converter proved to have advantages and efficient.

REFERENCES

- [1] Y. Jang and M.M. Jovanovic', "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end", *IEEE Trans. Power Electron*, vol. 22, no. 4, pp. 1394–1401, Jul. 2007
- [2] Yao-Ching Hsieh, Te-Chin Hsueh, and Hau-Chen Yen "An Interleaved Boost Converter with Zero-Voltage Transition", *IEEE Trans. Power Electron*, Vol. 24, No. 4, April 2009.
- [3] S. Rajagopalan, J.M. Aller, J.A. Restrepo, T.G. Habetler, and R.G. Harley, "Analytic-wavelet-ridge-based detection of dynamiceccentricity in brushless direct current (BLDC) motors functioning underoperating conditions", *IEEE Trans. Ind. Electron.*, vol. 54, no. 3, pp. 1410–1419, Jun. 2007.
- [4] G.J. Su and J.W. Mckeever, "Low-cost sensorless control of brushlessDC motors with improved speed range", *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 296–302, Mar. 2004.
- [5] C.T. Pan and E. Fang, "A phase-locked-loop-assisted internal modeladjustable-speed controller for BLDC motors", *IEEE Trans. Ind. Electron.* vol. 55, no. 9, pp. 3415–3425, Sep. 2008.
- [6] L. Parsa and H. Lei, "Interior permanent magnet motors with reduced torque pulsation", *IEEE Trans. Ind. Electron*, vol. 55, no. 2, pp. 602–609, Feb. 2008.
- [7] D.H. Jung and I.J. Ha, "Low-cost sensorless control of brushless DCmotors using a frequency-independent phase shifter", *IEEE Trans. PowerElectron*, vol. 15, no. 4, pp. 744–752, Jul. 2000.
- [8] J.H. Lee, S.C. Ahn, and D.S. Hyun, "A BLDCM drive with trapezoidalback EMF using four-switch three phase inverter", in *Conf. Rec. IEEE IASAnnu. Meeting*, 2000, vol. 3, pp. 1705–1709
- [9] M.S Jayakumar, Ajeesh G, "A High Efficient High Input Power Factor Interleaved Boost Converter International, *Journal of Electrical and Computer Engineering (IJECE)*, Vol. 2, No. 3, June 2012, pp. 339~344ISSN: 2088-8708

[10] Subramanya Bhat, Nagaraja HN "Effect of Parasitic Elements on the Performance of Buck-Boost Converter for PV Systems, *International Journal of Electrical and Computer Engineering (IJECE)*, Vol. 4, No. 6, December 2014, pp. 831~836 ISSN: 2088-8708

BIOGRAPHIES OF AUTHORS



V. Ramesh received his B.Tech degree in Electrical & Electronics Engineering from Vaagdevi Institute of Technology and Science, Proddatur, India and M.Tech degree from Sreenivasa Institute of Technology and Management Studies, Chittor, India in 2008 and 2013 respectively.He is presently pursing Ph.D in K L University, Vaddeswaram, India. His areas of interest are Power Electronics & Drives



Y. Kusuma Latha received the B.E (Electrical and Electronics Engineering) degree from Nagarjuna University, Guntur.A.P, India, M.Tech degree from Jawaharlal Nehru Technological University, Anantapur, India in 2000 and 2004 respectively. She received her Ph.D degree from Jawaharlal Nehru Technological University, Anantapur, in 2011. She is presently working as an Professor, Department of EEE, K L University, Green Fields, Vaddeswaram, Guntur District. Her areas of interest are Power Quality, Harmonic mitigation techniques, Active power filters and DSP Controllers