

A Modulation Scheme for Floating Source Multilevel Inverter Topology with Increased Number of Output Levels

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ABSTRACT

This paper presented and studied a new switching scheme for floating source multilevel inverters to produce more levels with the same number of switching devices. In the proposed scheme, the function of the dc sources, except the inner one, is to build up square wave or blocks that is close in the shape to the desired sinusoidal wave. The job of the inner switching devices is to increase the number of the levels to produce smother sinusoidal wave in the inverter output. This job can be done by adding or subtracting the value of the inner dc source to/from the blocks. The topology used in this paper is based on the conventional floating source multi-level inverter using two legs. This topology and modulation technique show substantial reduction in the total harmonics distortion when the modulation technique is the hybrid method. The performance of the proposed switching scheme in generating more levels has been evaluated by PSCAD/EMTDC simulation.

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1. INTRODUCTION

Multilevel inverters have attracted the attention of several researchers for different advantages such as its low output total harmonic distortion (THD), low switching device stress, and reduced switching stress [1]. Besides, it be used to improve systems power quality using modern FACTS application [2],[3]. In the industry, switching devices are used in Electric and hybrid Electric vehicles but limitation of these devices is one of the issues that need to be solved [4]. The voltage across each switching devices in DC-DC converters can be reduced by connecting series capacitor in the input. This voltage is equal to total input voltage divided by the number of the capacitors. For instance, if there are five series capacitors, the voltage across each switching device is one-fifth the input voltage. This method is explained in [5] and [6] using three capacitors. Multilevel inverters applied the same concept of distributing the input voltage evenly among the switching devices by connecting a set of series capacitors in the input. The resulted output voltage of this configuration has lower harmonics and less voltage stress across the switching devices. Multilevel inverters are divided into three main types: neutral-point clamped or diode-clamped (NPC) [7], [8], flying capacitor (FC) [9], [10] and cascaded H-bridge inverters [11]-[13]. These multilevel inverters are controlled by several techniques, as in [14], where the most common technique is multicarrier sinusoidal pulse width modulation (SPWM) [15] and [16]. As the number of levels in the multilevel inverter output increases, the wave is near sinusoidal shape with less harmonics. However, the increase in the number of the levels is associated with several issues such as significant DC-link voltage balancing difficulties and additional clamping diodes as in the NPC and FC [17] and [18]. There are several topologies that produce decent number of levels in the output, however, they use H-bridge to generate the negative polarity [4], [19] with very high rating power switches. While the

others used bidirectional switches instead of H-bridge as in [20] where it is preferable to use unidirectional switches instead of bidirectional ones due to its higher cost.

In this paper, a proposed switching scheme is evaluated and analyzed to control the floating source (FS-MLI) in [21] using two legs. This technique has the advantage of not utilizing H-bridge to produce negative levels. Besides, it uses unidirectional switches to with lower rates. The switching control method is can use hybrid modulation concept to further reduce harmonics distortion. This technique has a remarkable disadvantage that it lacks for modularity and is more suitable for medium- and low-voltage applications. The simulation results of 11-level inverter using PSCAD/EMTDC software are presented for the purpose of validity.

2. FLOATING SOURCE TOPOLOGY

The floating source multilevel inverters (FS-MLI) configuration with one leg is shown in Figure 1. It is similar to the flying-capacitor (FC) inverter except that the capacitors are replaced with separate dc voltage sources. As it is shown in the figure, it consists of three separate dc sources and three pairs of switching devices (S_{A1}, S'_{A1}), (S_{A2}, S'_{A2}), and (S_{A3}, S'_{A3}). These switching devices are unidirectional and each one of them consists of IGBT and an anti-parallel diode. The switches (S_{A3}, S'_{A3}) must not turn on simultaneously or they will short-circuit the source V_{A3} . When the voltage ratio of the dc sources $V_{A1} : V_{A2} : V_{A3}$ is 3 : 2 : 1, the output voltage of the inverter for each phase, v_o , is four levels. The general form of the FS-MLI should have the following expressions:

$$N_{switches} = 2N_{cells} \quad (1)$$

$$N_{levels} = N_{cells} + 1 \quad (2)$$

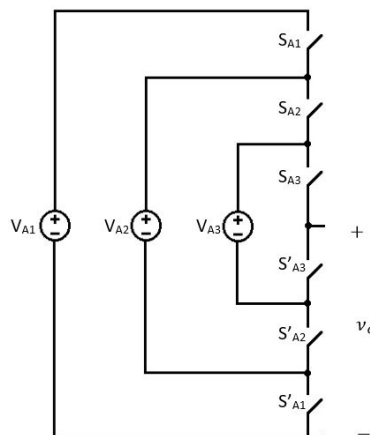


Figure 1. Three-cells floating source multilevel inverters (FS-MLI)

3. PROPOSED SWITCHING SCHEME

In this paper, the proposed switching technique is analyzed on 11-level MLI and then on n-level MLIs.

3.1. 11-level FS-MLI Configuration

In the proposed switching scheme, the negative part must be generated using the structure of the FS-MLI with no H-bridge. Therefore, the proposed switching scheme is designed to work on two legs of the FS-MLI instead of one. 11-level FS-MLI with two legs is shown in Figure 2. The leg on the left side is noted as leg A and the leg on the right side is noted as leg B. Each leg consists of three dc sources and six switching devices. The inner dc sources V_{A3} and V_{B3} may get short-circuited accidentally when (S_{A3}, S'_{A3}) and (S_{B3}, S'_{B3}), respectively, turn on simultaneously. The voltage ratio of the dc sources $V_{A1} : V_{A2} : V_{A3}$ and $V_{B1} : V_{B2} : V_{B3}$ must be 5 : 3 : 1. This ratio is a mandate to generate more levels at the output line voltage. Table 1 presents the switching states to produce 11-level line voltages at the output of the inverter. This switching scheme has the advantage that all the voltages of the dc sources build up core blocks similar to the sinusoidal

wave, Figure 3, except the inner dc sources, V_{A3} and V_{B3} where they are used to produce new levels at the mid of each block. In other words, the first block has the period between $t_1 < T < t_8$ with the magnitude of 2 pu, while the second block has the period between $t_3 < T < t_6$ is 2 pu as well. The sum of these two blocks is 4 pu to form a steps wave that mimics the desired sinusoidal wave. V_{A3} and V_{B3} are used to produce the levels 1 pu, 3 pu, and 5 pu by adding and deducting 1 pu (the magnitude of V_{A3} and V_{B3}) to and from the two blocks.

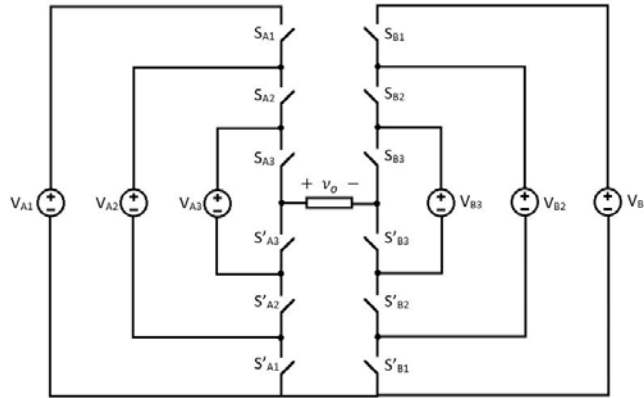


Figure 2. 11-level floating source multilevel inverters (FS-MLI) with two legs

Table 1. Recommended Switch Combination for v_o

State	Output v_o	Switch States					
		LEG-A			LEG-B		
		S_{A1}	S_{A2}	S_{A3}	S_{B1}	S_{B2}	S_{B3}
1	V_{A1}	1	1	1	0	0	0
2	$V_{A1} - V_{A3}$	1	1	0	0	0	0
3	$V_{A1} - V_{A3} - V_{B3}$	1	1	0	0	0	1
4	V_{A2}	0	1	1	0	0	0
5	$V_{A2} - V_{A3}$	0	1	0	0	0	0
6	$V_{A2} - V_{A3} - V_{B3}$	0	1	0	0	0	1
7	V_{A3}	0	0	1	0	0	0
8	0	0	0	0	0	0	0
9	$-V_{B3}$	0	0	1	0	1	0
10	$-(V_{B2} - V_{B3} - V_{A3})$	0	0	0	0	0	1
11	$-(V_{B2} - V_{B3})$	0	0	0	0	1	0
12	$-V_{B2}$	0	0	1	1	1	0
13	$-(V_{B1} - V_{B3} - V_{A3})$	0	0	0	0	1	1
14	$-(V_{B1} - V_{B3})$	0	0	0	1	1	0
15	$-V_{B1}$	0	0	0	1	1	1

3.2. n-level FS-MLI Configuration

By analyzing the 11-level FS-MLI, a general structure can be developed. Figure 4 shows the n-cell FS-MLI. The number of levels (N_{levels}), number of switching devices ($N_{switches}$), number of dc sources ($N_{sources}$), and total size of dc sources in pu ($T_{sources}$) are calculated as follows:

$$N_{levels} = 2N_{cells} - 1 \tag{3}$$

$$N_{switches} = 2N_{cells} \tag{4}$$

$$N_{sources} = N_{cells} \tag{5}$$

$$T_{sources} = 2 \sum_{i=1}^{N_{cells}} (2i - 1) \tag{6}$$

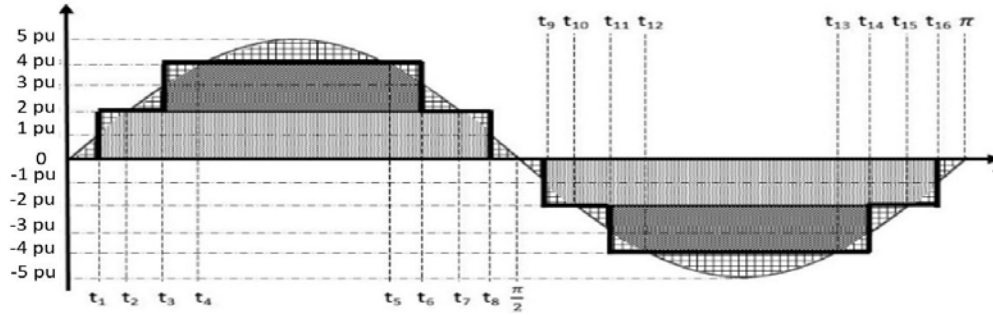


Figure 3. Desired sinusoidal wave with two blocks in each half-cycle

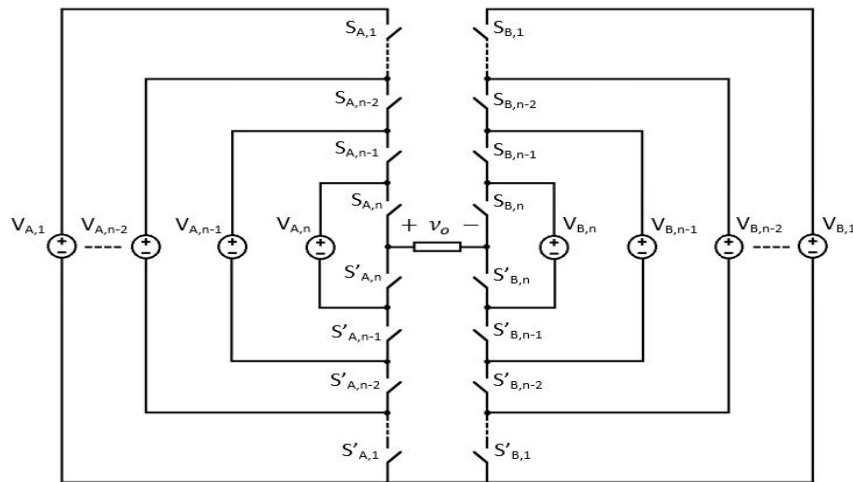


Figure 4. n-level floating source multilevel inverters (FS-MLI) with two legs

3.3. Hybrid modulation scheme

The switching frequency of the FS-MLI is equal to the frequency of the line, e.g., 60 Hz or 50 Hz. The inner switches ($S_{A,n}$, $S'_{A,n}$) and ($S_{B,n}$, $S'_{B,n}$) has the lowest stress, dv/dt . Therefore, these switches may turn at high frequency to reduce the THD without being subjected to high switching stress. When the switches operate at different frequency, the modulation scheme is denoted as hybrid modulation. The modulation of the inner switches is achieved by obtaining the waveform of the area shaded with large grid pattern Figure 3:

$$v_{ref} = V_1 \sin(2\pi ft) - 0.4[u(t - t_1) - u(t - t_8) - u(t - t_9) + u(t - t_{16})] - 0.4[u(t - t_3) - u(t - t_6) - u(t - t_{11}) + u(t - t_{14})] \quad (7)$$

Where $u(t)$ is a unit step function. One can obtain the general expression of the v_{ref} by first finding the number of blockes per half-cycle using the following equation:

$$N_{blocks} = N_{cells} - 1 \quad (8)$$

Then the peak of each block can be obtained as follows:

$$V_{block} = \frac{1}{N_{blocks} + 0.5} \quad (9)$$

By knowing the peak of the blocks it would be possible to find the intervals of each block. But first we need to find the number of starts and ends of the blocks per half-cycle, e.g., t_1 , t_3 . This step is achieved by using this formula

$$T_{blocks} = 4N_{blocks} \tag{10}$$

Finally, the general expression of v_{ref} is calculated as follows:

$$v_{ref} = V_1 \sin(2\pi ft) - V_{block} \left[\sum_{i=1,3,5,\dots}^{\frac{T_{blocks}-1}{2}} u(t - t_i) - u(t - t_{i+T_{blocks}}) + \sum_{j=2,4,6,\dots}^{\frac{T_{blocks}-2}{2}} u(t - t_{T_{blocks}-j}) - u(t - t_{2T_{blocks}-j}) \right] \tag{11}$$

In Figure 4, the reference wave v_{ref} is presented along with the gate signals. The reference wave v_{ref} is modulated using two triangular carriers, cr_1 and cr_2 . The positive side of v_{ref} is compared with the carrier wave cr_1 to drive the switch S_{A3} . And the carrier wave cr_2 is compared with v_{ref} in the negative side to control the switch S_{B3} . The modulation index, m , that has range from 0 to 1 is defined as

$$m = \frac{v_{ref}}{cr_{1,2(peak)}} \tag{12}$$

The total harmonics distortion is one of the major performance evaluation factors and it can be calculated using Fourier series. First, we need to obtain the amplitude of the n^{th} -harmonics of the FS-MLI output:

$$b_n = \frac{4V_{dc}}{n\pi} \left[1 + \sum_{i=1}^{N_{levels}-2} \cos(n\alpha_i) \right] \text{ for } n \text{ odd} \tag{13}$$

Where α_i is the angle corresponds to t_i and obtained by multiplying the time by 360π . The calculation of b_1 when $m = 0.9, 0.6,$ and 0.3 are listed in Table 2. According to the data shown in this table, when the modulation index m decreases, the number of the switching angles decreases as well.

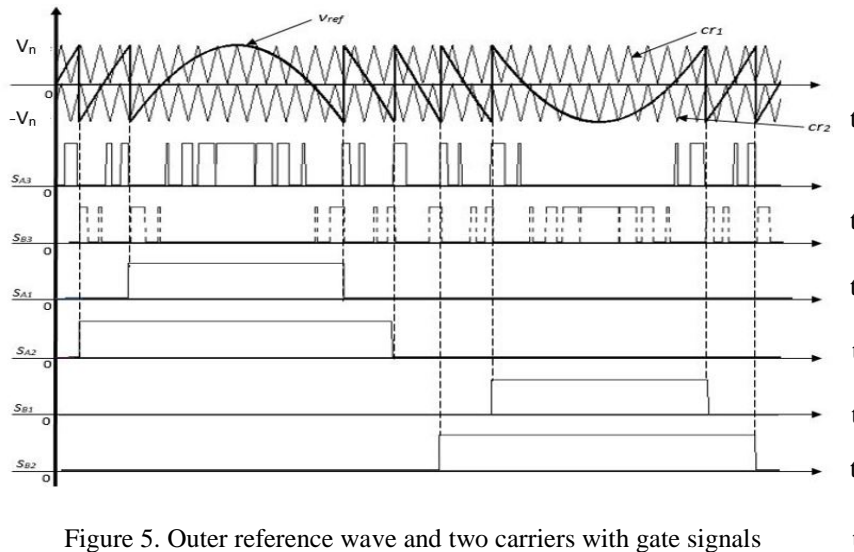


Figure 5. Outer reference wave and two carriers with gate signals

Finally the THD can be calculated using the following expression:

$$THD = \frac{\sqrt{\sum_{n=3,5,7,\dots}^{\infty} b_n^2}}{b_1} \tag{14}$$

Table 2. The value of Inverter Output with Corresponding Switching Angles (without Hybrid Modulation)

m	b_1 (rms) in pu*	α_1	α_2	α_3	α_4
0.9	0.73	12.84°	26.39°	41.81°	62.73°
0.6	0.48	19.47°	41.81°	-	-
0.3	0.31	41.81°	-	-	-

*Base Value is 1

4. COMPARATIVE ANALYSIS

The proposed switching method has advantages and disadvantages. To provide these advantages and disadvantages it is of great importance to compare it with some other topologies and modulation techniques mentioned in the literature. In [4], the DC sources has the feature of switching in series and in parallel. It contains an H-bridge to produce negative levels as well as the positive level. In this paper, this topology is indicated as “A” in the comparison. “B” notation is for the topology described in [19] that has several DC sources connected in series. In this topology, the DC sources have to be symmetric, i.e., $V_{DC1} = V_{DC2} = V_{DC3} = V_{DC4} = \dots = V_{DCn}$. The classical structure that the proposed switching scheme is based on is described in [21]. This topology is indicated as “C” in the comparison. The switches in the mentioned topologies are unidirectional while in [20] the switches are bidirectional. In this topology, each cell consists of one DC source and two bidirectional switch to generate two levels (one positive and the other is negative) and is indicated as “D” in the comparison. NPC-MLI, FC-MLI and CHB topologies are the conventional multilevel inverters that have been discussed in several articles, [7]-[12] and will be denoted as “E”, “F” and “G”, respectively, in the comparison. The comparison of the topologies based on the number of DC sources is shown in Figure 6. The number of the proposed technique is greater than the other topologies by one source only. Unlike the other topologies, the proposed technique does not rely on H-bridge to generate positive and negative levels. This a crucial disadvantage in the other topologies where the power switches in the H-bridge have to withstand high dv/dt stress.

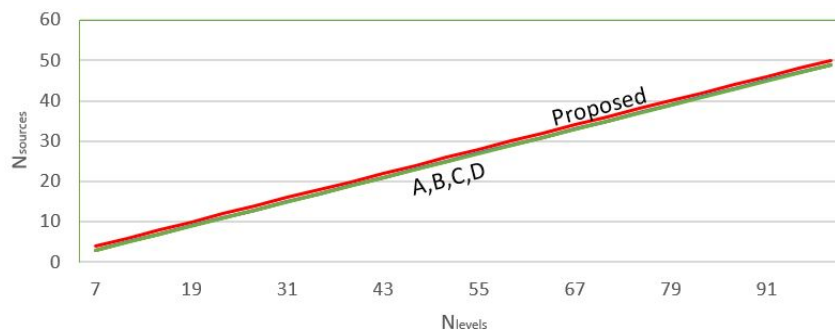


Figure 6. Comparison of $N_{sources}$ versus N_{levels}

Figure 7 shows the comparison based on the number of switching devices. It is obvious that the proposed technique has the lowest number of switches and rating. As mentioned before at “A”, “B”, “D” require high rating power switches to avoid any damages may be caused by high stress dv/dt. Also, “C” uses bidirectional switches which in most of the cases more expensive than the unidirectional switches. Therefore, it would be clear that the proposed technique outperformed the other topologies and modulation techniques.

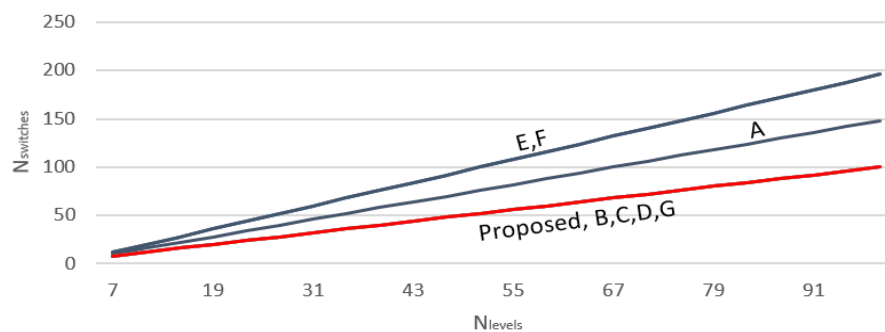


Figure 7. Comparison of $N_{switches}$ versus N_{levels}

4. SIMULATION RESULTS

The studied circuit is simulated using PSCAD/EMDCT, Figure 8. The value of V_{dc} is set to be 1000 V, the modulation index $m = 0.9, 0.6,$ and 0.3 respectively. The load is resistive and the modulation frequency is 2040 Hz. The output waveforms of the 11-level inverter with $m = 0.9, 0.6,$ and 0.3 are shown in Figure 9. The spectrum of the inverter output using the proposed scheme is shown in Figure 10. The values of b_1 in the simulation are 0.64 pu, 0.42 pu, and 0.21 pu. These values are close to the calculated values in Table 2. The difference in the resulted values is caused by applying the optional hybrid modulation in the simulation where it can be noticed that the calculated values are larger. Therefore the amplitude of the inverter output in the simulation is confirmed with the theoretical value. The highest magnitude of harmonics is present in the 34th harmonics. This happened because the switching frequency is 34 times 60 Hz. The THD of the investigated, NPC, and FC inverters are listed in Table 3.

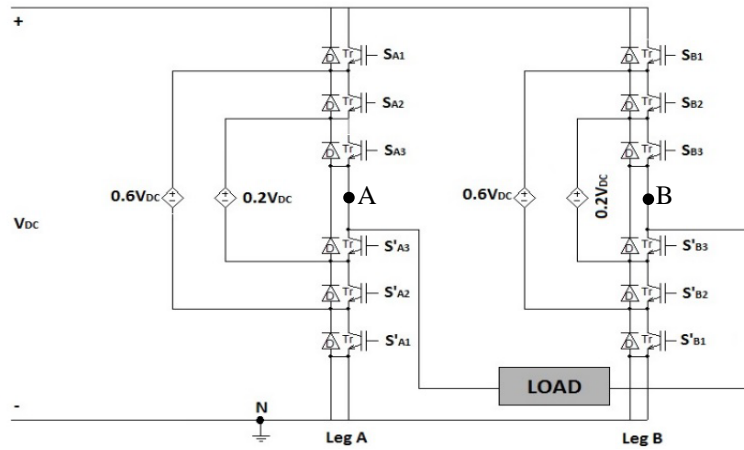


Figure 8. Simulation of the investigated 11-level inverter

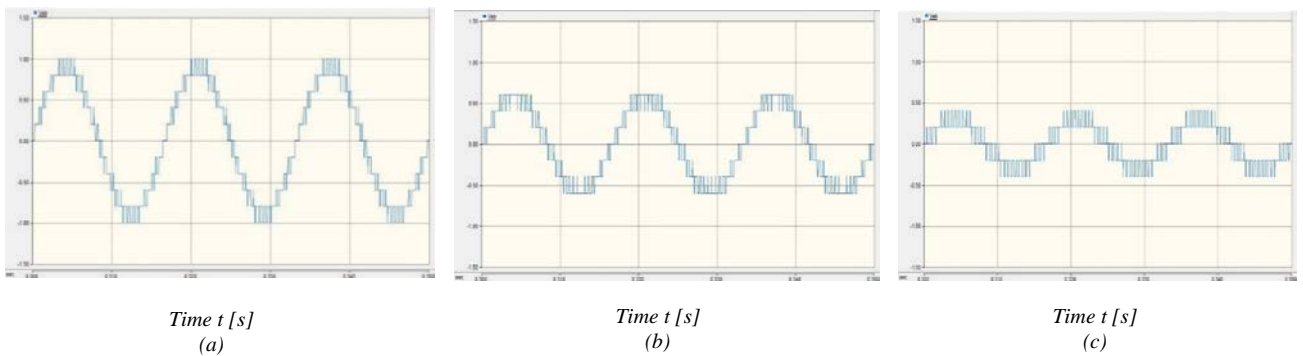


Figure 9. Simulation output of the proposed switching technique. (a) $m = 0.9.$ (b) $m = 0.6$ (c) $m = 0.3$

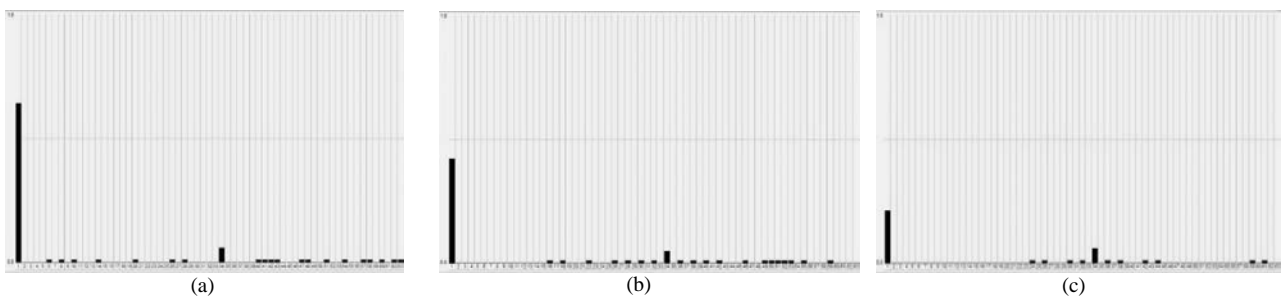


Figure 10. Inverter output spectrum when (a) $m = 0.9.$ (b) $m = 0.6.$ (c) $m = 0.3$

When $m=0.9$, the THD of the studied multilevel inverter is substantially smaller than the other conventional inverters. That is obvious because the inverter output has more levels than that when $m=0.6$ and $m=0.3$. This is expected because at that moment the number of the levels is low just like the conventional inverter. This circuit has disadvantages; it requires four DC sources as a total, two DC sources for each leg.

Table 3. Comparison of the Values of THD

M	THD %		
	Proposed	NPC	FC
0.9	10.9	19	13.9
0.6	14.7	21	19.8
0.3	33.5	35	35.5

5. CONCLUSION

In this paper, a studied modulation scheme that produces more levels in inverters output has been presented. The proposed technique is based on a conventional MLI circuit that uses separate dc voltage sources. The modulation technique may operate using the hybrid method. The mechanism of the switching technique is that all switching devices in the inverter circuit turn on once per cycle while the inner switching devices double up the number of levels and may operate at high frequency. This technique is compared with other recent MLI. The number of dc sources is greater than the other techniques by one while the number of switches is lowest. Besides, the proposed technique has an advantage that it uses low unidirectional switch ratings. This technique has a drawback that it is based on asymmetrical separate dc sources which would be more practical for low- and medium-voltage applications.

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Dr. Bassi worked as a site superintendent to monitor day-to-day construction activities at the working sites, even under high-pressure conditions, while maintaining the required loss prevention regulations. He was continuously updating his technical and managerial knowledge to handle the projects professionally. He worked for project management team (PMT) department at SAUDI ARAMCO to complete projects in instrumentation and power engineering areas until 2005.

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