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Effect of Device Variables on Surface Potential and Threshold Voltagein DG-GNRFET

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Article Info	ABSTRACT
	In this paper we present four simple analytical threshold voltage model for short- channel and length of saturation velocity region (LVSR) effect that takes into account the built – in potential of the source and drain channel junction, the surface potential and the surface electric field effect on double – gate graphene nanoribbon transistors. Four established models for surface potential, lateral electric field, LVSR and threshold voltage are presented. These models are based on the easy analytical solution of the two dimensional potential distribution in the graphene and Poisson equation which can be used to obtain surface potential, lateral electric field, LVSR and threshold voltage. These models give a closed form solution of the surface potential and electrical field distribution as a function of structural parameters and drain bias. Most of analytical outcomes are shown to correlate with outcomes acquired by Matlab simulation and the end model applicability to the published silicon base devices is demonstrated.

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1.   INTRODUCTION

Increasing demand for high speed efficiency in memory and logic applications has created a continuous tendency for smaller device sizes. CMOS technology has shifted to the submicron structure to achieve large density as well as higher efficiency integrated circuits, so the short channel effects can be greater. Among the important factors which determine short-channel effects are the decay of device threshold voltage by using reduced channel length [1]. In order to proceed with this type of scaling factor equality, the channel length regarding silicon MOSFETs as estimated by ITRS will probably need to be scaled to satisfy the needs of next-generation technologies. Nonetheless, there are several question related to the action of silicon devices under excessive scaling. Accordingly, some new material baseddevice has been proposed; for example, nanowire FETs, carbon nanoribbon FET [2-4]. Recent experimental studies have discussed the feasibility of manufacturing graphene nanoribbon transistors [5, 6]. The majority of scientists have become interested in this area and presented various types of GNR transistor features and applications [7-14]. However, there is an absence of research in modelling those features close to the drain junction, which is known breakdown voltage.

Woo et al and Guo and Wu [15, 16] has created short-channel threshold voltage designs by resolving the two-dimensional Poisson equation. Imam et al [17] designed the threshold voltage by formalizing the two dimensional Poisson formula as a pair of the one dimensional (1D) Poisson formula and two dimensional Laplace formula. For the threshold voltage an exponential function of L was estimated. Lately, Banna [18], applied the quasi two dimensional method and stated that the threshold voltage model

gave a quite similar dependence on L to thatstated by Imam et al. [17]. In this paper, an easy analytical method for threshold voltage with the short – channel, completely depleted DG-GNRFET can be explained. In addition, an analytical solution is based on the 2D potential distributions in the graphene film. Suitable boundary conditions can be set for uniform doping in the graphene film. Accordingly, this study presents an uncomplicated design for the surface potential and electrical field distribution of double - gate graphene nanoribbon field effect transistor. During the following section, the surface potential as well as the threshold voltage for short channel of GNR will be defined first. To be able to simplify the analysis, we do not assume interface charges. In addition, carrier accumulation or inversion has been ignored in the graphene film buried oxide. Moreover, we want to explain the behaviour of DG-GNRFET close to the drain junction as well as the breakdown voltage in comparison with the silicon base transistor.

2. RESEARCH METHOD

The Proposed Model for LVSR (Surface Potential) and the Short –Channel Solution

The velocity-saturation-region length of FETs as well as the width of the drain region in which carrier velocity saturation and impact ionization takes place can be more significant variables for short – channel devices in nanoscale transistors. The LVSR controls the hot-electron generation, substrate current, the drain breakdown voltage and drain current in the drain region [19-24]. At the FET, when the used drain voltage is greater than the saturation drain voltage, the electric field close to the drain region isgreater than the critical field power which leads to carrier velocity saturation [25]. A standard schematic cross-section from double gate GNRFET is demonstrated in figure 1. Where the oxide thickness of the front and back gates is mentioned by t_{OX} with a dielectric constant of ε_{OX}. The L, W, t_G and ε_G are the length, width, thickness and dielectric constant of the GNR respectively. In general, for analyzing the potential distribution in the graphene, it is necessary to solve the Poisson equation first: [26]
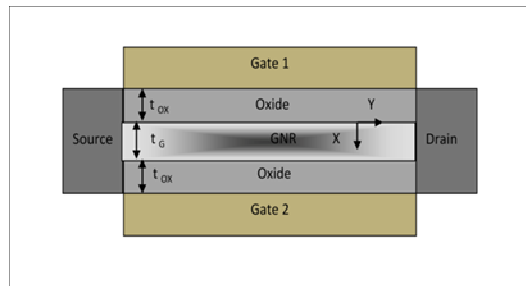

Figure 1. Schematic cross section of a Double Gate GNR FET

$$\nabla^2 \Psi(x,y) = \frac{-qN_d}{\varepsilon_G}, \qquad 0 \leq x \leq t_G , 0 \leq y \leq L \tag{1}$$

Where $\Psi(x, y)$ must be the potential anywhere of (x, y) throughout the GNR, the electric charge amount is q, the doping concentration of GNR is N_d. In fact, the built- in potential in GNR with a bandgap is not zero. However, in this work, we have included the built-in potential of the source and drain channel junction, for Eq. (1), whereby it is necessary to determine the boundary conditions as, $\Psi(0,0) = V_{bi}$ and $\Psi(0,,L) = V_{DS} + V_{bi}$, the built-in potential and the source-drain voltage are represented by V_{bi} and V_{DS} respectively. Since the electric flux across the top, down GNR and oxide boundary can be constant, the potential function has to satisfy [27].

$$\frac{\partial \Psi(x,y)}{\partial x}\Big|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{\Psi(0,y) - V_{g1}}{t_{OX}} \tag{2}$$

and

$$\frac{\partial \Psi(x,y)}{\partial x}\Big|_{x=t_G} = \frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{V_{g2} - \Psi(t_G,y)}{t_{OX}} \tag{3}$$

Where $V_{g1} = V_{GS1} - V_{FB1}, V_{g2} = V_{GS2} - V_{FB2}$, V_{GS1} is the gate-source for front and V_{GS2} is the gate-source for back flat band voltage. The flat band voltage is V_{FB} for the GNR by using a bandgap $E_G = \frac{hV_F}{3w_G}$[28]. $V_{FB} = \frac{hV_F}{6qw_G} - V_T \ln(N_d/n_i)$, whereverthe Fermi velocity of the graphene is $V_F \sim 10^6$ m/s. By following the same method analysis as in Refs, [26, 29] to solve Eq. (1), we can decompose $\Psi(x, y)$ into two parts, such that

$$\Psi(x, y) = V(x) + U(x, y) \tag{4}$$

V (x)can be the one dimension solution from the Poisson equation:

$$\frac{\partial^2 V(x)}{\partial x^2} = \frac{-qN_d}{\varepsilon_G} \tag{5}$$

Eq. (5) is usually used for the long – channel effects. The easiest solution that computes for two dimensional short channel effects is U(x, y) for determining V(x) as provided by Eq. (4), U(x, y) which must fulfil the Laplace equation:

$$\frac{\partial^2 U(x, y)}{\partial x^2} + \frac{\partial^2 U(x, y)}{\partial y^2} = 0 \tag{6}$$

In Eq. (4), the boundary conditions of $\Psi(x, y)$ can also be divided into two parts suitable for the solution of Eq. (5) and (6). However, by breaking up Eq. (2) and (3) the boundary conditions are usually displayed as follows:

$$\frac{\partial V(x)}{\partial x}\Big|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{V(0) - V_{g1}}{t_{OX}} \tag{7}$$

and

$$\frac{\partial V(x)}{\partial x}\Big|_{x=t_G} = \frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{V_{g2} - V(t_G)}{t_{OX}} \tag{8}$$

where before V_{g1} and V_{g2}, was expressed, it can also be stated V (0) = V_{S1}, which is a front surface potential obtained by resolving Eq. (5), using boundary conditions in Eq. (7), and Eq. (8), and where the device factors can be displayed along with bias conditions like:[27]

$$V_{S1} = \frac{C_G}{2C_G + C_{OX}}\left[V_{g2} + V_{g1}\left(\frac{C_{OX}}{C_G} + 1\right) + qN_d t_G\left(\frac{1}{C_G} + \frac{1}{C_{OX}}\right)\right] \tag{9}$$

We can apply the zero gate bias condition, $V_{GS1} = V_{GS2} = 0$, so from, Eq. (9) we can write

$$V_{S1} = \frac{qN_d(t_G C_{OX} + \varepsilon_G)}{C_{OX}(2C_G + C_{OX})} \tag{10}$$

On the other hand, if the device is at gate bias conditions by using $V_{g1} = V_{GS1} - V_{FB1}$ from Eq. (9), it can be stated that:

$$V_{GS1} = V_{FB1} + \frac{C_G}{C_G + C_{OX}}\left[V_{S1}\left(2 + \frac{C_{OX}}{C_G}\right) - V_{g2} - qN_d\left(\frac{t_G C_{OX} + \varepsilon_G}{C_{OX}C_G}\right)\right] \tag{11}$$

In Eq. (6) the boundary conditionscan be stated as; U(0, 0) = $V_{bi} - V_{S1}$ andU(0, L) = $V_{bi} + V_{DS} - V_{S1}$

$$\frac{\partial U(x, y)}{\partial x}\Big|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{U(0, y)}{t_{OX}} \tag{12}$$

And

$$\frac{\partial U(x,y)}{\partial x}\Big|_{x=t_G} = -\frac{\varepsilon_{ox}}{\varepsilon_G} \times \frac{U(t_G,y)}{t_{ox}} \tag{13}$$

with the previous boundary conditions, the results for Eq. (6) can be found from the technique for the differentiation of parameters. The solution obtained at x = 0 can be expressed using the series [29]

$$U(0,y) = \sum_{n=1}^{\infty} A_n \exp(\lambda_n y) + B_n \exp(-\lambda_n y) \tag{14}$$

where

$$A_n = \frac{(V_{bi} + V_{DS} - V_{S1})\exp(-\lambda_n L) + (V_{bi} - V_{S1})\exp(-2\lambda_n L)}{1 - \exp(-2\lambda_n L)} \tag{15}$$

$$B_n = (V_{bi} - V_{S1}) - A_n \tag{16}$$

In addition,λ_n is a parameter that depends on technology, which it can be described as being the solution to the equation:

$$t_G \lambda_n = \left(\frac{C_G}{2C_{OX}}\right)\left[(t_G\lambda_n)^2 - \left(\frac{C_{OX}}{C_G}\right)^2\right] tan(t_G\lambda_n) \tag{17}$$

The value of t_G is small (around 10^{-9}), so we can approximate tan $(t_G\lambda_n)$ to$t_G\lambda_n$. According to[27], $\lambda_n$is

$$\lambda_n = \frac{1}{t_G}\sqrt{1 + \frac{2C_{OX}}{C_G}} \tag{18}$$

We can approach $\Psi(0, y)$ the surface potential distribution of the just initial term n=1 from the series in Eq. (14). The main reason is that the results which can be significant for designing the threshold voltage produced from the surface potential are lowest when they happen to behappens close to the centre in the channel ($y_{min} \cong L/2$) [26].

$$U(0,y) = (V_{bi} + V_{DS} - V_{S1})\frac{\sinh(\lambda y)}{\sinh(\lambda L)} + (V_{bi} - V_{S1})\frac{\sinh[\lambda(L-y)]}{\sinh(\lambda L)} \tag{19}$$

Accordingly, for the short channel, the surface potential can be described as

$$\Psi(0,y) = V_{S1} + (V_{bi} + V_{DS} - V_{S1})\frac{\sinh(\lambda y)}{\sinh(\lambda L)} + (V_{bi} - V_{S1})\frac{\sinh[\lambda(L-y)]}{\sinh(\lambda L)} \tag{20}$$

with a minimum given by

$$\Psi_{min} = V_{S1} + \sqrt{\propto_1 \propto_2}\exp\left(-\frac{\lambda L}{2}\right) \tag{21}$$

We can determine $\propto_1$, $\propto_2$, and the value of V_{GS1} as the short − channel threshold voltage. With the lowest surface potentials Ψ_{min} equals $2\emptyset_F$as argued in [26]. Therefore, Eq. (21) can be indicated as:

$$V_{S1} = 2\emptyset_F - \sqrt{\propto_1 \propto_2}\exp\left(-\frac{\lambda L}{2}\right) \tag{22}$$

The value of V_{GS1} extracted from Eq. (22), by means of V_{S1} describes the threshold voltage in the short-channel graphene device.

$$V_{GS1} = \emptyset_{FB1} + \frac{C_G}{C_G + C_{OX}}\left[\left(2\emptyset_F - \sqrt{\alpha_1\alpha_2}exp\left(-\frac{\lambda L}{2}\right)\right)\left(2 + \frac{C_{OX}}{C_G}\right) - V_{g2} - qN_d\left(\frac{t_G C_{OX} + \varepsilon_G}{C_{OX}C_G}\right)\right] \quad (23)$$

The particular lateral electrical field across the semiconductor surface can be acquired from differentiating Eq. (20).

$$E_y(0,y) = -\frac{\partial\Psi(0,y)}{\partial y} = -\frac{\lambda(V_{bi}+V_{DS}-V_{S1})\cosh(\lambda y) - \lambda(V_{bi}-V_{S1})\cosh[\lambda(L-y)]}{\sinh(\lambda L)} \quad (24)$$

We take the 1st term (n = 1) from the series of Eq. (14), as a surface potential distribution U(0, y)[23]. According to [27] from Eq. (14) can be obtained Eq. (25).

$$U(0,y) = (V_{bi} + V_{DS} - V_{S1})e^{\lambda(y-L)} + (V_{bi} - V_{S1})e^{-\lambda y} \quad (25)$$

In Eq. (4), the surface potential along y can be displayed as

$$\Psi(0,y) = V_{S1} + (V_{bi} + V_{DS} - V_{S1})e^{\lambda(y-L)} + (V_{bi} - V_{S1})\,e^{-\lambda y} \quad (26)$$

Moreover, the lateral electrical field across the channel can be easily obtained by the derivation of Eq. (26), over y.

$$E\,(0,y) = -\lambda\left[(V_{bi} + V_{DS} - V_{S1})e^{\lambda(y-L)} + (V_{bi} - V_{S1})\,e^{-\lambda y}\right] \quad (27)$$

Additionally, by taking y = L$-L_D$, $\Psi(0,y) = V_{sat}$. Therefore, for L_D we can state that

$$L_D = L - \frac{1}{\lambda}\ln\left(\frac{\frac{(V_{bi}+V_{DS}-V_{S1})}{e^{\lambda y}}e^{2\lambda(L-L_D)}-V_{S1}}{V_{sat}-V_{S1}}\right) \quad (28)$$

which can be solved numerically. In Eq. (28), V_{sat} is drain saturation voltage and L_D is the length of the saturation velocity region. The relationship between the surface potential, electrical field and the length of saturation region with t_{OX}, t_G , V_{DS} and L is shown in the proposed equations.

3.   RESULTS AND DISCUSSION

In the following section, by using the above procedure, the threshold voltage can be computed in devices of 20 nm length and several t_{OX} thicknesses. In figure2, the design estimated threshold voltage has been displayed as the function of the channel length and can also be compared with silicon base devices, in ref [30]. Figure 2, shows the surface potential across the channel length in a threshold situation extracted from Eq. (17), as well as Eq. (20) plotted. The proximity between the source and drain in the short channel devices caused the surface potential to vary from V_{S1}. In ref [26] the estimation of the tangent function in $tan(t_G\lambda_n)$ by $t_G\lambda_n$ is based on very thin silicon films. In addition, this estimation was applied because the GNR thickness is very thin if our figureis compared with the threshold voltage in ref [31]. The simulation model used matches all the presumptions in the analysis. Quantum effects do not take into account effects when they begin to play a very important role in GNR thinner than 5nm. In figure3, the behavior for the threshold voltage versus channel length L with different t_{OX} thickness is shown. During this part, the profile of this surface electrical field as well as the potential change displayed and the results of various variables (for instance, drain-source voltage, oxide thickness, channel length and doping concentration on the length of saturation region) can be analyzed near to the drain region. The proposed model can be confirmed by comparing the computed values with the suggested sample, as well as simulations for a Si based device, in ref [30].
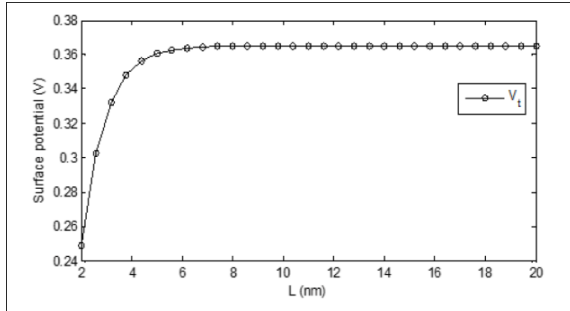
Figure 2. Threshold voltage along the channel length and represents data from the Matlab simulation with L=20 nm from Eq. (17) and Eq. (20)
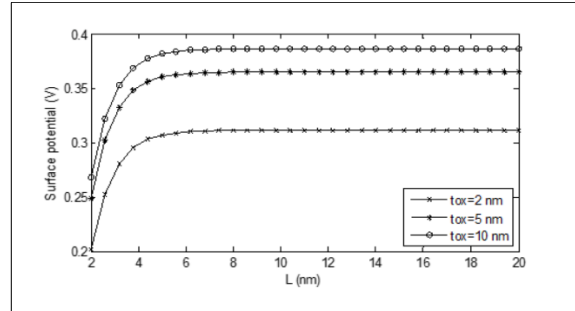
Figure 3. Threshold voltage versus channel length L for different t_{OX} thickness of the DG - GNRFET model and represents data from the Matlab simulation with L=20 nm from Eq. (17) and Eq. (20)

A fine settlement can be obtained among simulation outcomes plus the sample with various doping concentrations and oxide thicknesses along with the interval of the drain.The surface potential for $\Psi(0, y) = V_{sat}$. Figure 4, shows the variance of surface potential across the channel with a variety of drain biases. It can be observed, that as the drain bias is increased the surface potential around the drain side increases if it continues to be constant in the source area, which shows the reliability of our supposed boundary conditions. Figure 5, indicates the change of surface potential across the nanoribbon channel for various oxide thickness with drain bias, V_{ds}=1.5 V and channel length L=15 and N_d=1 × 10^{15}cm^{-3}. It can be demonstrated thatwhen the oxide thickness decreases the lowest potential close to the source side increases; however, the opposite phenomenon occurs close to the drain due to the fact that the oxide thickness decreases oxide capacitance increases. This boosts the surface charge and the surface potential for the corrected bias conditions. Hence, on the drain side by reducing of the oxide thickness, the oxide capacitance rises together with the off-state current which increases. As a result of this, the potential in the drain side is reduced. From figure6, it can be shown that as the channel lengths are reduced from L=20 nm to L=15 nm, the surface potential is similar to figure4 for V_{ds} = 1.5 V at each side of the device. However, the lowest potential moves in an upward direction as channel lengths are diminished. This takes place because of the extension of the depletion region below the gate at the surface. Figure 7, shows a strong correlation among the simulation outcomes and samples used in various doping concentrations, with t_{OX}= 5 nm and distances from the drain in double gate GNRFET. When the surface potential model was confirmed the particular LVSR model was also proven to be efficient since it is an ideal method of the surface potential $\Psi(0, y) = V_{S1}$, [27]. Furthermore, the surface potential differs in the location of the channel for various peak doping concentrations. It can be stated that when efficient carrier concentration across the channel increases, the surface potential rises. The exact outcomes are as displayed for V_{ds}=1.5 V. Figure 8, shows the field distribution over the nanoribbon surface to the various field oxide layer thicknesses. As explained before,figure5,shows the potential distribution across the channel length for the various field oxide thicknesses. As a result, there is similar effect of the front interface oxide layer thicknesses on the field as well as potential distribution to the silicon based devices. As shown in figure 8, the opposite phenomenon was observed, because the highest field usually occurs in the p^+n^-junction interface in which the avalanche breakdown takes place. The field oxide layer thickness effects the breakdown voltage. If it is thick enough tocausea breakdown voltage when the voltage becomes weaker [32].

Figure 9, exhibit the analytical outcomes of the results of the electric field distribution extracted from Eq. (24) for nanoribbon transistors with various doping concentrations N_d. A reasonable evaluation amongst the analytical and numerical final outcomes might usually be discovered. The differences between the two could be as a result of the influence from the space charge region into the p^+ Base region and n^+ Drain diffusion region, which is visible from the field at x=0 and x=L. Figure 9, shows that the electrical field distribution across the GNR surface for the various doping, compared to the silicon film surface with various doping. It can be clearly shown that there exists two electrical field peaks across the silicon surface, one happens in the p^+n^- junction interface and next on the n^+n^- junction interface. Close to the drain region demonstrate exactly the same behaviorin theSi based device. As can be seen, the magnitude of the electric field decreases with as the N_d increases [32]. The substrate doping concentration isthe main factor in the optimization of the GNR transistor and defines the amplitude and the position of the maximum peak electric field.
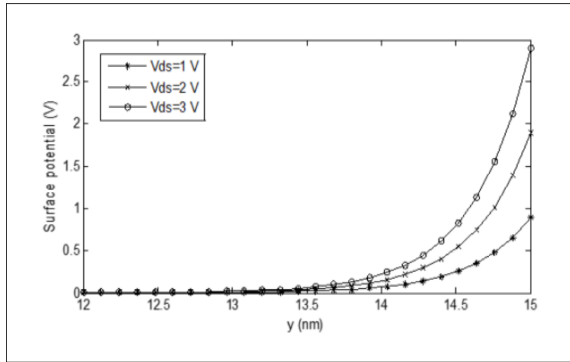
Figure 3. Surface potential versus channel length curves with various drain biases, L=15nm and oxide thickness t_{OX}=10 nm

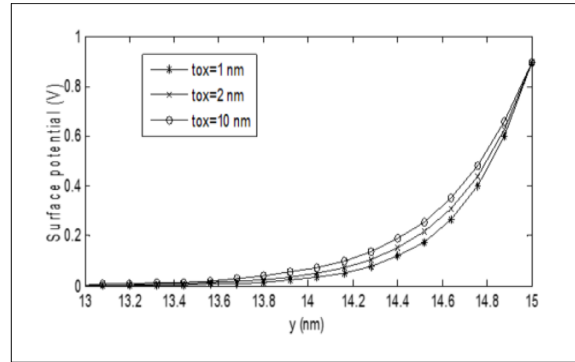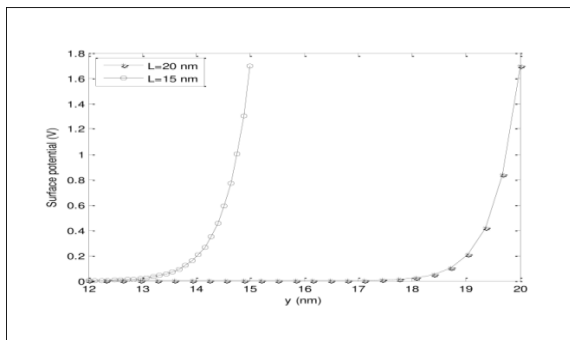Figure 4. Surface potential curves across the channel with various oxide thicknesses, L=15 nm and V_{ds} =1.5 V

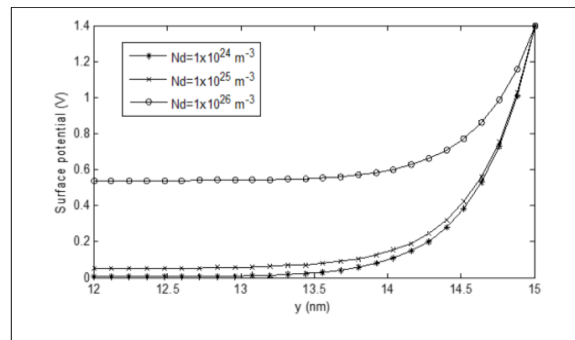Figure 5. Surface potential curves across the channel with various channel lengths, t_{OX}=5 nm, V_{ds}=1.5 V

Figure 6. Surface potential curves across the channel with various profile doping concentrations, L = 15 nm and Vds=1.5 V
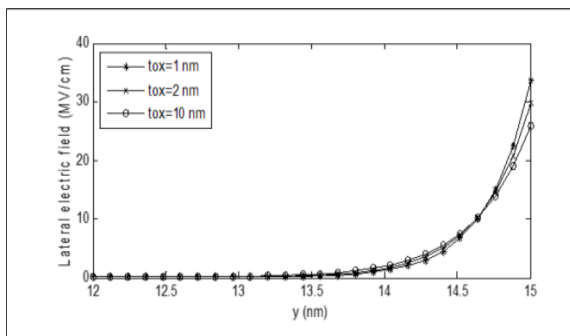

Figure 7. Electrical field distributions across the lateral direction for nanoribbon with various front interface oxide layer thicknesses
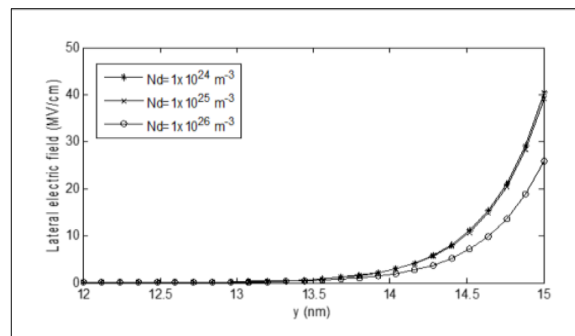

Figure 8. Electrical field distribution across the nanoribbon surface with various doping N_d

4. CONCLUSION

From this work, an uncomplicated analytical approach has been found to obtain samples of the threshold voltage for short channel double gate nanoribbon FET which induced the surface potential effects that are usually described and accounted for in our model. Generally, there are analytical models to find the surface potential and electrical field along with LVSR from DG-GNR transistors for the saturation region which was investigated using the recommended model. Additionally, by using the introduced models, the consequences of device variables; for instance nanoribbon thickness, doping concentration and channel

length was analyzed and compared to the silicon based devices and was proven to beclose to them. As expected, as a result of small-scale geometry for the product, the large lateral electrical field was discovered to be close to the drain junction, becoming a point of trust and reliability of such devices. In addition, the connection among the critical doping concentration around the drift region along with the thickness was described. Most of the analytical outcomes were being shown correlate with the outcomes acquired by Matlab simulation. To increase the breakdown properties for devices, however getting perfect surface field distribution and the critical doping concentration has significant value [32].

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