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High Speed and Low Pedestal Error Bootstrapped CMOS Sample and Hold Circuit

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Abstract

A new high speed, low pedestal error bootstrapped CMOS sample and hold (S/H) circuit is proposed for high speed analog-to-digital converter (ADC). The proposed circuit is made up of CMOS transmission gate (TG) switch and two new bootstrap circuits for each transistor in TG switch. Both TG switch and bootstrap circuits are used to decrease channel charge injection and on-resistance input signal dependency. In result, distortion can be reduced. The decrease of channel charge injection input signal dependency also makes the minimizing of pedestal error by adjusting the width of NMOS and PMOS of TG switch possible. The performance of the proposed circuit was evaluated using HSPICE 0.18-μm CMOS process. For 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock, the proposed circuit achieves 2.75 mV maximum pedestal error, 0.542 mW power consumption, 90.87 dB SNR, 73.50 SINAD which is equal to 11.92 bits ENOB, -73.58 dB THD, and 73.95 dB SFDR.

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1. INTRODUCTION

Analog techniques have dominated signal processing for years, but digital techniques are slowly encroaching into this domain. Digital signal processing (DSP) is becoming popular because its flexibility to perform various processing operations. This technology is widely used in many different domains, such as wireless communications, medical electronics, measurement instrumentation, digital multimedia, etc. One of the essential component of DSP is analog to digital converter (ADC), because most natural signals in the world (such as voltage, current, temperature and pressure) are analog. ADC perform the digitalization of analog signals at fixed time period, which is generally specified by the application. Since the digital signal that will be processed by DSP is originally from ADC, performance of the DSP is highly dependent to the performance of ADC itself. To avoid premature signal degradation, the ADC must achieve specified sampling speed, resolution and precision. To meet the specifications, several techniques and ADC architectures have been proposed. Parallel (flash) ADC is by far the fastest and conceptually simplest has been reported [1]. The drawbacks of this architecture are the resolution is limited by circuit complexity, high power dissipation, and comparator and reference mismatch. To reduce hardware complexity, power dissipation and die area, and to increase the resolution but to maintain high conversion rates, flash converters can be extended to pipeline [2], delta-sigma ADC [3, 4], or successive approximation ADC [5].

The key building block in front-end of ADC is Sample and Hold circuit (S/H). This front-end circuit is almost inevitable in some types of ADC. The main function of S/H is to take analog input signal samples and hold its value until ADC can process the information. In other word, the accuracy and the speed of the

converter is strongly dependent on performance of S/H, because this circuit provide the information which will be processed by the converter. The architectures of S/H can roughly be divided into two, open-loop and closed-loop architectures. The main difference between them is that in closed-loop architectures, the hold capacitor is placed in a feedback loop, at least in hold mode, whereas the open-loop one has no feedback. Moreover, the characteristics between these two architectures are mostly different. The open-loop architecture offer the simplicity and speed solution, however its accuracy is limited by distortion arising from nonlinearity of the switch which is caused by its signal dependent on-resistance and pedestal error which is caused by the signal dependent channel charge injection and clock feedthrough. On the other hand, enclosing the capacitor in the feedback loop on the close-loop architecture can reduces the effect of nonlinearity and signal-dependent charge injection and clock feedthrough from the MOS switches, offering better accuracy as a result. Unfortunately, an inevitable consequence of the use of feedback is conditionally stability problem. Furthermore, since close-loop architecture uses Op-Amp, its bandwidth and slew rate directly limit the speed of the S/H. The complexity and power consumption of the Op-Amp also rise another problem.

In order to maintain the simplicity and the speed, and to increase the accuracy of S/H, in this paper a new open-loop CMOS S/H is proposed. The proposed circuit consists of new bootstrap circuit to overcome channel charge injection and clock feedthrough signal dependent problem, and transmission gate (TG) switch to deal with on-resistance problem. In this paper, a simple theoretical and numerical method to minimize the pedestal error is also presented. The rest of this paper is organized as follows. Section 2 explain the operation of S/H, especially open-loop S/H. In this section, channel charge injection and clock feedthrough mechanism will be reanalyzed in detail. Several previous existing techniques related to open-loop S/H will also be presented in this section. Section 3 presents the proposed circuit and its theoretical analysis. Section 4 presents the simulation result of proposed circuit and the comparison with other works. At last, the conclusion is presented in section 5.

2. OPEN-LOOP SAMPLE AND HOLD CIRCUIT

Simple open-loop S/H circuit consists of two main part, first part is analog switch and second one is hold capacitor. The analog switch is used to control the connection between signal-source (input) node and data-holding (output) node, whereas the hold capacitor is used to hold the data in output node. The operation of S/H circuit takes place in two phases: sampling and hold. When the clock voltage (ϕ) which is applied to the gate of transistor is high, transistor is on. Channel is appearing underneath the gate and connecting drain and source of the transistor. In this phase, input node and output node is connected and sampling function is performed. After the switch is turned off, the data appearing in the holding (output) node will be held until the next operation step occurs, this phase is called hold phase. In the transition phase between sampling and hold, the channel charge disappears through either the source/drain electrodes or substrate electrodes. Charge which disappears through source/drain is deposited on hold capacitor creating an error component to the sample voltage. This phenomenon is called channel charge injection. In an MOS transistor it is also known that it has parasitic capacitance that is formed by overlapping between gate and diffusion (source and drain). When transistor turns off, this overlap capacitance also flows the charge to hold capacitor creating another error component to sample voltage. This phenomenon is called clock feed through. These two mechanisms are the main sources that create an error in sample voltage. Some researches have been done and published regarding these two mechanisms[6, 7].

2.1. Channel Charge Injection, Clock Feedthrough and On-Resistance Problem

In the sampling phase, transistor is on and a channel exists at the oxide-silicon interface. This phase can be depicted in Figure. 1. (a). Assuming V_{in} = V_{out}, the total charge in the inversion layer (channel) can be obtained as

$$Q_{ch} = -WLC_{ox}(\phi_h - V_{in} - V_t) \tag{1}$$

$$Q_{ch} = -WLC_{ox}(V_{dd} - V_{in} - V_t) \tag{2}$$

where W is channel width, L is channel length, C_{ox} is oxide capacitance per unit area, ϕ_h is the high level of clock voltage, and V_t is threshold voltage of the transistor. In many application the high level of clock voltage is equal to supply voltage (ϕ_h = V_{dd}). Thus, the equation (1) can be rewritten as (2).

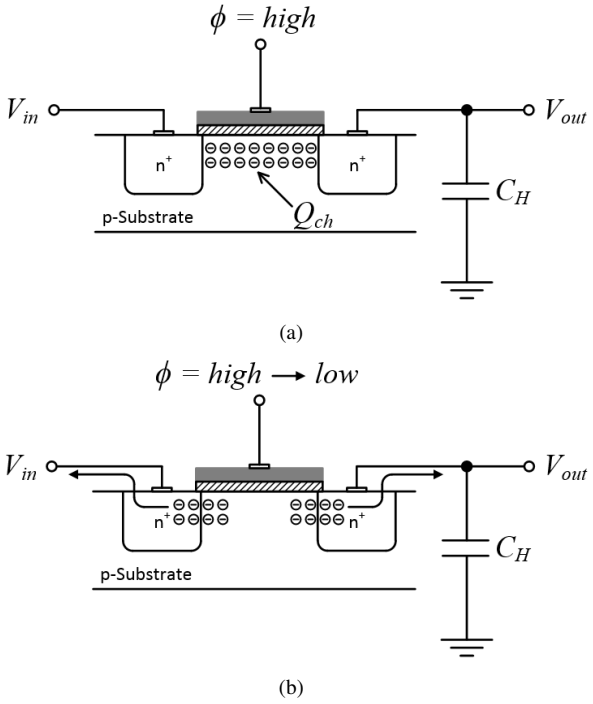


Figure 1. S/H phases: (a) Sampling phase of S/H circuit, (b) On-off transition phase of S/H circuit

When the switch turns off (S/H circuit enter hold phase), Q_{ch} exits through the source and drain terminals like shown in Figure. 1. (b). The charge injected to left side of Figure. 1. (b) is absorbed by the input source, creating no error. Whereas, the charge injected to the right side is deposited on C_H, creating an error in the output node. Assuming that the amount of charge which flow to the left side equal to the one which flow to the right side, it is obtained that the amount of charge causes error in the output node is $Q_{ch}/2$. Therefore, the error voltage caused by channel charge injection then can be written as follow

$$\Delta V_{cci} = -\frac{WLC_{ox}(V_{dd} - V_{in} - V_t)}{2C_H} \tag{3}$$

On the turning off process, the MOS switch also couples the clock transition to the hold capacitor (C_H) through this overlap capacitance (gate-drain or gate-source overlap capacitance). The coupling current that flow from gate to drain/source through overlap capacitance causes an error in the output node. The error voltage caused by clock feedthrough can be written as follow

$$\Delta V_{cft} = -\frac{L_{ov}WC_{ox}}{L_{ov}WC_{ox} + C_H}\phi_h \tag{4}$$

Where L_{ov} is gate-drain or gate-source overlap length. These errors are the main source of accuracy problem in open-loop S/H. Error caused by channel charge injection is more dominant compared with error caused by clock feedthrough, because the length of overlap capacitance in eq. (4) is very small. In some cases, this error is often neglected. The other problem that limit the accuracy of open-loop S/H is nonlinearity. This nonlinearity is caused by signal dependent on-resistance shown in eq. (5). Where μ is mobility of the electron. From the equation, it also can be inferred that the switch has narrow input swing. because as the input signal equal to $V_{dd} - V_t$, the on-resistance become infinity.

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{dd} - V_{in} - V_t)} \tag{5}$$

2.2. Open-Loop S/H Circuit Using TG Switch

The simple way to decrease the error and nonlinearity caused by channel charge injection, clock feedthrough and non-uniform on-resistance of the switch is by using TG switch. Figure 2 shows schematic of basic S/H circuit using CMOS switch. The switch part of this circuit consist of two MOS transistors, N type MOS transistor and P type MOS transistor (TG switch). By using TG switch, the problem of narrow input voltage swing and non-uniform on-resistance can be solved. Input range of this switch is nearly 0 V - V_{dd}, on-resistance of this switch is also relatively uniform compared with single transistor switch. On-resistance of TG switch is written in eq. (6).

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)(V_{dd} - V_{in} - V_{tn}) + \mu_p C_{ox}\left(\frac{W_p}{L_p}\right)(V_{in} - |V_{tp}|)} \tag{6}$$

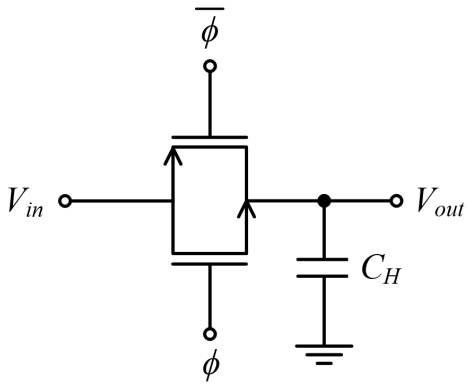


Figure 2. S/H circuit using TG switch

Since the TG switch is built using two type MOS transistors, the error in this switch is also caused by those two transistor. And as well-known that the characteristic of N type and P type MOS transistor are mutually opposite. Thus, the error of NMOS and PMOS are mutually compensate. The total error in this S/H circuit is written in eq. (7).

$$\begin{aligned}\Delta V = \frac{1}{2C_H} C_{ox}[W_p L_p(V_{in} - |V_{tp}|) - W_n L_n(V_{dd} - V_{in} - V_{tn})] \\ + \frac{L_{ovp}W_p - L_{ovn}W_n}{L_{ovn}W_n C_{ox} + L_{ovp}W_p C_{ox} + C_H} C_{ox}\phi_h\end{aligned} \tag{7}$$

Where subscript *n* and *p* refer to N type and P type MOS transistor, respectively. The equations used for modeling hold error in this paper is basic model, neglecting body effect and gate/clock voltage falling rate. The first term in this equation is the error caused by channel charge injection. This term is dominant term. The second term is error caused by clock feedthrough. This term is less dominant and can be neglected in some application with less accuracy consideration.

Theoretically, the performance of open-loop S/H circuit using TG switch is better than the other one with single MOS transistor. However, in the high speed and high accuracy application, the use of open-loop S/H circuit with TG switch is not recommended. Because the effect of channel charge injection, clock feedthrough and on-resistance signal dependent is still very significant to accuracy degradation. To overcome this problem, many researchers develop and propose new techniques. The use of dummy transistor to eliminate the effect of channel charge injection and clock feedthrough has been reported. However, the performance of dummy transistor is limited by the transistor mismatch and unbalance impedance at drain and source terminal of the switch. The other technique is bottom plate sampling. Recently, the improvement of bottom plate sampling is reported in [8, 9]. This technique shows decent performance to decrease charge injection and clock feedthrough effect, but the complex clocking phase in this technique rises another problem in system complexity. Several other techniques also have been reported, such as the use of current conveyor as analog switch, current controlled

current mirror switching, distributed S/H, substrate-biasing-effect attenuated T switch [10], cross couple switch capacitor network, offset cancellation replica circuit [11], bootstrapping techniques [12], and other techniques [13, 14, 15, 16]. For open-loop S/H circuit the bootstrapping technique is a suitable one, this technique keeps the gate-source voltage of sampling transistor fix at particular value. This approach keeps the on-resistance constant and thus improve the switch linearity. By keeping the gate-source voltage fix, it also decreases the channel charge injection and clock feedthrough signal dependent.

3. PROPOSED S/H CIRCUIT

To solve the problems presented in section 2., a new bootstrapped S/H circuit with TG switch is proposed. As depicted in Figure. 3, unlike the common bootstrap circuit [12], the proposed circuit is made up of CMOS TG switch and novel bootstrap circuit structure for each transistor in TG switch (NMOS bootstrap circuit and PMOS bootstrap circuit). The proposed circuit is operated in differential mode, but for simplicity, Figure. 3 shows only single input mode circuit. CMOS TG switch is formed by M_{s1} and M_{s2}, while C_1, M_{1-5} and C_2, M_{6-10} form NMOS and PMOS bootstrap circuits, respectively.

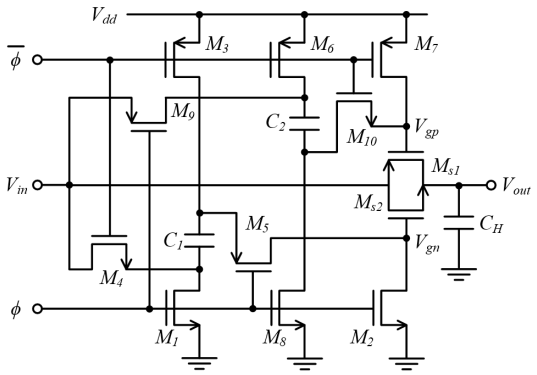


Figure 3. Proposed S/H circuit

These circuits are controlled by ϕ and $\bar{\phi}$ which are non-overlapping clocks with opposite phases. The operation principles of the proposed circuit is explained as follows. When ϕ is high, ($\phi = 1$, $\bar{\phi} = 0$), in NMOS bootstrap circuit, M_{1-3} are on and M_{4-5} are off, cause V_{dd} is applied at top plate of capacitor C_1, and since M_2 is on, the output of this circuit which is connected to the gate of NMOS in TG switch is connected to ground ($V_{gn} = 0$). While in PMOS bootstrap circuit, M_{6-8} are on and M_{9-10} are off. Thus, V_{dd} is applied at top plate of capacitor C_2, and since M_7 is on, the output of this circuit which is connected to the gate of PMOS in TG switch is connected to V_{dd} ($V_{gp} = V_{dd}$). In this phase, the circuit is in hold phase as depicted in Figure. 4.

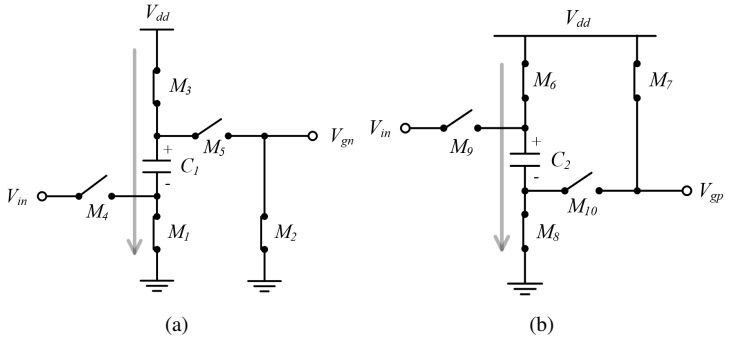


Figure 4. Hold phase in bootstrap circuit: (a) NMOS bootstrap, (b) PMOS bootstrap

When ϕ is low, ($\phi = 0$, $\bar{\phi} = 1$), in NMOS bootstrap circuit, M_{1-3} are off and M_{4-5} are on, cause the bottom plate of capacitor C_1 connects to V_{in} and its top plate connects to V_{gn}. Thus, the output of this circuit, V_{gn} equal to $V_{in} + V_{dd}$. While in PMOS bootstrap circuit, M_{6-8} are off and M_{9-10} are on, cause the top plate of capacitor C_2 connects to V_{in} and its bottom plate connects to V_{gp}. Therefore, the output of the circuit, V_{gp} equal to $V_{in} - V_{dd}$. In this phase, the circuit is in sampling phase as depicted in Figure. 5. Based on the operation principles explanation, the output of NMOS and PMOS bootstrap circuits can be written in Eqs. (8) and (9), respectively.

$$V_{gn} = \begin{cases} V_{in} + V_{dd}, & \text{in sampling phase} \\ 0, & \text{in hold phase} \end{cases} \tag{8}$$

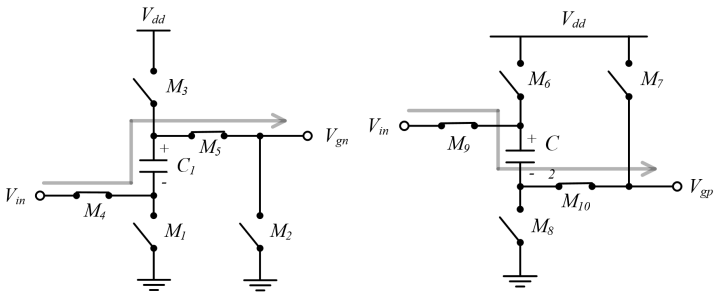


Figure 5. Sampling phase in bootstrap circuit: (a) NMOS bootstrap, (b) PMOS bootstrap

$$V_{gp} = \begin{cases} V_{in} - V_{dd}, & \text{in sampling phase} \\ V_{dd}, & \text{in hold phase} \end{cases} \tag{9}$$

By using Eqs. (8) and (9), the on-resistance and the total error of the proposed circuit can be written in Eqs. (10) and (11), respectively.

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W_n}{L_n}\right)(V_{dd} - V_{tn}) + \mu_p C_{ox} \left(\frac{W_p}{L_p}\right)(V_{dd} - |V_{tp}|)} \tag{10}$$

$$\begin{aligned} \Delta V = & \frac{1}{2C_H} C_{ox}[W_p L_p (V_{dd} - |V_{tp}|) - W_n L_n (V_{dd} - V_{tn})] \\ & + \frac{L_{ovp} W_p (2V_{dd} - V_{in}) - L_{ovn} W_n (V_{dd} + V_{in})}{L_{ovn} W_n C_{ox} + L_{ovp} W_p C_{ox} + C_H} C_{ox} \end{aligned} \tag{11}$$

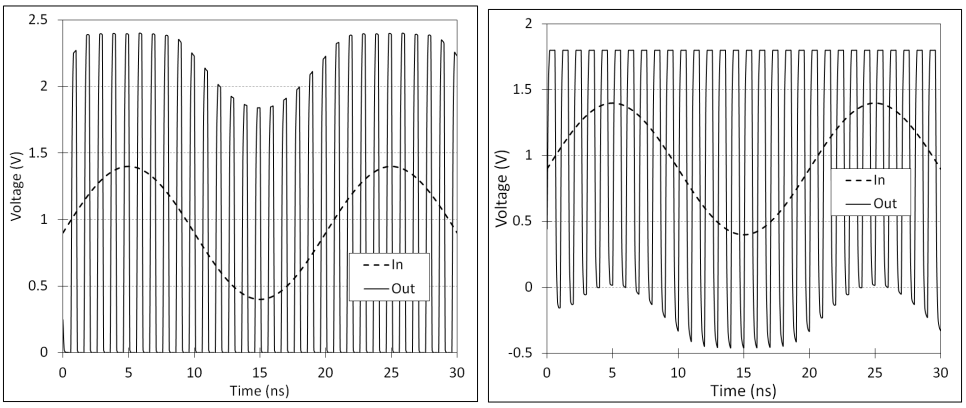
Equation (10) shows that the on-resistance of proposed S/H circuit is independent to input signal. Although it is well known that the threshold voltage of transistor is input signal dependent, it can be neglected because its value variation is small enough. By this condition, the linearity of S/H can be increased and the distortion can be reduced. This equation also shows that the overdrive voltage of each transistor in TG switch increase by V_{in}. It means the value of on-resistance becomes smaller and it can increase the switching speed.

Equation (11) shows that the total error dominant term (error caused by channel charge injection) is independent to input signal V_{in}. Although the second term (error caused by clock feedthrough) becomes input signal dependent, this technique still gives the advantages. Because the input signal dependent shifts from dominant term to less dominant term, so that the total input signal dependent can decrease.

4. SIMULATION RESULTS

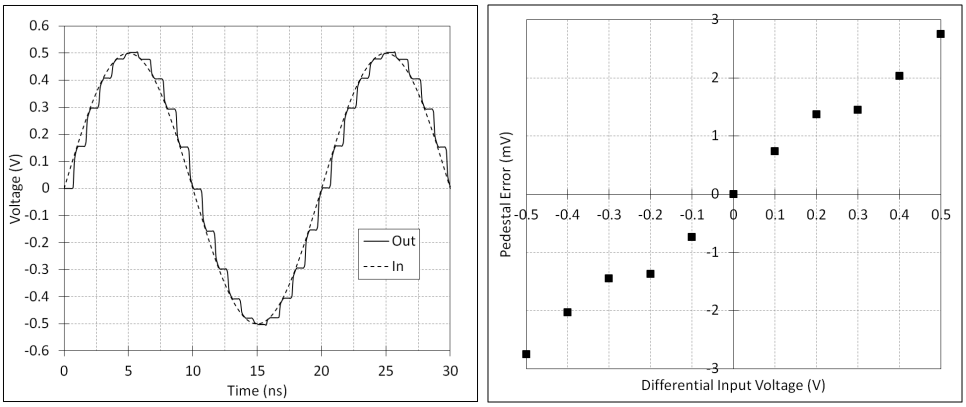
The performance of the proposed circuit was evaluated using HSPICE with 1P, 5M, 3-well, 0.18-m CMOS process (BSIM3v3.2 LEVEL53). Figure 6 shows the input and output waveform of bootstrap circuit for a sinusoidal input of 1 V peak-to-peak at 50 MHz with a 1 GHz sampling clock. From this simulation result it can

be known that in the sampling phase the circuit can track the input (dashed line) voltage and give the output (solid line) of $V_{in} + V_{dd}$ for NMOS bootstrap circuit and $V_{in} - V_{dd}$ for PMOS bootstrap circuit. Figure 7 (a) shows the transient response of the proposed S/H circuit for 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock. The common mode (CM) level of differential signal is 0.25 V. The pedestal error as the function of differential input voltage is shown in Figure. 7 (b). For 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock, the maximum absolute value and root-means-square (RMS) value of pedestal error are 2.75 mV and 1.72 mV, respectively with 0.542 mW power consumption.



(a) (b)

Figure 6. The input and output waveform of bootstrap circuit for a sinusoidal input of 1 V peak-to-peak at 50 MHz with a 1 GHz sampling clock: (a) NMOS bootstrap circuit, (b) PMOS bootstrap circuit



(a) (b)

Figure 7. Simulation results of proposed S/H circuit for 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock: (a) Input and output waveform, (b) Pedestal error

Figure 8 shows the sampled signal spectrum of 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock. From the analysis, in the Nyquist bandwidth the proposed circuit has performances of 90.87 dB SNR, 73.50 SINAD/SNDR which is equal to 11.92 bits ENOB, -73.58 dB THD, and 73.95 dB SFDR. Furthermore, the simulation of the circuit in various sampling frequencies and input frequencies are done. The input frequency varies from 10 MHz to 50 MHz in the step of 10 MHz while the sample frequency varies from 300 MHz to 1 GHz in the step of 100 MHz. From this condition the proposed circuit has average performances of 69.64 dB SNR, 64.50 SINAD/SNDR which is equal to 10.42 bits ENOB, -77.59 THD, and 69.64 dB SFDR. At last, a comparison of main performance of the proposed circuit with other works is summarized in Table. 1. In general, the proposed circuit shows better performance than other work. Compared with the same bootstrapping technique [12], the proposed circuit also shows better SNDR and higher sampling rate.

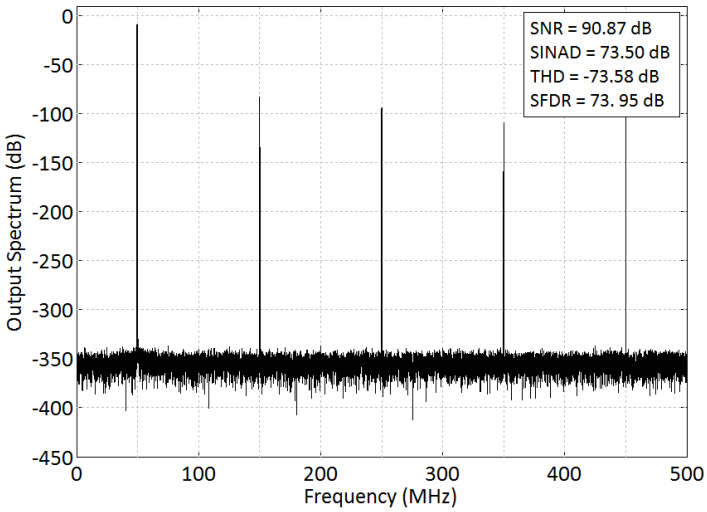


Figure 8. Sampled signal spectrum of 50 MHz sinusoidal 1 V peak-to-peak differential input signal with a 1 GHz sampling clock

Table 1. Comparison of main performance of the proposed circuit with other works

Parameter	Proposed	[11]	[13]	[14]	[15]	[16]	[10]	[9]	[8]	[12]
Sampling rate (MS/s)	1000	500	40	200	330	200	100	500	250	280
Input frequency (MHz)	50	10	-	40	80	-	10	220	20	7
Input Amplitude (V)	1	0.8	1.4	0.8	1.2	2	2	1.6	1.6	0.5
SNR (dB)	90.87	-	67	-	-	-	-	-	-	-
SINAD/SNDR (dB)	73.50	60.50	-	45	-	-	85.5	76	-	57.01
ENOB (bits)	11.92	9.8	9	7.2	11	12	13.9	12.33	14	9.18
THD (dB)	-73.58	-60.5	-56	-	-68.3	-	-	-	-	-
SFDR (dB)	73.95	69	57	60	-	87	92.87	-	80	-
Pedestal Error (mV)	$<$2.75	$<$4.9	-	-	$<$0.8	-	-	-	-	-
Power consumption (mW)	0.542	6	0.5	22	26.4	-	-	-	-	0.88×10^{-3}
CMOS Technology (nm)	180	90	130	180	350	350	130	350	350	90

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