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Performance Evaluation of GaN Based Thin Film Transistor using TCAD Simulation

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Article Info	ABSTRACT
	As reported in past decades, gallium nitride as one of the most capable compound semiconductor, GaN-based high-electron mobility transistors are the focus of intense research activities in the area of high power, high-speed, and high-temperature transistors. In this paper we present a design and simulation of the GaN based thin film transistor using sentaurus TCAD for the extracting the electrical performance. The resulting GaN TFTs exhibits good electrical performance in the simulated results, including, a threshold voltage of 12-15 V, an on/off current ratio of $6.5 \times 10^7 \sim 8.3 \times 10^8$, and a sub-threshold slope of 0.44V/dec. Sentaurus TCAD simulations is the tool which offers study of comprehensive behavior of semiconductor structures with ease. The simulation results of the TFT structure based on gallium nitride active channel have great prospective in the next-generation flat-panel display applications.

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1.   INTRODUCTION

A TFT is a special kind of Field effect transistor which is made by depositing thin films of a semiconductor active layer as well as dielectric layer and metallic contacts over a supporting substrate. A common substrate is glass, since the primary application of TFTs is in liquid crystal displays (LCD). This differs from the conventional transistor where substrate is semiconductor material itself, such as a Si wafer. The basic operation of a TFT is illustrated in Figure 1.
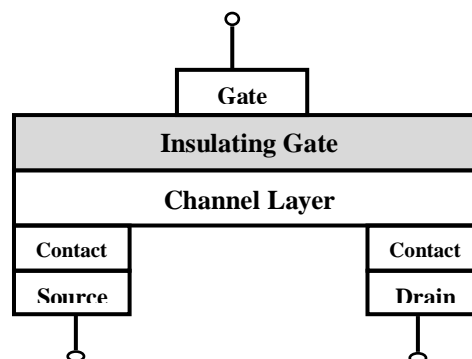

Figure 1. Illustration of TFT Basic Operation

Hydrogenated amorphous silicon (a-Si:H) is still most popular technology in Thin Film Transistors (TFTs) for large area electronics such as X-ray imagers, and it is also heavily utilized in photovoltaic applications. a-Si:H TFTs have low off current and sufficient on/off current ratio for current large area applications; however, their field effect mobility and stability of threshold volta**ge.** The low mobility limits not only pixel size but also prohibits complementary circuit implementation using a-Si:H. Since the hole mobility in a-Si:H is several orders lower than electron mobility, p-type transistor implementation is not practical which makes designing usable complementary circuit impossible [1]. On the other hand, the drifting threshold voltage means that a-Si:H TFTs cannot be implemented in column multiplexor and row shift register circuits [2]. Polycrystalline silicon (Poly-Si) had been proposed to resolve these problems and replace a-Si:H. However, Poly-Si technology has drawbacks on production side since it requires a large and expensive laser annealing system.

Over the past several years, the inherent scaling limitations of electron devices have fueled the exploration of high carrier mobility semiconductors as a Si replacement to further enhance the device performance. In particular, compound semiconductors heterogeneously integrated on Si substrates have been actively studied, combining the high mobility of compound semiconductors and the well-established, low cost processing of Si technology [3].

It can be comprehended that there are three regions of operation. For small gate voltages, the Fermi level lies in the deep states and it can be assumed that the energy bands are close to flat band condition. With an increase in the positive gate bias, causes bending near to the gate dielectric interface and this increases fermi level through the deep states and towards the band tail states [4].

In this state, most of induced electrons are trapped in deep defect states, a small but negligible amount of electrons may occupy tail states yield a small amount of drain current. This operation region is called the sub threshold region shown in Figure 1. The sub–threshold region continues until the deep states are filled up with electrons and the concentration of electrons in tail states exceeds that of trapped electrons in deep states. As the gate bias continues to increase, it finally exceeds a threshold voltage (V_{th}) which implies the Fermi level now lies in the tail states [5-6]. For gate–source bias (V_{gs}) higher than V_{th}, the TFT is operating in the above threshold regime, i.e. ON state.

With the continuous demand in reduction of physical gate lengths of the electronic devices such as TFTs new device architectures will be required to reach the performance of the future technology generation [7]. In addition, control of gate leakage current requires the introduction of gate insulators with high dielectric constants, and the need for increased carrier mobility pushes the use of unconventional channel materials and processing to induce appropriate stresses. The availability of advanced models and simulation tools has significant importance to achieve these goals due to following reasons:

1) Early evaluations of the most promising device architectures and materials in terms of performance and potential for continued scaling.
2) Assessments of processing and design strategies.
3) Reductions of cycle time and of R&D costs. Measurements and tests at the nanoscale tend to be much more expensive than at the microscale and macroscale [8].

The main aim of this paper is to simulate the thin–film transistor using GaN as an active channel layer. This involves the generation of the thin film based TFT structures using Sentaurus TCAD software. Simulations of the same to obtain the electrical characteristics and hence the extraction of electrical parameters like threshold voltage, mobility and ON/OFF ratio will enable in determining the functioning characteristics of the device.

2. ELECTRICAL PROPERTIES AND CHARACTERISTICS OF TFT

The uniqueness of the thin film transistor technology lies in the composing materials and structure with few parameters on the substrate material and size. V_{th} measured in Volts, Ion/off, field effect mobility in cm^2/Vs and subthreshold voltage in V/decade are the parameters which conclude the electrical performance of the device.

2.1. Threshold Voltage

V_{th} is the gate voltage necessary to turn on the transistor. It should be low so that it takes low voltage to turn TFT on or off. It is measured in the saturation region i.e. $VDS \geq VGS - VT$.

Ids using square law model of TFT can be given by [9]:

$$I_d = \frac{1}{2} \mu C_G \left(\frac{W}{L}\right) \left(V_{gs} - V_{th}\right)^2 \tag{1}$$

where W, L, C_G and μ are the TFT channel width, length, gate capacitance and field-effect mobility respectively. To measure V_{th} after square root the equation (1) we get

$$\sqrt{I_d} = \left\{\frac{1}{2}\mu C_G \left(\frac{W}{L}\right)\right\}^{\frac{1}{2}} (V_{gs} - V_{th}) \qquad (2)$$

Now by plotting √IDS *vs. VGS* and by extrapolating down to the x-axis as shown in Figure 2, the threshold voltage can be determined.
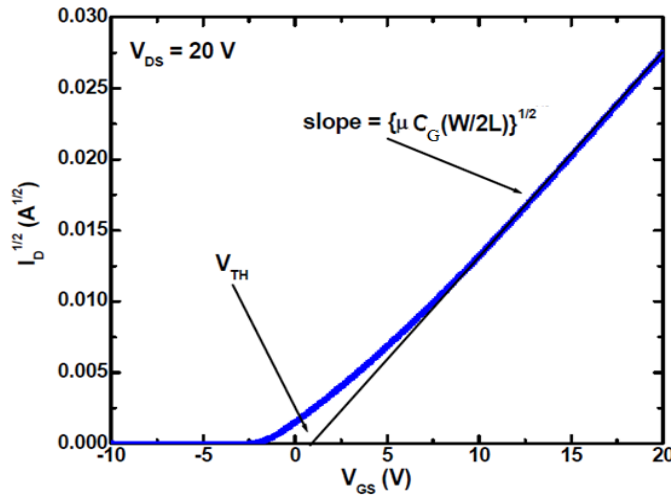

Figure 2. Linear fit on square root of transfer characteristics of a typical TFT, adopted from [5]

2.2. On/Off Current Ratio

Drain current on/off ratio is another measure of the switching behavior of the TFT. It is simply the ratio between highest measured current (the on-state current, *Ion*) to the lowest measured current (the off-state current, *Ioff*) as shown in Figure. *Ioff* is also a measure of the gate leakage present in the device.

2.3. Mobilty

The mobility characterizes how quickly an electron can move through a metal or semiconductor, when pulled by an electric field. Mobility, μ, is defined as a linear proportionality constant relating the carrier drift velocity, v_d, to the applied electric field E. Effective mobility, μ_{EFF}, and field-effect mobility, μ_{FE}, are the two commonly used definitions for the assessment of the mobility of carriers in a field effect transistor. Effective mobility, μ_{EFF}, is extracted from the drain conductance, g_D, which is dI_d/dV_{ds} measured in the linear regime of operation. As Field effect mobility, μ_{EFF}, is extracted from the transconductance, gm, which is dI_d/dV_{ds} g_m can be known by transfer characteristics. Means V_{GS} I_D curve. μ_{FE} employed as estimators of TFT channel mobility.

2.4. Sub Threshold

Another important parameter is subthreshold slope, which characterizes the effectiveness of the Gate voltage in reducing drain current to zero.

The subthreshold slope can be given by equation (3)

$$S = \frac{\partial V_{GS}}{\partial \log I_{DS}} \qquad (3)$$

To achieve high on/off current ratios, subthreshold slopes should be low so that the same difference in V_{GS} can decrease the drain current by more decades. Depending on the gate-source voltage V_{GS}, different regions of operation can be identified: above-threshold, subthreshold, and Poole-Frenkel emission.

In the subthreshold region of operation, the TFT switches from off to on and the current changes exponentially from a low off current, which is in pA, to a high on current, which is in μA.

Forward subthreshold regionis Vth >V_{GS} > 0

The drain current equation (4) in the forward subthreshold region is given by [11]:

$$I_{DS} = \frac{I_{sub0}W}{L} exp \frac{V_{GS}-V_{TS}}{S_f} \tag{4}$$

where I_{sub0} is the magnitude of current in the subthreshold region, and S_f is the forward subthreshold region. The drain current equation (5) in the reverse subthreshold region is defined by following equation [11]

$$I_{DS} = \frac{I_{sub0}W}{L} exp \frac{V_{GS}-V_{TS}}{S_r+\gamma_n|V_{DS}|} \tag{5}$$

where Sr is the reverse subthreshold slope and γ_n is a unitless parameter accounting for two dimensional effects.

3. DESIGNING OF STRUCTURE
Semiconductor manufacturers face the challenge of developing process technologies within strict time and cost constraints. TCAD reduces the number of engineering wafers, saving time and money.

3.1. Generation of TFT Structure using Sentaurus TCAD
Using the Sentaurus Structure Editor the 2D structure of the TFT is drawn. Graphical User interface of Structure editor opens a window after pressing command line. This window has its three part.The menu bar, toolbars, and lists are in the upper part of the main window; the view window is in the center; and the command-line window is in the lower part of the main window. Contacts can be defined to allow the constructed device to be connected to outside power sources. The contacts name, sets, properties, edge color, thickness are defined for the specific structure. Figure 3 shows the structure of TFT with with GaN as an active channel layer which is designed with a 100/50 μm as a W/L.
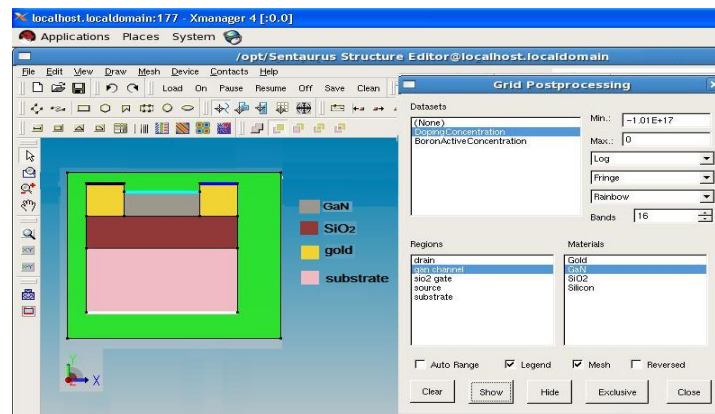

Figure 3. Structure used for Two Dimensional Simulation of GaN Channel TFT using Sentaurus TCAD

3.2. Defining doping of the TFT Structure using Sentaurus TCAD
A constant boron background doping of 1×10^{15} cm^{-3} in the silicon material is introduced by appropriate selection in the constant profile placement dialog box with placement name, material, species, and concentration field. The doping profile is chosen with and concentration of 1e+15and arsenic active concentration are dopants are included by the addition of constant doping profile into the silicon for obtaining the increased mobility in the dielectric semiconductor interface.

3.3. Defining meshing Strategy of the Structure and Generation of Mesh
After the device is structured, contacts are set and doping profile has been selected. The next step is called meshing. Sentaurus Mesh is a modular 2D and 3D mesh generator that can create both axis-aligned and tensor meshes to be used in simulators that use the box discretization or finite-difference time-domain (FDTD) methods for spatial device discretization. Sentaurus Mesh produces triangles in the case of 2D devices and tetrahedra in the case of 3D devices. Generated grids can be loaded into Sentaurus Device and

Sentaurus Process. Depending on the mesh generator used, Sentaurus Mesh produces different output formats. The axis-aligned mesh generator always produces a TDR unstructured mesh. In Sentaurus Structure Editor, the mesh generation process is performed in two steps. The first step defines the meshing strategy, which includes the maximum and minimum meshing step definition in each device dimensions as well as the mesh refinement strategies. The second step links the defined strategy from the first step to a specific target, which is, in general, a material, or a device region, or a user-defined evaluation window. Note that different device regions have different roles in terms of determining the device performance, thereby the required meshing strategies for these regions are typically different. Figure 4 and figure 5 shows the meshing strategy adopted for the min-max element size and build mesh is successfully generated as shown in the Figure 6.
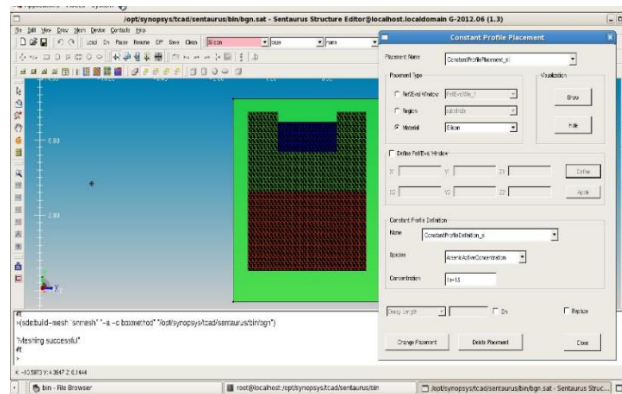

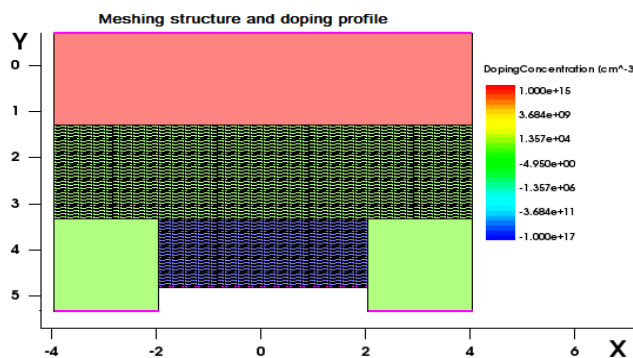Figure 4. Structure used for two dimensional simulation of bottom gate GaN channel TFT using sentaurus TCAD

Figure 5. Defining Meshing Strategy and doping profile GaN channel TFT
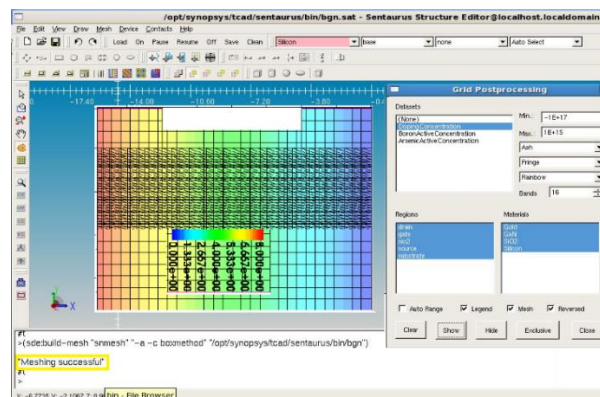

Figure 6. Defining doping profile build mesh of the structure

4. RESULT AND DISCUSSION

On increasing gate bias the carriers induced in the inversion get trapped in the defect sates and potential barrier increases in height and the traps become full and the additional carriers then reduces the depletion width. Therefore, a threshold voltage is required to overcome the potential barrier created due to defect states and to drive the thin film transistor in ON state. Figure 7 represents the transfer curves of the simulated structure. Standard FET theory has been used to extract the channel threshold voltage. The achieved current ON/OFF ratio is quite good because of presence of low defects as compared to the a–si: H. These values are quite comparable to a–si: H, a–C: H values [12], [13]. The drain current is clearly modulated by the applied gate bias. For the extraction of electrical paraetrs drain vloatage current charcaterics are obatined depicted in Figure 8.
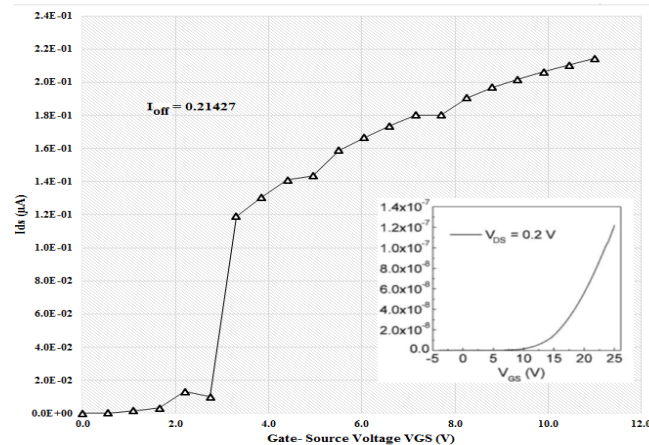

Figure 7. Simulated transfer characteristics for different values of drain to source bias
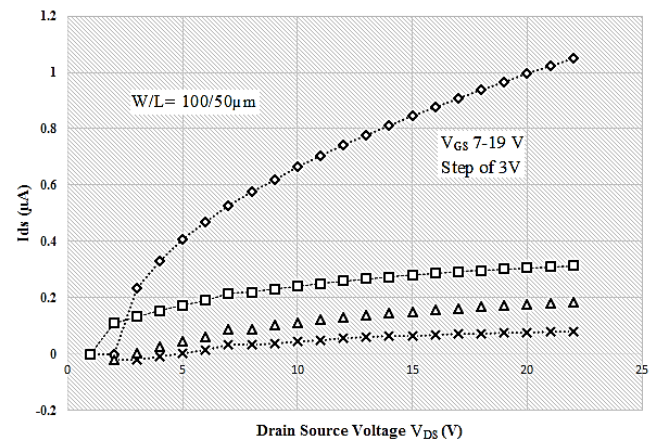

Figure 8. Simulated drain characteristics for different values of gate to source bias

5. CONCLUSION

Design and simulation of the GaN based thin film transistor using sentaurus TCAD is presented in this paper. This lead to extract and evaluate the electrical performance of thin film transistor. The resulting GaN TFTs exhibits good electrical performance in the simulated results, including, a threshold voltage of 12-15 V, an on/off current ratio of $6.5 \times 10^7 \sim 8.3 \times 10^8$, and a sub-threshold slope of 0.44V/dec. All these values have to be corroborated with experimental values, which is a part of future work. Sentaurus TCAD simulations is the tool which offers study of comprehensive behavior of semiconductor structures with ease. The simulation results of the TFT structure based on gallium nitride active channel have great prospective in the next-generation flat-panel display applications. With further experimentation may be carried for the better

approximation to estimate electrical characteristics of the semiconductor device by use of simulation of similar TFTs by incorporating different structure, doping profile, and variation of materials in regions.

Table 2.Threshold Voltage, ON/OFF Ratio, Saturation Mobility and Sub–Threshold Slope Values under different DOS Values

Parameter	Density of States (1×10^{15}) in cm^{-3} eV^{-1}	Density of States (1×10^{18}) in cm^{-3} eV^{-1}
Threshold Voltage (V)	~ 15	~ 12
ON current	1.4×10^7	2.5×10^8
Off current	0.21427	0.31224
ON/OFF ratio	6.5×10^7	8.3×10^8
Saturation Mobility	3.36×10^{-6}	6.97×10^{-3}
Sub-threshold slope(V/decade)	0.44	0.36

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