Switching pulse generation for DC-DC boost converter using Xilinx-ISE with FPGA processor

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Article Info	ABSTRACT
Article history:	This paper explains steps to generate switching pulse using Xilinx-ISE with
Received Apr 15, 2019	FPGA processor for DC-DC boost converter. The switching pulse generated using Very high speed integrated circuit Hardware Description Language
Revised Oct 22, 2019	(VHDL) with Xilinx-ISE. VHDL is a programming language, which is used
Accepted Nov 30, 2019	to model and design any complex circuits in a dynamic environment.
	This paper gives the course of action for generation of switching pulses for dc-dc boost converter using Xilinx-ISE and matlab simulink. The switching
Keywords:	pulse generated using Xilinx-ISE with FPGA-Spartan 6 processor compared
DC-DC boost converter	with switching pulse generated using matlab.
Field Programmable Gate Array	
(FPGA) Processor	
Hardware Description	
Language (VHDL)	Copyright © 2020 Institute of Advanced Engineering and Science.
Xilinx-ISE	All rights reserved.

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1. INTRODUCTION

In recent years the usage and progress of Programmable Logic Devices (FPGA, CPLD) are increasing for the power electronic applications without microprocessors (CPU or DSP) and microcontrollers [1-2]. Complex control algorithm can be implementing for any power electronic system using FPGA processor and computational time also significantly reduced using programmable logic devices [3], but in terms of business based applications for power electronic systems are designed using microprocessor & microcontroller [4-6]. Generally to improve the output of renewable energy system or dc source, the dc-dc boost converters are employed. The relevance of dc-dc converters engross the following requirements like high step up output voltage gain, low input current and low current ripples, high output voltage and low voltage ripples and higher efficiency [7-10]. The various dc-dc converters are design with help of conventional coupled inductor, switched capacitor, clamping diodes and controlled power semiconductor device, which is controlled by duty ratio. Based on duty ratio of dc-dc converter the output voltage can be increased or decreased [11-14]. In this paper gives the procedure to generate switching pulse for dc-dc boost converter using Xilinx-ISE with FPGA processor.

2. DC-DC BOOST CONVERTER

The dc-dc converter is electronic system which converts dc source voltage from one voltage range to another voltage range [15-17]. It attracts many researchers to boost or increases output voltage from the renewable energy systems like fuel cell, PV system and wind energy system [16]. The conventional dc-dc converters are power switching converter which innately introduces a certain amount ripple in current

output, which is minimized with help of advanced dc-dc converters [17-19]. Generally the conventional dc-dc converters only applicable for low power applications, which are developed to high power applications using isolated and non isolated converters [20-22]. In Figure 1 shows the diagram for boost converter, which is used to boost input dc voltage. When the power switch is ON condition, the inductor charge energy in the form of electromagnetic field and discharge energy when power switch is off condition. The time constant RC of the circuit depends on the capacitor size. The output voltage boost level depends on the duty ratio of the switch and applied input voltage, which is defined as,

$$V_0 = V_i (1 - G)$$
(1)

Where, Vo is output voltage, Vi – input voltage and G- duty ratio.

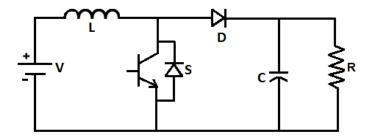


Figure 1. Circuit diagram of DC-DC Boost converter

3. SWITCHING PULSE GENERATION

The switching pulse for dc-dc boost converter is generated using Sinusoidal Pulse Width Modulation (SPWM). Pulse Width Modulation is a method wherein a fixed DC input voltage is given to inverters and controlled AC output voltage is obtained by adjusting the duty cycle [23]. Output signal alternates between ON and OFF within specified period; controls power received by a device and the voltage seen by the load is directly proportional to the source voltage [24]. Pulse Width Modulation allows us to vary how much time the signal is high in an analog way [25-26]. While the signal can only be high (usually 5V) or low (ground) but we can vary the proportion of time the signal is high compared to when it is low is shown in Figure 2.

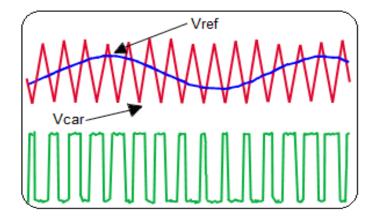


Figure 2. SPWM - switching pulse generation

The main advantage of PWM is that power loss in the switching devices is very low. The technique we are using is the Sinusoidal Pulse Width Modulation. SPWM is one of the most popular modulation technique used and finds more applications in industries. The gating signal can be generated by comparing a sinusoidal reference signal with a triangular carrier wave and width of each pulse varied proportionally to amplitude of a sine wave evaluated at the centre of same pulse. SPWM is one technique which helps in reducing the harmonics present in quasi state.

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The modulation index is defined as, $M_a = A_m / Ac$

(2)

Where, A_m = reference signal amplitude, Ac = carrier signal amplitude.

4. VHDL CODING USING XILINX-ISE

The switching pulse for dc/dc converter is engendered using VHDL coding by Xilinx ISE with help of FPGA processor. Xilinx-ISE is the platform environment for writing VHDL code and to feed into the FPGA processor. To generate single switching pulse for dc/dc converter the following VHDL coding written in Xilinx software.

```
a. Coding
Library IEEE
 USE IEEE.STD LOGIC 1164.ALL;
 USE IEEE.STD_LOGIC_ARITH.ALL;
   Entity top_SPWM
      Port (CLK: IN STD_LOGIC;
      PWM DIR: OUT STD LOGIC;
      PWM OE: OUT_STD_LOGIC;
      PWM 1: OUT STD_LOGIC; );
  ARCHITECTURE BEHAV OF TOP_PWM IS
    Signal CAR: integer:=0
       Begin
           Process(clk)
           Variable counter: integer:=0;
       Begin
          if rising_edge(clk) then
            COUNTER:=COUNTER+1;
           If counter > 0 and counter <=1000;
           CAR \leq CAR + 1;
           ELSEIF COUNTER >1000 AND COUNTER <= 2000 THEN
           CAR<=CAR-1;
      ELSEIF COUNTER >2000 THEN
           COUNTER:=0:
           CAR <= 0;
     END IF:
     END IF:
           IF 500>=CAR THEN
              PWM 1<= '1';
           ELSE
              PWM 1 <= '0';
             END IF;
        END PROCESS;
```

b. Steps to generate bit file from VHDL coding

After initializing the spartan-6 FPGA processor; the VHDL has written for single switching pulse generation to control the dc-dc converter. The flowchart for generation of bit files from VHDL code is shown in Figure 3 and the generated bit file is feed into the FPGA processor to control the dc-dc converter, which is shown in Figure.4.

5. SIMULATION AND HARDWARE RESULTS & DISCUSSION

The system is simulated and implemented to generate switching pulse using Xilinx-ISE with FPGA processor for DC-DC boost converter. The switching pulse generated using Very high speed integrated circuit Hardware Description Language (VHDL) with Xilinx-ISE. VHDL is a programming language, which is used to model and design any complex circuits in a dynamic environment. the switching pulse generated through SPWM method and it is implemented through FPGA professor with help of Xilinx software, which is shown in Figure 5. The DC input supply applied to dc-dc converter is 12V and it is converted 32V, which is 2.6 times of applied input voltage and is shown in Figure 6.

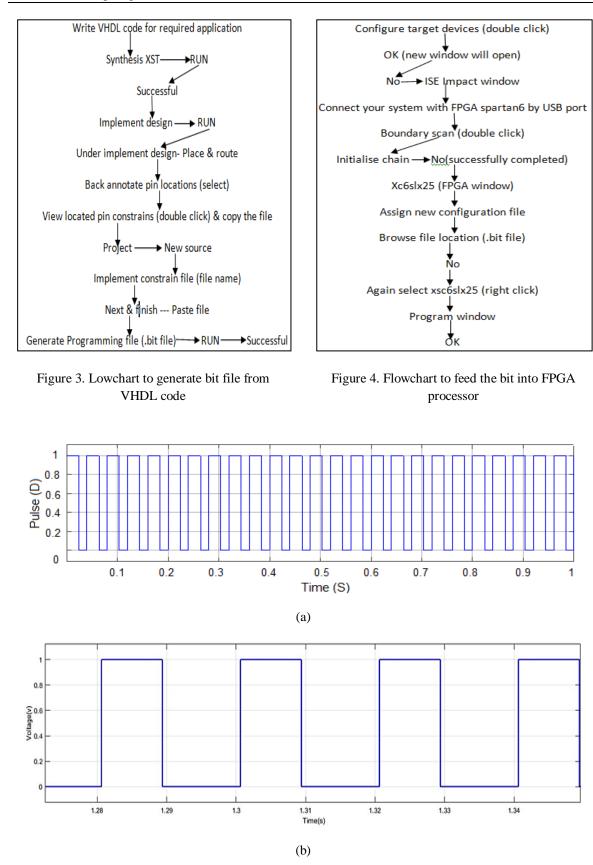
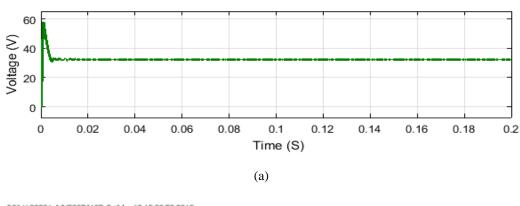
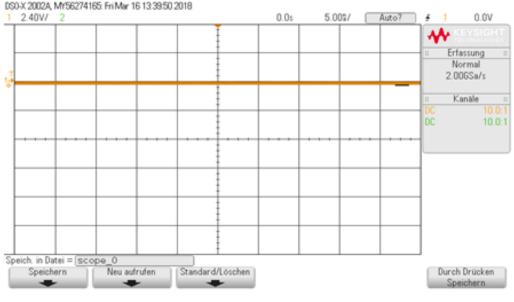


Figure 5. Switching pulse generation using SPWM (a) simulation (b) hardware





(b)

Figure 6. Output voltage of dc-dc boost converter (a) simulation (b) hardware

6. CONCLUSION

Generally various dc-dc converter topologies are used for energy conversion system. In this paper, switching pulse generation for dc to dc converter using Xilinx – Spartan 6 controller. The output voltage of the dc-dc converters are varied, which attains as increased, decreased or equal to applied voltage depends on the duty ratio produced by the sinusoidal pulse width modulation technique. The simulation & hardware results are verified using matlab/simulink and FPGA processor.

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