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Achieving Pull-in Avoiding Cycle Slip using Second-order PLLs

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ABSTRACT

Synchronization is an essential process and one of the first tasks of the receiver in case of coherent communications as well synchronous digital data transfer. The phase lock loop (PLL), which employs the error tracking technique, has been a very popular way to implement this synchronizer since the early 1930s. A phenomenon called cycle slip occurs when the number of cycles present in the transmitted carrier (clock) differs from that of the recovered carrier (clock) at the receiver. The cycle slip can be very detrimental to some applications such as frequency modulated communications systems (FSK, multi-carrier etc.), burst digital data transfer, training pulse retrieval, and so on. This paper presents a remedy to avoid the cycle slip by using properly designedsecond-order Type II PLL.

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1. INTRODUCTION

When information is sent from one point to another, regardless of the type of processing (analog or digital), extraction of the time base from the transmitter is immensely important. The process of this time base extraction, at the receiver, is known as *synchronization*. Most commonly found synchronization can be divided in three main categories. In the case of *carrier synchronization*, found both in digital and analog communications systems, a local oscillator in the receiver is locked to the carrier of the transmitted message. In the case of *clock synchronization*, found particularly in digital communications, the rising or the falling edge of the receiver clock is lined up with that of the transmitter, so that the data can be captured correctly. In the third category of synchronization, known as *word synchronization* found in digital packet data transfer, the beginning and the end of a data packet are ascertained by the receiver.

The process of synchronization is equally essential for any *coherent communication* independent of the medium used, e.g., wire or wireless, cable or fiber; however, the implementation details may vary. This fact remains true for any transmitter(s)-receiver(s) connection topology, such as *point-to-point*, *multicast*, *broadcast*, *shared*, *mesh*, etc. For instance, in the case of a shared channel communications, where the dedicated messages for each user are combined (multiplexed) in different time slots (TDMA) or frequency slots (FDMA), or, a combination of both, the individual receiver has to perform the synchronization before extracting (decoding) the message intended for it.

There are at least three ways to implement a synchronizer, namely, 1) error tracking, 2) maximum seeking followed by selection filtering and 3) non-linear operation followed by passive filtering. The most common synchronizer, known as phase lock loop that uses the error tracking technique, has been used since the coherent communications has been invented in the early 1930s.

2. PLL MODEL

In essence, a *model* is an abstraction of something real. That thing can be an idea, a condition, an existing system or a potential system. *Mathematical modeling*, in particular, is a technique of translating one of the above items from an application arena into tractable mathematical formulations whose theoretical and/or numerical analysis provides useful insights, details and guidance. As for an existing or potential system, the model represents its key characteristics and attributes in a broken-down, component level fashion. Often, models are analyzed in an effort to build a system or to control, remediate or optimize its performance [1], [2].

There are three key steps in formulating a mathematical model as depicted in Figure 1.

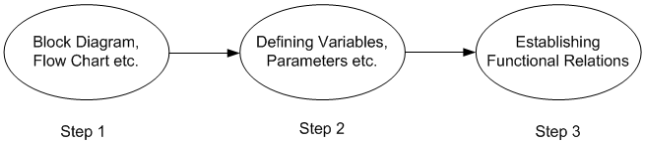

Figure 1. Key steps of mathematical modeling

2.1. Why We Need a Model

There are many practical reasons to use mathematical models. In the engineering design process, in particular, the usage of mathematical models are primarily of great benefit due to the fact that they allow us to determine the possible behavior of a system without having to build it, which in many cases, could be huge and/or costly. Surprisingly, sometimes the models help clarify underlying assumptions in the design process. They may also suggest/identify the crucial data that should be collected while conducting measurements or may generate data that cannot be collected from real-life measurements. Another important feature of the models is that they may predict the outcome under varying conditions by modifying the system parameters [3], [4].

2.2. Basic Architecture of a PLL

As mentioned earlier, a phase lock loop (PLL) is basically an error tracking feedback control system. It tracks the phase of a reference signal (most commonly *bandpass*) and tries to lock on to it. Figure 2 shows the basic architecture of a PLL system, containing three component blocks, namely, the *phase* comparator (detector), the loop filter and the voltage controlled*oscillator (VCO).* While building a full-up system, each of these component blocks can be realized in many different ways.

The external reference input signal is commonly modeled as the sum of a desired frequency $\omega_0$component, the undesired frequency components and the additive noise component. A voltage controlled oscillator with a center frequency at ω_0 is chosen to track the phase of the reference input. Suppose $\theta_i(t)$ and $\theta_v(t)$ are the *instantaneous phase* of the *reference input signal* and that of the VCO *output signal*, respectively. The phase comparator produces a signal that contains a component quantifying the *phase error* $\emptyset(t) = \theta_i(t) - \theta_v(t)$, along with the *random noise*. This signal is fed into the *loop filter* (usually *lowpass*), and the filtered output is applied to the VCO as the *control input* with the hope that it adjusts the phase of the VCO output signal so that the phase error $\emptyset$diminishes monotonically. If the loop is designed and operated properly, the phase error $\emptyset$(absolute value) becomes very small under the phase-locked condition.

In the PLL literature, the default architecture shown in Figure 2 is called a *short-loop* or baseband model, to be specific. There is another version, called *long-loop*, found in some receivers that deals with an IF signal as the reference. In the long-loop architecture, a stage of down conversion to IF followed by bandpass filtering is followed by another stage of down conversion (to baseband) followed by a lowpass filtering that is done prior to the VCO feed. Our work will be restricted to the baseband loop (short-loop) model that operates in a noise-free environment.

2.3. Component Models

There are three main component blocks in a basic (short- loop) PLL construction as shown in Figure 2. Any one of these three blocks can be implemented in various ways using various different techniques and/or technologies; hence, their corresponding models change accordingly. Each form has its own advantages and disadvantages. Commonly, the technical requirements of a given application and the cost associated with a particular implementation determine the right choice.

As mentioned in the previous section, the phase comparator, hereafter known as the phase detector (PD), produces a signal that contains a component quantifying the instantaneous phase difference between the input reference and the VCO output signal. Thus, a simple model for the phase detector, shown in Figure 2, could be expressed as a function of the instantaneous phase difference

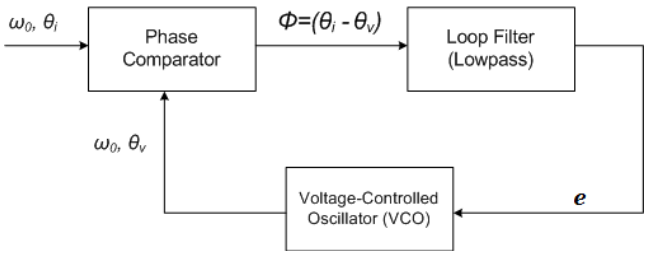

Figure 2. Basic architecture of a PLL system

$$g(\emptyset) = g(\theta_i - \theta_v \quad (1)$$

Exact function for $g(\emptyset)$ will be determined by the nature of the phase detector used in the system and our work will be restricted to two most commonly used PDs, one known as sinusoidal PD and the other one as triangular PD.

Mathematically, an nth-order filter, shown as loop filter in Figure 2, can be modeled in the Laplace domain as

$$F(s) = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_0}, m \leq n \quad (2)$$

Both active and passive loop filters are common in the PLLs, though active filters implemented with OP-AMPs are more common in modern applications.

The voltage controlled oscillator (VCO) takes in a control voltage e(t) and produces a sinusoid with instantaneous phase $\theta_v(t)$, as depicted in Figure 2. A popular way to mathematically model such a VCO is by relating these two quantities as

$$\frac{d\theta_v}{dt} = \omega_0 + k_v e \quad (3)$$

where constants ω_0 and K_v are known as the center or quiescent frequency and gain parameter of the VCO, respectively. Thus, the frequency of the VCO is proportional to the control voltage $e(t)$ around the center frequency. Redefining the instantaneous phases of the reference input to the PD and the output of the VCO by subtracting a phase ramp term, sometimes known as a quiescent phase $(\omega_0 t)$, simplifies the analysis. Thus, the new instantaneous relative phase quantities into the PD and out of the VCO becomes respectively

$$\theta_1(t) = \theta_i(t) - \omega_0 t \quad (4)$$

and

$$\theta_2(t) = \theta_v(t) - \omega_0 t \quad (5)$$

where $\theta_1(t)$ is the instantaneous phase of the reference input to the PD, as defined earlier. With this, the phase error at the output of the PD is also redefined as

$$\emptyset(t) = \theta_i(t) - \theta_v(t) = \theta_1(t) - \theta_2(t) \quad (6)$$

Further assuming $\theta_2(0) = 0$ leads to the VCO model in thetime domain as

$$\frac{d}{dt}\theta_2(t) = K_v e \quad (7)$$

which is represented in the VCO block diagram shown in Figure 3. After applying the proper boundary condition, the VCO model in the Laplace domain becomes

$$H_{vco}(s) = \frac{\vartheta_2(s)}{E(s)} \quad (8)$$

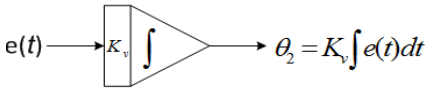

Figure 3. Mathematical model of a VCO

Thus, it implies that the response $\theta_2(t)$ of the VCO is inversely proportional to the frequency of the control voltage $e(t)$. Such a first-order lowpass filter is sometimes known as an integrator. Therefore, the VCO adds an order to the order of the loop filter (which is usually another lowpass filter) when it comes to the overall order of the PLL system.

2.4. Order and Type of a PLL System

The order of a PLL is the (highest) degree of the denominator polynomial of the closed loop transfer function of the system. Therefore, the order of the loop filter is one less than that of the PLL, since the VCO itself is a first-order lowpass filter, commonly termed as an integrator. On the other hand, the Type of a PLL is determined by the number of integrators present in the system. Type I PLL, therefore, does not contain any integrator in the loop filter; the sole integrator is contributed by the VCO. Likewise, Type II contains one integrator in the loop filter, Type III contains two and so on. For instance, a third-order Type II PLL will have one integrator in the VCO and another integrator in its second-order loop filter.

2.5. Why Second-Order PLL

The complexity of behavioral analysis as well as the construction of a PLL system grows drastically as the order of the PLL increases. From that perspective, the first-order loop appears to be the most attractive choice. However, they are not often used because narrow bandwidth and good tracking, commonly achieved by large DC gain, are incompatible in the first-order loops [5]. Next comes the second-order PLL, which offers satisfactory performance for most applications despite its simplicity. As hinted earlier, when the order of the PLL grows to three, the complexity of analysis grows significantly. Therefore, it is rarely used except for specific applications where extremely tight jitter tolerance is required. Besides, due to the fact that a second-order system can be decomposed into a set of two simultaneous first-order systems, enabling the visualization of the solutions in a 2-D plane, known as phase portrait, a second-order loop has a distinct edge in terms of dynamical system analysis over its higher order counterparts.

2.6. Common Types of Phase Detectors

As mentioned earlier, every block in the PLL system can be realized in more than one way, thus, the first block in the system, the phase detector, can be implemented in many ways. The *Sinusoidal* phase detector and the *Triangular* phase detectors are the most common ones found in the PLL architectures. The sinusoidal detectors are usually implemented by analog multipliers and are very common in the legacy systems. The model for it can be expressed as$g(\emptyset) = K_{pd} \sin \emptyset$, where $K_{pd}$is known as the phase detector gain. On the other hand, the triangular phase detectors, which are implemented relatively easily with an XOR gate and hard limiters, are very common these days. When the reference input and the output of the VCO are already in digital format, even the need for hard limiters goes away and the PD can be realized with only an XOR gate. The model for a triangular PD, likewise, can be expressed as $g(\emptyset) = K_{pd}\,\mathrm{tri}(\emptyset)$, where 'tri' represents a (bipolar) triangular function of $\emptyset$having unity amplitude.

3. RESEARCH METHOD: BEHAVIORAL ANAYLISIS OF SECOND-ORDER PLL

Now that we have touched upon the individual models for the component blocks in the system, we are ready to construct the model for a full-up second-order PLL system. As suggested in the previous section, only a first-order loop filter (lowpass) is required to build a second-order PLL since the VCO itself also acts as a first-order lowpass filter. The transfer function of a first-order lowpass filter can be written as

$$F(s) = K_{lf}\frac{s+a}{s+b} \quad (9)$$

whereK_{lf} is known as the loop filter gain and $-a$ and $-b$ are respectively the zero and the pole of the filter. To ensure the stability of the loop, it is also required that $a > b > 0$. The closed loop gain of the system can be defined as $G \equiv K_{pd}K_{lf}K_v$by lumping all the individual gain parameters together. It is worth noting that G can be placed anywhere in the loop without affecting the analysis. Thus, in the block diagram for a second-order PLL shown in Figure 4, the closed loop gain G is arbitrarily included in the VCO block.

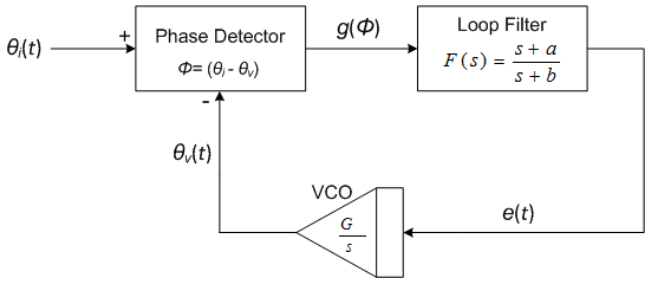

Figure 4. Block diagram of a second-order PLL system

Finally, by defining another loop parameter, known as the detuning parameter in the PLL literature, as $\omega_\Delta = \omega_i - \omega_0$, the mathematical model for a gain normalized second-orderPLL system can be expressed as

$$\frac{d^2\emptyset}{dt^2} + [b' + g_\emptyset(\emptyset)]\frac{d\emptyset}{dt} + a'g(\emptyset) = b'\omega'_\Delta \tag{10}$$

where $g_\emptyset(\emptyset)$ is the derivative of $g(\emptyset)$, the PD output, w.r.t. $\emptyset$, $\tau = tG$ and the gain normalized system parameters are

$$\left.\begin{aligned} a' &= a/G \\ b' &= b/G \\ \omega'_\Delta &= \omega_\Delta/G \end{aligned}\right\} \tag{11}$$

For non-zero b, the above system has only one integrator, coming from the VCO, and such a system is termed as second- order Type I. In contrast, when b becomes zero, the loop filter becomes a proportional plus integrator having a pole at the origin and hence the system contains two integrators. Such a system is then termed as second-order Type II.

In the theory of differential equation, a second-order equation can be decomposed into a set of two simultaneous first- order equations and the solutions can be portrayed in a 2-D plane, known as phase plane. Thus, the system described by Eqn. (11) can be rewritten as

$$\left.\begin{aligned} \frac{d\emptyset}{d\tau} &= \dot{\emptyset} \\ \frac{d\dot{\emptyset}}{d\tau} &= -[b' + g_\emptyset(\emptyset)]\dot{\emptyset} + [b'\omega'_\Delta - a'g(\emptyset)] \end{aligned}\right\} \tag{12}$$

This attractive technique, called phase portrayed, can be applied to second-order loops in order to visualize the dynamical behavior of the system on the phase plane, which is not possible for higher order loops. Many a times, a non-linear second-order system does not have closed form solutions. In particular for the system described by Eqn. (10), the source of non-linearity is in $g(\emptyset)$ and/or $g_\emptyset(\emptyset)$, and both of our candidate PDs produce non-linear $g(\emptyset)$. Furthermore, due to the presence of the periodicity (of 2π period) in$g(\emptyset)$, as well as in $g_\emptyset(\emptyset)$, results in a similar periodicity in the phase portrait of the system. Thus, the phase portrait of the above system can be completely visualized by wrapping it up on the surface of a cylinder of unit radius [6]. Therefore, the dynamic behavioral study of the system can be restricted in one such period, sometimes also known as cell, without loss of generality. Lastly, there is a theorem in the theory of differential equation that states that the local behavior of a non-linear system can be derived from its corresponding linearized system around an equilibrium point, as long as the equilibrium point is not non-hyperbolic. Furthermore, at times, this local behavior can be extended to obtain a reasonable idea about the

global behavior of the system. All of these features are capitalized in analyzing the system at hand and following two subsections briefly touch upon the results of the analysis for two popular kinds of PDs used in many PLLs up to this date.

3.1. Dynamic Behavior of a Second-order PLL Using Sinusoidal PD

The analysis is restricted to one period $(-\pi \leq \emptyset \leq \pi)$ of $g(\emptyset)$ (also $g_{\emptyset}(\emptyset)$) without the loss of generality, since the phase portrait repeats after the same period.

The two equilibrium points in the period of interest are $(\emptyset, \dot{\emptyset}) = (\emptyset_0, 0)$ and$(\emptyset, \dot{\emptyset}) = (\pi - \emptyset_0, 0)$, where $\emptyset_0 = \sin^{-1}\left(\frac{b'\omega'_\Delta}{a'}\right)$ and $(0 \leq \emptyset_0 \leq \pi/2)$. The first equilibrium point turns out to be a *focus* and the second one is a *saddle node* [5], [6], [7].

It is important to note here that the locations of the equilibria are dependent on the loop parameters $a', b'$and ω'_Δ. Moreover, the equilibrium point exists if $|\omega'_\Delta| \leq \Omega'_h$ and $\Omega'_h \equiv \frac{a'}{b'}$. Thus, the behavior of the system changes drastically if anyone or any combination of those parameters keeps varying and cross that limit. This phenomenon is known as *bifurcation*. Again, the phase portrait can also be affected by the closed loop gain *G* of the system. However, we will briefly discuss the behavior of the system for only high gain cases, since the low gain loops are rare in practice.

The *bifurcation parameter*, commonly denoted by μ, for a Type I loop can be defined by any of the loop parameters or any combination thereof. The most common and practical way to define it is to use the detuning parameter as $\mu = \omega'_\Delta$. Two particular values of this parameter give rise to a drastic change in the global behavior of a second-order Type I loops employing a sinusoidal PD.

The first one is known as *pull-in range* (Ω_p), where a special periodic orbit, commonly called *limit cycle*, appears on the phase portrait. This phenomenon is commonly known as *saddle node bifurcation*. An approximating formula to calculate the gain normalized pull-in range for a high gain Type I PLL with a sinusoidal PD is given as [7]

$$\Omega'_p = \Omega_p / G \approx \sqrt{2\frac{a'}{b'}} \tag{13}$$

A numerical procedure to calculate it accurately can be found in [8].

The second one is known as *half-plane pull-in frequency* (Ω_2), where a periodic limit cycle connects all the saddle nodes on the phase portrait. This phenomenon is commonly known as *separatrix cycle bifurcation*, which only applies to high gain cases. There has neither been an exact nor an approximating formula to calculate the half-plane pull-in frequency for a Type I loop employing a sinusoidal PD.

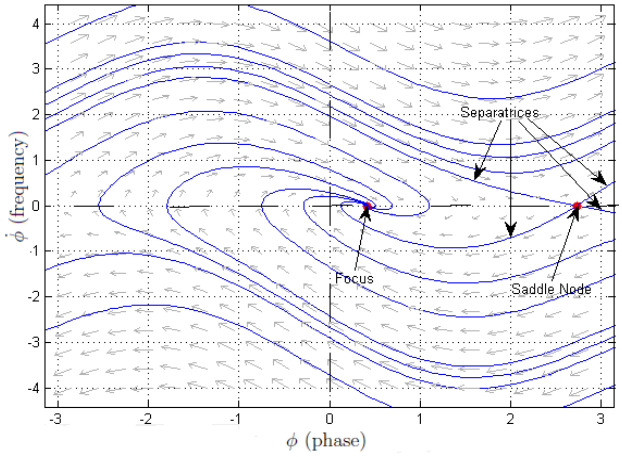

Figure 5. Region I phase portrait for a Type I PLL with Sinusoidal PD

3.1.1. Phase Portrait in Region I

This region is defined by the range $|\mu| < \Omega_p$. Figure 5 is a representative phase portrait of a second-order Type I PLL employing a sinusoidal PD in this region, which is drawn for $a' = 0.5, b' = 0.1, \omega_\Delta = 2.5$,

using an open source Matlab program, called pplane8. The foci are the global attracting points for the entire phase plane except for the points on the separatrices. For $\omega_\Delta < 0$, the phase portrait swaps the upper half plane with the lower half plane.

3.1.2. Phase Portrait in Region II

This region is defined by the range $\Omega_p' < |\mu| < \Omega_h'$. Figure 6 is a representative phase portraitwhich is drawn for$a' = 0.5, b' = 0.1$, $\omega_\Delta' = 3.1$. In this region, there exist two limit cycles. The *stable limit cycle moves* higherand higher up on the phase portrait and the *unstable limit cycle* moves closer and closer to the separatrix as μincreases. All the trajectories above the stable limit cycle and between the limit cycles asymptotically approach the stable limit cycle.On the other hand, all the trajectories below the unstable limitcycle approach one of the foci. For $\omega_\Delta' < 0$, the phase portrait swaps the upper half plane with the lower half plane. Thus, the stable and the unstable limit cycles will show up in thelower half plane instead of the upper half plane.

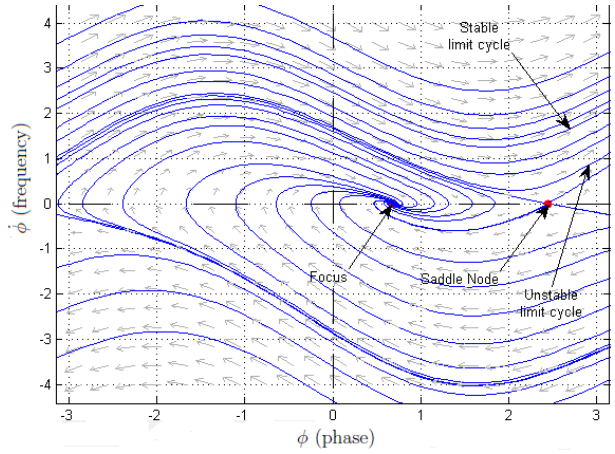

Figure 6. Region II phase portrait for a Type I PLL with Sinusoidal PD

3.1.3. Phase Portrait in Region III

This region is defined by the range $|\mu| > \Omega_h'$. Figure 7 is a representative phase portrait which is drawn for $a' = 0.5, b' = 0.1$, $\omega_\Delta' = 6$. In this region, the behavior of theType I PLL drastically differs from that of the previous two regions. All the equilibrium points on the phase plane disappear, therefore no pull-in is possible. However, there exists a stable limit cycle which asymptotically attracts all the trajectories on the phase plane. For $\omega_\Delta' < 0$, the phase portrait swaps the upper half plane with the lower half plane. Thus, the stable limit cycle will show up in the lower half plane instead of the upper half plane.

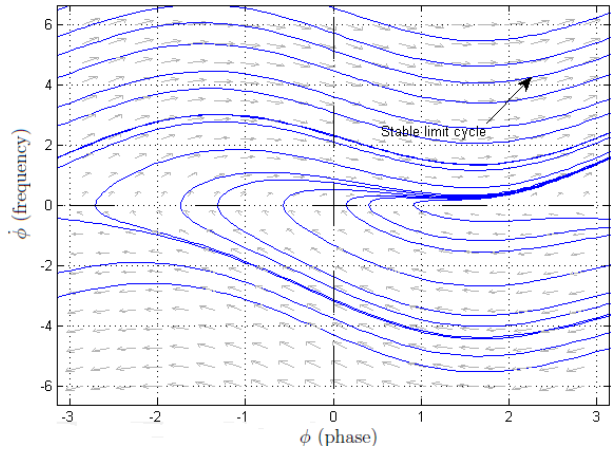

Figure 7. Region III phase portrait for a Type I PLL with Sinusoidal PD

Now, setting b = 0 turns the system into a second-order but Type II PLL. In that case, the two equilibrium points in the same cell become $(\emptyset, \dot{\emptyset}) = (\emptyset_0, 0)$and $(\emptyset, \dot{\emptyset}) = (\pi, 0)$.They still remain to be a focus and a saddle node respectively, just like in Type I case. However, they always exist and their locations are fixed regardless of the value of the loop parameters, unlike the Type II case. Moreover, the possibility of bifurcation by varying any of the loop parameters is eliminated. Figure 8 is a representative phase portrait of a second-order Type II PLL employing a sinusoidal PD, spanned little over a period, drawn for a' = 0.5.

3.2. Dynamic Behavior of a Second-order PLL Using Triangular PD

The two equilibrium points in the period of interest are $(\emptyset, \dot{\emptyset}) = (\pi - \frac{b'\omega'_\Delta}{a'}, 0)$ and$(\emptyset, \dot{\emptyset}) = (\frac{b'\omega'_\Delta}{a'}, 0)$. The first equilibrium point turns out to be a focus and the second one is a saddle node [5], [6], [7].

Just like in the case of a Type I PLL using Sinusoidal PD, the existence as well as the location of the equilibria of a Type I loop using Triangular PD depends on a', b', and ω'_Δ. Therefore, the phase portrait has to be studied separately for different ranges of these parameters.

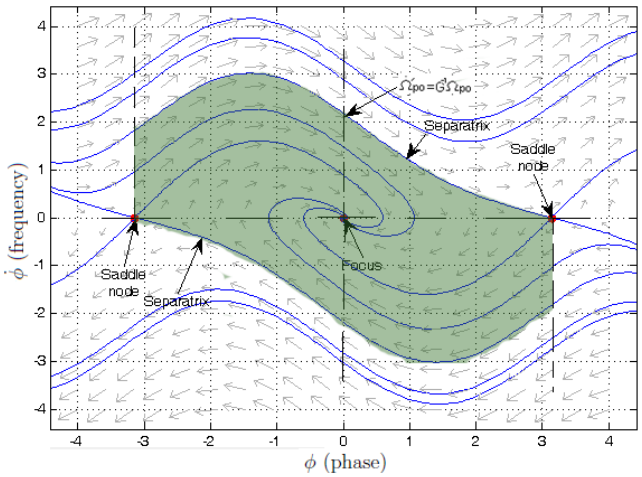

Figure 8. Typical phase portrait for a Type II PLL with Sinusoidal PD

Unlike the loops employing a sinusoidal PD, there has neither been an exact nor an approximating formula to calculate the pull-in range for a Type I loop employing a triangular PD. However, there exists an exact formula deduced by *J. L. Stensby*to calculate the half-plane pull-in frequency for a Type I loop employing a triangular PD [9].

3.2.1. Phase Portrait in Region I

This region is defined by the range $|\mu| < \Omega'_p$. Figure 9 is a representative phase portraitof a second-order Type I PLL employing a triangular PD inthis region, which is drawn for$a' = 0.5, b' = 0.1$, $\omega'_\Delta = 2.0$. Thisphase portrait resembles that of a sinusoidal PD Type I PLLin the same region as depicted in Figure 5.

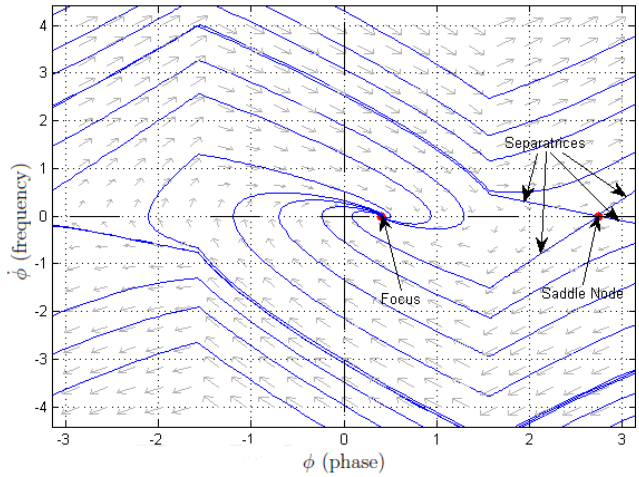

Figure 9. Region I phase portrait for a Type I PLL with Triangular PD

3.2.2. Phase Portrait in Region II

This region is defined by the range $\Omega_p' < |\mu| < \Omega_h'$. Figure 10 is a representative phase portrait which is drawn for $a' = 0.5, b' = 0.1$, $\omega_\Delta' = 4.4$ and it resembles the phase portrait of a Type I PLL employing sinusoidal PD in the same region as depicted in Figure 6.

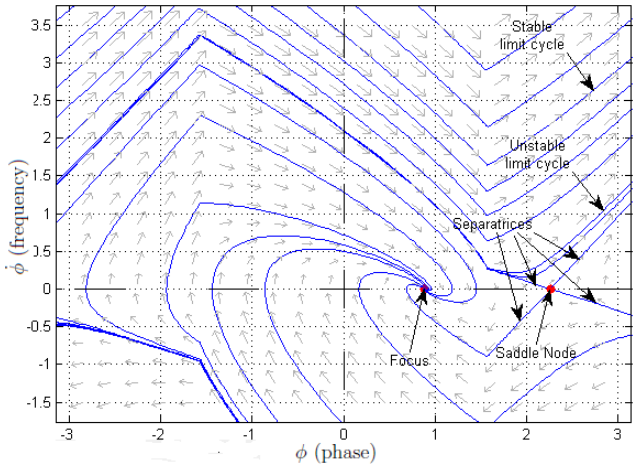

Figure 10. Region II phase portrait for a Type I PLL with Triangular PD

3.2.3. Phase Portrait in Region III

This region is defined by the range $|\mu| > \Omega_h'$. Figure 11 is a representative phase portraitwhich is drawn for$a' = 0.5, b' = 0.1$,$\omega_\Delta' = 8$ and it resembles thephase portrait of a Type I PLL employing sinusoidal PD inthe same region as depicted in Figure 7.

Now, setting b = 0 turns the system into a second-order but Type II PLL. In that case, the two equilibrium points in thesame cell become $(\emptyset, \dot{\emptyset}) = (\emptyset_0, 0)and(\emptyset, \dot{\emptyset}) = (\pi, 0)$. They still remain to be a focus and a saddle node respectively, just like in Type I case. However, they always exist and their locationsare fixed regardless of the value of the loop parameters, unlike the Type II case. Moreover, the possibility of bifurcation vanishes when any of the loop parameters is varied. Figure 12 is a representative phase portrait of a second-order Type II PLL employing a sinusoidal PD, spanned little over a period, drawn for $a' = 0.5$.

3.3. Why Type II

Based on our discussion in the previous section, it is clear at this point that the analysis as well as the behavior of a Type I loop, compared to its Type II counterpart, is much more complex. We will touch

upon a few reasons, based on their respective phase portraits, in what follows. The equilibria for Type II loops are independent of any of the loop parameters. In contrast, the equilibria for the Type I loops depend on the loop parameter/s, and therefore, they move as any one of the parameters is varied. They may even disappear for certain values of those parameters.

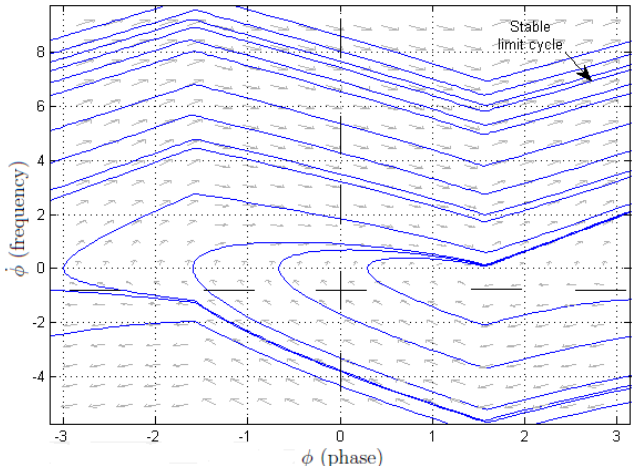

Figure 11. Region III phase portrait for a Type I PLL with Triangular PD

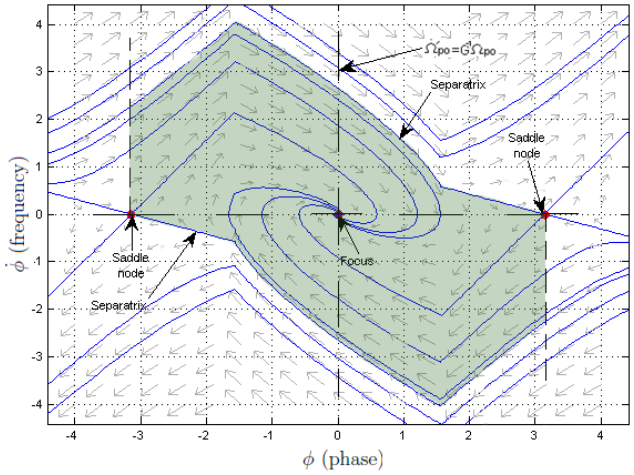

Figure 12. Typical phase portrait for a Type II PLL with Triangular PD

There is a symmetry in the phase portrait for Type II loops, meaning that a trajectory remains a trajectory if both the axes are negated. However, in case of Type I loops, no such symmetry exists.

In the case of Type II loops, the entire phase plane constitutes the region of convergence for the foci, except for the separatrices. However, this may be true for Type I loops up to a certain range of the loop parameters' values. For another range of the loop parameters (or some combination thereof), phase portrait may have more than one cell, exhibiting distinctly different behaviors.For another range, the whole system may fail to produce pull-in all together and so on.

In the case of Type II loops, there is no drastic change in the phase portrait as the loop parameters are varied. There is no appearance/disappearance of the equilibrium point and/or the limit cycle. Whereas, Type I loops exhibit two instances of such bifurcation. In the PLL literature, one is known as saddle node bifurcation and the other one is known as separatrix cycle bifurcation.

The phase-locked condition of a Type II PLL implies both zero phase and zero frequency error. However, in case of Type I PLL, it only implies zero frequency error. For nonzero detuning parameter, phase error is always *nonzero*.

False lock does not occur in Type II loops. However, in case of Type I loops, false lock can occur due to a potential presence of limit cycle on the phase portrait, giving rise to a phenomenon known as *beat node*.

The close loop gain has almost no affect in the study of Type II loops, it only acts as a scaling factor. Whereas, the high gain Type I loops behave differently than the low gain ones, even when the other loop parameters are kept unchanged.

Therefore, the second-order Type II PLL remains a good and safe starting point in the PLL design process for most applications till today.

4. CYCLE SLIP IN PULL-IN

If the loop is designed and operated properly, the phase error ∅(absolute value) becomes very small under the phase-locked condition. The process of achieving this phase lock from the out-of-lock condition is known as pull-in. This pull-in may or may not take place for a given PLL. Even if it happens, it may take an unreasonably long time, which is not practical for the application for which it was intended. In such situations, sometimes additional circuitry, known as aiding circuitry, is introduced in the architecture to expedite the phase acquisition (pull-in) [5], [7], [10], [11], [12].

The phenomenon of cycle slip occurs when the number of cycles present in the reference input (carrier/clock) deviates from the number of cycles found in the VCO output. It is expected to occur in the power up and reset recovery, when the system tries to achieve the initial phase-lock. This kind of scenario can hardly be avoided and therefore tolerated for most applications. However, the cycle slip may also happen when a PLL is in the locked condition and suddenly loses the lock. In such scenarios, the PLL may miss one or more reference input (carrier/clock) cycles in the process of locking back to the reference input. Such an event can be detrimental in many applications, both in digital and in analog systems. In some applications, this cycle slip may even cause the VCO to tune its output in the wrong direction.

5. CAUSES FOR LOSING LOCK

A PLL may lose its lock and give rise to cycle slip, when an unintended (intended) circumstance corrupts (changes) the reference input and/or the VCO output signal. The unintended random noise present in the reference input and/or in the VCO output signal can induce enough phase and/or frequency error to make the PLL lose the lock. The cycle slip, caused by such undesired noise, can be extremely detrimental to many applications. Particularly, in the case of digital packet data synchronization, as shown in Figure 13, a miss-count between the transmitted clock cycle and the VCO clock cycle, commonly termed as recovered clock, causes erroneous reception of the packet due to incorrect received word (packet) alignment. With appropriate coding, this error may be corrected or the packet needs to be retransmitted. In either case, it imposes an additional overhead on the hardware and/or software, system latency etc. Similarly, this is true in the case of training pulse recovery. Cycle slip in such situations may lead to not recognizing the pulse pattern and thus failing to turn on the reception mode at the right time. Thus, the cycle slip causes the receiver to misread the packet (word) boundaries and, hence, mixes up the received data stream.

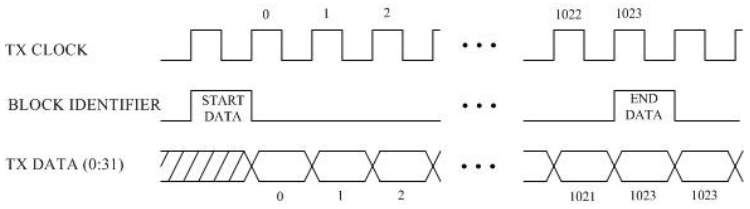

Figure 13. Synchronous transmission of 1Kx4B block data

As for the intended loss of lock of the PLL, it is an obvious consequence of frequency modulation (FM) scheme, when acarrier is changed from one frequency (to which the loop was already locked) to another. For instance, in case of binary FSK modulation, a carrier at frequency f_m , commonly known as the

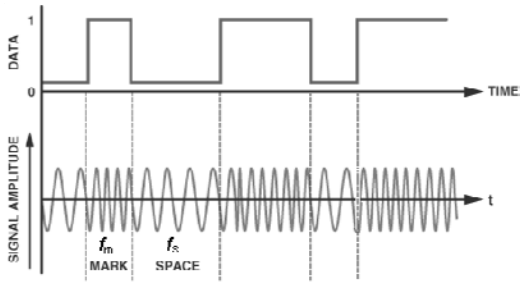

Figure 14. FSK modulation scheme

Mark frequency, is used to transmit a binary '1' while, a carrier at frequency f_s , commonly known as the *Space* frequency, is used to transmit a binary '0'. Figure 14, shows a digital (binary) data stream and the corresponding analog waveform after FSK modulation in such scheme.

In essence, this kind of modulation causes an abrupt jump in the input reference at the zero phase and zero frequency error condition of the PLL, which equally holds for any frequency modulated systems,e.g., FSK, OFDM, multicarrier, frequency-hopped etc. Such an application may require that the reacquisition of the new frequency without any phase error has to happen in the same cycle, which leaves no room for cycle slip.

6. RESULT AND DISCUSSION: ACHIEVING PULL-IN AVOIDING CYCLE SLIP

The source of noise can be radiated or conducted, deterministic or undeterministic. Although the VCO output is supposed to be very stable for the PLL to operate properly, low frequency power supply noise and/or ground bounce can corrupt its spectral purity if the digital and the analog grounds are not isolated properly on the circuit board. In any case, if either one of the inputs to the phase detector is corrupted by the unwanted noise the loop may lose its lock. It is quite common to model all of the unwanted noise as AWGN and include it in the PLL system model as a forcing function. This indeed further complicates the analysis of a nonlinear system. However, instead, the effect of noise can be qualitatively investigated relatively easily with the help of separatrix on the phase portrait. Approaching from that angle, all the analyses presented in this paper, were done on the premise of a noise-free environment. The two separatrices on the two half planes in the phase plane, as shown in Figure 8 and Figure 12 spanned over a 2π period (saddle node to saddle node), can determine the convergence region of the PLL. As long as the phase and the frequency error, caused by the random noise, stays within that bound, the loop will regain its lock without a cycle slip. On the other hand, if the corruption in the input(s) caused by the noise is too large to induce a phase and/orfrequency error to cross the separatrix, then one or more cycles will be missed in the pull-in process. In other words, the region of convergence provides a measure of the noise-immunity of a Type II PLL. Thus, as long as we have the noise characterized for a particular application and/or an environment, deterministically or statistically, we can tweak the Type II PLL loop parameter/s to adjust the separatrix to contain the noise within the above mentioned convergence region and guarantee no cycle slip during reacquisition of the lock.

As for the loss of lock caused by the modulation (intended), the pull-out frequency becomes the key parameter to guarantee zero cycle slip in relocking. In the frequency modulation schemes, when a carrier is moved from one frequency to another, it does introduce an abrupt jump in the input reference to the PLL at locked condition and the pull-out frequency is a direct measure of the maximum allowable jump that guarantees no cycle slip in the reacquisition of the new frequency. Thus, by using this fact, an FSK demodulator can be constructed simply with only a second-order Type II PLL as shown in Figure 15. The purpose of the power amplifier (PA) before the PLL is to boost the signal level received by the antenna and the comparator after the PLL, built with an OP- AMP, reconstructs the binary waveform by comparing the PLL output with a threshold. As long as the difference between $f_m$and f_s is smaller than the pull-out frequency of the PLL, the demodulator can successfully retrieve the transmitted binary data. In fact, the PLL-based FSK demodulators have been built in a single chip (XR2211, NJM2211 etc.) for more than three decades. Likewise, in multi-carrier (OFDM), frequency hopping, etc., systems, many discrete frequencies from a specified band are assigned to the users as carriers, in a predefined pattern or in a pseudo random manner and, those carriers have to be locked at the receiver front end in the same cycle. A second-order Type II PLL can adapt to this abrupt (yet frequent) change in input reference and relock to those frequencies

without slipping a cycle, as long as the frequency band (from which the carriers are chosen) is smaller than the pull-out frequency of the PLL. Thus, the pull-out frequency of a Type II PLL can determine the width of that band, or, the specified band can guide a Type II PLL design effort to secure a pull-out frequency that can guarantee zero cycle slip in reacquisition. For the above mentioned applications, the PLL employing triangular PD offers more headroom for the frequency jump than the PLL employing sinusoidal PD, designed with the same loop parameter [13] and this pull-out frequency can be calculated exactly (approximately) forType II PLL using a sinusoidal PD (using a triangular PD) by using the formula deduced by the author [14], [15]. It is important to mention that such systems are also subject to the influence of the unwanted/unintended noise as discussed in the previous paragraph. However, the convergence region mentioned therein can provide immunity to this noise, whereas pull-out frequency can guarantee the zero cycle slip for intended disturbance with respect to PLL locked condition.

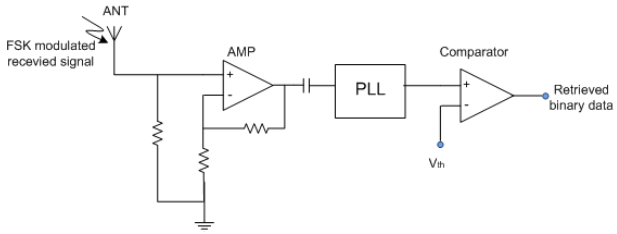

Figure 15. Block diagram of FSK demodulator built with a PLL

7. CONCLUSION

Synchronization is the first step in the coherent communication, digital data transmission and many other applications. This synchronization is achieved by locking the phase of a local oscillator to the carrier (clock) of the transmitted analog message (digital bit stream). This lock may be lost in more than one way due to many reasons. If the lock is lost, it has to be regained and this reacquisition of lock may happen in the same cycle, in more than one cycle (which gives rise to what is known as cycle slip) or may never happen. One very common way to achieve this synchronization is to use phase lock loop, which is implemented based on error tracking technique. In the engineering practice, building models and analyzing them before building the proto-type or the product, is almost a standard procedure. There exist many PLL models in varying orders and Types. This paper starts out with the model for a generic second-order PLL since it performs satisfactorily for most applications and, beyond second-order, the model-analysis as well as the real construction becomes significantly complicated. Then the paper discusses the dynamical behavior of such a model using two of the most widely used phase detectors (comparators). Next, a comparative study based on the behavioral analysis between Type I and Type II is presented to show why Type II in second-order PLL stands out as the first choice as a starting point for analog PLL design effort. Then follows a brief discussion about the reasons that cause the loss of lock and potentially leads to cycle slip, which may be very detrimental and hence, unacceptable in many applications. Finally, the paper proposes the ways, with demonstrating examples, to avoid this undesirable event, cycle slip, by using a properly designed second-order Type II PLL.

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