Inverse sinusoidal pulse width modulation switched electric vehicles' battery charger

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Article Info	ABSTRACT
	This paper presents an efficient, cost-effective and sustainable grid-connected electric vehicles' (EVs') battery charger based on a buck converter to reduce the harmonics injected into the mains power line. To utilize the switching converter as an effective power factor controller (PFC), inverse sinusoidal pulse width modulation (ISPWM) signals are applied. However, a mathematical relationship between the sending-end power factor and the duty ratio of the switching buck converter is derived. To ensure the sustenance of the proposed method, a simulation model of the battery charging system is tested in PSIM simulation platform. The simulation results yield to a lossless charging system with a sending-end power factor close to unity. An experimental testbed comprising a 60 V battery bank of 100 A-h capacity with a charging current of 7 A is developed. The laboratory assessments present an 88.1% efficient charging prototype with a resultant sending-end power factor of 0.89. The laboratory framework concerns with the comparative analysis of the sending-end power factor, system efficiency, and mains line current total harmonic distortion (THD) obtained for different charging methods - simple battery charger, fixed duty ratio controlled buck converter and the proposed topology. The performance evaluations corroborate the reliability of the presented work.

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1. INTRODUCTION

Electrifying transportation is one of the most promising approaches to alleviate climate change issues in the modern world [1]. Energy crisis and environmental issues have encouraged the adoption of electric vehicles (EVs) as an immaculate alternative to the conventional transportation options [2]. EVs can improve energy security by diversifying energy sources, foster economic growth by creating new advanced industries and most importantly, protect environment by reducing pollutions [1]. The continual development of EVs urge significant development of battery and charger technologies.

Intensive research works have been conducted regarding efficient and economically feasible battery chargers for EVs ensuring low harmonics injection into the grid with ameliorated sending-end power factor. EV battery charger can be classified as onboard and off-board types [3]. A conductive on-board charger indicates a physical contact between the vehicle and charging inlet whereas an inductive charger provides a contact-less power transmission based on magnetic interference [3]. Off-board chargers use fast charging methodology with fewer limitations of size and weight [3]. A novel hybrid energy storage tech-

nique for EVs and a monitoring-combined siting scheme for EVs' battery chargers are reported in [4] and [5] respectively. An efficient battery-assisted charging system and a voltage-based controller for EV chargers are documented in [6] and [7] respectively. However, several battery charger topologies for plug-in EVs are proposed in [8-14].

Power factor correction is inevitable in case of grid-integrated battery charging systems to shape the input line current for increasing the sending-end power factor and reducing the current THD. An active PFC topology involving different types of semiconductor switching devices like BJT, MOSFET and IGBT is articulated in [15]. Buck-boost PFC based battery charging systems for plug-in EVs are presented in [16] and [17].

A power factor improvement methodology using nine switches for 3-ϕ applications is reported in [18]. The loss analysis and improvement techniques of the battery charging systems for light EVs are presented in [19]. An active boost derived PFC topology is proposed in [20] where almost unity power factor has been achieved, but it suffers from a line current THD of 7.4%, which violates IEEE519 regulation [21]. Seven level ac-dc power converter with an isolated dc-dc converter is proposed in [22] ensuring high efficiency, almost unity power factor with an acceptable rate of THD. A unidirectional current-source active rectifier with a boost converter for onboard battery charging system is proposed in [23].

Moreover, an LLC Resonant converter with two transformers in parallel for EVs' battery charging application is presented in [24]. Yang et al., Ejury, Rashid [25-27] present the discontinuous conduction mode (DCM) operation techniques of buck converters. The aforementioned designs of EVs' battery chargers with PFC units are complex for practical implementation and can not be considered as cost-effective solutions for frequent application in many cases. Therefore, in this paper a reliable, more cost-effective and comparatively simple battery charging system is proposed for frequent practical applications.

To overcome the limitations of increased switching losses, complex methodologies and implementation costs, a simpler and reliable battery charging method with power factor correction and current THD improvement is articulated here. A buck derived PFC topology is designed and implemented for EVs' battery charging premises. The vehicle for test purpose is an electric three-wheeler. The battery bank contains five series connected 12 V Lead-acid batteries, each with a capacity of 100 A-h. The major drawback of a buck converter, known as crossover distortion, is mitigated by employing a larger percentage width duty ratio of the switching inverse sinusoidal pulse width modulation (ISPWM) signals. A reverse mechanism for controlling the duty ratio of the switching signal is applied when the rectified dc voltage becomes higher than the battery's dc voltage. The automatic optimization of the converter's duty ratio facilitates the efficacious operation of the charging unit of the proposed system. Since the ISPWM signals are generated by comparing a 20 kHz triangular carrier signal with the rectified dc voltage signal, the charging system only needs to sense the line and load (battery) voltage to ensure constant charging current.

The testbed consists of prototypes of a conventional simple battery charger, a conventionally fixed duty ratio buck converter charger and the proposed ISPWM switching based buck converter charger respectively. These three topologies are simulated in PSIM software and with the same design specifications, laboratory prototypes are developed and respective assessments in four criteria: sending-end power factor, mains line current THD, system power efficiency and frequency spectrum profiles based on Fast Fourier Transformation (FFT) values are carried out. From simulations, the proposed system implies a power efficiency of 98%, power factor of 0.98 and a current THD of 12%. From laboratory assessments, the proposed system implies a power efficiency of 88.1%, power factor of 0.89 and a mains line current THD of 23%. [28] presents the simulation results and comparative analysis of different battery charging systems.

Section 2 briefly presents the conventional battery charging topologies. Section 3 describes the proposed charging method. Section 4 articulates the simulation results and relevant analysis. Section 5 and 6 present the laboratory prototype and detailed analysis of experimental outcomes respectively. Section 7 and 8 draw conclusion and acknowledgment of the presented framework.

2. CONVENTIONAL BATTERY CHARGERS

The most common battery charging systems operate in constant current mode. A step-down transformer is used to lower the mains line voltage down to the battery voltage; then the voltage is rectified using a full bridge rectifier. The rectified signal is passed through an output L-C filter. The diode bridge rectifier, which is nonlinear in nature, injects harmonics into the line current and deforms the waveform leading to poor

sending-end power factor. Current is fed to the load (battery) only when the peak of the instantaneous line voltage exceeds the charging voltage across the output filter capacitor. This leads to a pulse-shaped input line current, introducing a significant phase displacement between the line voltage and current. Thereby, the system results in a low power factor of approximately 0.65~0.70, making it an inefficient charger [29].

Another conventional battery charging system is the fixed duty ratio controlled switching PWM based buck converter. The generic switching converter is controlled by a fixed duty ratio pulses of a specific frequency and the input of the converter is a rectifier output. The drawback of this grid-connected charging system is the non-linearity of the diode bridge rectifier and significant harmonics injection into the line current causing a poor power factor.

3.   PROPOSED CHARGING SYSTEM

Figure 1 presents the proposed EV battery charging system. The ac power of the grid is first rectified using a bridge rectifier and then the rectified voltage is inputted to the buck converter. The control unit will generate the appropriate ISPWM signal to operate the buck PFC.
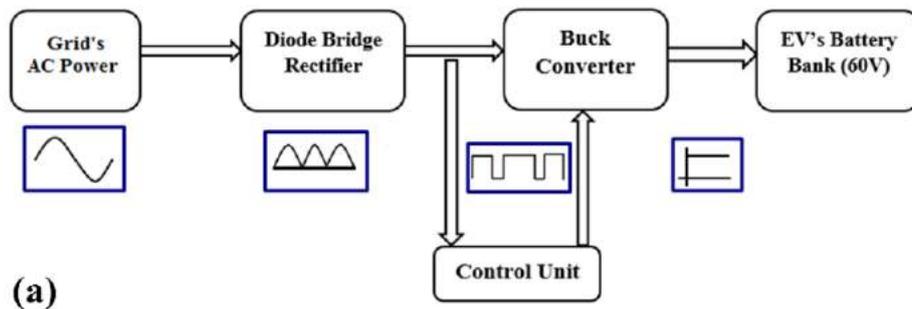
Figure 1. Proposed battery charging System functional diagram

3.1.   Reference signal and ISPWM signal generation

Figure 2 presents the comparator circuit topology to generate the switching ISPWM signals. The rectified pulsating dc signal acts as the reference voltage and the 20 kHz triangular wave acts as the carrier signal. The comparator creates the ISPWM signals by comparing these two input signals. The center-tapped step-down transformer along with two diodes are used for generating pulsating dc output, which is required for modulation purpose in which the amplitude controls the rate of charging current to the battery. Figure 1 presents the ISPWM signals based on the proposed method. The width of the ISPWM signals gets higher where the reference signal is lower than the battery voltage level and vice versa.
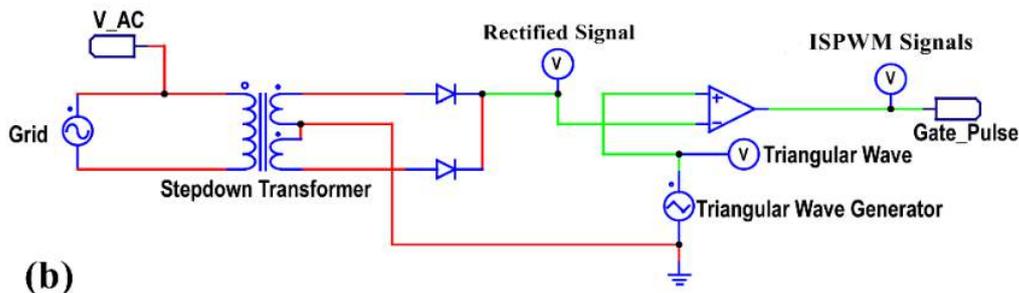
Figure 2. Proposed battery charging system ISPWM signal generation circuit in PSIM
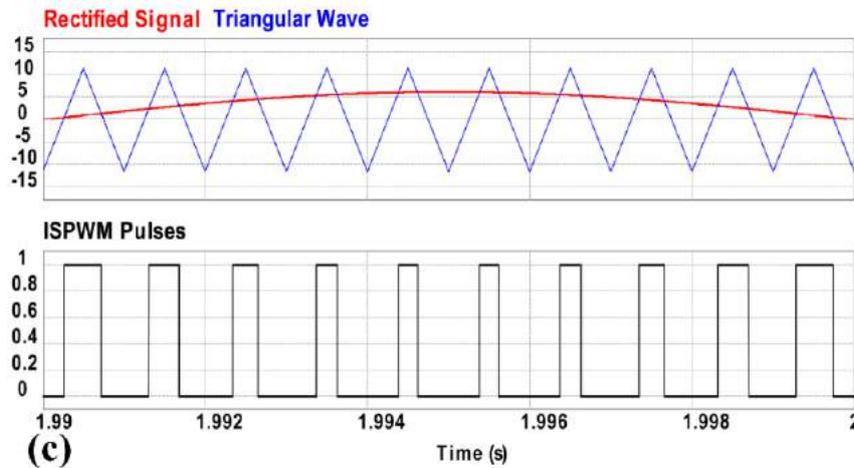
Figure 3. Proposed battery charging system simulated ISPWM signal profile

3.2. Buck converter operation

The buck PFC of the proposed system follows the generic configuration of a step-down switching regulator. Figure 4 presents the implemented buck converter circuit. Table 1 presents the design specifications of the charger. In this proposed system the rectified line current is sampled and compared to the peak of the input inductor current and is used to generate variable duty ratio ISPWM. This reduces the necessity of the current feedback control loop for input and output side of the converter.
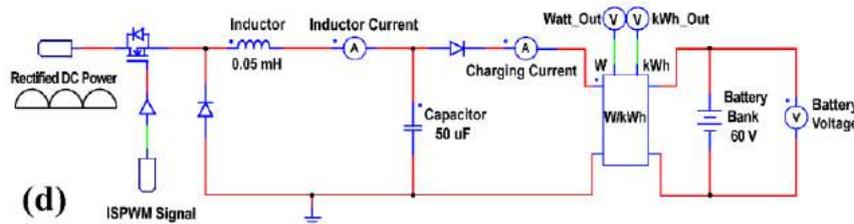
Figure 4. Proposed battery charging system buck converter circuit in PSIM

Table 1. Design specifications of the proposed buck PFC charging system

Symbol	Actual Meaning	Value
V_{in}	Input Ac Voltage	230 V (rms)
V_{out}	Output Dc Voltage	60 V
I_{out}	Maximum Output Current	30 A
f_s	Applied Switching Frequency	20 kHz
L_{buck}	Filter Inductance	0.05 mH
L_{input}	Line Inductance	1.0 mH
C_{buck}	Filter Capacitance	50 μF
P	Rated Capacity	1 kW

The grid-connected ISPWM switched buck converter charges the battery when the input supply voltage (or the rectified voltage) is greater than the battery voltage. In this condition, the buck converter operates in continuous conduction mode (CCM). During the system operation, when the input supply voltage (or the rectified voltage) gets lower than the battery voltage, the buck converter can not charge the battery. In this condition, the buck converter operates in discontinuous conduction mode (DCM). Thereby, the buck PFC can operate in both modes.
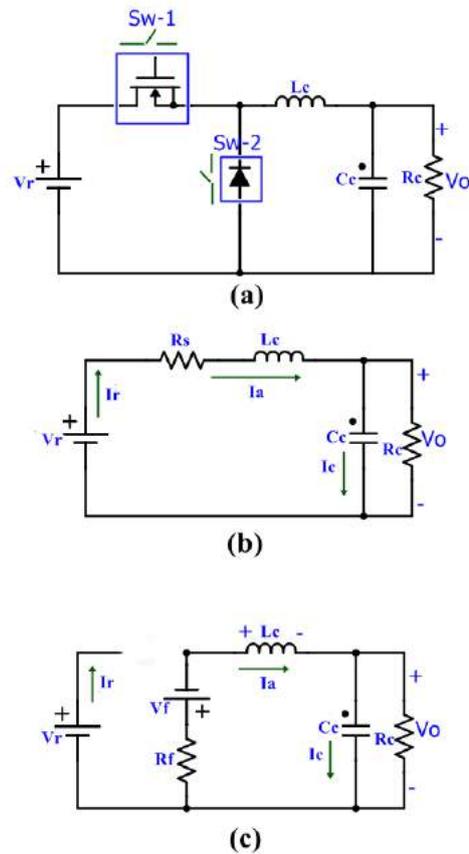
Figure 5. (a) Buck PFC circuit model (b) equivalent buck PFC circuit for dT sub-interval (c) equivalent buck PFC circuit for $(1-d)T$ sub-interval

3.3.   Relationship between duty ratio of the buck PFC and sending-end power factor

This subsection documents a circuit analysis of the proposed buck PFC operating in both CCM and DCM to establish a relationship between the duty ratio of the switching converter and the mains line current. A similar approach to derive a relationship between the duty ratio of a switching buck converter operating in CCM and the mains line current is presented in [30]. However, state space analysis of a soft-switched buck converter acting as a PFC is reported in [31]. The circuit analysis approach described in this paper for both CCM and DCM operations follows the analyses reported in [32]. The following excerpts subsume the derivation of a relationship between the duty ratio of the buck PFC and the sending-end power factor for both CCM and DCM operations.

3.3.1. CCM operation

Figure 5(a) presents a buck PFC circuit model. Sw-1 (MOSFET) can be modeled as an on-state resistance, R_s, and sw-2 (diode) can be modeled as a constant voltage source, V_f, with a series resistance, R_f. During dT_p sub-interval, sw-1 operates and during $(1-d)T_p$ sub-interval, sw-2 operates; d = duty ratio and T_p = switching period. Figure 5(b) and Figure 5(c) present the equivalent circuits of these two sub-intervals respectively. The circuit analysis approach assumes a small ripple approximation. For dT_p sub-interval, the average inductor voltage, and capacitor current are:

$$V_a = V_r - I_a R_s - V_o \tag{1}$$

$$I_c = I_a - \frac{V_o}{R_c} \tag{2}$$

where I_a is the steady state inductor current. During $(1-d)T_p$ sub-interval, the average inductor voltage and capacitor current are:

$$V_a = -V_o - V_f - I_a R_f \tag{3}$$

$$I_c = I_a - \frac{V_o}{R_c} \tag{4}$$

From inductor volt-second and capacitor charge balance conditions, it can be obtained as:

$$[V_r - I_a R_s V_o][d] + [-V_o - V_f - I_a R_f][1 - d] = 0 \tag{5}$$

$$[I_a - \frac{V_o}{R_c}][d] + [I_a - \frac{V_o}{R_c}][1 - d] = 0 \tag{6}$$

$$V_o = \frac{d[V_r - d'V_f]}{[1 + \frac{dR_s}{R_c} + \frac{d'R_f}{R_c}]} \tag{7}$$

Here $d' = 1 - d$

$$I_a = \frac{V_o}{R_c} \tag{8}$$

The mains line current, I_m is a function of the rectifier output current, I_d and the PFC input current, I_r as shown:

$$I_m = f(I_d, I_r) \tag{9}$$

Where:

$$I_r = dI_a = \frac{dV_o}{R_c} = d^2 \frac{[V_r - d'V_f]}{[R_c + dR_s + d'R_f]} \tag{10}$$

$$I_r = g(d, R_s, R_f, R_c, V_r, V_f) \tag{11}$$

$$I_m = f_g(I_d, d, R_s, R_f, R_c, V_r, V_f) \tag{12}$$

I_d is a fixed quantity which is not prone to change with any switching operation. The other resistive and voltage quantities are constant as well. Therefore, (12) can be simplified as:

$$I_m \approx f_g(d) \tag{13}$$

$$\Delta I_m \approx f_g(\Delta d) \tag{14}$$

Here Δ denotes a change in quantity. The analysis yields that the change in PFC duty-ratio during CCM operation determines the change in mains current. The change in mains line current determines the change in source-end power factor of the system with a constant mains voltage and power supply.

3.3.2. DCM operation

In DCM operation, both of the switches sw-1 and sw-2 are off during a sub-interval and the duty ratio can be decomposed into three parts - d_1, d_2 and d_3. The operation of the buck converter can be analyzed in three sub-intervals - $0 < t < d_1 T_p$, $d_1 T_p < t < (d_1 + d_2)T_p$ and $(d_1 + d_2)T_p < t < T_p$. In this case, the switches are modeled in the same manner as presented in 3.3.1.

During $0 < t < d_1 T_p$ interval, sw-1 operates and hence the average inductor voltage and capacitor current are the same as (1) and (2) respectively. During $d_1 T_p < t < (d_1 + d_2)T_p$ interval, sw-2 operates and hence the average inductor voltage and capacitor current are the same as (3) and (4) respectively. During $(d_1 + d_2)T_p < t < T_p$ interval, both of the switches are off and it can be obtained as:

$$V_a = 0 \quad I_a = 0 \tag{15}$$

$$I_c = I_a - \frac{V_o}{R_c} \tag{16}$$

From inductor volt-second balance condition, it can be derived as:

$$[V_r - I_a R_s V_o][d_1] + [-V_o - V_f - I_a R_f][d_2] + [0][d_3] = 0 \tag{17}$$

$$V_r d_1 - I_a R_s d_1 - V_o d_1 - V_o d_2 - V_f d_2 - I_a R_f d_2 = 0 \tag{18}$$

$$-V_o(d_1 + d_2) + V_r d_1 - I_a(R_s d_1 + R_f d_2) - V_f d_2 = 0 \tag{19}$$

$$V_o(d_1 + d_2) = V_r d_1 - I_a(R_s d_1 + R_f d_2) - V_f d_2 \tag{20}$$

$$V_o = \frac{1}{(d_1 + d_2)}[V_r d_1 - I_a(R_s d_1 + R_f d_2) - V_f d_2] \tag{21}$$

From the node equation of the converter network, it can be derived as:

$$I_a = I_c + \frac{V_o}{R_c} \tag{22}$$

Using the capacitor charge balance condition, it is implied that $I_c = 0$ and hence the dc component of the inductor current is equal to the dc load current.

$$I_a = \frac{V_o}{R_c} \tag{23}$$

Using (23), (21) can be modified as:

$$V_o = \frac{1}{(d_1 + d_2)}[V_r d_1 - \frac{V_o}{R_c}(R_s d_1 + R_f d_2) - V_f d_2] \tag{24}$$

$$V_o = \frac{d_1}{(d_1 + d_2)}V_r - [\frac{R_s d_1 + R_f d_2}{R_c(d_1 + d_2)}]V_o - \frac{d_2}{(d_1 + d_2)}V_f \tag{25}$$

$$[1 - \frac{R_s d_1 + R_f d_2}{R_c(d_1 + d_2)}]V_o = \frac{d_1}{(d_1 + d_2)}[V_r - \frac{d_2}{d_1}V_f] \tag{26}$$

$$V_o = \frac{\frac{d_1}{(d_1 + d_2)}[V_r - \frac{d_2}{d_1}V_f]}{[1 - \frac{R_s d_1 + R_f d_2}{R_c(d_1 + d_2)}]} \tag{27}$$

Again, the mains line current, I_m is a function of the rectifier output current, I_d and the PFC input current, I_r as shown:

$$I_m = f(I_d, I_r) \tag{28}$$

Where:

$$I_r = d_1 I_a = \frac{d_1 V_o}{R_c} = \frac{d_1^2[V_r - \frac{d_2}{d_1}V_f]}{R_c(d_1 + d_2) - R_s d_1 - R_f d_2} \tag{29}$$

$$I_r = h(d_1, d_2, R_s, R_f, R_c, V_r, V_f) \tag{30}$$

$$I_m = f_h(I_d, d_1, d_2, R_s, R_f, R_c, V_r, V_f) \tag{31}$$

Again, I_d is a fixed quantity which is not prone to change with any switching operation. The other resistive and voltage quantities are constant as well. Therefore, (31) can be simplified as:

$$I_m \approx f_h(d_1, d_2) \tag{32}$$

$$\Delta I_m \approx f_h(\Delta d_1, \Delta d_2) \tag{33}$$

It can be implied that the change in PFC duty ratio during DCM operation determines the change in mains current and hence determines the change in power factor.

4. SIMULATION RESULTS & ANALYSIS

The simulation is carried out using PSIM software. The simulation depicts a 60 V battery bank being charged at 20 A charging current using the simple charger, conventional buck converter and the proposed charger. Figure 6 presents the mains line voltage, distorted line current and corresponding THD analysis using the aforementioned methods. It can be seen in both cases (simple charger and the conventional buck converter with 50% duty ratio) that there is a phase difference between the line voltage and current waveforms. In addition, the THD analysis of the line current yields to higher order harmonics being injected into the mains current for both cases, which exceed the maximum allowable rate according to IEEE519 [21]. Conversely, the charging operation by the proposed method presents an improved result where mains line voltage and current

waveforms remain almost in the same phase and the line current THD is 5%, which is within the allowable range according to IEEE519 [21].

Figure 7 presents the power factor, THD and system efficiency values for the three battery charger topologies operated at different charging currents ranging from 5 A to 30 A. Figure 7(a) presents that the power factor remains steady (0.98) while charging batteries by the proposed method for different charging currents; whereas, for the other two cases, the power factor curve falls rapidly as charging current increases. Figure 7(b) presents a THD analysis for different rates of charging current. In case of the proposed charging method, the THD rate remains within the permitted limit when the charging current exceeds 20 A. On the other hand, for the other two charging methods, the THD rate always exceeds the maximum IEEE519 permitted value for high charging currents. In case of system efficiency analysis, Figure 7(c) presents a maximum efficiency of 98% for the proposed method and this efficiency is maintained for all charging currents. For conventional buck converter with fixed 50% duty cycle, the efficiency is slightly lower at 92% and it remains steady for all charging currents. On the other hand, for the conventional simple charger, the efficiency decreases as the charging current increases, with the highest efficiency of 94% at 5 A charging current, but the efficiency falls below 90% after 15 A. Among all of the mentioned topologies of battery charger, the proposed charging method produces the most satisfactory outcomes in simulations.
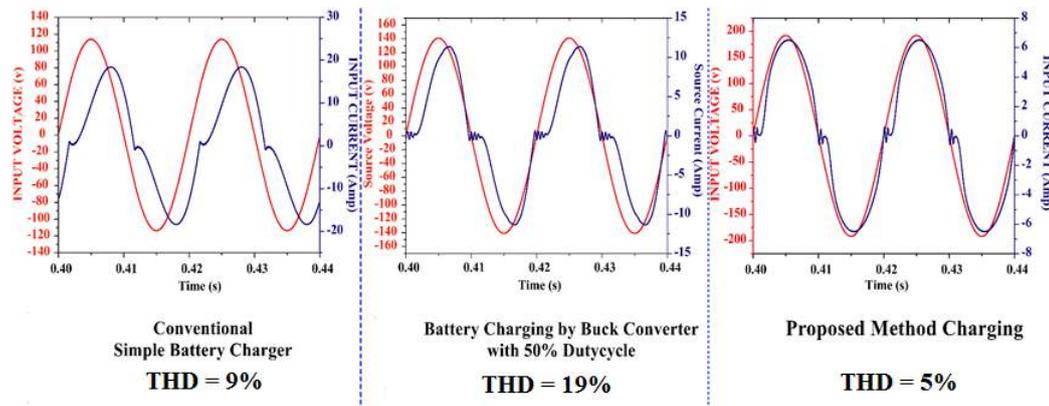
Figure 6. Mains line voltage and current waveforms along with mains line current THD values for different charging methods at 20 A charging current
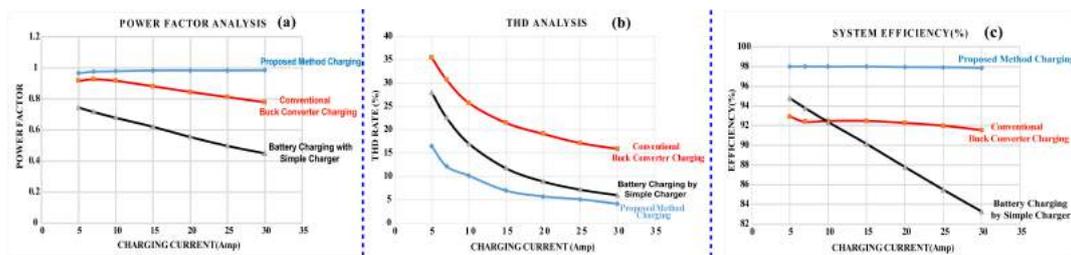
Figure 7. Graphical representation of the analysis of (a) power factor (b) THD (c) system efficiency of the different battery charger topologies

5.   LABORATORY PROTOTYPE

In order to experimentally verify efficacy of the proposed charging method, a prototype hardware is developed as presented in Figure 8. Figure 9 presents the overall experimental setup for charging the EV battery bank. For comparative analysis, all the three charging topologies are developed and tested in the laboratory. PIC18F4431 micro-controller is used as the controller of PFC operation. It receives the mains rectified pulsating dc signal from a 6-0-6 V step-down transformer and based on this information it processes the duty ratio of the generated ISPWM signals. These ISPWM signals are then sent to the IGBT (IRG4PC40UD) for switching applications via IGBT driver unit (IR2104).
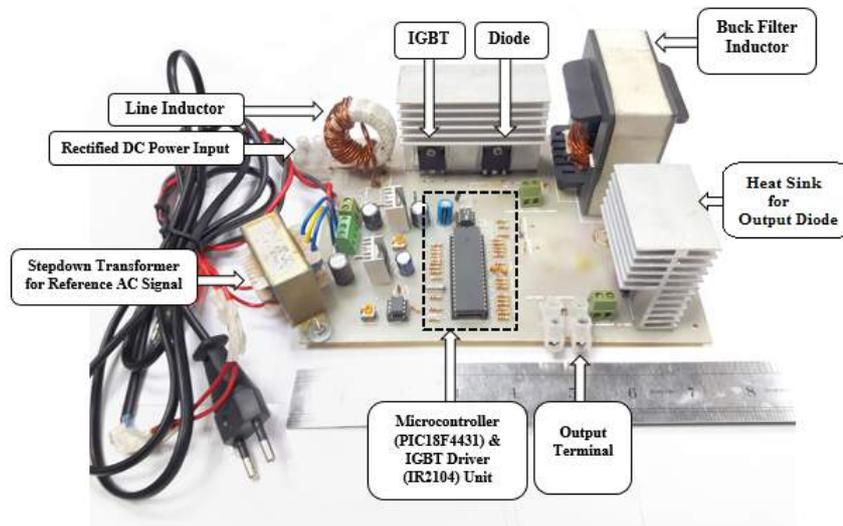
Figure 8. Experimental prototype of the proposed charger
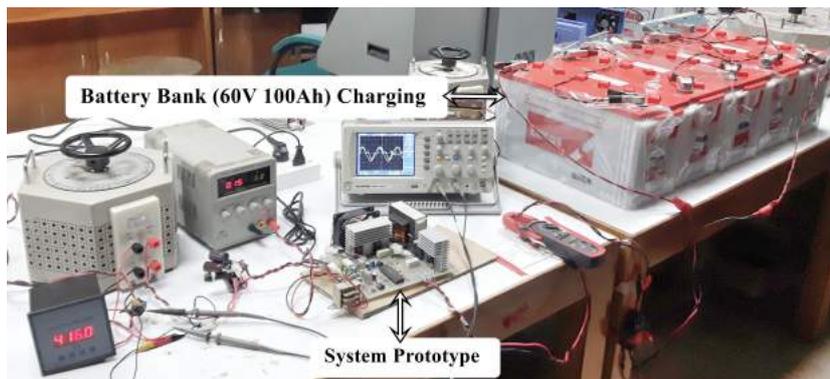
Figure 9. Experimental setup of the battery charging system

6. LABORATORY RESULTS & ANALYSIS

This section describes the experimental outcomes of the developed prototype on the basis of switching ISPWM signal generation, and sending-end power factor, system efficiency, line current THD and Fourier transform evaluations for different types of battery chargers.

6.1. ISPWM signal generation

The switching ISPWM signal is generated according to the amplitude of the rectified pulsating dc signal and Figure 10 presents the generated ISPWM signals. Figure 10(b) and Figure 10(c) present that the generation of the smallest width ISPWM pulses occurs when the amplitude of the pulsating dc signal is the largest, and the largest width ISPWM pulses occur when the amplitude of the pulsating dc signal is the smallest. Since the frequency of the mains ac signal is 50 Hz and the developed switching frequency is 20 kHz, 400 samples of the full wave rectified output are taken to generate the ISPWM pulses. The width of the ISPWM signals is determined by the difference between the largest width duty ratio value and the analog-to-digital conversion (ADC) value of the input rectified analog signal. To avoid the short circuit and open circuit conditions between collector and emitter of the IGBT, critical switching condition is also taken into consideration by limiting the switching ranges. The developed algorithm for ISPWM signal generation is presented in Algorithm 1.
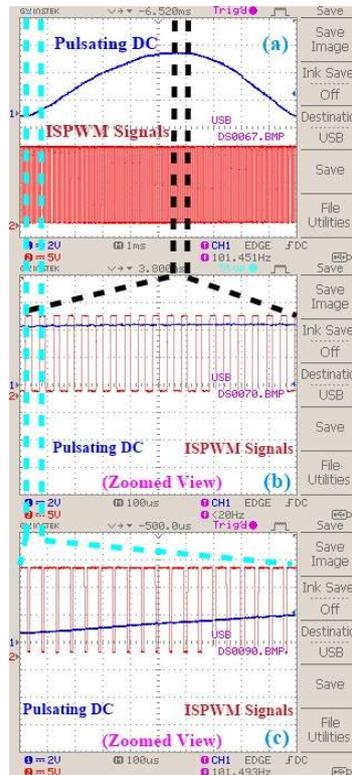
Figure 10. (a) ISPWM signal generation (b) smallest width ISPWM signals (zoom-in view) (c) largest width ISPWM signals (zoom-in view)

Algorithm 1 ISPWM Signal Generation

1: **Variable Declaration:**
2: $X[400] \leftarrow$ grid's rectified analog signal
3: $ADC_{in}[400] \leftarrow X[400]$
4: $ADC_{out}[400] \leftarrow ADC_{In}[400]$
5: $F \leftarrow$ ISPWM switching frequency (kHz)
6: $Y[400] \leftarrow ADC_{out}[400]$
7: $D_{in}[400] \leftarrow Y[400]$
8: $D_{out}[400] \rightarrow$ duty ratio (%) of ISPWM signal based on ADC value
9: $i \rightarrow$ index variable.
10: $M \rightarrow$ highest width duty ratio value for switching
11: $S \rightarrow$ switch state variable; $S = 0$ is OFF state and $S = 1$ is ON state.
12: **Initialization:**
13: $i \leftarrow 1$
14: $X[400] \leftarrow 0$
15: $ADC_{out}[400] \leftarrow 0$
16: $Y[400] \leftarrow 0$
17: $D_{in}[400] \leftarrow 0$
18: $D_{out}[400] \leftarrow 0$
19: $F \leftarrow 20$
20: $S \leftarrow 1$
21: **Start:**
22: Read value of $X[400]$
23: **for** $(i = 1; i \leq 400; i = i + 1)$ **do**
24:     $ADC_{in}[i] \leftarrow X[i]$
25:     $ADC_{out}[i] \leftarrow ADC_{in}[i]$
26:     $Y[i] \leftarrow ADC_{out}[i]$
27:     $D_{in}[i] \leftarrow Y[i]$
28:     $D_{out}[i] \rightarrow M - D_{in}[i]$
29: **end for**
30: **Goto Start**

6.2. Analysis of power factor for different battery charging methods

The proposed battery charging system is assessed in accordance with several performance parameters like power factor analysis, efficiency calculation, Fourier transform analysis and THD evaluation for different charging topologies. The three charging structures are interchangeably executed on the laboratory prototypes to analyze the practical performance characteristics for each case. The practical implementations of the proposed and the previously reported charging systems enable this paper to present a substantial comparison between each other.

The experimental line voltage and current waveforms while charging the battery bank at 7 A by the simple battery charger, conventional buck converter and the proposed charging configuration are presented in details in Figure 11. Power factor is calculated as a ratio of the real power (watts) to the apparent power (VA). The voltage is measured directly in the digital oscilloscope (GDS-1102-U), while the current sensor (TA1309-100) is used to observe the shape of the line current. Table 2 compares the power factor for the three chargers for both simulations and experimental evaluations. It can be noticed that although the experimental results are not as good as the simulation results, the pattern of the outcomes are the same with the proposed charger having the best performance, and the conventional simple charger showing the worst performance.
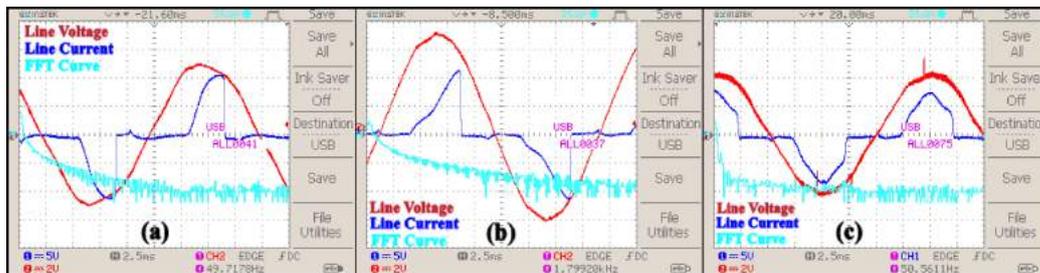
Figure 11. Mains line voltage and current waveforms while charging battery bank at 7 A by (a) simple battery charger (b) buck converter with 50% duty ratio and (c) the proposed charger

Table 2. Power factor (PF) comparison among the investigated charging methods for 7 A output

Charging Methods	Simulated PF	Experimental PF	% Difference Between Simulation & Practical Outcome
Simple Charger	0.72	0.68	4%
Buck Converter (50% duty ratio PWM)	0.87	0.78	9%
Proposed Charging Method	0.98	0.89	9%

6.3. Analysis of system efficiency for different battery charging methods

The grid-tied EV charging system is practically tested for power loss determination in case of different charging methodologies. The hardware prototype consists of a single phase variable ac transformer attached to the mains line, with a maximum power rating of 3 kVA. In each case, the battery charging current is kept constant at 7 A. Table 3 enlists the determined input and output voltage and current values, along with the simulation and experiment based system efficiencies for three different charging topologies. Again it is found that the experimental results mimic the simulation results with the proposed charger presenting the best performance and the conventional buck charger having the worst performance.

Table 3. Power efficiency comparison among the investigated charging methods for 7 A output

Charging Methods	Charging Voltage	Input Power (Watt)	Experimental Power Efficiency	Simulated Power Efficiency
Simple Charger	$V_{out} = 66.1$ V	579	80.9%	91%
Buck Converter (50% duty ratio PWM)	$V_{out} = 72$ V	651	80.4%	89%
Proposed Charging Method	$V_{out} = 74$ V	588	88.1%	98%

6.4. Analysis of THD for different battery charging methods

The mains line current THD is calculated by analyzing the raw data of current waveforms collected during the experiments by the oscilloscope in MATLAB software. The THD is calculated as the ratio of the equivalent root mean square (rms) value of the signal of all the harmonic frequencies (from the 2nd harmonic onwards) over the rms of the fundamental frequency (50 Hz) component. Table 4 presents the difference between the simulated and experimental outcomes for THD analysis with 7 A charging current. In both cases, the proposed method shows the best performance, while the conventional simple charger shows the worst performance experimentally and the conventional buck charger presents the worst performance in simulation.

Table 4. Mains line current THD comparison among the investigated charging methods for 7 A output

Charging Methods	Simulated THD	Experimental THD	% Difference Between Simulation & Practical Outcome
Simple Charger	0.23	0.35	12%
Buck Converter (50% duty ratio PWM)	0.31	0.45	14%
Proposed Charging Method	0.12	0.23	11%

6.5. Analysis of discrete fourier transform for different battery charging methods

Discrete Fourier Transform (DFT) analysis is conducted by investigating the raw data of current waveforms collected during the experiments by the oscilloscope in MATLAB software. The traditional DFT algorithm, which is a Fast Fourier Transform (FFT), is used with a Hanning window. Figure 12 shows that the proposed charger produces the best performance with peaks at the fundamental frequency and at the 3rd harmonic, while the conventional buck charger has peaks till the 11th harmonic and the conventional simple charger has peaks till the 17th harmonic.
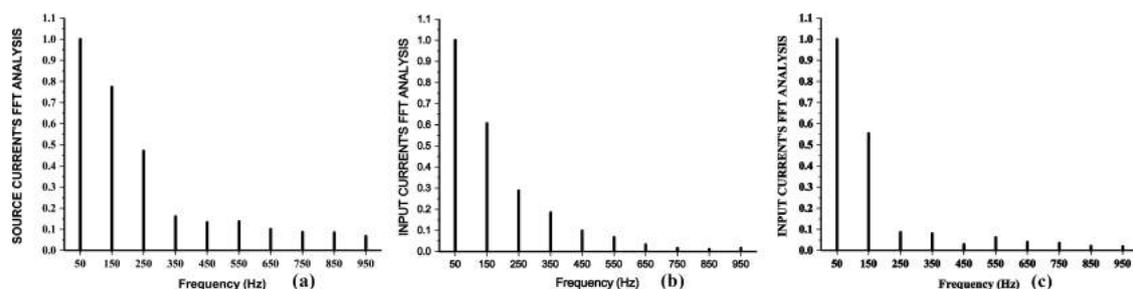
Figure 12. FFT analysis of the mains line current while charging battery bank at 7 A by (a) simple battery charger (b) conventional buck converter and (c) the proposed charger

7. CONCLUSION

In this paper, a detailed description of ISPWM switched buck converter as a power factor correction unit for EVs' battery charging applications is presented. A direct comparison of the proposed charging technique with the conventional and previously applied battery charging methods is evaluated for the same charging current. The simulated results and experimental findings suggest that although the experimental results are not as good and satisfactory as the simulation results, however, comparison within the different charging methodologies shows that the proposed system produces much better performance in all three categories - sending-end power factor, system efficiency and mains line current THD. Additionally, the proposed system shows the least variation between simulation and experimental results yielding to a sustainable charging system.

8. ACKNOWLEDGMENT

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