High Speed Power Efficient CMOS Inverter Based Current Comparator in UMC 90 nm Technology

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Article Info	ABSTRACT
	A novel power-speed efficient current comparator is proposed in this paper. It comprises of only CMOS inverters in its structure, employing a simple biasing method. The structure offers simplicity of design. It posesses the very desirable features of high speed and low power dissipation, making this structure a highly desirable one for various current mode applications. The simulations have been performed using UMC 90 nm CMOS technology and the results demonstrate the propagation delay of about 3.1 ns and the average power consumption of 24.3 µW for 300 nA input current at supply voltage of 1V.

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1.   INTRODUCTION

Current mode signal processing in CMOS technology has received great interest in the past few decades [1]-[9]. Of numerous current mode building blocks that exist, a current comparator is one fundamental block that finds usage in various applications such as temperature sensors, photo-sensors, current Schmitt Triggers, current-mode Analog to Digital converters, oscillators, current to frequency converters, neural networks, function generators etc. [10]-[20]

For an efficient current comparator, the most important requirement is a fast time response followed by its accuracy. Numerous architectures of current comparators have been put forth in the literature but the earliest known true CMOS current comparator was proposed by Frietas and Current in [20]. This structure was based on the use of a simple current mirror for current comparison purpose. However, it was limited by its speed of operation. To improve upon this limitation, the current comparators using a nonlinear positive feedback were proposed in [22]-[23]. In [22] the first true low input impedance current comparator was proposed. This circuit used a source follower input stage to obtain low input resistancebut it suffers from longer response time for low input currents, which limits its performance. [23] Proposed two CMOS current comparator structures to obtain better resolution and offset than that attained with [22]. One of these structures utilizes current switching as in [22] to obtain a linear transient evolution dominated by a Miller capacitance. Second structure, the current steering comparator an alternate principle to reduce Miller effect exhibits better transient response along with high-resolution. But the positive feedback applied at the input led to a lower sensitivity which, in turn, lowered the speed for low input levels. Various structures subsequently were proposed in [24]-[30] to over come the limitations posed by the previous structures, each having its own respective merits and demerits. In [24], the structure of [22] has been modified to include

class AB operation in order to reduce the voltage swing, thus resulting in greater speed at small input currents. The structure proposed in [25] is a modification of [22] to obtain a fast response time along with low input impedance by appending two inverters to the structure of [22]. Further, in [26] the structure of [22] has been modified for reducing delay times. It employs diode-connected NMOS and PMOS transistors that restrict the input transistors from entering deep subthreshold region of operation. Since this structure requires two wide width diode-connected transistors stacked together, hence it leads to the complication in the circuit topology.

Many structure employ feedback mechanism in order to reduce in put resistance, thereby increasing the speed. Such structures have been reported in [27]-[30]. [27] Employs a resistive feedback network in a current-source inverting amplifier at input stage of [22] in order to reduce the input resistance. This leads to a high speed current comparator that offers low input resistance for increased input current sinking and sourcing capabilities. [28] Proposes a continuous-time current comparator to achieve short response delay time, low power consumption, small area and process robustness. It employs a CMOS complementary amplifier two resistive-load amplifiers and two CMOS inverters. A transistor working in linear region serves as the negative feedback resistor of the CMOS complementary amplifier. The structure offers low input and output impedance, owing to the resistive feedback. These low input and output resistances decrease the voltage swings thereby reducing the response time of the circuit. [29] Employs a feedback system to the input stage of [22] that allows high-speed operation at low currents and also consumes lesser power than [22]. The current comparator in [30] is developed by applying positive feedback concept around an active block namely CC-II and gives a high speed response.

Further, [31]-[34] employ various biasing techniques to reduce input impedance and hence achieve higher speeds of operation while maintaining lower power consumption. Specifically, simple biasing method is used in [31] and [33] whereas [32] uses negative feedback scheme at the transimpedance stage with an aim to achieve a very large loop-gain while maintaining the transformed voltage signal gain at the lowest swing in order to achieve speed

The quest to develop more efficient structures that meet the criteria of high speed and accuracy along with additional features such as low power dissipation is on-going. Authors have also proposed two such structures in [34]-[35]. In [34], a current comparator comprising a current difference stage, a gain stage with non linear feedback and an output stage has been proposed. It uses a current mirror structure as a current difference stage and a CMOS inverter is used as the output stage for rail to rail swing. Further, in [35] a low power, high speed and high resolution current comparator has been proposed as an improvement upon [22] wherein the gain stage has been modified leading to a significant improvement in the delay.

In this paper, we have proposed a high speed, low power current comparator structure eploying only CMOS inverters as the basic building blocks. A CMOS inverter is a fundamental block in the digital integrated circuit design techniques. It finds wide usage in implementation of various structures as reported in [36]-[40], that are made exclusively out of CMOS inverters thus offering symmetry of structure, endowed with all qualities of the CMOS inverter. The current comparator proposed in this work has highly desirable features of speed and power efficiency with ease of operation using UMC 90 nm CMOS technology.

2.   PROPOSED CURRENT COMPARATOR

The proposed high speed and low power consumption current comparator design based on conventional CMOS inverter is shown in Figure 1. The architecture consists of three stages of CMOS inverters: a bias stage (A_1), an input stage (A_2) which accepts the input current pulse and translates it into corresponding voltage level and an output stage (A_3) to obtain a full swing output.
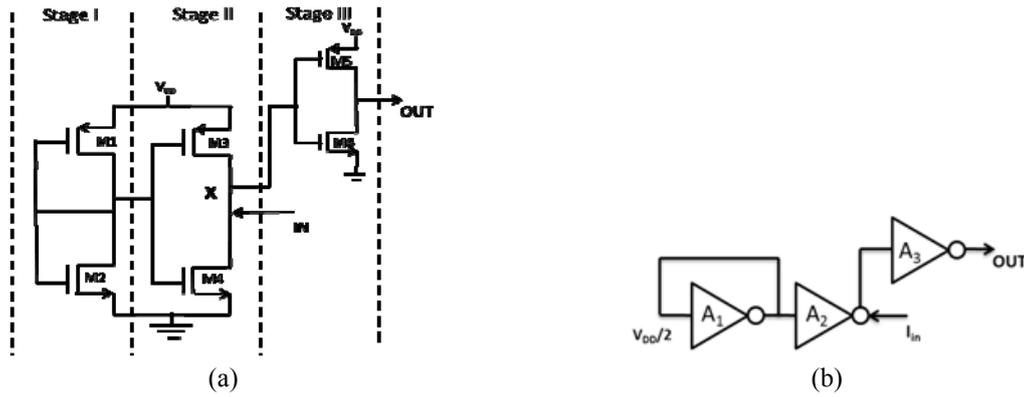
Figure 1. Proposed CMOS inverter Based Current Comparator Structure (a) transistor configuration, (b) equivalent symbol representation

The operational concept of proposed current comparator design can be elucidated as follows. A_1 comprises of a shorted gate drain CMOS inverter (M_1-M_2). The primary function of this stage is to provide a constant voltage bias of about $V_{DD}/2$ to the input stage A_2. Around this common mode voltage of $V_{DD}/2$, the voltage signal swing at X can be maintained as small as possible and situated exactly around the inverter threshold voltage of A_2. This ensures a very high speed operation of the current comparator. The transistor lengths and widths ratios W_1/L_1 and W_2/L_2 of A_1 are set in order to obtain the required bias. This can be verified by equating the saturation drain current equation of PMOS and NMOS since both M_1 and M_2 being diode connected MOSFETs will operate in the saturation region of operation.

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{gs}-V_{tn}\right)^2 \left(1+\lambda V_{ds}\right) = \mu_p C_{ox}\left(\frac{W}{L}\right)_1 \left(V_{sg}-V_{tp}\right)^2 \left(1+\lambda V_{sd}\right) \tag{1}$$

$$\frac{\left(\dfrac{W}{L}\right)_1}{\left(\dfrac{W}{L}\right)_2} = \frac{\mu_n C_{ox}\left(V_{gs}-V_{tn}\right)^2\left(1+\lambda V_{ds}\right)}{\mu_p C_{ox}\left(V_{sg}-V_{tp}\right)^2\left(1+\lambda V_{sd}\right)} \tag{2}$$

For small channel lengths, λ (channel modulation coefficient) cannot be ignored. Hence, by fixing the channel length and substituting the typical values of technology dependent parameters like λ, Vt and k'(μC_{ox}), the aspect ratios of two devices can be calculated using eq (1) and (2). The input stage A_2 also serving as the transimpedance stage consists of M_3-M_4. In this novel approach, the input current Iin which is the difference of signal and reference current is injected into the drain terminal of input stage. A corresponding voltage level with respect to the input current pulse is generated at node X. Essentially; this voltage level appearing at X is a potential drop across $r_{o3} \parallel r_{o4}$ where r_{o3} and r_{o4} are output resistances of M3 and M4 respectively. This is also a measure of net transimpedance in the circuit. Note that an output resistance r_{oi} is approximately inversely proportional to the drain current I_{di}, i.e. $r_{oi} = 1/(\lambda I_{di})$ in saturation region of operation. The key point here is that the I_{in} should vary the voltage at X by a small amount only which can be sensed by the output stage. This ensures the high speed operation of the comparator circuit. Dimensions of M_3-M_4 are chosen taking into consideration the inverse relationship between the drain current and r_{oi} to ensure a large sensitivity of V_x with respect to I_{in}. Thus, even a small input signal will cause large variations in the potential at node X. At the same time, the absence of any input signal will cause the potential at X to drop, thereby resulting in a low voltage level at X. Non-idealities in the form of finite input impedance of output stage will affect the performance of the circuit.

The voltage generated at node X feeds the transistors of output stage (M_5-M_6). The transistor pair (M_5-M_6) senses the distinctions applied in the form of gate voltage and outputs high or low voltage as logic '1' or logic '0'. This inverter (A_3) produces full swing output without degrading the speed of the circuit.

3.   RESULTS AND ANALYSIS

The proposed current comparator topology based on CMOS inverters have been designed using 90 nm CMOS technology parameters and Analog Virtuoso Environment of the Cadence Software. The sizes of the transistors are listed in Table 1. The simulations are performed at a supply voltage (V_{DD}) of 1 V. The input current varying between 0 and 300 nA is injected and compared. Figure 2 illustrates the transient input–output characteristics of the proposed current comparator along with the instantaneous power dissipation of the structure. A short average propagation delay of 3.1 nsec is observed at the specified input current, reinstating the operating frequency range of circuit between 200 MHz- 400 MHz.

Table 1. Transistor Sizes

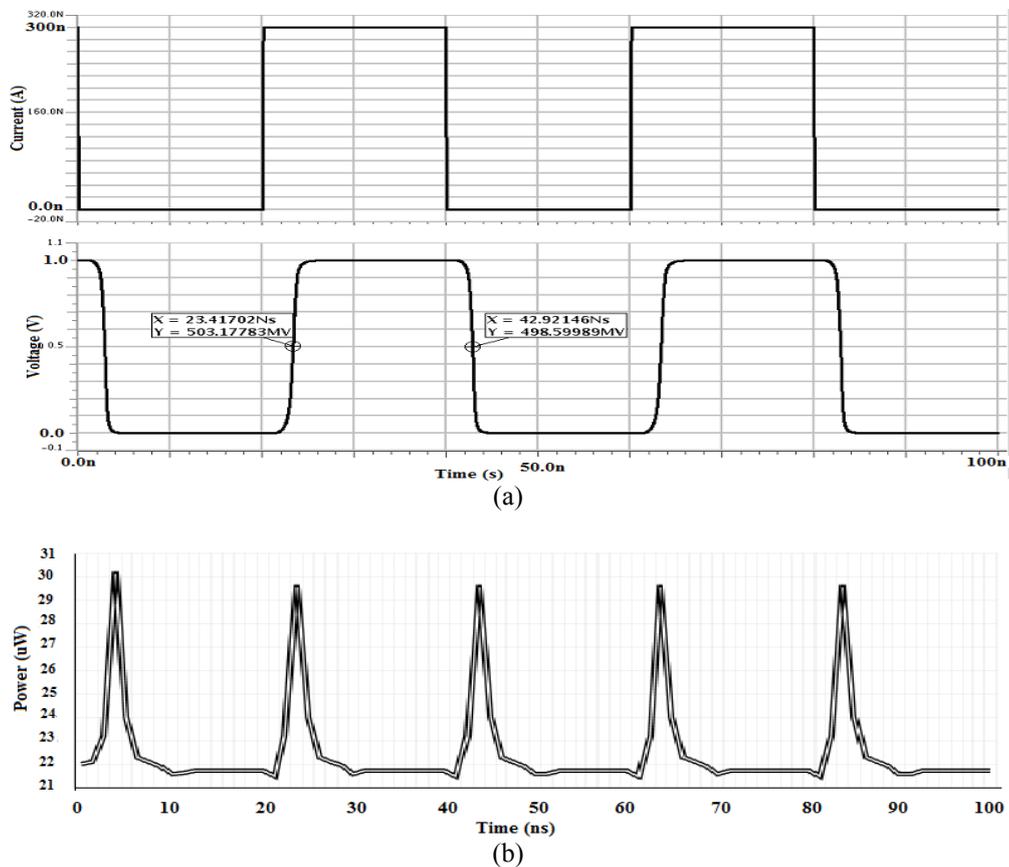|	W	L
M1	1.32μ	0.18μ
M2	0.2μ	0.18μ
M3	4.5μ	1.0μ
M4	1.5μ	2.0μ
M5	1.32μ	0.18μ
M6	0.2μ	0.18μ

(a)

(b)

Figure 2. Transient Response showing (a) Input Current and Output Voltage and (b) Instantaneous Power Dissipation of the proposed structure when Iin = 300 nA.
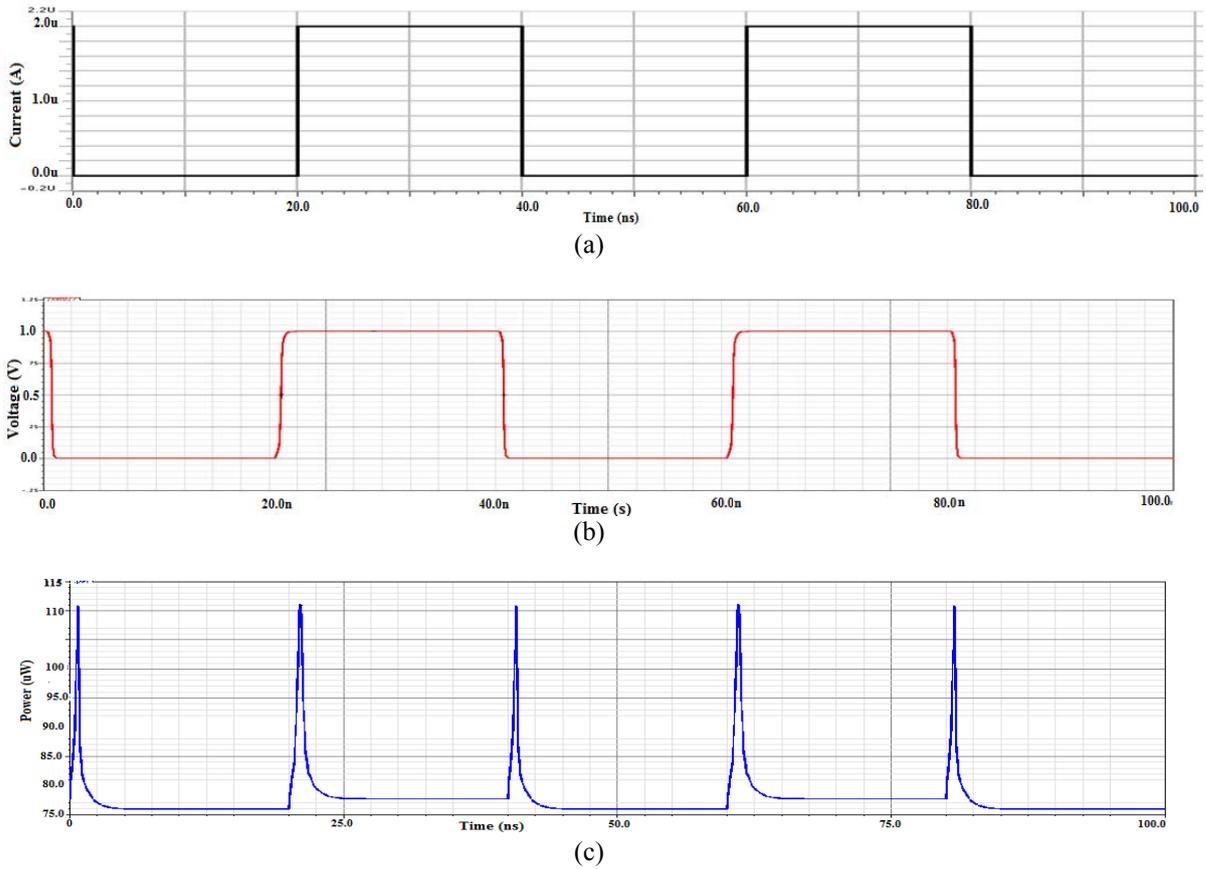
(a)

(b)

(c)

Figure 3. Transient Response showing (a) Input Current, (b) Output Voltage and (c) Instantaneous Power Dissipation of the proposed structure when Iin = 2 µA.

Power dissipation for various input currents is one of the characteristics of this circuit. The instantaneous power dissipation of the circuit is shown in Figure 2(b). Based upon this characteristic, the average power dissipation is calculated to be 24.3 µW at 1 V for 300 nA input current. To exhibit the performance of the circuit at current greater than, 1 µA, the circuit performance is evaluated at 2 µA and the same is depicted in Figure 3. The simulation results show that a six fold increase in current doesn't escalates the power consumption of the circuit by the same amount. Besides, the propagation delay reduces substantially for currents greater than 1 µA thereby increasing the speed of comparator considerably.

The average propagation delay of the circuit, under different input currents are presented in Figure 4(a) and the variation of average propagation delay with supply voltage has been illustrated in Figure 4(b). As expected, the delay decreases as the supply voltage increases because of increase in drain current.
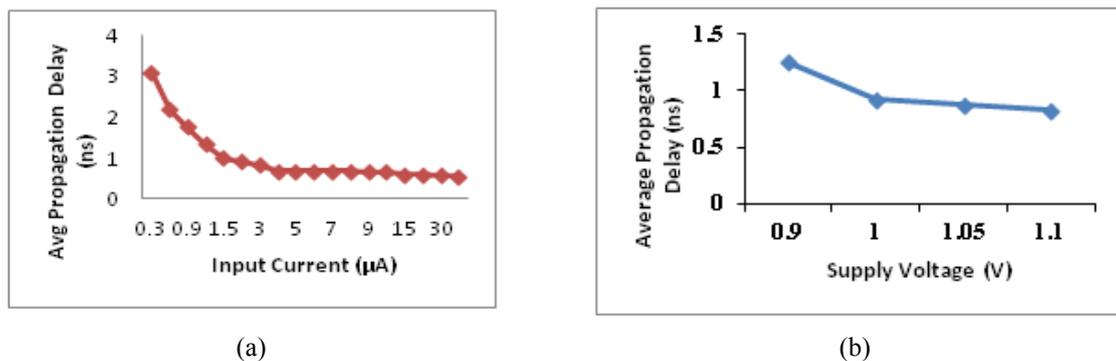

(a)

(b)

Figure 4. Propagation Delay vs. (a) Input Current and (b) Supply Voltage

Temperature variations and Process parameters have significant impact on the performance of CMOS circuits. To illustrate the robustness of proposed architecture, average propagation delay and power dissipation have been calculated for various values of temperature ranging from as low as -5°C to as high as 150°C. From Figure 6(a), as temperature increases from -5°C to around room temperature the delay decreases and then delay increases almost linearly with temperature due to decrease in drain current. Similar temperature variations have been simulated for power dissipation of proposed current comparator (Figure 6 (b)). In these simulations both maximum and minimum values of power have been illustrated. The noteworthy aspect of the power model is that even with large variations in temperature (-5°C to 150°C), the power dissipation remains almost constant. Furthermore, the difference between maximum and minimum propagation delay is not more than 2 ns.
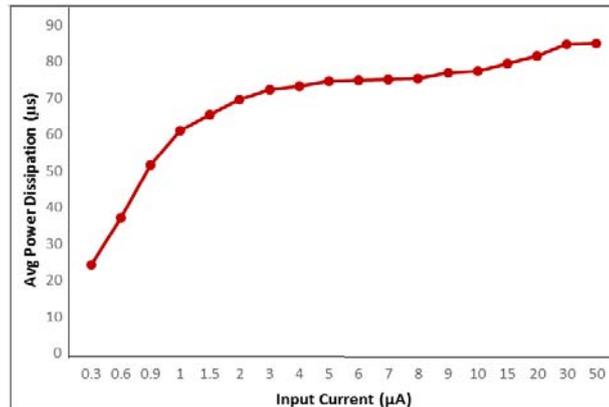

Figure 5. Average Power Dissipation vs. Input Current
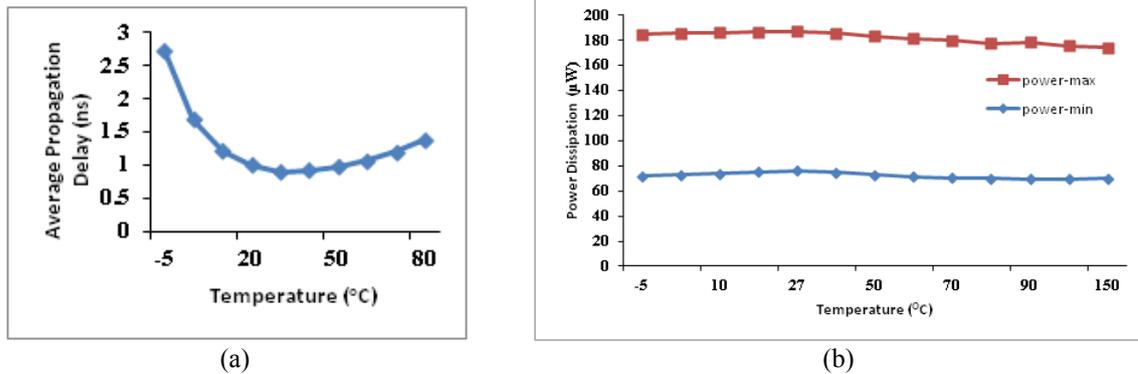

| (a) | (b) |

Figure 6. (a) Average Propagation Delay vs. Temperature, (b) Power Dissipation vs. Temperature

Figure 7 illustrates the variation of output voltage with temperature in a much eloquent manner.
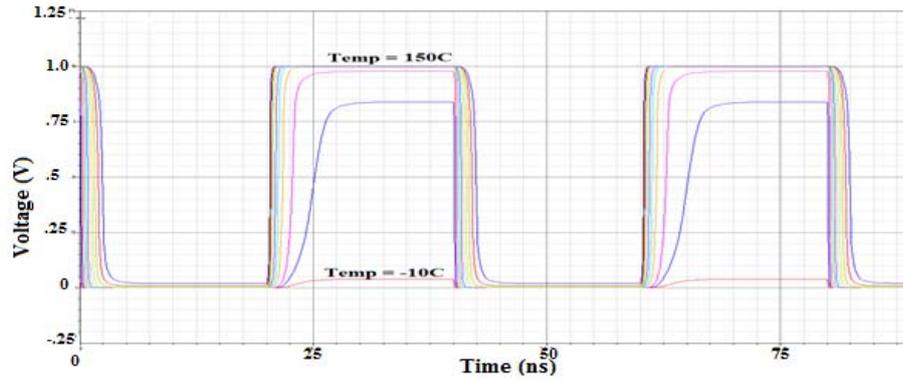
Figure 7. Transient Response of the Output Voltage of Proposed Current Comparator for varying Temperature

To further exemplify the functionality of circuit, the proposed design has been simulated for all the process corners as shown in Figure 8.
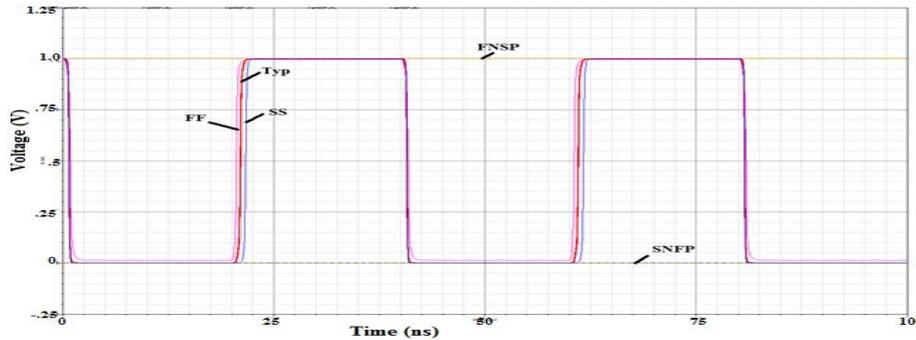

Figure 8. Transient Response of the Output Voltage of Proposed Current Comparator at various Process Corners

The structure proposed in [22] is one of the pioneering works in terms of the design of a current comparator. [23]-[30] have reported various current comparators that are a modification of [22]. Of all these, [24] gives the highest speed and lowest power dissipation. Hence, a comparison of the performance parameters of the proposed current comparator to those reported in [22] and [24] has been drawn and same has been reported in Table 2. It can be seen that the proposed structure offers fastest response and reasonably low power dissipation at the lowest supply voltage of 1V with a much lower input current. Figure 9 illustrates the output response of [22] while that of [24] has been illustrated in Figure10.
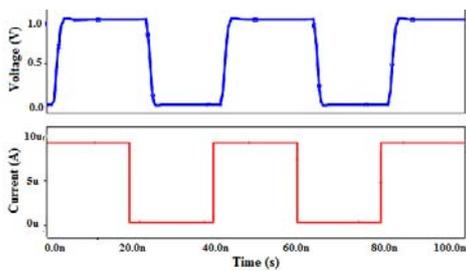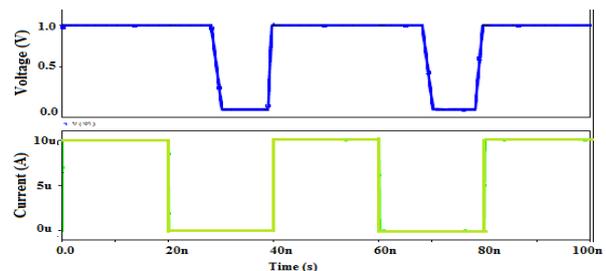

Figure 9. Output response of [22]

Figure10. Output response of [24]

Table 2. Comparison of Proposed Current Comparator with Popular Architectures [22] and [24]

	Process	Supply Voltage (V)	Minimum Input Current	Avg Propagation Delay(ns)	Power Dissipation (μW)	Power-Delay Product (fJ)	No. of Transistors
Traff [21]	90 nm	1	5 μA	3.35	120.2	112.57	4
Tang[23]	90 nm	1	10 μA	4.6	112.57	517.8	14
Proposed	90 nm	1	300 nA	3.1	24.3	93	6

4. CONCLUSION

A fast and power efficient current comparator has been reported comprising solely of CMOS inverters, thus offering symmetry of structure. The proposed current comparator provides a commendable performance in comparison to the other popularly used current comparators as reported in the literature. The proposed structure has been simulated on 90 nm technology and operates at a supply voltage of 1V.

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