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A Novel Low Noise High Gain CMOS Instrumentation Amplifier for Biomedical Applications

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ABSTRACT

This work describes a novel technique of designing a low noise high gain CMOS instrumentation amplifier for biomedical applications. A three op-amp instrumentation amplifier have been designed by employing two simple op-amps at the two inputs and a folded cascode op-amp at the output. Both input and output stage op-amps are 2-stage. Most of the earlier designed op-amp in literature uses same type of op-amp at the input and output stages of instrumentation amplifier. By using folded cascode two stage op-amp at the output, we have achieved significant improvement in gain and CMRR. Transistors sizing plays a vital role in achieving high gain and CMRR. To achieve a desirable gain, common mode rejection ratio and other performance metrics, selection of most appropriate op-amp circuit topologies & optimum transistor sizing was the main criteria for design of instrumentation amplifier for biomedical applications. The instrumentation amplifier is simulated using Cadence Spectre tool and layout is designed in Cadence Layout editor at 0.18µm CMOS technology. Each of the input op-amp provides a gain and CMRR of 45dB and 72dB respectively. The output stage folded cascode amplifier provides a gain of 82dB and a CMRR of 92dB. The design achieves an overall gain and CMRR of 67dB and 92db respectively. The designed instrumentation amplifier consumes only 263µW of power suitable for biomedical signal processing applications.

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1. INTRODUCTION

Biomedical signal processing aims at fetching useful information from biomedical signals. Earlier the primary focus was on processing the biomedical signal to extract the original signal and remove noise. Detecting biomedical signals is a very challenging task as these signals normally consists of very weak amplitude in the order of few mV with almost equivalent noise signal levels. These signals also have a very low frequency range usually below 1KHZ. With the growth of microelectronics and embedded design more and more applications require very weak amplitude signal detection and measurement. These weak amplitude biomedical signals need to be suitably amplified along with rejection of noise. To overcome this problem instrumentation amplifiers are used to suppress any unwanted noise or the common mode signals that affects the original signal and also provide proper amplification to the desired signal. Due to this property of rejecting common mode noise and providing amplification, instrumentation amplifier is widely used in various applications like transducers, micro-electro mechanical systems and biomedical applications. Unlike op-amp, instrumentation amplifier is a closed loop gain block that has a differential block with two opposite inputs and a single ended output. The impedances of the two input terminals are balanced and have high values typically 10^9 ohm or greater. The major achievements of designed instrumentation amplifier as compared to the previous similar works in literature are increment of 22.7db gain, and low noise due to the

addition of folded cascode stage at the output. Section II explains the proposed CMOS instrumentation amplifier design. Section III discusses the simulation results and comparison while Section IV describes the conclusion.

2. PROPOSED INSTRUMENTATION AMPLIFIER CIRCUIT DESIGN

One of the main concerns while designing an instrumentation amplifier is the interferences generated in the form of common mode voltages [5]. To reduce these interferences and to improve the gain, we have designed a conventional three stage instrumentation amplifier by employing two simple op-amps at the input stage and a folded cascode op-amp at the output stage. Figure 1. shows the proposed design with symbols 1 and 2 showing the simple two stage op-amps and symbol 3 showing two stage folded cascode op-amp.

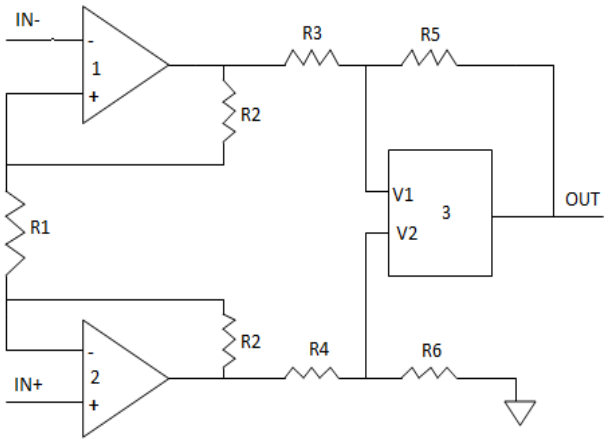

Figure 1. Instrumentation Amplifier

The advantages of three op-amp type of configuration are high gain, High Common Mode Rejection Ratio and easy gain control by changing value of only single resistance. A major drawback of this instrumentation amplifier is its larger chip area due to the use of different resistances. So, we have drawn layout of instrumentation amplifier with both on-chip and off-chip resistors.

The op-amp blocks 1 & 2 shown in Fig.1 are connected in non-inverting configuration. The complete circuit of simple two stage op-amp [4] is shown in figure 2. Input stage comprises of a differential pair MN1 & MN2 and a current mirror load MP1 &MP2. The output stage comprises of transistors MP3 & MN5. Transistors MN3 & MN4 form the current sink for proper biasing of the circuit.

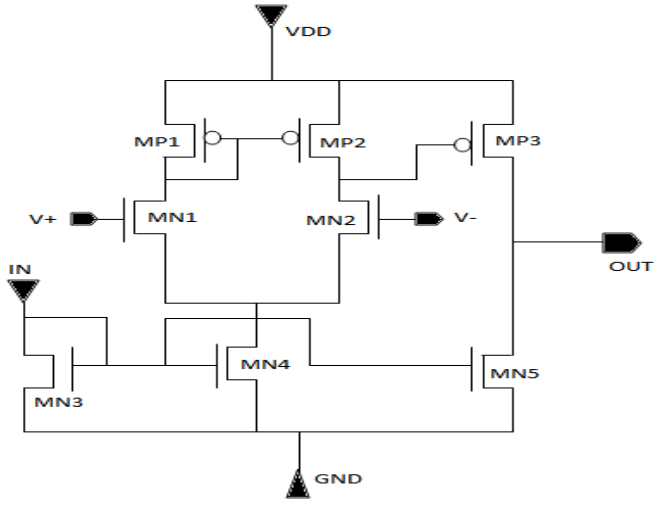

Figure 2. Two Stage CMOS OP-AMP

For calculating the aspect ratio of various transistors $\frac{G_m}{I_d}$ methodology [3] is widely used for transistor sizing of the analog circuits. Apart from calculation of transistor sizing, $\frac{G_m}{I_d}$ methodology also helps in identifying device operating region. The mode of operation can be found according to the following equation

$$\frac{G_m}{I_d} = \frac{1}{I_d} * \frac{\partial I_d}{\partial V_g} = \partial (\ln I_d / \partial V_g) = \frac{\partial \left(ln \left(\frac{I_d}{\frac{W}{L}} \right) \right)}{V_g} \quad (1)$$

The $\frac{G_m}{I_d}$ ratio decreases as the operating point moves toward strong inversion. The main focus is on transistor sizing of differential pair MN1 & MN2 which senses the difference between the two input voltages. Biasing current to the differential pair is calculated by the transistors MN3 and MN4. Output current can be calculated by using the relation 2.

$$I' = I_d /W/L \quad (2)$$

Where I' represents the total output current, I_d is the drain current and W/L is the aspect ratio of the transistor. The Table 1 shows optimum calculated aspect ratios of various transistor of a two stage CMOS op-amps used in blocks 1 & 2 respectively.

Table 1. Input stage op-amp 1 & 2 transistor sizing

TRANSISTORS	ASPECT RATIO (W/L)
MN1, MN2	3µ/1µ
MN3	9µ/1µ
MN5	10µ/1µ
MN4	4.5µ/1µ
MP1, MP2	15µ/1µ
MP3	30µ/1µ

To enhance the gain of instrumentation amplifier, we have added the folded cascode stage [9] at the output as block 3 shown in Figure 3. The folded cascode op-amp circuit is shown in Figure 3.

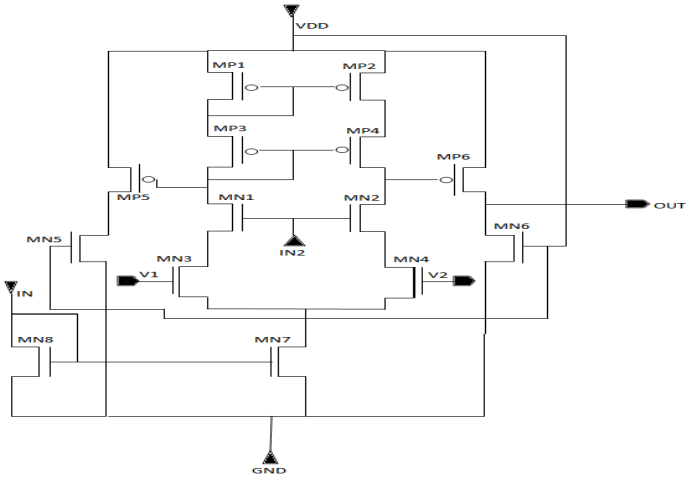

Figure 3. Two Stage Folded Cascode CMOS OP-AMP

The Table 2 shows optimum calculated aspect ratios of various transistor of a two stage folded cascode CMOS op-amp used in block 3.

Table 2. Output Folded Cascode Stage op-amp Transistor Sizing

TRANSISTORS	ASPECT RATIO(W/L)
MN1,NM2	5µ/200n
MN3,MN4	3µ/200n
MN5,MN6	20µ/200n
MP1,MP2	20µ/200n
MP3.PM4	20µ/200n
MP5,MP6	50µ/200n
MN8	5µ/200n
MN7	10µ/200n

As we know the input signal of a common-gate stage may be a current and also that in the common-source arrangement a transistor converts a voltage signal to a current signal. The cascade of a CS stage and a CG stage is called a 'cascode' topology, which provides many useful properties. The main advantage of using the folded cascode at the output is that the gain can be further increased without affecting the output swing. As shown in Fig 3 MN3 and MN4 act as a differential pair used to sense the input voltage difference. Special care has been exercised to operate the input differential pair in the saturation region not in the triode region. The operation in triode region causes non-linerity in the behavior of the folded cascode op-amp as non linear and also results in poor DC gain.

In this proposed instrumentation amplifier we have set the values of the resistances according to gain requirement. For a good common mode rejection ratio and gain proper resistance matching should be done such that R3=R4 and R5=R6. The output voltage of the instrumentation amplifier is given by relation 3.

$$V_0 = -(V_{in+} - V_{in-}) * \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{R_5}{R_4}\right) \quad (3)$$

The two input op amps 1 & 2 are used in buffer configuration so as to provide high input impedance followed by the third folded cascode two stage op-amps is used in differential configuration. The above configuration is capable of amplifying low amplitude signals in the order of few mV to operational range for further processing in several volts. With the use of active impedances not only temperature dependency but also power consumption is greatly reduced. To check the effects of on chip & off-chip resistors on the proposed instrumentation amplifier performance & area, the layouts of the proposed circuit have been generated with both on-chip and off-chip resistors. If on chip resistors are used than a much larger area is consumed by the instrumentation amplifier as very high value resistors are required and the gain is also fixed as the value of the resistors cannot be changed. But with off chip resistors a significant reduction in the area is achieved with benefit of variable gain as it can be adjusted by changing the value of the single resistor R1. The values of the resistors used in instrumentation amplifier are given in Table 3. These values can be adjusted according to the need of the amplification.

Table 3. Resistance Value for IA

Resistors	Resistance Value (Ω)
R1, R2	100, 1K
R3,R4	32K
R5,R6	1K

3. SIMULATION RESULTS

To achieve a desirable gain, common mode rejection ratio and other performance metrics, selection of most appropriate op-amp circuit topologies & optimum transistor sizing was the main criteria for design of low noise high gain CMOS instrumentation amplifier for biomedical applications. Layouts of the proposed instrumentation amplifier with on-chip & off-chip resistors have been generated. The schematic of proposed CMOS instrumentation amplifier is generated in Virtuoso Schematic Editor. Cadence Spectre is used for

circuit simulator using BSIM3v3 models in 180nm CMOS technology. The layouts of proposed CMOS instrumentation amplifier with on-chip resistor and without on-chip resistors are generated in Virtuoso Layout Editor.

Figure 4 and 5 shows gain versus frequency plot in both magnitude and dB of the proposed instrumentation amplifier design. Here we have applied a 5mV amplitude signal at the input. The output AC response has been plotted with frequency range from 10Hz to 100MHz.The fig. 5 shows the obtained gain of 67.7dB, 3-dB bandwidth of 1.1MHz and unity gain frequency of 91.33MHz.

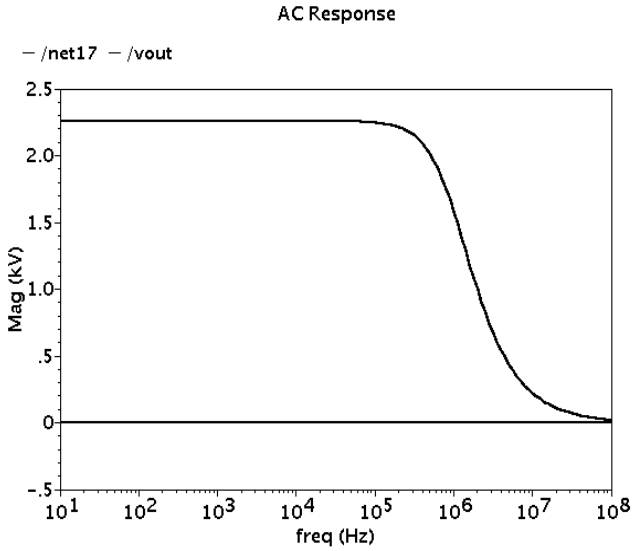

Figure 4. Gain Curve in Magnitude

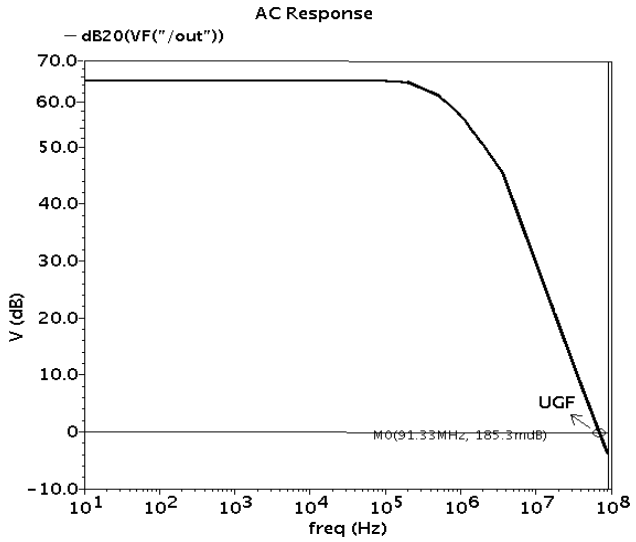

Figure 5. Gain Curve in Decibels

To perform noise analysis, a 50Ω resistor is connected at the output. The input/output referred noise graphs have been plotted in Cadence Spectre simulator. The output referred noise plot in Figure 6 gives a peak value of 1.75 pV/√Hz. Noise analysis has been performed with a 5mV signal applied at the input. The input referred noise plot in Figure 7 gives a peak value of 89nV/√Hz.

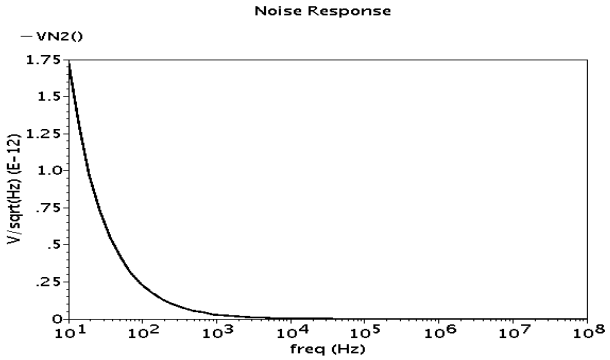

Figure 6. Output Referred Noise Voltage

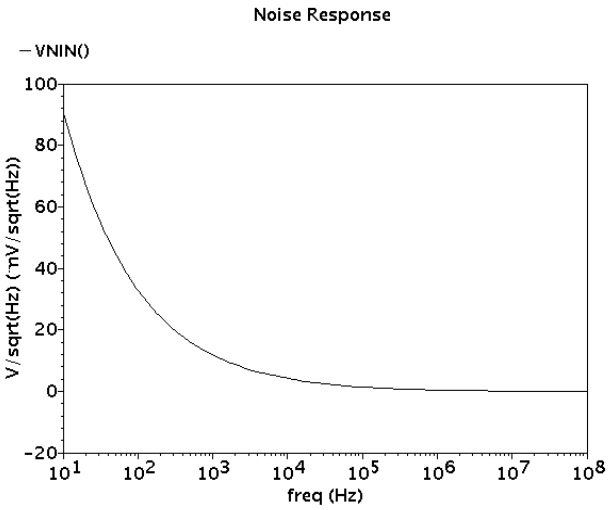

Figure 7. Input Referred Noise Voltage

Figure 8 shows layout of designed instrumentation amplifier with on-chip resistors. The layout of area of the chip is 1.49×10^6 µm^2. The area consumed by the on-chip resistors R1, R2, R3, R4, R5, and R6 is 1.48×10^6 µm^2 of the total area.

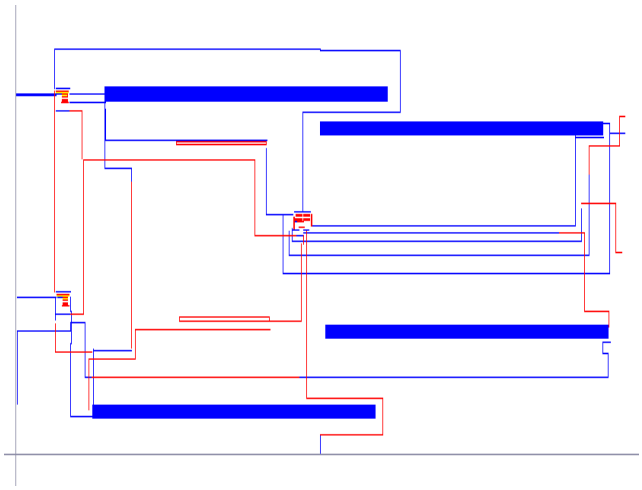

Figure 8. Layout with On-Chip Resistors

Figure 9 shows layout of designed instrumentation amplifier without on-chip resistors. The layout of area of the chip is $1.28x10^4$ μm^2.

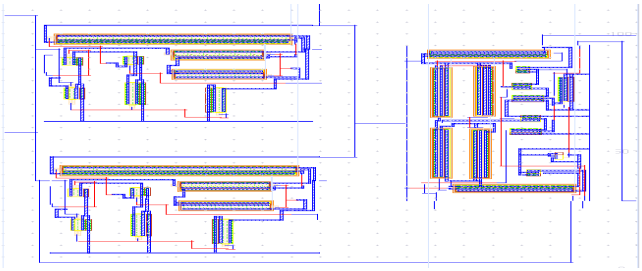

Figure 9. Layout without On-Chip Resistors

Layout of with and without on chip resistors instrumentation amplifier shows that the area consumed by without on-chip resistor is much lesser than with on-chip resistors. Moreover, with off-chip resistors the gain can be easily controlled externally.

Table 4 shows a comparison of the proposed instrumentation amplifier with some related existing instrumentation amplifier designs in literature. The critical performance metrics taken into consideration for comparison are gain, power dissipation, unity gain frequency, input referred noise, output referred noise and common mode rejection ratio for proposed design and other related references. The comparison explicitly shows an effective increment of 22.7 dB in gain, 17 dB in CMRR and 3.88 (nV/√Hz) in output referred noise.

Table 4. Comparison With Previous Designs

PARAMETER	THIS WORK	[5]	[1]	[2]	[3]
Technology (µm)	0.18	0.5	0.5	0.18	0.8
Gain (dB)	67.7	45	19.9	19.6	40
CMRR(dB)	92	75	>11	92	N/A
Unity Gain Frequency	91.33M	N/A	N/A	N/A	N/A
GB(Hz)	1.75	1.1M	20K	100M	N/A
Power Dissipation (µW)	263	283	N/A	N/A	122
Output Referred Noise (pV/√Hz)	1.75	5.63	N/A	N/A	N/A
Input Referred Noise (V/√Hz)	89n	22n	175n	22.8 m	N/A

4. CONCLUSION

A novel high gain and low noise CMOS instrumentation amplifier design for biomedical applications has been presented. The post and the pre layout simulations show that the design achieves comparatively high gain and low noise as compared to the previous designs existing in literature. The design also ensures low output referred noise one of main requirement of biomedical signal processing.

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