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# Digital Encoder Designing for Mobile Robot Control

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**ABSTRACT**

In this paper we present the design of a quadrature decoder/counter interface IC (ASIC) that performs the decoding, counting, and bus interface function in digital motor control systems, employing an Altra FLEX 10KA, 2s150fg456 Xilinx device. The ASIC contains a pair of digital filters, a quadrature decoder, an up/down counter, a latch and inhibit circuit, and an 8-bit bus interface to a digital processing system. The design of digital of the digital filter is based on the finite state machine model with datapath (FSMD). A novel scheme for detecting the motor rotation direction is also proposed. The ASIC can be applied to a digital motor control system forgetting the rotation speed or position of the motor, which is quipped with an optical encoder. The data acquisition can be extended to 16-bit integer format by two continuos reading cycles. Simulation and experimental tests are shown to verify the ASIC function properly.



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## 1. INTRODUCTION

In high-performance digital motor control systems with wide speed control range,certain interface integrated circuit (ICs) are still required through which to get the motor feedback position or speed signals, although sensorless control has got much attention recently [1]. Tachometers, potentiometers, resolvers, an optical encoder, for getting the motor rotation angle or speed. among them, the optical encoder is the most commonly used because its output signal is digital with high noise immunity and high resolution.

There are three types of optical encoder Commonly used in motion control. They are lockwise/counterclockwise, (CW/CCW), pulsedirection (pulse/DIR) and quadrature (A/B phase). Among them, the last one is the most popular because it can produce 4-time rate resolution.

Over the past two decades, mostly the digital motor control was done by using microprocessors [2], as shown in Figure 1. Some interface ICs, such as HP HCTL2000 and HCTL2016, for quadrature decoding and counting the output signal of the optical encoder are also available in commercial arkets [3]. However, the construction of whole control system is complex and the cost is not cheap. Recently, the progress in VLSI technology has made possible the use of complex programmable logicdevices (CPLD) of field programmable gated arrays (FPGA) for the design of digital controller, interface IC, or other application-specific ICs (ASICs) in the same chip Although the design of the quadrature decoder/counter interface IC in Literature is not lacking [7], the work was done in transistor level.In this paper, we present the design of interface IC in ate and register level, employing an Altra FLEX 10KA and 2s150 Xilinx device [8]. Using the scheme, the implementation of the circuit is easier than the previous work. The interface IC can perform flitering, quadrature ecoding,positioning counting and bus interface function.Simulation and experimental tests are shown to verify the function of the interface IC properly. The circuit can be integrated as a part of circuit of an application-specific digital control IC for motion control.

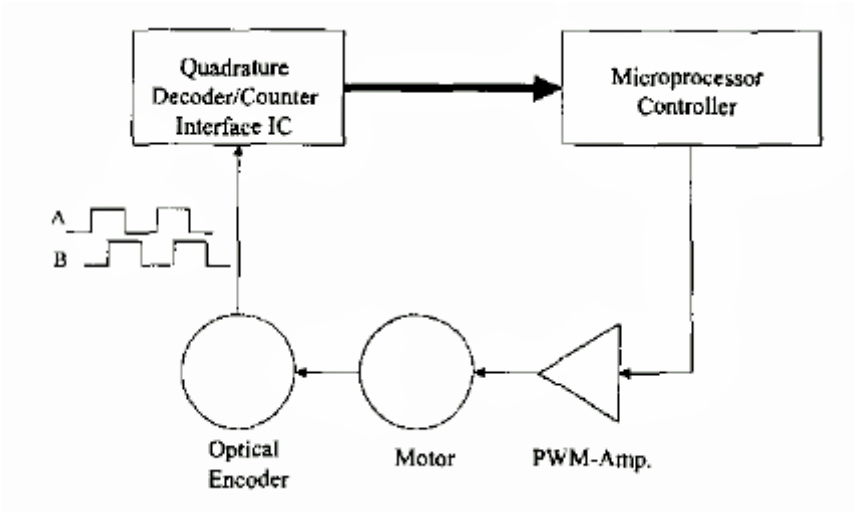


Figure 1. A microprocessor-based motor control system.

## 2. THE REQUIRED FUNCTION

Figure 2 shows the system function block diagram of the interface IC, which has an two-phase interface to an optical encoder and an 8-bit interface to a standard microprocessor or application-specific digital system. The required function of the interface IC are described as follows. Since many motors are usually working in noisy environments, which might introduce unwanted noise in the encoder's ouput due to electromagnetic coupling or vibration.A pair of digital filters, one for the channel A and the other one for the channel B, are required to filter out the noise on the incoming signals. A uadrature decoder circuit is also required to decode the incoming filtered signals for determining the motor rotation direction and multiply the resolution of the input signals by a factor of four. A position couter is then needed to up or down count the resulting decoded pulse according to the rotation direction indication from one of the decoder outputs.

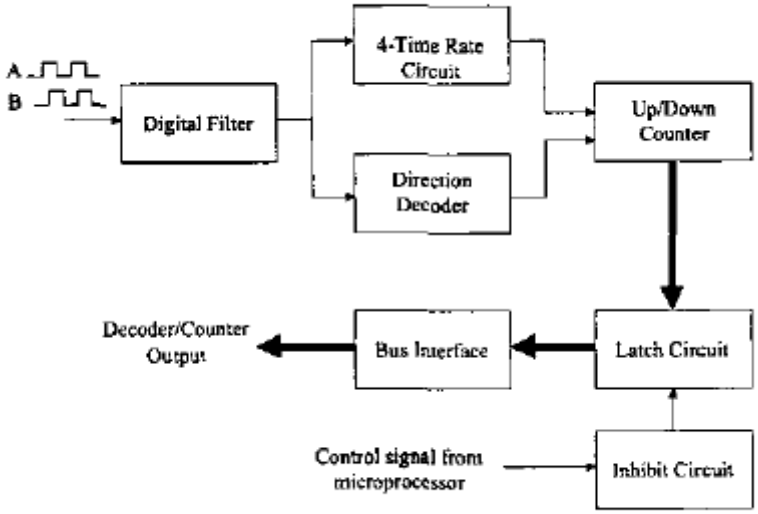


Figure 2. System function block of interface IC.

After the pulses been counted, the system can utilize the counter in two ways. First, the 16-bit latch and inhibit logic on the chip allows access to 16 bits of count required, a simple 8-bit mode is vailable by disabling the inhibit logic. The inhibit logic on the chip inhibits the transfer of data from the counter to the position data latch during the time interval that the latch output are being read. The inhibit logic allows the microprocessor or digital system to firstly read the low order byte form the latch. Meanwhile, the counter can

continue to keep track of the quadrature decoder states from thechannel-A and channel-B input signal. In the following, only the designs for the digital filters Quadrature decoder, and inhibit logic are described. The position counter and latch circuit, which are very common, are not described here.

## 3. DESIGN OF THE INTERFACE IC

### 3.1. Digital Filter

The design of the digital filters is based on the finite state machine model with datapath (FSMD) [9]. Figure 3 shows the circuit architecture of digital filter which consists of control unit and datapath on each channel. The control unit is recognizer that checks if the input from the optical encoder has short duration pulses, and a D flip flop. If the input level has same value (1 or 0) on at least threeconsecutive clock cycles, then the input is not considered as a noise. In this case the output of the recognizer is active high,which then allows the input data to flow through the datapath. The data value thus becomes the new output of filter. Otherwise the input is considered as a noise and the datapath output of the filter remain the same

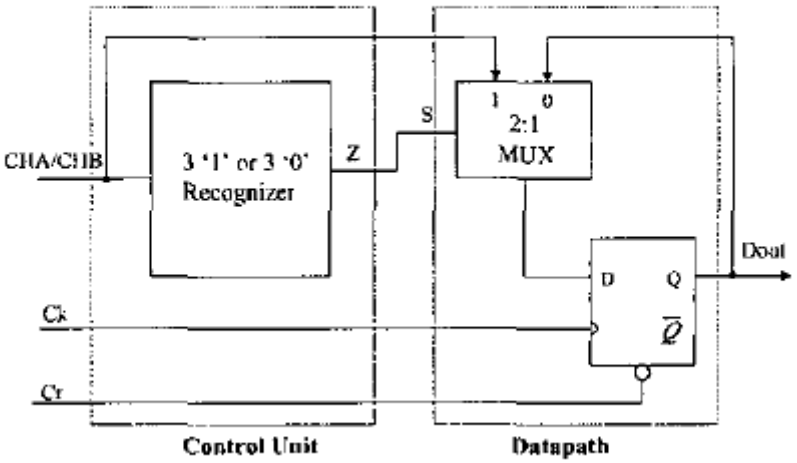


Figure 3. Implementation of digital filter.

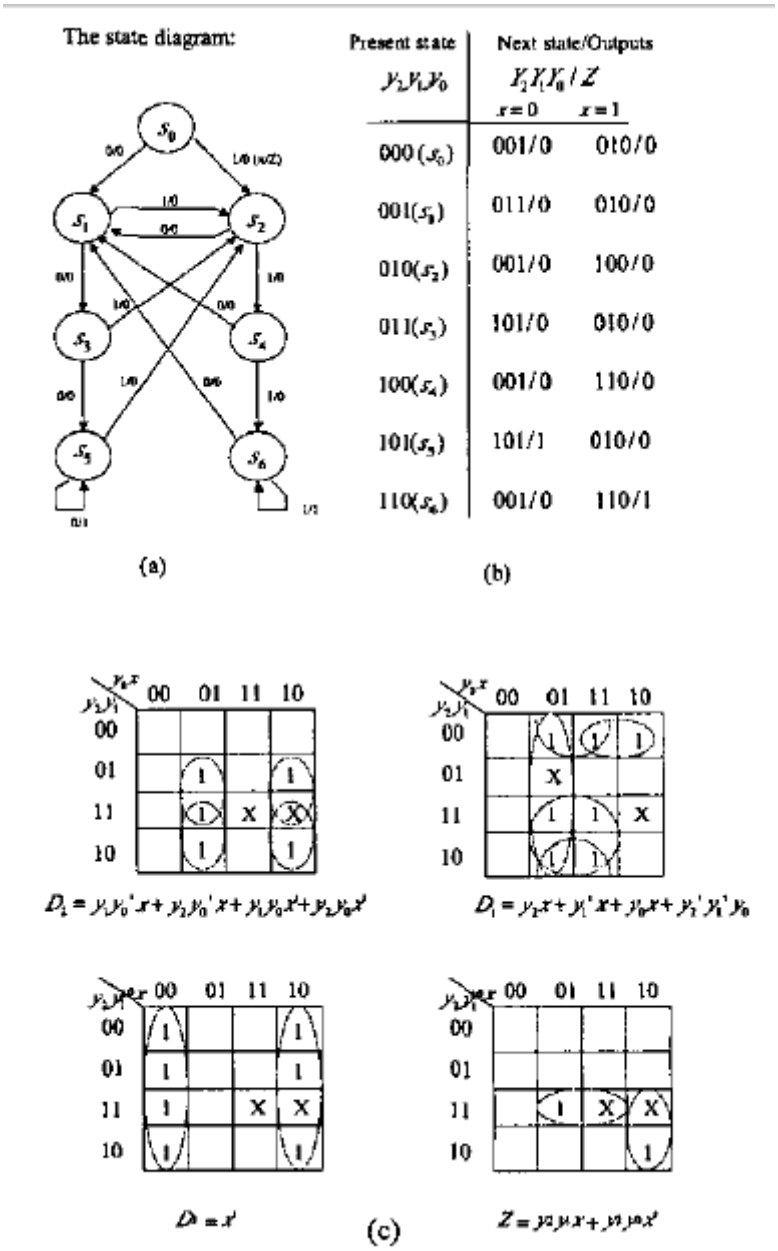


Figure 4. Design of the recognizer of digitalfilter: (a) state diagram (b) next state/ouput table, (c) excitationtable, excitation and output equations.

We assume that the design of control unit follows the finite state machine (FSM) model, consisiting of next-state logic, a state register, and an output logic [9, 10, 11].

Construction of the model starts with the generation of state diagram and/or next state and output tables. Figure 4(a) shows the state diagram of the recognizer which contains seven optimized states, where each state has different next state or output for every input. The correcponding next-state/output table with appropriate state encoding is shown in Figure 4(b). After completing the processof state minimization and state encoding, we are ready to choose the proper type of flip flop forimplementation of the FSM model. Since D flip flops required fewer connetions, they are chosen for our design. The excitation table, excitation and output equations by using the D flip flops acted as the state register are shown in Figure 4(c). The digital filter circuit and simulation result are shown in figure 5(a) and (b), respectively. As can be seen from Figure 5(b), the short-duration noise on the input signal (x) is rejected on the output (dfout) at the expense of three clocks time delay.

### 3.2. Quadratuer Decoder

The aqadrature decoder section consisits of a direction decoder and a 4-time rate circuit. It samples the two quadrature signal from the digital filters outputs and observes changes in these outputs on therising clock edge. The two quadrature signals can be encodered as four states. The state changes can be detected by comparing the previously sampled state to the current sampled state. This can in turn multiply the input signal frequency by a factor of four. A new method for detecting the rotationdirection of the motor is shown in Figure 6. It can be seen that the encoded state of 8, 14, 7, and 1 in clockwise direction are different from those states of 2, 11, 13, and 4. Thus we can use a 4-to 16 demultiplexer and some output logic to detect the direction.The count direction(up or down) is also determined by observing the previous and current states. The design circuit is shown in the bottom part of Figure 7. The upper part of Figure 7 shows the design of the 4-time rate circuit, the output of which is going to fetch into an up/down position counter.

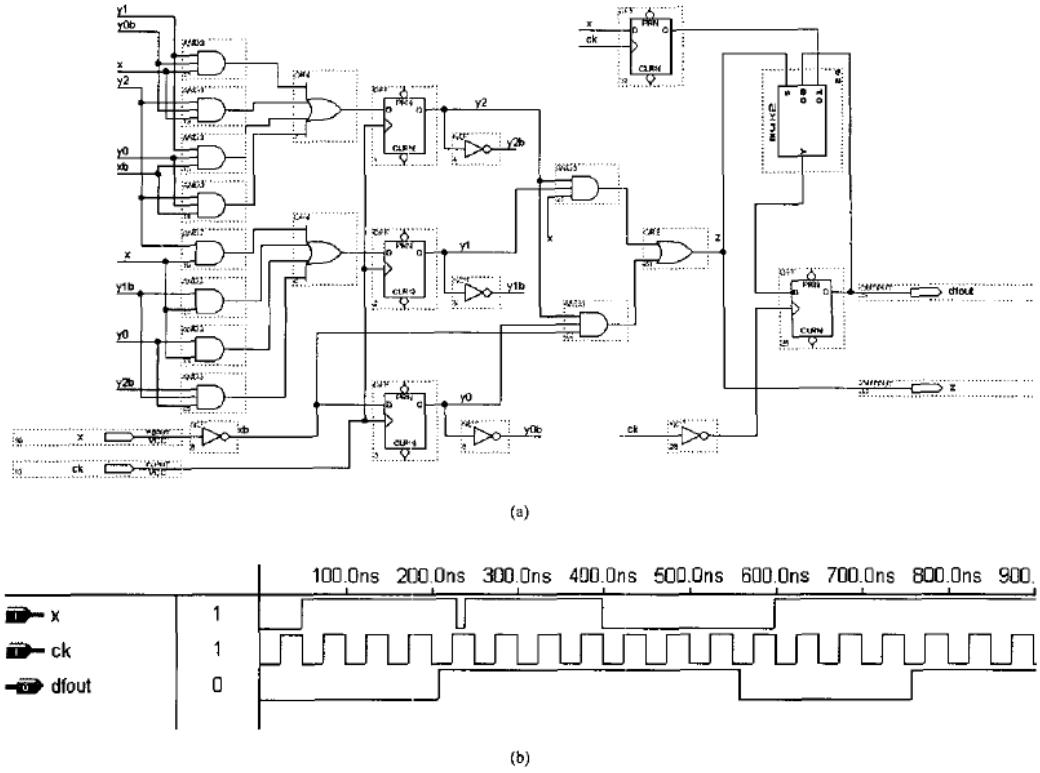


Figure 5. (a) the digital filter circuit (b)simulation result

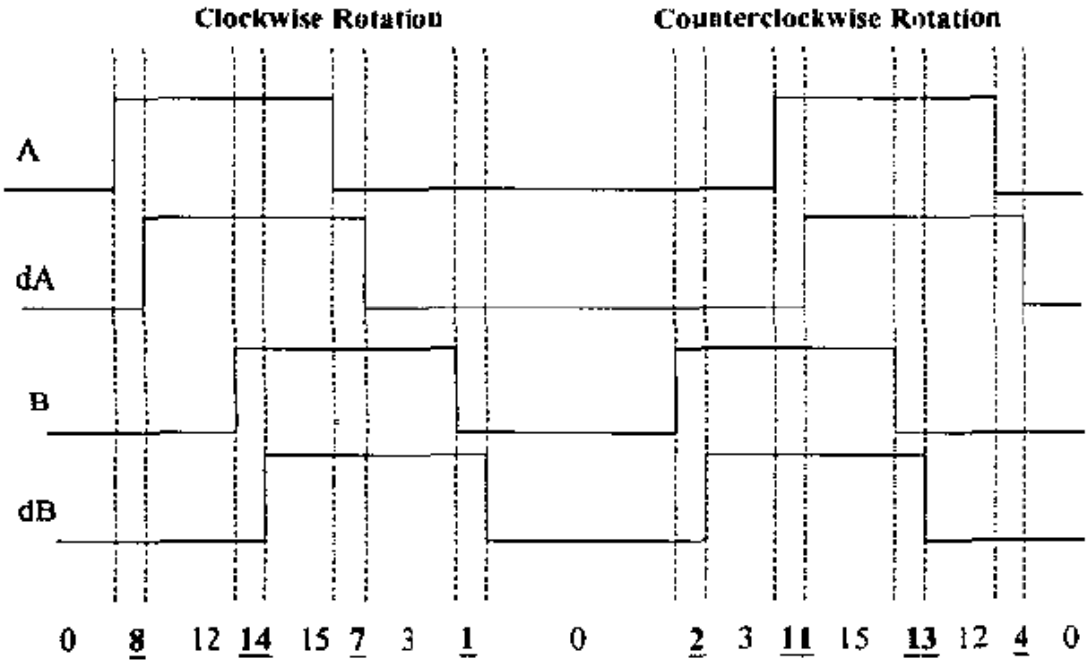


Figure 6. The determining strategy for rotation direction.

### 3.3. Inhibit Logic

The inhibit logic section samples the oe/ and sel reading command signal from the microprocessor or digital system on the falling edge of the clock and inhibits the position data latch to avoid the latcheddata being updated during a two-byte reading cycles for a 16-bit data access. The desisn of the inhibit logic also follows the FSM models as described above.The state diagram and next – state/output able are shown in figure 8(a) and (b), respectively.As can be seen, there are three minimum states and only two flip flops are need for the implementation of the model. Similarly, we use the D flip flop as the state registers due to its simplicity. The excitation table equation logic are shown in figure 8(c). The output is just the same as second flip flop output state.

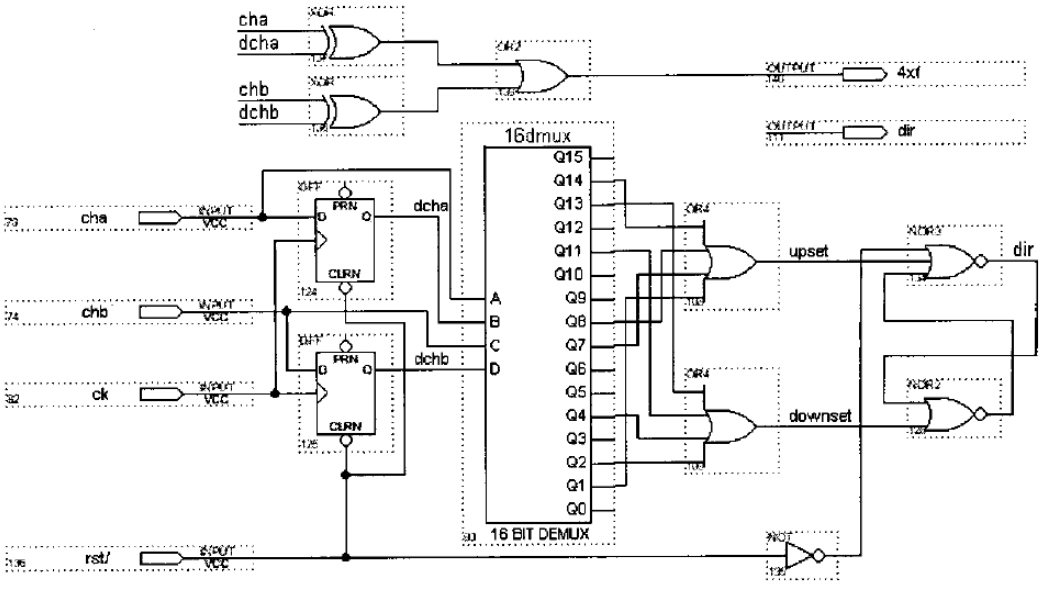


Figure 7. The Quadrature decoder and four-time rate circuit.

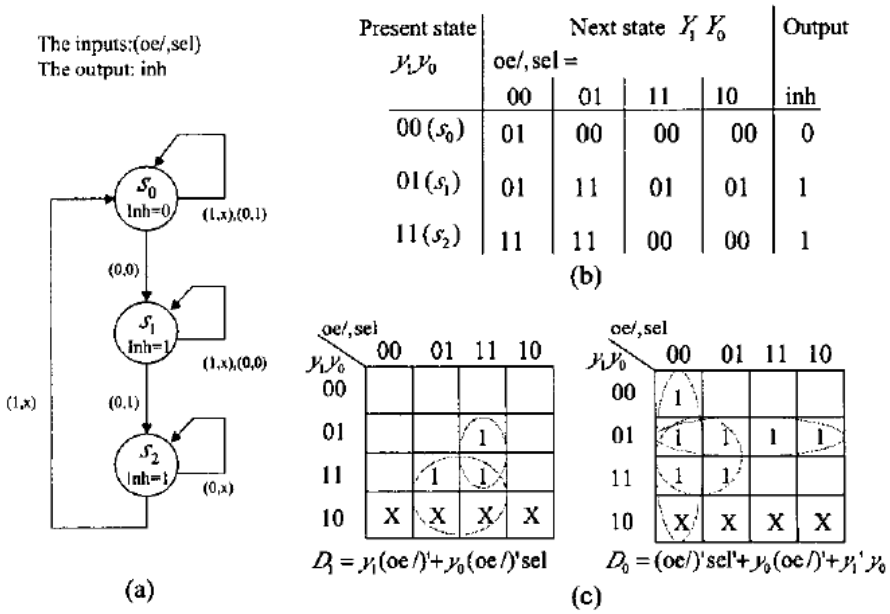


Figure 8. Design of inhibit logic (a) state diagram,(b) next-state/outputtable, (c) excitation table and excitation equation.

## 4. SIMULATION AND TEST

The overall circuit of the interface IC plotted by using the Altra MAXPLUS II and ISE Xilinx. Is shown in figure 9. The wave form simulation provided in this tool has verified each circuit symbol in this figure. An overall simulation result to test the function of the interface IC is shown in Figure 10 by giving two quadrature input signal (cha and chb) and a clock signal with much higher frequency than the input quadrature signals. As can be seen, a 4-time rate signal (4xff) whose frequency is four times of that of input pulses is successfully generated In addition, the direction signal (dir) is active low if thephase A signal is leading the phase B signal and active high if the phase Asignal is lagging the phas B signal. The position up/down counter up counts from 0 to 9 while the dir signal is active high.

The position data latch output (latch [7..0]) Remains at 6 when the oe/signal is active low for a 16-bit data access. At the same time the inhibit logic output signal (inh) is active high and remains high until the low-byte data has been read out on the second reading cycle. The simulation results indicate that the function of quadrature decoder/counter interface IC are correct. The design circuit has been further tested by the experimental system, as shown in Figure 11. The motor optical encoder can produce two quadrature A/B phase signals with the rate of 2000 pulses per revolution. A test program in the personal computer has been designed to read the count number latched on the interface IC. For decoding and counting the pulses, we rotate the motor shaft manually in about every five seconds.

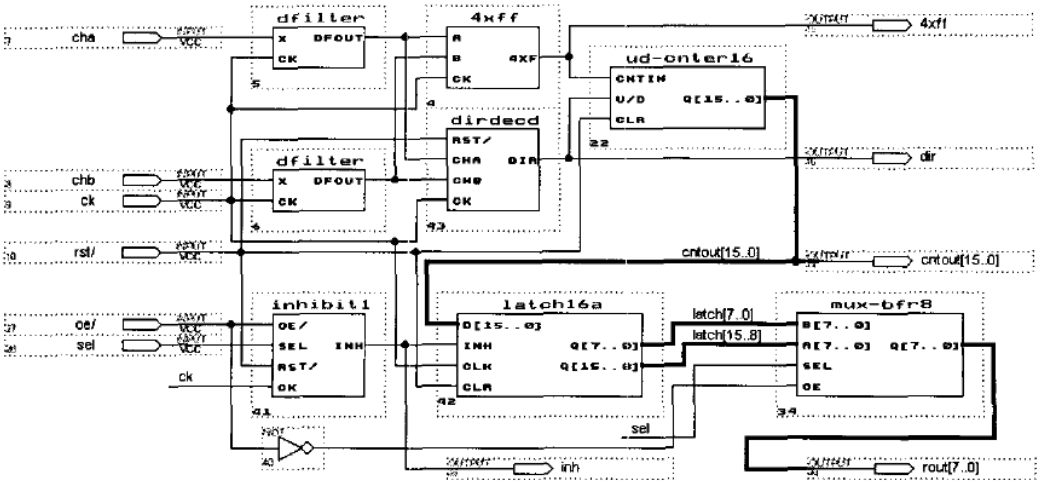


Figure 9. The overall circuit of quadrature decoder/counter interface IC.

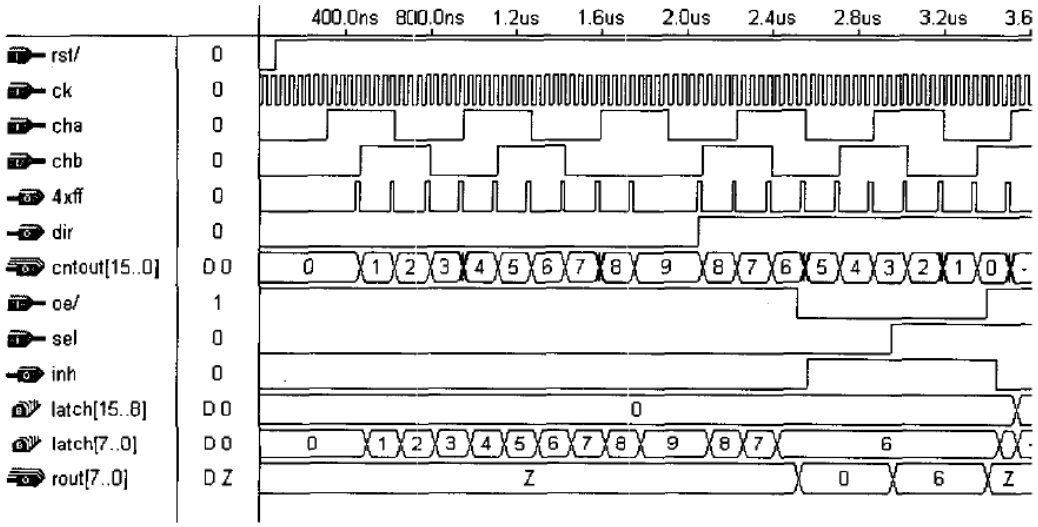


Figure 10.Simulation result of the quadrature decoder/counter Interface IC

During the time interval,we can see the latched count number displayed on the PC monitor clearly. For one rotation in the clockwise rotation, there will be 8000 pulses to be counted, and then the display number is 1F40 in hex-decimal data format. Table I summaries the cout number corresponding to the rotation cycles in clockwise and counter clockwise direction, respectively. The results also verify the function of the quadrature ecoder/counter interface IC properly.

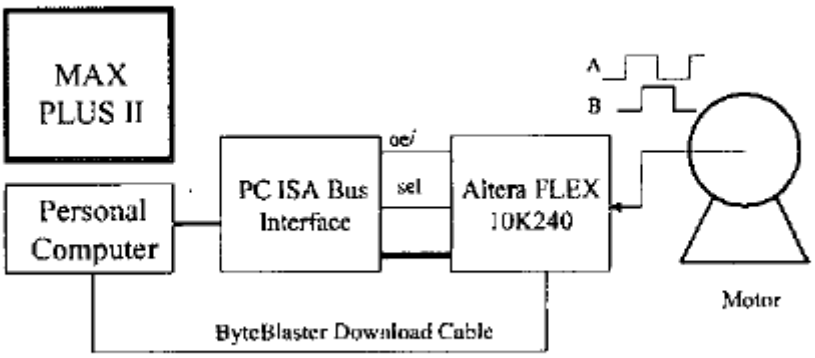


Figure 11. The experimental system fortesting the interface IC.

Table 1. The motor rotation cycles and corresponding counts.

| Rotation cycles per 5 sec | Counts in Clockwise Direction | Counts in Counter Clockwise Direction |
|---|---|---|
| 1 | 1F40 | E0BF |
| 2 | 3E80 | C17F |
| 3 | 5DC0 | A23F |
| 4 | 7D00 | 82FF |
| 5 | 9C40 | 63BF |

Implement in 2s150fg256 xilinxin ISE
Device Utilization for 2s150fg4 56

| Resource | used | Avail | utilize |
|---|---|---|---|
| I/Os | 57 | 288 | 19.79% |
| Function generator | 57 | 3456 | 1.65% |
| CLB Slices | 35 | 1728 | 2.03% |
| DFFs | 70 | 4320 | 1.62% |

## 5. CONCLUSION

This paper presents the design of quadrature decoder/counter interface IC in the gate and register level by using an Altra FLEX 10kA, XC95144XL Xilinx device. Implementation of the circuit using the CPLD device is easier than the previous work done in transistor level. Simulation and experimental tests are shown to verify the ASIC functions properly. The interface IC can be appliedas an interface to a microprocessor – based motor control system. It can be also integrated as a part of circuit of an application-specific digital control IC for motion control.

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Reza Afshar was born in Qazvin-Iran in 1989. He received the B.Sc. degree in electrical engineering from the Islamic Azad University, Buin Zahra, Iran, in 2014. Currently, he is working toward his M.S degree in Electrical Engineering at Islamic Azad University Miyaneh Branch, Miyaneh, Iran. His research interests include analysis and designing of Digital VLSI.