

A Single-Stage Low-Power Double-Balanced Mixer Merged with LNA and VCO

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ABSTRACT

This paper proposes three types of single stage low-power RF front-end, called double-balanced LMVs, by merging LNA, mixer, and voltage-controlled oscillator (VCO) exploiting a series LC (SLC) network. The low intermediate frequency (IF) or baseband signal can be directly sensed at the drain nodes of the VCO switching transistors by adding a simple resistor-capacitor (RC) low-pass filter (LPF). By adopting a double-balanced mixer topology, the strong leakage of the local oscillator (LO) at the IF output is effectively suppressed. Using a 65 nm CMOS technology, the proposed double-balanced LMVs (DB-LMVs) are designed. Oscillating at around 2.4 GHz ISM band, the phase noise of the proposed three DB-LMVs is -111 dBc/Hz at 1 MHz offset frequency. The simulated voltage conversion gain is larger than 36 dB and the double-side band (DSB) noise figure (NF) is less than 7.7 dB. The DB-LMVs consume only 0.2 mW *dc* power from 1-V supply voltage.

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1. INTRODUCTION

Low power, low-voltage, and highly integrated circuits are always the main topics for integrated circuit design, especially very important for mobile wireless communication systems due to the limitation of battery life. Single stage circuits combining mixer and oscillator have been designed for the purpose of a higher degree of integration and reducing power consumption. For highly integrated low-power receiver front-end, a current reuse technique is typically chosen across different functional blocks. A popular method is stacking the mixer on top of the input stage of the low-noise amplifier (LNA), while less frequent one is stacking mixer and voltage-controlled oscillator (VCO) [1-4]. In [1], a double balanced mixer is stacked on top of the voltage-controlled oscillator (VCO) by using the current reuse topology. The radio frequency (RF) input signal is applied to the input of the mixer, and the oscillator signal is applied to the source nodes of the mixer. Moreover, this topology applies a separate dc bias to the VCO.

In [2], the RF front-end merges LNA, mixer, and VCO (LMV) in a single stage (Figure 1). This topology stacks VCO on top of the mixer. The current source of the mixer is modified as the LNA with inductor degeneration. This topology performs RF amplification, mixing, and local oscillator (LO) generation while sharing the same bias current and the same devices among all the blocks of the RF front-end, resulting in a very low-power and small-area chip solution. Since the intermediate frequency (IF) outputs are connected to the source nodes of the VCO, the voltage gain is limited due to the low impedance at the source nodes.

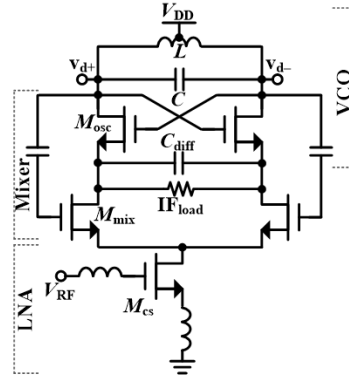


Figure 1. Liscidini's LMV Cell in [2]

A conventional VCO with a current source can be considered as a mixer when a RF signal is applied to the input port of the current source. For the conventional VCO, the down-converted IF signal at the VCO output is negligible due to the low impedance at the low frequency. If a series resonator is employed, the impedance is high at the low frequency and the IF signal can be recovered without any signal loss. A single-balanced LMV is proposed in [5]. However, the single-balanced topology has a disadvantage of strong LO leakage at the IF output which can saturate the following stages. If a double-balanced topology is adopted for the mixer, the strong LO leakage can be rejected successfully. For the RF front-end from antenna to LNA, the input and output signal is typically single-ended and requires a single-to-differential conversion balun for the following double-balanced mixer. This extra balun can degrade the overall system noise figure of the receiver. Therefore, a single-ended input is desirable for the double-balanced mixer [6-7].

In this paper, single-stage double-balanced LMVs (DB-LMVs) with differential and single-ended input are proposed combining LNA, mixer, and VCO to suppress the LO leakage at the IF output. By exploiting a series LC (SLC) network instead of a parallel LC (PLC) network, the low frequency IF or baseband signal can be directly extracted from the drain outputs of the VCO. This paper is organized as follows. In Section II, the traditional LC tank oscillator is described as a mixer, and a detailed analysis for the proposed DB-LMVs are given. In Section III, an experimental performance is given based on simulation using 65 nm CMOS technology. Finally, a conclusion is given.

2. CIRCUIT DESIGN OF DB-LMV

A conventional LC tank oscillator, as shown in Figure 2, performs the mixing process since an RF signal in the VCO bias current is down-converted by the switching transistors. Also, by the same mechanism, the dc current of M_{cs} is up-converted to the LO frequency. With the complete switching is assumed for the M_{sw1} and M_{sw2} , the amplitude of the VCO output is given by

$$V_{LO} = \frac{4I_{CS}R_L}{\pi} \quad (1)$$

and the current at the VCO output port is given by

$$i_{O,SB} = \frac{4I_{CS}}{\pi} \cos\omega_{LO}t + \frac{2}{\pi} g_m v_{RF} \cos(\omega_{LO} - \omega_{RF})t + \dots \quad (2)$$

where I_{CS} and g_m are the dc current and transconductance of the current source M_{CS} , respectively. The first term in (2) is the LO component of the VCO. The low frequency IF signal (the second term) is severely attenuated since the inductor of the PLC tank is short at around dc . Also, the higher order frequency components are attenuated by the PLC tank. In Figure 2, attempting to sense the down-converted component at the VCO output unavoidably degrades the phase noise [2]. One possible solution is to exploit the SLC network for the VCO to extract both LO and IF signals. Figure 3(b) shows a SLC VCO where the coupling capacitor C_{cpl} and the inductor $2L$ form a SLC network. When an RF signal is applied to the input of the transconductance stage, the topology in Figure 3(b) is exactly the same as the single-balanced mixer since the coupling capacitor C_{cpl} is open at IF frequency. Also, a modified version can be implemented in Figure 3

replacing the load resistor R_L with the complementary PMOS transistors. In [8], a new LMV is proposed using a SLC tank resonator instead of using a PLC tank resonator for low-phase noise design by combining a single-balanced mixer and a complementary VCO. Figure 4 shows the single-balanced LMV (SB-LMV) cell by modifying the current source as an inductive degenerated LNA and adding simple first-order RC low-pass filter (LPF). The RC low-pass filter is designed to attenuate the LO component at the drain nodes of the VCO while somewhat degrading the phase noise performance. The transistor M_{cs} acts as an LNA at RF, while providing the dc bias current to the VCO. The transistor $M_{sw,n}$ performs the mixing operation while contributing the negative resistance to the VCO. As shown in Figure 4, RF component is down-converted around dc, and the dc component is up-converted to the LO frequency.

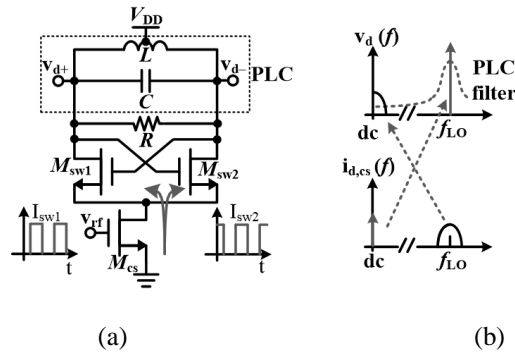


Figure 2. (a) Conventional PLC VCO as a mixer and (b) its frequency response

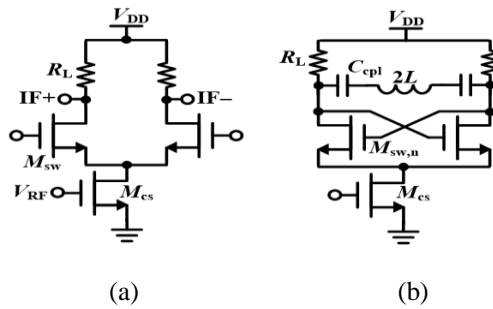


Figure 3. (a) Single-balanced mixer and (b) SLC VCO

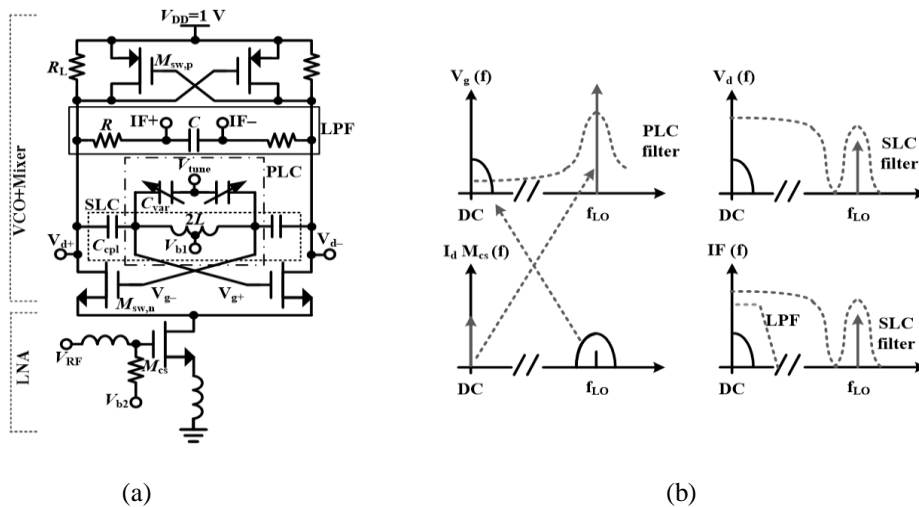


Figure 4. Single-balanced SLC LMV cell [8] and (b) frequency responses

Looking at the gate nodes, the IF component is severely attenuated since the inductor is short at around dc . However, looking at the drain nodes, the IF component appears without attenuation since the C_{cp1} is open at around dc . With just adding the simple RC low-pass filter (LPF) to the drain nodes, the LO component can be suppressed with significant attenuation and leaving the down-converted signal at the IF output. The SB-LMV cell requires only small size capacitance for the LPF compared to that of the Liscidini's LMV cell in Figure 1 which requires quite large size capacitance for the same LPF corner frequency since the impedance looking at the source nodes at the IF outputs is quite low.

Figure 5 shows the impedances looking at the gate and drain nodes of the switching transistors. Since the coupling capacitor C_{cp1} is just short at the LO frequency, the final VCO oscillation frequency is mainly determined by the PLC resonator. Figure 6 shows the output spectrum at the gate and drain nodes of the switching transistors. As shown in Figure 6, the IF component is severely attenuated at the gate nodes, but appears at the drain nodes without attenuation.

This IF component at the drain nodes can be further filtered out with the RC LPF to suppress the strong LO component. However, the LO component is still strong after the filtering and can saturate the following stages coming after the LMV cell. If a double-balanced mixer topology is adopted, the LO component can be severely rejected.

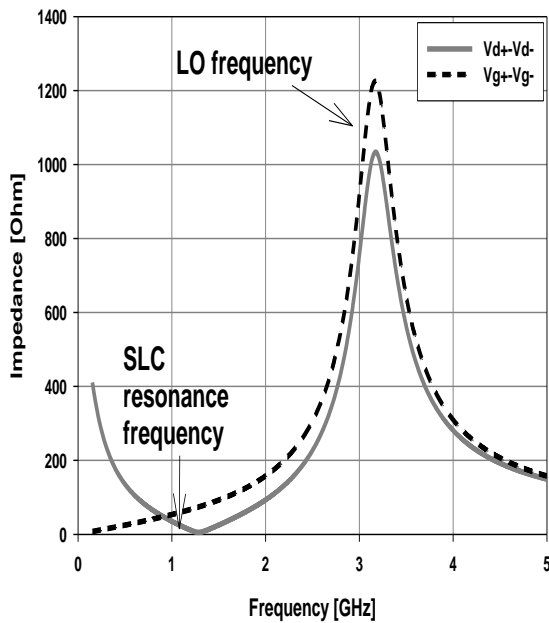


Figure 5. Impedances of the SB-LMV Cell looking at the gate and Drain Nodes

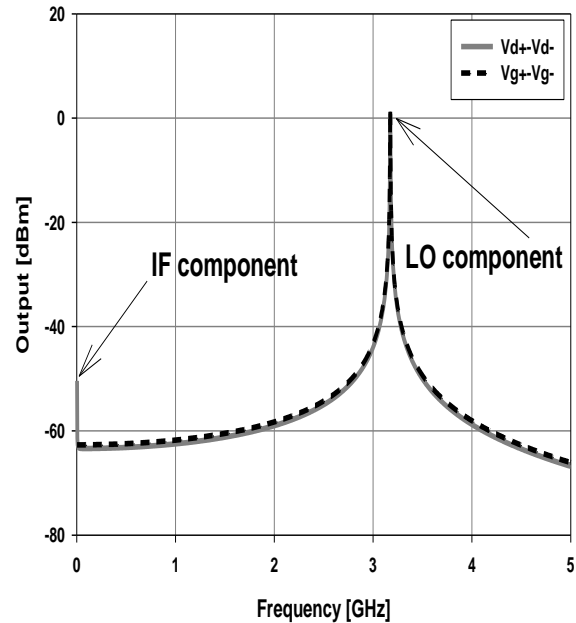


Figure 6. Output Spectrum of the SB-LMV Cell looking at the gate and Drain Nodes [8]

Figure 7 shows the double-balanced mixer topologies. For the double-balanced mixer, the IF output from the drain of M_{sw1} and M_{sw3} is directly combined. The output current at the IF output of the double-balanced mixer is given by

$$i_{O,DB} = \frac{2}{\pi} g_m v_{RF} [\cos(\omega_{LO} - \omega_{RF})t + \cos(\omega_{LO} + \omega_{RF})t \dots] \quad (3)$$

From (3), it can be seen that the LO component is rejected with the double-balanced topology.

Figure 8 shows the proposed three kinds of double-balanced LMVs with differential and single-ended input by combining two SB-LMV cells. For the double-balanced LMV cell, the IF output from the drain of $M_{sw,n1}$ and $M_{sw,n3}$ is indirectly combined through the resistor R of the RC LPF to keep the oscillation of the LMV cell (the outputs LO+ and LO- would be shorted without the resistor R). The inductor is shared between two SB-LMV cells. Compared to the SB-LMV (which has higher LO leakage at the IF output and requires large size capacitor for sufficient LO rejection), the capacitor value for the RC LPF in the DB-LMV can be minimized just to reject the higher order harmonic frequencies at the IF output.

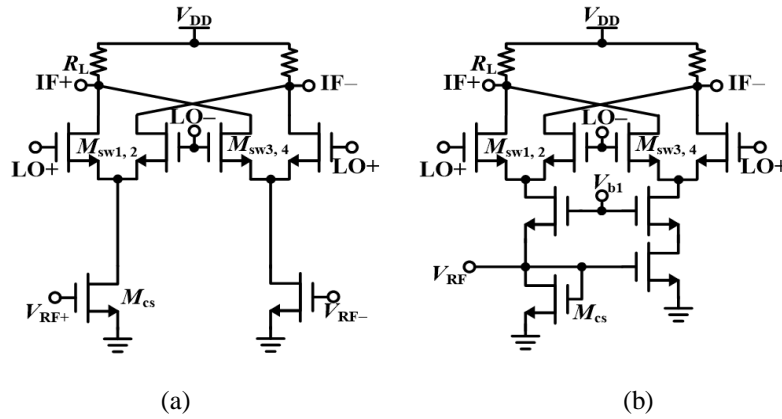


Figure 7. (a) Differential Input Double-Balanced mixer and (b) Single-Ended Input CMOS Micromixer [6-7]

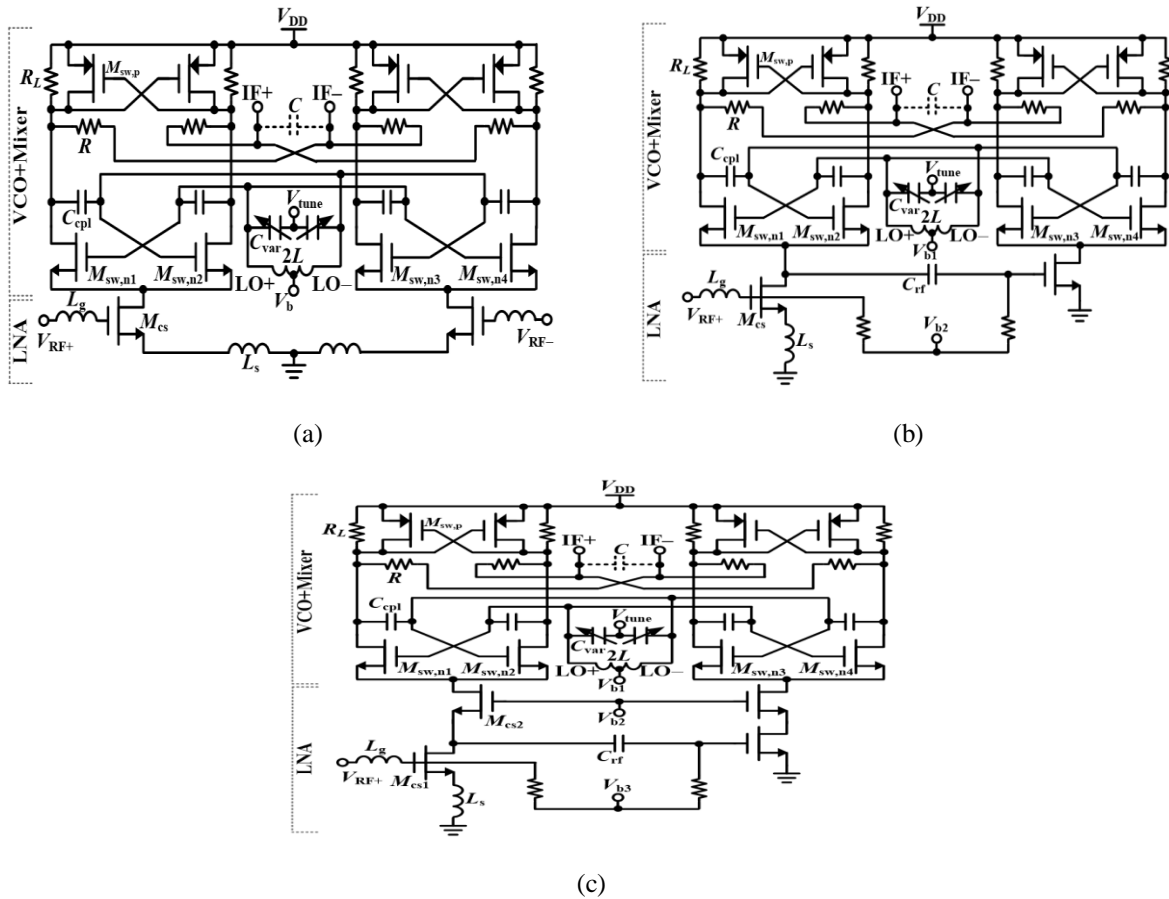


Figure 8. Proposed DB-LMVs (a) differential Input DB-LMV (DI-DB-LMV), (b) single-ended Input DB-LMV (SE-DB-LMV1), and (c) single-ended Input DB-LMV (SE-DB-LMV2) [9]

3. SIMULATION RESULTS OF DB-LMV

A symmetric inductor is used to have a higher quality (Q) factor to have a better phase noise performance. For the proposed DB-LMV cell, the *dc* bias current is set to have about 0.22 mA from 1 V supply voltage for the LO output swing of 0.6 V peak-to-peak. The *ac* coupling capacitor C_{cpl} is implemented with metal-insulator-metal (MIM) capacitor. The tuning range can be varied with the MOS varactors. For fair comparison, all the devices of the DB-LMVs are designed to have the same size.

Table 1. Device Parameters of DB-LMVs

Device	Value
$M_{sw,n}$	32 $\mu\text{m}/90\text{ nm}$
$M_{sw,p}$	16 $\mu\text{m}/90\text{ nm}$
M_{cs}, M_{cs1}, M_{cs2}	32 $\mu\text{m}/90\text{ nm}$
C_{cpl}	1 pF
R_L	5 k Ω
R	4.6 k Ω
$2L$	10~11.4 nH
C_{var}	90 fF

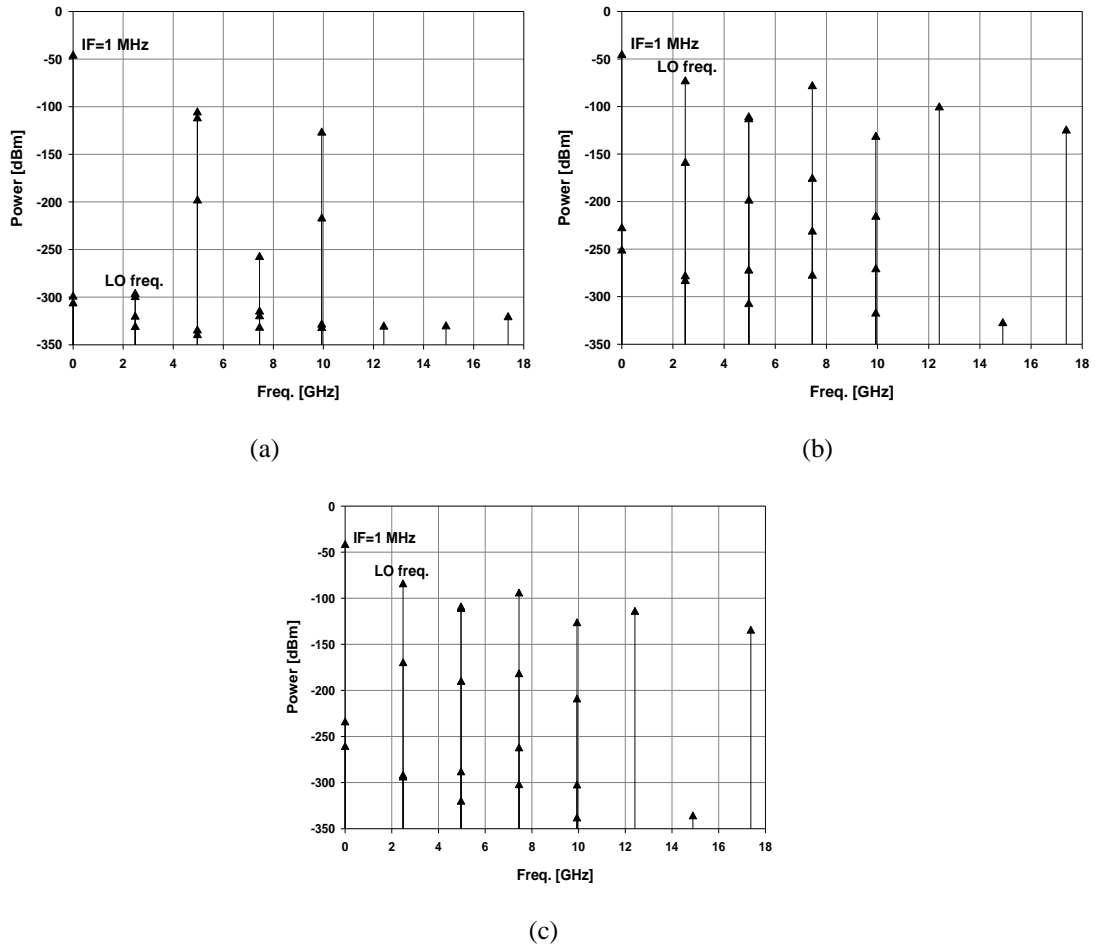


Figure 9. Harmonic balance simulation results of the DB-LMVs. (a) DI-B-LMV, (b) SE-DB-LMV1, and (c) SE-DB-LMV2. The applied RF input power is -80 dBm

Table 1 gives the device parameters for DB-LMVs. Figure 9 shows the harmonic balance simulation results at IF outputs for three DB-LMVs with neglecting the capacitor C of the RC LPF. As shown in Figure 9(a), LO leakage at the IF output is severely suppressed for the differential input DB-LMV. For the single-ended DB-LMVs, the LO leakage is much higher due to the unsymmetry of the transconductance stage. The RF input stage in Figure 8(b) can be cascoded as shown in Figure 8(c) to have better symmetry which results in more LO leakage suppression (Figure 9(c)).

Figure 10 shows the signal swing at the RF input and IF outputs of three DB-LMVs. A clean signal is extracted at the IF output with suppressed LO leakage. The voltage conversion gain is about 36–39 dB. Figure 11 shows the phase noise performance of the proposed DB-LMVs. The three DB-LMVs have similar phase noise performance with the phase noise of about -111 dBc/Hz at 1 MHz offset frequency. The close-in phase noise performance of the SE-DB-LMV1 is somewhat inferior compared to other DB-LMVs. Figure 12 shows the double-sideband (DSB) noise-figure (NF) performance.

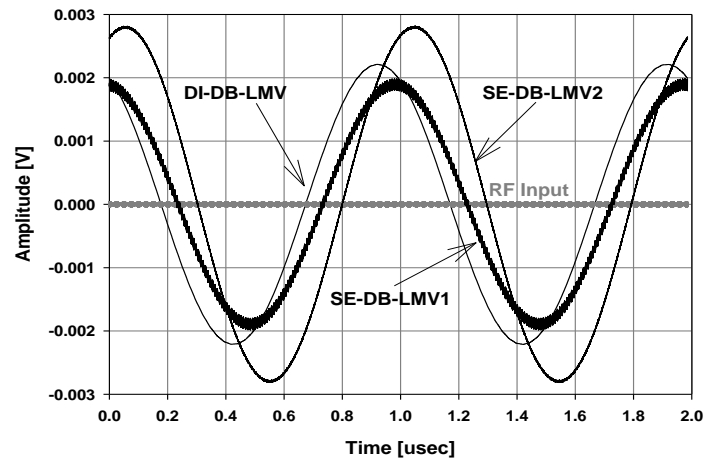


Figure 10. Voltage swing at the RF Input and IF Output of the Proposed DB-LMVs. The RF Input Power is -80 dBm

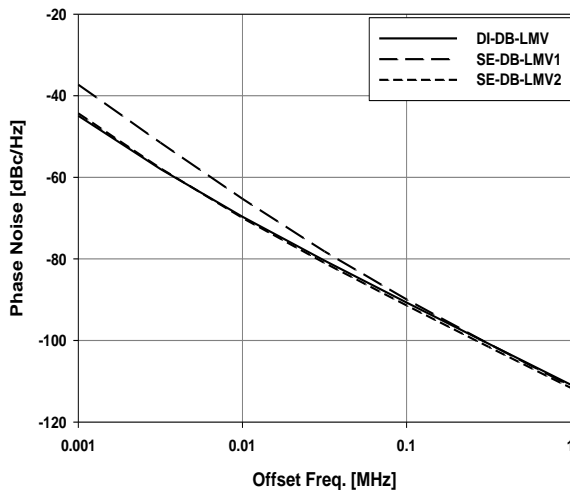


Figure 11. Phase noise of the Proposed DB-LMV cell

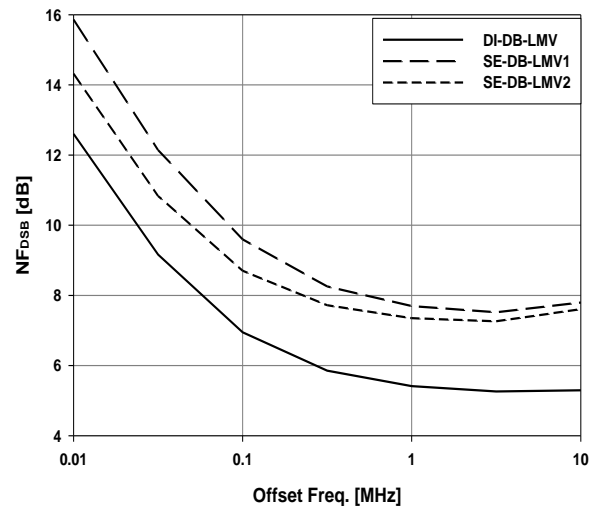


Figure 12. Double-side band noise figure of the proposed DB-LMVs

The DSB NF of the DI-DB-LMV is about 5.4 dB at the over 1 MHz IF frequency. The DSB NF of other DB-LMVs is about 7.5 dB. The RF input of each DB-LMV is matched to 50 ohm signal source impedance with input reflection coefficient less than -10 dB. Table 2 summarizes the performance of DB-LMVs. From the simulation results, the proposed DB-LMV cell is expected to be successfully integrated for the direct conversion receiver such as Global Positioning System (GPS), satellite communication receiver, medical applications, and cable TV set-top box, etc while consuming low power with just one integrated block.

Table 2. Performance Summary of DB-LMVs (Simulation)

	DI-DB-LMV	SE-DB-LMV1	SE-DB-LMV2
f_{osc} (GHz)	2.48	2.45	2.46
P_{DC} (mW)	0.22	0.22	0.24
V_{GAIN} (dB)	37	36	39
LO Leakage (dBm)	-289	-74	-85
Phase Noise (dBc/Hz@1 MHz)	-110.8	-111.2	-111.6
NF_{DSB} (dB@1 MHz)	5.4	7.7	7.3
Process	65 nm CMOS		

4. CONCLUSION

By utilizing a series LC resonator, this paper proposes three kinds of fully integrated RF front-end DB-LMVs by merging LNA [10], [11], double-balanced mixer, and VCO. The proposed DB-LMVs are designed and simulated using 65 nm TSMC CMOS technology. Operating at around 2.4 GHz ISM band, the proposed DB-LMVs can be easily integrated on a chip, and applied for low-power high-performance direct conversion RF front-end receiver.

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Nam-Jin Oh received the B.S. degree in physics from Hanyang University, Seoul, Korea, in 1992, the M.S. degree in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 1999, and the Ph.D. degree from the Korea Advanced Institute of Science and Technology–IT Convergence Campus (KAIST–ICC) (formerly the Information and Communications University), Daejeon, Korea, in 2006. From 1992 to 1997, he was with LG Corporate Institute of Technology, Seoul, Korea. From 1999 to 2001, he was with Samsung Electronics, Suwon, Korea. From 2006 to 2007, he was with Auto-ID Lab., Fudan University, China, as a post-doctor. He joined the department of Electronic Engineering, Korea National University of Transportation (formerly Chungju National University), Korea, in 2007, where he is currently an associate professor. His research interests are focused on analog and mixed-signal integrated circuits, digital integrated circuits, system level behavioral simulation of wireless communications, and device modeling of CMOS active and passive circuits.