

Modeling and Simulation of Biaxial Strained P-MOSFETs: Application to a Single and Dual Channel Heterostructure

Amine Mohammed Taberkit, Ahlam Guen-Bouazza, Benyounes Bouazza

Research Unit of Materials and Renewable Energies,

Department of Electronic and Electrical Engineering, University of Abou-BakrBelkaid, Tlemcen, Algeria

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ABSTRACT

The objectives of this work are focused on the application of strained silicon on MOSFET transistor. To do this, impact and benefits obtained with the use of strained silicon technology on p-channel MOSFETs are presented. This research attempt to create conventional and two-strained silicon MOSFETs fabricated from the use of TCAD, which is a simulation tool from Silvaco. In our research, two-dimensional simulation of conventional MOSFET, biaxial strained PMOSFET and dual channel strained P-MOSFET has been achieved to extract their characteristics. ATHENA and ATLAS have been used to simulate the process and validate the electronic characteristics. Our results allow showing improvements obtained by comparing the three structures and their characteristics. The maximum of carrier mobility improvement is achieved with percentage of 35.29 % and 70.59 % respectively, by result an improvement in drive current with percentage of 36.54 % and 236.71 %, and reduction of leakage current with percentage of 59.45 % and 82.75 %, the threshold voltage is also enhanced with percentage of: 60 % and 61.4%. Our simulation results highlight the importance of incorporating strain technology in MOSFET transistors.

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Corresponding Author:

Amine Mohammed Taberkit,

Research Unit of Materials and Renewable Energies,

Department of Electronic and Electrical Engineering,

University of Abou-BakrBelkaid, 13000, Tlemcen, .Algeria.

Email: taberkit.amine@yahoo.fr

1. INTRODUCTION

In 1965, Gordon Moore predicted that transistor density on an integrated circuit would double approximately every 2 years [1]. The metal oxide semiconductor field effect transistor (MOSFET) is one of the major and important components in the semiconductor industry. Since its first practical use fifty years ago, the MOSFET has a major use in integrated circuits (ICs) to serve as a basic operating device in switching functions for digital circuits and as an amplifier device for analog applications.

While the basic planar structure of the MOSFET has remained mostly unchanged, its size has been shrunk by many orders of magnitude over the past thirty years, however, "No exponential is forever. But you can delay forever" [2]. Further, MOSFETs scaling down causes short channel effects (SCEs), to intensify, accordingly degrading the current drivability, electron mobility, with an apparition of high leakage current. In order to enhance conventional MOSFETs, ITRS presented two alternatives, the first one has been the use of new designs such as FDSOI, PDSOI, MUGFETs on SOI and others technologies, the second one, was about using materials with high permittivity and mobility. Among these technologies, we find devices based on strained silicon technology. The use of Strained Silicon (S-Si) channel is one of the expected technology boosters introduced by the ITRS roadmap to sustain the improvement of performance in future device generations [3]. The interest in the strain engineering has in fact been speed-up recently as a need in a speed scaling of CMOS technology devices for high-speed and low power applications. On another side, transport

properties improvement of new materials such as high-k gate dielectrics, metal and midgap gate metal electrodes, strained-Si, silicon-germanium alloys and III-V semiconductors along with new device designs, such as dual-gate and tri-gate FinFETs can decrease the gate leakage current and gate resistance, reduce the poly-gate electrode depletion capacitance, and increase the device speed. Non-classical CMOS structures offer a better control of SCEs, improved I_{on} current *via* channel mobility, lower load capacitance and lower propagation delay time. These structures also offer lower I_{off} current and lower switching energy. In addition, the combination of strain techniques with other options, such as Multiple Gate MOSFETs, high-k materials and metal gates, are currently considered to keep on track with Moore's law.

In this paper, the combination of strain techniques with heterostructure dual P-channel MOSFET, has been considered to keep on track with Moore's law. To, do this, a two dimensional simulation of conventional MOSFET, biaxial strained P-MOSFET and dual channel heterostructure strained P-MOSFET has been done to compare these devices characteristics. This study allows showing the improvement obtained with Strained Silicon channels. Comparison between the unstrained and strained MOSFET allows proving that strained silicon with identical channel length performs better than an unstrained MOSFET.

1.1. Fundamentals of Strain Technology

A way of improving MOSFET transistors performances is to change the properties of materials used in their conception. The property of silicon to exhibit modified characteristics of transport parameters while strained is used for this purpose [4], [5]. Fundamentally, there are different kinds of strain that are essentially tensile strain and compressive strain, depending on the lattice constants of two different materials. The value of the lattice parameter of the $Si_{1-x}Ge_x$ alloy at a given Ge composition "x" is determined following the Vegard law and research work of DISMUKES et al [6], which are described by the equations given below:

$$a_{Si_{1-x}Ge_x} = a_{Si}(1-x) + a_{Ge}x \quad (1)$$

$$a_{Si_{1-x}Ge_x} = a_{Si} + 0.200326(1-x) + (a_{Ge} - a_{Si})x^2 \quad (2)$$

The concept of strained Silicon basically relies on an alteration of the equilibrium lattice constant of silicon through externally applied stress. In this case, the electronic band structure of Silicon is changed due to the modified lattice constant. This modification results in superior electronic properties, particularly, the carrier mobilities are enhanced, with the mobility enhancement being a strong function of the magnitude and the direction in which the crystal is stressed.

The fabrication of strained transistors relied heavily on epitaxial deposition of SiGe onto silicon substrates. Conventionally, strain is created by an epitaxial grown of a thin film of Si on a relaxed buffer layer of SiGe alloy, known as a virtual substrate (VS) [7]. The lattice mismatch between the two layers causes biaxial tensile strain in the Si, like it is shown in Figure 1, resulting in improvements of its electrical properties.

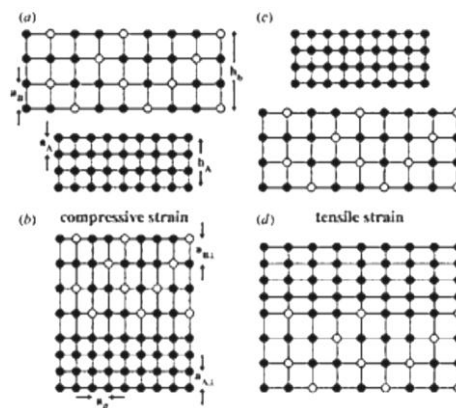


Figure 1. (a) A schematic diagram of the bulk lattice constant of a thin $Si_{1-x}Ge_x$ film to be grown on top of a thin bulk-silicon layer. (b) A schematic diagram showing the tetragonal lattice distortion when the two films from (a) are placed together with the top $Si_{1-x}Ge_x$ film being compressively strained. (c) A schematic diagram of the bulk lattice constants of a bulk-Si film to be grown on top of a bulk- $Si_{1-y}Ge_y$ film. (d) A schematic diagram of the two films in (c) placed together with the top film being tensile strained [8]

When a silicon layer is deposited on a $\text{Si}_{1-x}\text{Ge}_x$ layer, as mentioned before, we notice a symmetry breaking along the axis of growth. The components of the deformation tensor in the silicon layer are given by:

$$\varepsilon_{II} = \frac{a_{\text{Si}_{1-x}\text{Ge}_x} - a_{\text{Si}}}{a_{\text{Si}}} \quad (3)$$

$$\varepsilon_{\perp} = \frac{-2 C_{12}}{C_{11}} \cdot \varepsilon_{II} \quad (4)$$

Where: ε_{II} is the parallel strain deformation following the growth plane (x, y), ε_{\perp} is the perpendicular deformation to the plane of growth (z), $C_{11} = 167$ Gpa and $C_{12} = 65$ Gpa are the elastic constants of Si. The effective mobility is expressed by:

$$\mu_{\text{eff}} = (q \cdot \tau) / m^* \quad (5)$$

Where q: is the charge of carriers, $1/\tau$ the collision frequency of carriers, and m^* : their effective mass. The mobility improvement is due to the reduction of the effective mass m^* that is itself due to the band engineering where the valance band splitting of heavy hole and lightly hole is more significant [13]. This is why there will be more holes to travel with a lighter effective mass.

2. RESULTS AND DISCUSSION

As cited before, different heterostructure substrates can be applied in order to obtain biaxial strain and high mobility channel materials. To do this, epitaxially grown $\text{Si}_{1-x}\text{Ge}_x$ layers on Si bulk wafers are usually applied acting as substrate for a strained silicon layer that grows on the top. In this work, ATHENA and ATLAS from SILVACO TCAD have been used consecutively to simulate the process, and extract the electrical characteristics of a biaxial strained and a strained dual channel heterostructure PMOSFETs.

Silvaco TCAD Tool is used for Virtual fabrication and simulation. ATHENA process simulator is used for virtual fabrication and ATLAS device simulator is used for device characterization. [14]

In order to study with accuracy the impact of strain on device performance, a SiGe layer is introduced in the structure. The new strained device has the same geometrical dimensions, the same S/D doping concentration and a same mesh initialization, which is more refined in the channel region.

In our structures, the doping concentration for bulk Silicon is set at $1 \times 10^{16} \text{ cm}^{-3}$. The p+ S/D regions were formed by an implantation at 20 keV with a dose of $3 \times 10^{15} \text{ cm}^{-2}$. A silicon substrate with crystal orientation $\langle 100 \rangle$ was used in our study due to the better interface between Si/SiO₂. The oxide is diffused into the surface of the strained silicon layer with 930 °C and pressure of 1 atm. Polysilicon is deposited with a phosphorous concentration of $1 \times 10^{16} \text{ cm}^{-3}$. The strained-Si devices were fabricated using strained-Si epitaxial layers grown on relaxed-SiGe by gas source MBE at 800 °C. This is what explains our choice of a temperature of 800 °C which is a very important parameter.

First, we simulated a conventional structure for which a 43.9 nm gate oxide thickness is chosen, for the second device, which is a single channel biaxial strained PMOS, gate oxide thickness is about 10 nm. For this second device, a 15 nm SiGe layer with a proportion of Ge starting at 0 gradually increase to 0.8 is used, a 27.1 nm second layer is deposited on top of the previous one with Ge concentration of 0.9. For the third structure that is a dual-channel biaxial strained PMOS the SiGe layer thickness is equal to 17 nm, a gradually increase of Ge proportion from 0 to 0.5 is used. A 28 nm $\text{Si}_{1-y}\text{Ge}_y$ layer thickness with Ge proportion of 0.8 is deposited on top of the previous layer followed by a thin SiO₂. Lombardi (CVT) Model including N, T, E// and E \perp effects, and Shockley-Read-Hall (SRH) are used in our simulations.

The structures obtained using ATHENA process simulator are using as inputs this time in ATLAS to extract and study the characteristics. By this way, we can analyse and compare the performances of the three structures. The different results of our conventional PMOSFET are given in Figure 2, Figure 3 and Figure 4.

Our conventional PMOS device has a threshold voltage $V_{\text{TH}} = -0.802631 \text{ V}$, subthreshold slope (SS) = 0.341355 mV/decade, $I_{\text{on}} = 5.39836 \mu\text{A}$ and $I_{\text{off}} = 51.2608 \text{ nA}$ at $V_{\text{DS}} = -0.1 \text{ V}$, as shown in Figure 3.

The range of gate voltage chosen is between -1.2 volt and 0 volt, due to the industry needs, to have smaller power consumption and yet nano-devices consume less power, thus this range is chosen also to promote and gain benefits of operating in lower voltage.

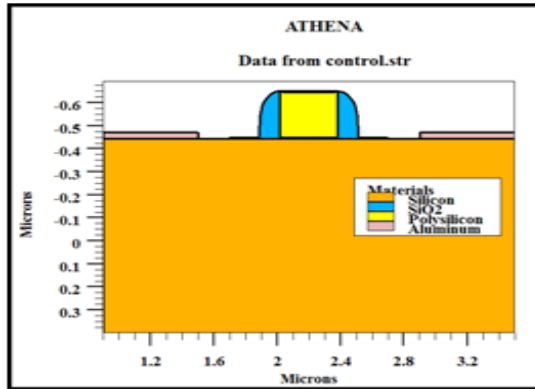


Figure 2. Conventional P-Channel MOSFET structure using silicon and ATHENA module

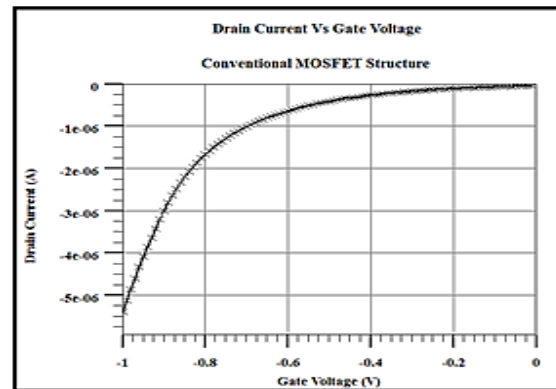


Figure 3. Transfer characteristic for the conventional PMOSFET, obtained using ATLAS Module

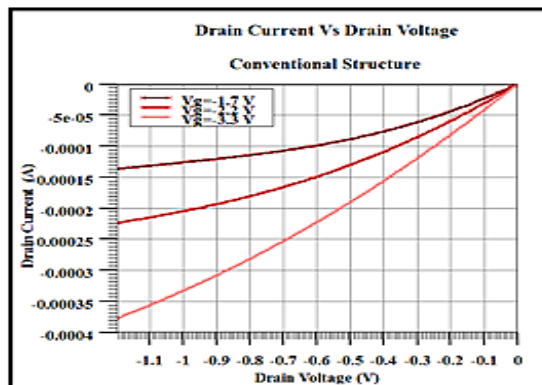


Figure 4. Output characteristics for the conventional structure, obtained using ATLAS module

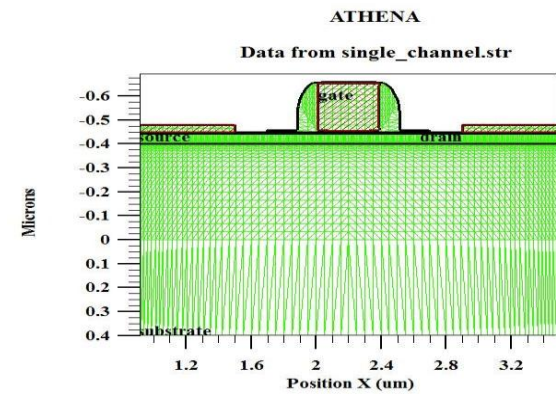


Figure 5. Mesh initialization for the the biaxial strained P-MOSFET, obtained using ATHENA module

Meshing initialization of the strained biaxial p-channel MOSFET, transfer and output characteristics are given in Figure 5, Figure 6 and Figure 7.

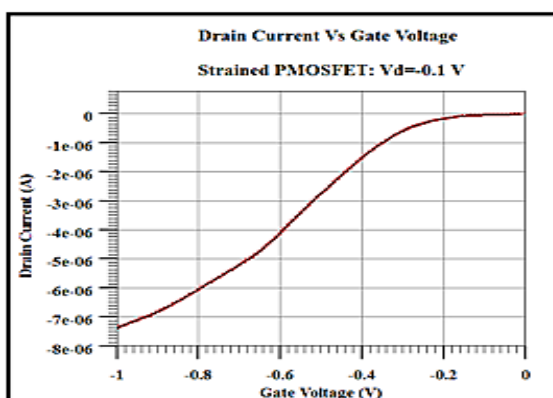


Figure 6. Transfer characteristic for the biaxial strained P-MOSFET, obtained using ATLAS module

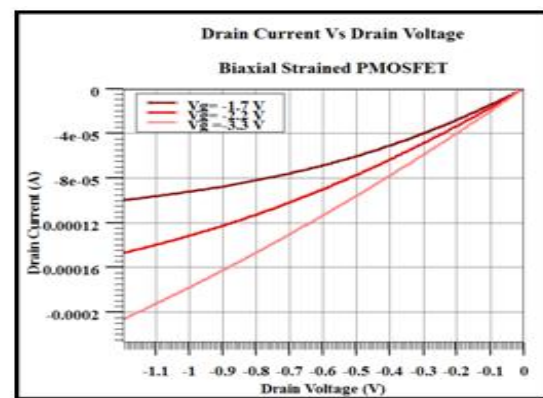


Figure 7. Output characteristics for the Biaxial strained P-MOSFET, obtained using ATLAS module

Our strained biaxial PMOS device has a threshold voltage $V_{TH} = -0.316045$ V, subthreshold slope (SS) = 0.159513 mV/decade, $I_{on} = 7.37086 \mu A$ and $I_{off} = 20.7883$ nA at $V_{DS} = -0.1$ V, as we can see in Figure 6.

Meshing initialization, transfer and output characteristics of the strained dual channel heterostructure p-channel MOSFET studied are given in Figure 8, Figure 9 and Figure 10.

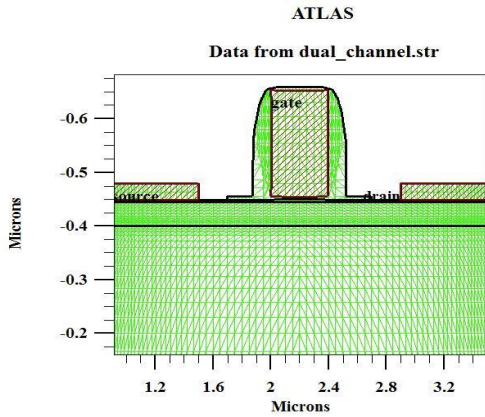


Figure 8. Mesh initialization for the dual channel heterostructure P-MOSFET, obtained using ATLAS module

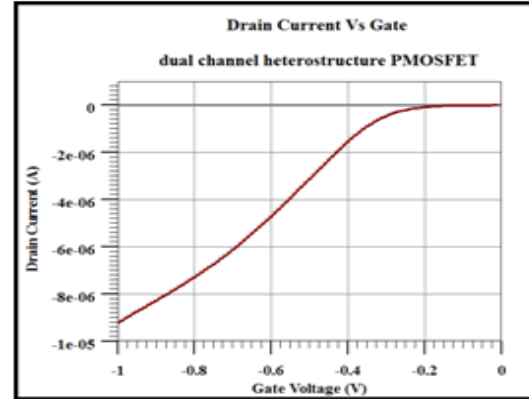


Figure 9. Transfer characteristic for the strained dual channel heterostructure P-MOSFET, obtained using ATLAS module

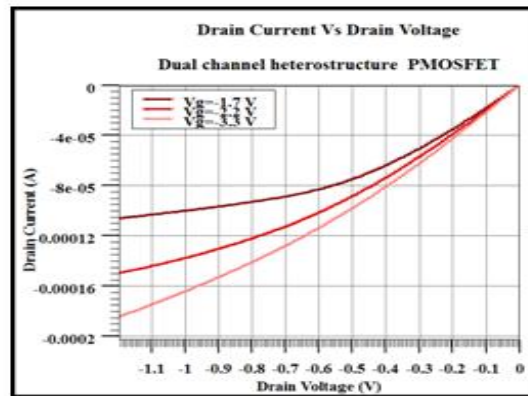


Figure 10. Output characteristics for the strained dual channel heterostructure P-MOSFET, obtained using ATLAS module

Our strained dual channel heterostructure PMOS device has a threshold voltage $V_{TH} = -0.309853$ V, subthreshold slope (SS) = 0.13159 mV/decade, $I_{on} = 18.1771 \mu A$ and $I_{off} = 8.84222$ nA at $V_{DS} = -0.1$ V, as we can see in Figure 10.

The following table: Table 1 compares between the results obtained in the three structures:

Table 1. Comparison between the results obtained in the three structures simulated

Structure	Threshold voltage (V _{th})	Drive current (I _{on})	Leakage current (I _{off})	Subthreshold Slope (SS)
Conventional	-0.802613 V	5.39836 μA	51.2608 nA	0.341355 mV/Dec
Biaxial Strained	-0.316045 V	7.37086 μA	20.7883 nA	0.159513 mV/Dec
Dual strained channel Heterostructure	-0.309853 V	18.1771 μA	8.84222 nA	0.13159 mV/Dec

Our results allow comparing our devices characteristics. We can see the I_{on} current increasing, I_{off} current decreasing are two very important achievements allowing to have a faster switching devices especially

for digital circuits applications. This improvement results can be explained by effective mobility improvement. As the drain current is proportional to channel mobility, this current also increases and is higher for strained silicon PMOS transistors compared to conventional ones. These support the equation below for the relationship between current and mobility, as well as drain bias increment:

$$I_d(\text{lin}) = \mu \cdot C_{ox} \cdot \frac{W}{L} \left(V_G - V_T - \frac{V_d}{2} \right) \cdot V_d \tag{6}$$

$$I_d(\text{sat}) = \frac{1}{2} \mu_{\text{eff}} \cdot C_{ox} \cdot \frac{W_{\text{eff}}}{L_{\text{eff}}} (V_G - V_T)^2 \tag{7}$$

μ is the channel carrier mobility, W is transistor's width, L is transistor's length, and C_{ox} the oxide capacitance.

In this part of our work, we focused our efforts on the universal part of the mobility curve. This mobility improvement is well illustrated in Figure 11 and Figure 12, where we can notice a considerable enhancement of mobility in single biaxial strained P-MOSFET compared to the conventional P-MOSFET and an extra improvement of it in the dual channel heterostructure P-MOSFET. An important improvement is achieved at $V_{gs} = -1.25$ V, with the values of about: 425, 575 and 725, which constitutes an important improvement of 35.29 % and 70.59 % respectively.

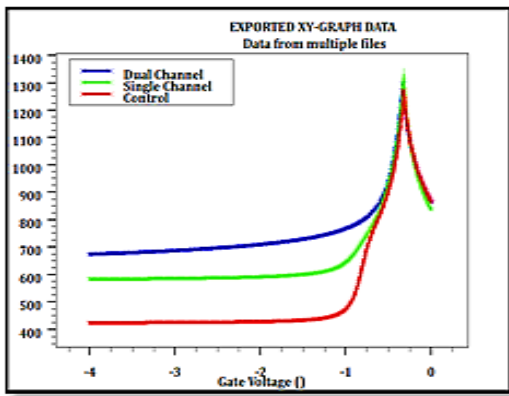


Figure 11. Comparison of mobility versus gate voltage obtained in the three different structure using ATLAS module

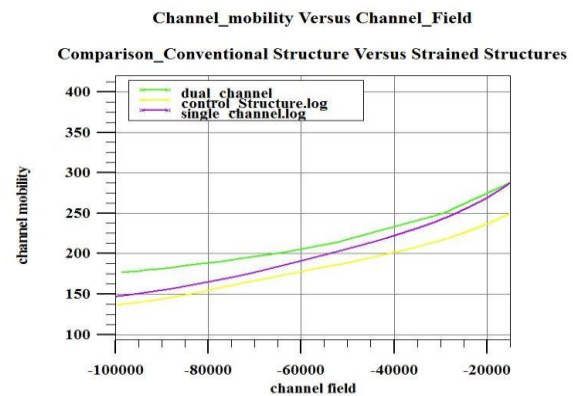


Figure 12. Comparison of mobility versus channel field obtained in the three different structure using ATLAS module

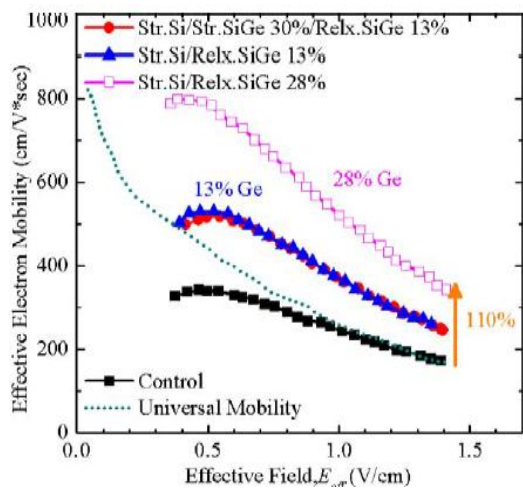


Figure 13. Effective Electron Mobility versus Effective Field in conventional structure and different strained structure using different Ge percentage content [11]

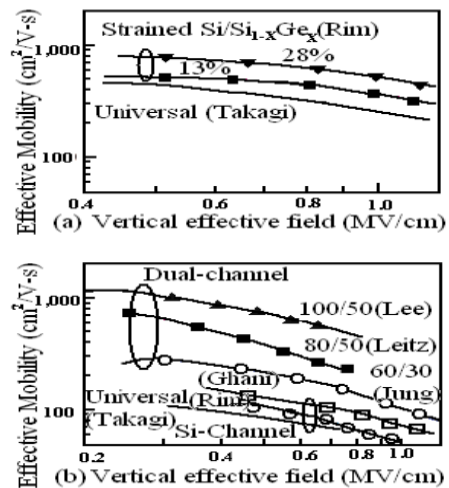


Figure 14. Measured electron mobility enhancement in strained-Si MOSFET comparing to the Si-channel MOSFET and the extra enhancement in the dual-channel structure [12]

Figure and Figure show output curves, with an improvement obtained for the biaxial strained MOSFET and an extra improvement with the dual channel heterostructure PMOFET.

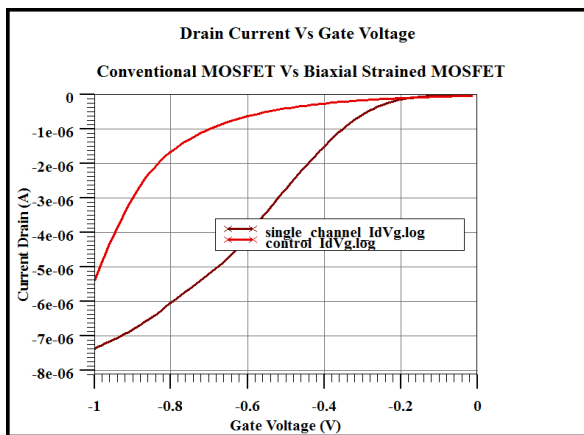


Figure 15. Comparison between the transfert characteristics obtained in conventional and biaxial strained MOSFET

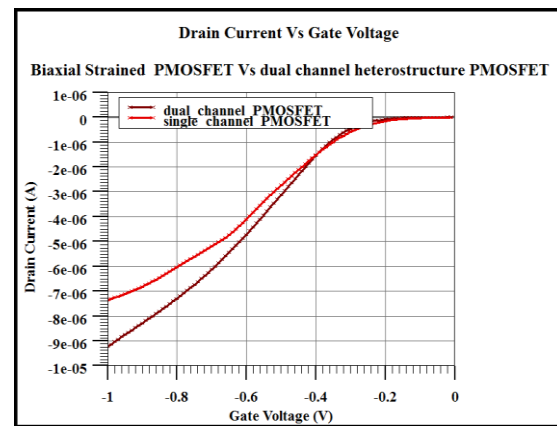


Figure 16. Id/Vgs Extraction of biaxialstrained PMOSFET and dual channel heterostructure PMOSFET

Our different results allow appreciating different improvements obtained using dual channel heterostructure PMOSFET compared to a single channel and conventional P-channel MOSFETs.

In the literature we can find very important articles on the improvements brought about by the use of the strained silicon or the importance of using the heterostructure [9], [15], but the majority of the works concentrate on the physics and the operation principle as well as the improvements in terms of mobility. The particularity of our work is that it also covers other important parameters that contribute to good DC analysis of strained devices. This analyse allow to give more clear ideas about what is expected after using the technology of strain silicon.

3. CONCLUSION

Scaling has increased transistor performance, allowing displaying enhanced electrical properties such as mobility enhancement and lower threshold voltage, in the same way strain techniques allow boosting performance further in future generations of CMOS transistors without the necessity to radically scale transistor dimensions. The combination of strain techniques with other options, such as Multiple Gate MOSFETs, high-k materials, is generally used to keep on track with Moore's law. In this paper, impact and benefits obtained with the use of strained silicon technology on a single p-channel MOSFET and a double gate P-MOSFET have been presented. The different results we obtained allow first to show mobility increases of carriers in the channel of our strain device. The increase of the carrier mobility in the channel that is implemented by a correct silicon strain allows providing a higher current drive. The results obtained in terms of output, transfer characteristics, and leakage current highlight the importance of incorporating strain technology in MOSFET transistors, and confirm what researchers report. We conclude that the use of strain silicon technology is very important to improve considerably the mobility of carriers and as results the device performances while maintaining the same structure and device process of MOSFETs. At the end of our study, we can conclude that strain techniques introduction has been able to extend the Moore's law for nanometer of CMOS generations. This technique has become nowadays the most successful technique for the state-of-the-art planar CMOS technologies.

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BIOGRAPHIES OF AUTHORS



Mr. Amine Mohammed Taberkit was born in Tlemcen in 1988. He became an Electronic Engineer in 2010 from the university of Tlemcen, he got the master degree in Electronic instrumentation in 2012 from the university of Tlemcen, and actually, he is a PhD Student at the university of Tlemcen and a member of the research Unit of Materials and Renewable Energy Research (URMER). His research interests include Strain Silicon Technology and MOSFET transistors. Email: taberkit.amine@yahoo.fr



Pr. Ahlam Bouazza-Guen was born in Tlemcen in 1965. She received the B.S degree in Electronic Engineering in 1988 from Oran university, her MSc degree In 1992, her PhD degree in Microelectronics in 2007 from Tlemcen university. She is a professor with the engineering department and Research team leader at the research Unit of Materials and Renewable Energy (URMER). Her research interests include MUGFET devices, CMOS analog/mixed ICs and interconnects. E-mail: guenahlam@yahoo.fr



Pr. Benyounes Bouazza is a professor in AbouBekrBelkaid University, Tlemcen, faculty of Technology Department of Electronic and Electrical Engineering, also a researcher at the research Unit of Materials and Renewable Energy (URMER), and responsible of the ph.D program of Electronic Instrumentation. E-mail: bouaguene@yahoo.fr