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Low Power CMOS Electrocardiogram Amplifier Design for Wearable Cardiac Screening

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ABSTRACT

The trend of health care screening devices in the world is increasingly towards the favor of portability and wearability. This is because these wearable screening devices are not restricting the patient's freedom and daily activities. While the demand of low power and low cost biomedical system on chip is increasing in exponential way, the front-end electrocardiogram (ECG) amplifiers are still suffering from flicker noise for low frequency cardiac signal acquisition, 50Hz power line electromagnetic interference, and the large unstable input offsets due to the electrode-skin interface is not attached properly. In this paper, a CMOS based ECG amplifier that suitable for low power wearable cardiac screening is proposed. The amplifier adopts the highly stable folded cascode topology and later being implemented into RC feedback circuit for low frequency DC offset cancellation. By using 0.13µm CMOS technology from Silterra, the simulation results show that this front-end circuit can achieve a very low input referred noise of $1pV/Hz^{1/2}$ and high common mode rejection ratio of 174.05dB. It also gives voltage gain of 75.45dB with good power supply rejection ratio of 92.12dB. The total power consumption is only 3µW and thus suitable to be implemented with further signal processing and classification back end for low power wearable biomedical device.

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1. INTRODUCTION

Cardiovascular disease is the number one killer disease in Malaysia. Although sudden cardiac arrest is the main cause of death, the Malaysian awareness of towards cardiovascular disease is still low. Having threatened by the cardiovascular disease in among the middle age to old people is very worrying especially when these people are staying alone or have no relatives staying nearby to him or her. While sudden cardiac arrest is the main cause of death due to the sudden stop-functioning of the heart [1], the case is even worst when the patient is staying alone where nobody is aware of the patient's mortality. To reduce the risk of fatality, continuous monitoring of the electrocardiogram (ECG) signal and analyzing the heart rate variability (HRV) is desired in public community for early prevention as well as emergency treatment of serious heart diseases. Hence, it is important to make a complete cardiac screening system on chip (SoC) that is suitable to be used with the wearable devices and internet of things (IoT).

The trend and demand in the health care devices is increasing towards more portability and less patient mobility restriction as compared to the previous year, especially in this era where the emerging of IoT is very promising in near future. In the last few decades, the introduction of full system on a silicon chip (SoC) has introduced the world to the low power small size devices, which has been evolved to today's ultra low power wearable device. With the advancement of complementary metal oxide semiconductor (CMOS)

technology, this SoC has enabled the implementation of biomedical signal acquisition and processing such that the cardiac signal monitoring.

The existing one lead ECG front-end amplifiers are very prone to noisy environment such as 50Hz powerline magnetic field interference, causing the signal is being interfered with the powerline noise [2]-[5]. As the heart signal is a low frequency signal, flicker noise at low frequency is also very prominent in the circuit output. Large and unstable input offsets due to impedance between electrodes and skin causes the amplifier to be saturated easily. These noise and offset are not suitable to be used for wearable monitoring system implementation. [2], [4], [5]. Therefore, a low noise and low power amplifier circuit is required for a future realization of a SoC ECG monitoring system. This paper proposed a front-end ECG amplifier by using a standard 0.13µm CMOS technology from Silterra with power supply of 1.2V.

2. CIRCUIT IMPLEMENTATION

ECG signal is a systematic electrical signal that is generated by the heart muscle to trigger the heart pumping activity or the cardiac cycle rhythmically and precisely. Typical cardiac signal strength is ranged between 5µV to 8mV while its frequency is ranged at 0.05Hz to 250Hz. This work focuses on designing a front-end CMOS amplifier circuit that is capable to detect this weak ECG signal while achieving low power and low noise circuit performance. Several considerations are counted into the amplifier design in order to eliminate the noise such as the transistor's threshold biasing and circuit approach to get highest common mode rejection ratio (CMRR).

2.1. Subthreshold biasing

Subthreshold biasing of the transistors can reduce the transistor noise and the power consumption as the minimum operating voltage can be achieved [6]. In fact, it is getting more attention in biomedical amplifier research in recent times due to the ability to design ultra-low power sensors and amplifiers for low frequency applications [7], [8]. Sub-threshold equation for transconductance in sub-threshold region is shown in Equation (1).

$$g_m = \frac{1}{NV_T} I_D \quad (1)$$

Equation (1) shows that the transconductance of the transistor is linearly proportional to the biasing current I_D rather than proportional to square root I_D. Thus, lower current can be used to achieve the same amount of transconductance and gain of the amplifier leading to low power design.

Equation (2) shows the drain current of the transistor in subthreshold operation where I_{DO} is the current when $V = V_T$. The current is directly proportional to the aspect ratio of the transistor, as similar to the transistor operation in saturation region, shown in Equation (3).

$$I_D = I_{DO}\left(\frac{W}{L}\right) e^{[V_{gs} - V_T\left(\frac{q}{nkT}\right)]} \quad (2)$$

$$I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{gs} - V_T)^2 \quad (3)$$

2.2. Design topology

Folded cascode operational amplifier was used as the input signal amplifier design topology. This is because folded cascode topology achieves single pole, stable phase margin, and higher swing while maintaining the same gain as the telescopic cascode amplifier topology [9]. The folded cascode amplifier can also able to achieve low power consumption and low noise design [10], [11]. PMOS transistor was used as the input transistors because it can achieve higher CMRR and lower flicker noise since the flicker noise is inversely proportional with the size of the transistor [12].

Figure 1 shows the proposed folded cascode operational amplifier with self-biasing circuit. This design uses PMOS amplifier as the input and the modified current mirror to eliminate the extra threshold voltage used in the headroom. The design parameters was started by allocating biasing current to the branches of the transistors. After that the minimum drain-to-source voltage or overdrive voltage of the transistors was set by using initial guess based on the allocated current to the branches. Higher overdrive voltage was given to M_{bs} and $M_{5,6}$ as they need to drive more current comparing to other transistors. Design performance optimization was done by repeatedly changing the sizing aspect ratio and the biasing current until the performance specification is met. Subthreshold transistor biasing was made possible as the cardiac signal frequency is low and the noise can be reduced.

The transistors' aspect ratio were shown in Table 1. As can be seen from the table, the transistors sizing ratio especially near to the power supply and input section are larger to eliminate the flicker noise and increase the CMRR as much as possible. Larger input transistors size ratio is also contributing to a higher gain due to the transconductance g_m is directly contributing to the gain of the amplifier. The biasing current is set to 250nA at the voltage supply, V_{DD} of 1.2V. Finally, the designed transistor circuit was then encapsulated into an op-amp circuit with the instrumentation amplifier connection to test its functional and the performance such as gain, phase margin, CMRR, power supply rejection ratio (PSRR) and noise.

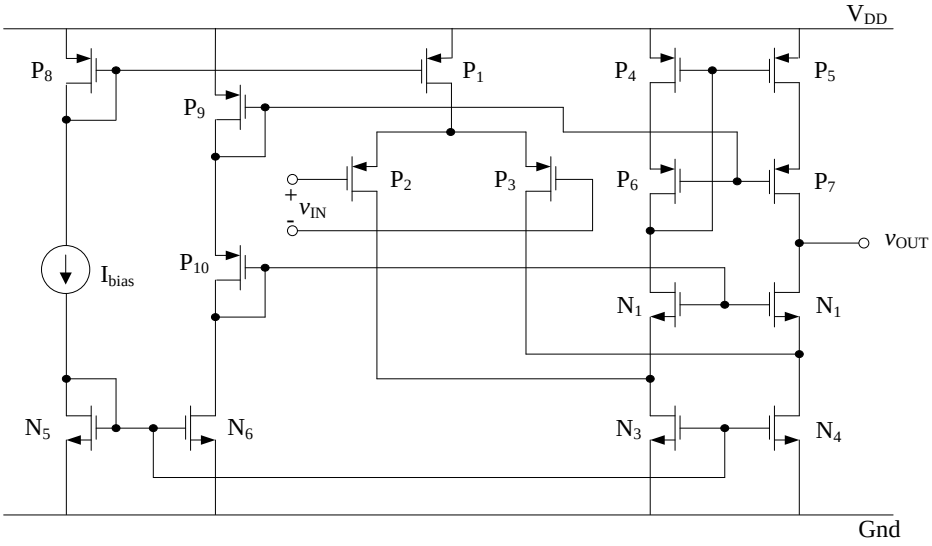

Figure 1. Self-biased folded cascode amplifier circuit

Table 1. Transistor Sizing Ratio

Transistor	P1	P2-P3	P4-P5	P6-P7	P8	P9	P10	N1-N2	N3-N4	N5-N6
Aspect ratio (*W/L*)	10.6/1	60/1	30/3	20/1	2.5/1	1.25/1	15/1	10/1	11/1	2.5/1

3. RESULTS AND DISCUSSION

All results are simulated using Cadence Electronics Design Automation (EDA) tools. Virtuoso Analog Design Environment L was used for circuit schematic design simulation works and Virtuoso Visualization & Analysis XL was used to plot the signal waveforms and measurements.

3.1. Transient response

The output transient waveform of the circuit is simulated to ensure that the amplifier is working when the input is low peak-to-peak voltage, V_{p-p} and the swing is not saturated when the input is high V_{p-p}. The simulated output swing of $1.018V_{p-p}$ is observed when the input voltage is at maximum swing of $20mV_{p-p}$, meanwhile output swing of $0.6mV_{p-p}$ is obtained when the input voltage maximum swing is at $10\mu V_{p-p}$.

From the simulation, it is found that the optimized circuit can succesfully response to different frequency and amplitude within the range from 0.05 Hz to 250 Hz and 5 µV to 10 mV respectively which means able to support the cardiac signal characteristics range. The DC biasing point is set at 0.6 V for maximum voltage swing.

3.2. AC response

The circuit ac response was simulated using the Middlebrook's method [13]. This is because this method can achieve stable DC operating point and the loop gain can be obtained by directly calculating the voltage gain. Figure 2 shows the simulated ac response of the amplifier. The circuit can achieve gain of 75.45dB, phase margin of 80.9^o, unity gain bandwidth (GBW) of 667.5kHz, and -3dB frequency of 128.82Hz. The load capacitor of the amplifier is 1pF.

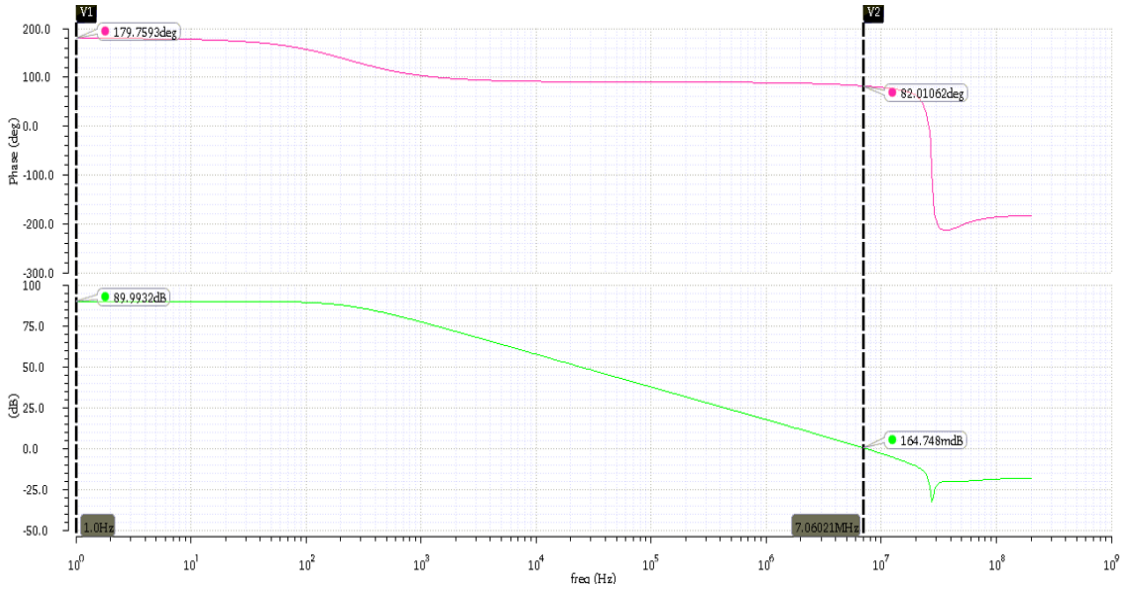

Figure 2. AC response of amplifier circuit. Upper graph shows the phase response and lower graph shows the gain response

3.3. Circuit performance

The common mode rejection ratio (CMRR) of the circuit is defined as the ratio of the differential gain to the common mode gain and is calculated based on the following equation.

$$CMRR = 20log\frac{A_d}{A_c} \quad (4)$$

Here, A_c is the common mode gain and A_d is the differential gain of the circuit. The common mode gain simulation was obtained by injecting a common mode signal into both amplifier input and the output ac response is measured. The measured common mode gain is -98.65 dB and the resulting CMRR is 174.05dB.

Power supply rejection ratio (PSRR) of the amplifier is defined as a ratio of the variation of supply voltage to the amplifier to the variation of output voltage the amplifier produces. During simulation, a small sinusoidal voltage of 10mV was placed in series with the supply voltage and the ratio of the power supply variation to the output variation of the amplifier is measured. The obtained PSRR of the amplifier is found to be 92.12dB.

Input referred noise includes the thermal noise and flicker noise. However, the flicker noise is more concern due to the ECG is a low frequency signal. Flicker noise as shown in equation below is inversely proportional to the size of the transistor.

$$\overline{V_n^2} = \frac{K}{f(W/L)C_{ox}} \quad (5)$$

Here, *K* is the transistor flicker noise factor. Figure 3 shows the noise voltage model used to derive the input referred noise.

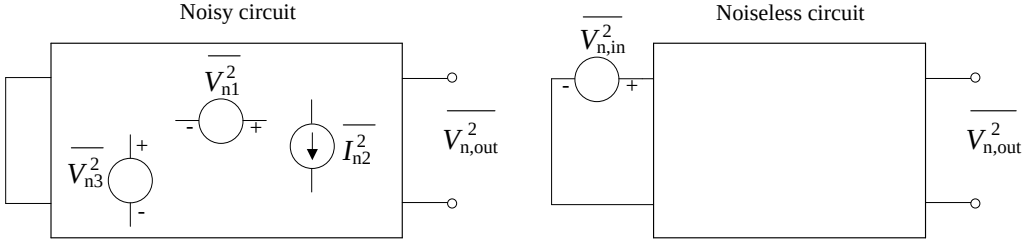

Figure 3. Input referred noise modelling

The input referred noise for the circuit in Figure 1 can be expressed by the equation below.

$$V_n{}^2 = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2g_{m5,6}}{3g_{m1,2}{}^2} + \frac{2g_{m9,10}}{3g_{m1,2}{}^2}\right) + \frac{2K_p}{\left(\frac{W}{L}\right)_{1,2}C_{oxf}} + \frac{2K_p}{\left(\frac{W}{L}\right)_{9,10}C_{oxf}}\frac{g_{m9,10}{}^2}{g_{m1,2}{}^2} + \frac{2K_p}{\left(\frac{W}{L}\right)_{5,6}C_{oxf}}\frac{g_{m5,6}{}^2}{g_{m1,2}{}^2} + \frac{2K_p}{(W/L)_{5,6}C_{oxf}} \quad (6)$$

From Equation (6), K_n and K_p are the flicker noise coefficients for NMOS and PMOS, respectively. It is shown that the *W/L* ratio of the transistors P_9, P_{10}, N_5, and N_6 are critical in reducing the flicker noise as the flicker noise is inversely proportional to the product of the *W* and *L* of the transistor and $g_{m1,2}$ of the input transistors. The *L* was kept minimum to ensure that the capacitance effect of the transistor is as less as possible. Figure 4 shows the input referred noise response of the circuit. The noise was set as a variable during the simulation. It is observed that the input response noise of the circuit is $1.01\text{pV}/\sqrt{\text{Hz}}$.

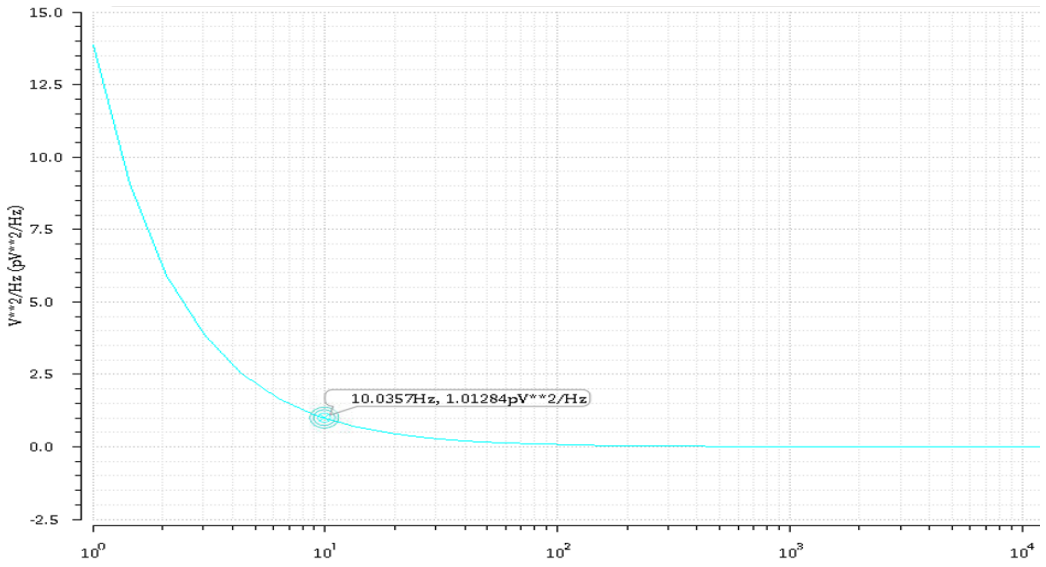

Figure 4. Input referred noise response of designed circuit

3.4. Design performance comparison

The simulated response performance of the designed circuit has been compared with the previous related works. Table 2 summarizes the performance comparison between the proposed design and the previous work. This work has been shown to improve CMRR, PSRR and reduce the noise introduced to the front end amplifier system.

Table 2. Perfomance Comparison

Parameter	This work	[10]	[12]	[14]	[15]
Technology (µm)	0.13	0.09	0.18	0.18	0.18
Supply voltage (V)	1.2	1.0	1.8	1.8	0.9
CMRR (dB)	174.05	131	71	124	107
PSRR (dB)	92	70.7	n/a	65	n/a
Input referred noise ($V/Hz^{1/2}$)	1p	138n	17.2µ	160n	0.68µ
Gain (dB)	75.4	48	54.5	20.12	116
UGB (Hz)	667.5k	15.3k	1M	90.25M	100k
Phase margin (degree)	80	69.46	n/a	n/a	57
Power consumption (W)	3µ	2.6µ	5.51µ	520µ	46.8µ

4. CONCLUSION

A low power and low noise with high CMRR and PSRR cardiac signal amplifier is presented to improve the noise issue known in a cardiac signal. The amplifier achieves gain of 75.4dB, phase margin of

80^o, CMRR of 174.05dB, PSRR of 92dB, and input referred noise of $1.01 pV/\sqrt{Hz}$. This amplifier design can achieve lower power consumption of 3µW which is comparable to previous works and also suitable to be implemented into a SoC design.

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