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Little Core Based System on Chip Platform for Internet of Thing

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ABSTRACT

Although the technology scaling has enabled designers to integrate a large number of hardware blocks onto a single chip realizing System on Chip (SoC), problems arising from leakage current have made power reduction an important issue. The internet of thing (IoT) platform has restricted power consumption because of battery power. In this paper, we propose our little core based IoT platform focusing on the low power and expandability. The experimental results demonstrate the feasibility of our proposal to the IoT.

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1. INTRODUCTION

Modern Internet of Thing (IoT) allows that object is organized on the network using the small IoT platform. The wireless communication is usually used as a network of IoT, and it transmits a small packet with a device status. Even though the technology scaling has enabled designers to integrate a large number of hardware blocks, the unnecessary hardware is not required because it increases the leakage current of the processor. The low power consumption is more important rather than high performance because most of IoT platform has restricted power budget for small battery. The Cortex-M0 processor has low power properties which use smaller gate count.

Modern IoT system and wearable devices have been studied using diverse wireless network [1-4]. The data communication among objects realizes ubiquitous computing and various user experience applications [5-10]. On these studies, the sensor node usually uses a microprocessor which includes restrictive hardware peripheral. The FPGA has flexibility and can implement an expandable system. Also, core and peripheral system have important properties about low power consumption. The power efficiency of the system components and the other peripherals has been studied for this purpose [11-14].

In this paper, we implement an IoT platform that includes a Cortex-M0 processor, AHB-Lite bus interface, memory controller, RS-232 communication module, and VGA controller.

The rest of our paper is organized as follows. We first briefly introduces the features of the Cortex-M0 DS based IoT platform in section 2, and present the hardware implementation of our prototype in Section 3. Section 4 shows the experimental result and Section 5 concludes this paper by outlining the direction for future work on this topic.

2. IoT PLATFORM

The IoT platform consists of the little core, the system bus and the peripherals. The Cortex-M0 core is low power 32 bit microprocessor that has 12K gates and the maximum operating frequency is under 100MHz. This core cannot construct the IoT platform by oneself. The system bus and the peripherals are required to support the operation of the core. Most of the IoT system, the peripherals include the network interfacing hardware for the communication. The wireless communication is used on the IoT system to communicate with the other devices. In this network, the expandability is more important rather than high speed communication.

The Operating System (OS) is required because it is helpful for handing the packet to the network. The Linux is a general purpose operating system that has been ported on various processors. However, it requires a high performance processor and Memory Management Unit (MMU) hardware. The Cortex-M0 core is little core and it does not contain MMU. Therefore, our system adopts a uC/OS-II real time kernel that supports up to 64 tasks. In addition, it supports TCP/IP ethernet packet library for the network.

2.1. Processor and System Bus

ARM Corporation is providing the Cortex-M0 Design Start (Cortex-M0 DS) core, and it operates at 50MHz frequency. The basic Cortex-M0 core has various options for optimization such as the performance of multiplier, the number of interrupt, and the JTAG interface. However the Cortex-M0 DS core includes the simplest hardware. Multiplier takes 13 clocks for each multiplications, the number of interrupt is fixed at 32, and does not use JTAG. The Cortex-M0 DS has weakness on performance optimization, but it has a smaller gate count rather than the Cortex-M0 core. It is suitable for small sized low power processor.

Also, this little core is synthesizable in an FPGA and it can organize a processor that contains flexible peripherals. The FPGA enables configuring the system bus and the peripheral hardware. The Cortex-M0 DS core uses AMBA AHB-Lite system bus to control 4GB address space and it enables only one master device. In this system, arbitration is not required and it is helpful to reduce power consumption. The Direct Memory Access (DMA) hardware cannot be used on the system bus because the system bus does not allow the master device except the Cortex-M0 DS core. This is a weakness in terms of data processing even though the IoT platform does not deal with big data.

2.2. Peripheral System

The peripheral system supports the operation of the core. The Figure 1 illustrates the block diagram of the memory subsystem. The ROM is a read-only area that stores a binary file. The core reads the code from the ROM, and the temporary data is stored in the RAM. These memories are implemented by using internal memory of the FPGA to support high performance. It has a dependency on the inherent structure of the FPGA such as a memory size and a memory interface. The memory subsystem uses quad 8 bit memory blocks because the Cortex-M0 DS core uses byte addressing. The write byte enable signal is asserted according to the byte address of AHB-Lite write command. On the other hand the read data returns 32 bits and ignores byte address. The core internally uses the necessary bytes among these 32 bits.

The USART uses RS-232 protocol and it supports up to 115200bps to communicate with the other devices. It collects a required data from other devices or transmits data to the host PC. The USART has FIFO in order to enhance the slow communication speed compared to the system bus. This communication hardware can be implemented on FPGA. On the other hand, almost of wireless communication uses analog

hardware, and which cannot be integrated on the FPGA. This analog hardware is available as an external module, and the USART could be used for controlling the module.

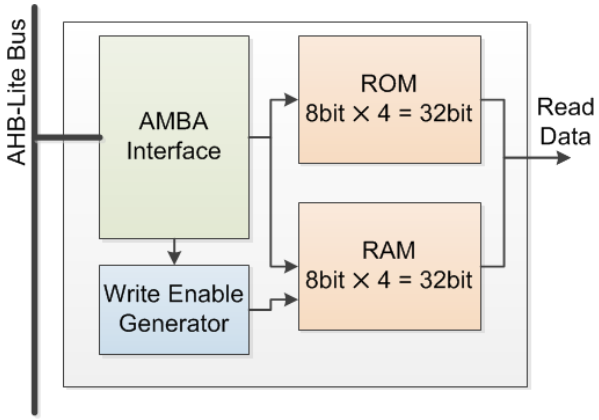

Figure 1. Block diagram of memory subsystem

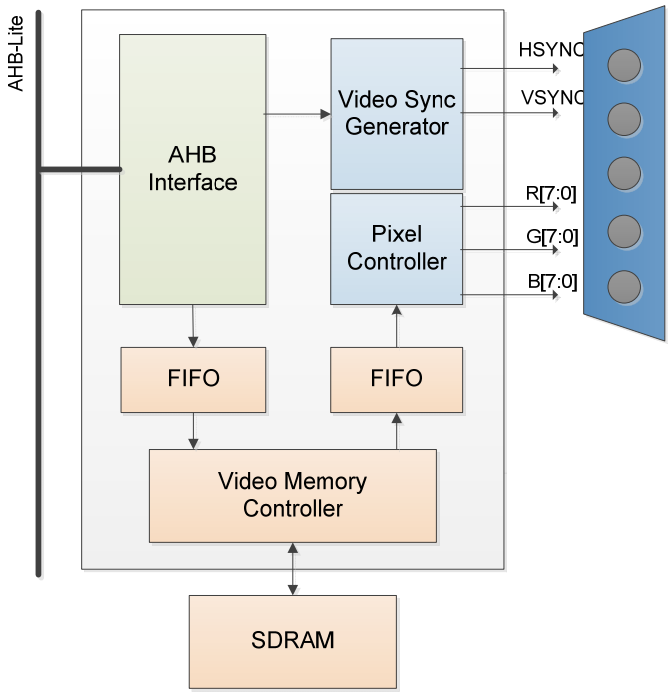

Figure 2. Block diagram of VGA controller

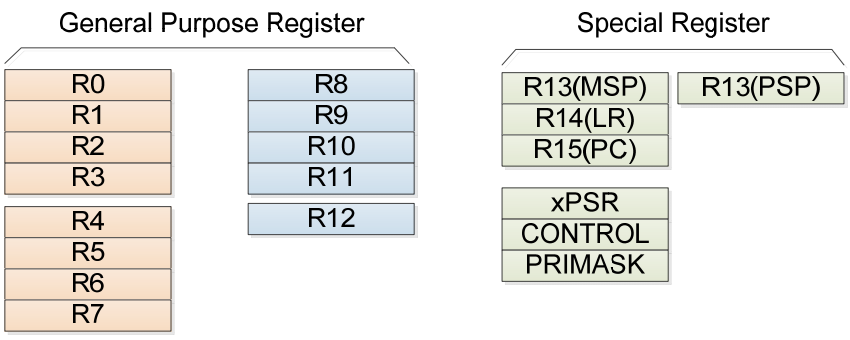

Figure 3. Register bank of Cortex-M0 DS core

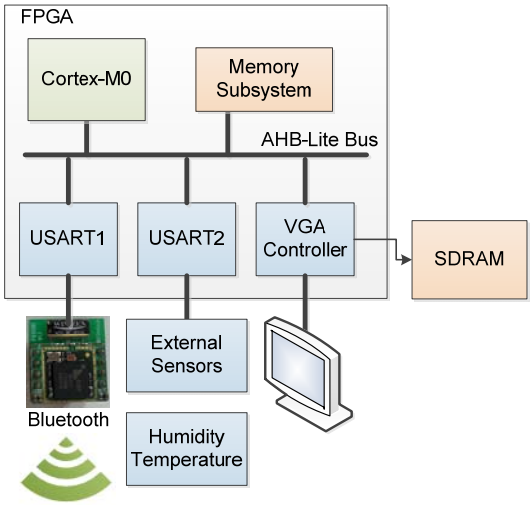

Figure 4. Implemented IoT platform

Even though the VGA controller is not an essential unit on the IoT system, it supports the visualization of system status (See Figure 2.). The maximum resolution is 640×480 and it supports 24 bit true color. The VGA controller has image buffer that stores each image frame. On the IoT platform, the image buffer uses SRAM or SDRAM. The SDRAM is slower than SRAM, however it has a high capacity and cheaper than the other memories. The image buffer size should be larger than frame size of an image. Therefore, the minimum size of the image buffer is 900Kbytes.

2.3. Operating System

The uC/OS-II is a kind of real-time OS that has been ported on the various processors. This operating system uses a small kernel and it does not require the MMU. The number of maximum task is up to 64, and the reserved task is configured according to the software application. The implemented task is initialized when the start of an operating system. The task initialization sequence should be ported according to the architecture of the core. Figure 3 shows a register of the Cortex-M0 core. It consists of 13 general purpose register and some of special registers. The stack of task is have to prepare the memory space for context switching. However, in case of Cortex-M0 DS core, the general purpose register 8 to 12 is not used in the context switching. It is important for kernel porting sequence. The context switching operation has to prepare space for a general purpose register region, which includes from 0 to 7, the special purpose register region and the stack pointer region.

3. IMPLEMENTATION

We adopt the Altera DE1 board [15] for implementation of the IoT platform whose features include Altera Cyclone II FPGA, 8MB SDRAM. The implemented hardware is available for download as a pre-configured Verilog HDL. Our system includes a Cortex-M0 DS core, an AMBA AHB-Lite system bus, a memory subsystem, a USART and a VGA controller (See Figure 4). Cortex-M0 DS core is provided by ARM, and it does not support any hardware configuration options such as multiplier, number of interrupt and JTAG interface. AMBA AHB-Lite system bus divides the 4GB addressing space to support multiple slave devices. The arbitration hardware is not required because of supporting only one master device. The memory subsystem contains the 128 KB ROM and the 32 KB RAM. These memory capacities are adjustable depending on the internal memory size of the FPGA. There are two communication channels; USART1 transmits data through the wireless module and USART2 is collecting data for transmission. The VGA controller is visualizing the status of system via external LCD monitor. The VGA controller integrates an SDRAM controller which operates at 100MHz frequency.

4. EXPERIMENTAL RESULT

In order to program the binary code for Cortex-M0 DS core, a pre-compiled binary file is required that includes the uC/OS-II kernel and the applications. Figure 5 shows our experimental environment which consists of the FPGA which configured IoT platform, the Bluetooth module, the sensor module, and VGA connector. On the test application, the IoT platform collects the temperature and humidity data from external sensors via the USART2. Then, the collected data is packetized and transmitted through the USART1 and wireless communication module. Optionally, the VGA controller can display the image on a VGA monitor. However, it takes about 1 second to display an image because the core is too slow. If this platform does not have an operating system, displaying time of image might be an obstacle to real time application. However data transmission is stable because the uC/OS-II kernel handles each task in real time. Therefore, this is an appropriate platform for real time application such as data collection module of IoT system.

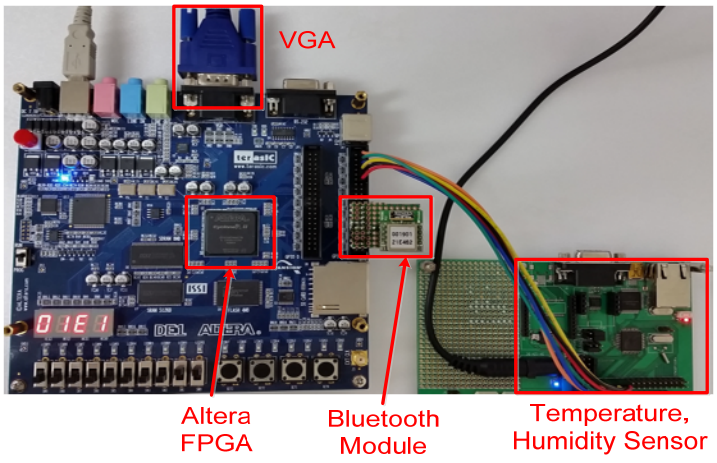

Figure 5. Photograph of our validation environment

5. CONCLUSION

In this paper, we present our IoT platform which consists of the Cortex-M0 DS core, system bus, and principal peripherals focusing on low power capability and the expandability. The USART communication module collects a data and transmits data to the wireless communication module such as Bluetooth or Wi-Fi. This system can be connected to IoT network, and used as a fundamental system for sensor node. The implemented system contains the necessary hardware to minimize leakage current, and the FPGA synthesizable AHB-Lite system bus enables additional hardware implementation to provide expandability. The uC/OS-II real-time kernel controls peripherals according to priority. In the future, we plan to integrate more synthesizable peripherals to control diverse sensor networks.

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