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Active Gate Drivers for High-Frequency Application of SiC MOSFETs

By

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A mi madre,

María Luisa Camacho Ramos

Abstract

The trend in the development of power converters is focused on efficient systems with high power density, reliability and low cost. The challenges to cover the new power converters requirements are mainly concentered on the use of new switching-device technologies such as silicon carbide MOSFETs (SiC). SiC MOSFETs have better characteristics than their silicon counterparts; they have low conduction resistance, can work at higher switching speeds and can operate at higher temperature and voltage levels. Despite the advantages of SiC transistors, operating at high switching frequencies, with these devices, reveal new challenges. The fast switching speeds of SiC MOSFETs can cause over-voltages and over-currents that lead to electromagnetic interference (EMI) problems.

For this reason, gate drivers (GD) development is a fundamental stage in SiC MOSFETs circuitry design. The reduction of the problems at high switching frequencies, thus increasing their performance, will allow to take advantage of these devices and achieve more efficient and high power density systems.

This Thesis consists of a study, design and development of active gate drivers (AGDs) aimed to improve the switching performance of SiC MOSFETs applied to high-frequency power converters. Every developed stage regarding the GDs is validated through tests and experimental studies. In addition, the developed GDs are applied to converters for wireless charging systems of electric vehicle batteries. The results show the effectiveness of the proposed GDs and their viability in power converters based on SiC MOSFET devices.

Keywords

Electromagnetic interference	Silicon carbide
High frequency converters	SiC MOSFETs
Gate drivers	Wide-bandgap devices

Resumen

La tendencia en el diseño y desarrollo de convertidores de potencia está enfocada en realizar sistemas eficientes con alta densidad de potencia, fiabilidad y bajo costo. Los retos para cubrir esta tendencia están centrados principalmente en el uso de nuevas tecnologías de dispositivos de conmutación tales como, MOSFETs de carburo de silicio (SiC). Los MOSFETs de SiC presentan mejores características que sus homólogos de silicio; tienen baja resistencia de conducción, pueden trabajar a mayores velocidades de conmutación y pueden operar a mayores niveles de temperatura y tensión. A pesar de las ventajas de los transistores de SiC, existen problemas que se manifiestan cuando estos dispositivos operan a altas frecuencias de conmutación. Las rápidas velocidades de conmutación de los MOSFETs de SiC pueden provocar sobre-voltajes y sobre-corrientes que conllevan a problemas de interferencia electromagnética (EMI).

Por tal motivo, el desarrollo de controladores de puertas es una etapa fundamental en los MOSFETs de SiC para eliminar los problemas a altas frecuencias de conmutación y aumentar su rendimiento. En consecuencia, aprovechar las ventajas de estos dispositivos y lograr sistemas más eficientes y con alta densidad de potencia.

En esta tesis, se realiza un estudio, diseño y desarrollo de controladores activos de puerta para mejorar el rendimiento de conmutación de los MOSFETs de SiC aplicados a convertidores de potencia de alta frecuencia. Los controladores son validados a través de pruebas y estudios experimentales. Además, los controladores de puerta desarrollados son aplicados en convertidores para sistemas de carga inalámbrica de baterías de vehículos eléctricos. Los resultados muestran la importancia de los controladores de compuerta propuestos y su viabilidad en convertidores de potencia basados en carburo de silicio.

Palabras clave

Controladores de puerta	Interferencia electromagnética
Convertidores de alta frecuencia	Dispositivos de banda ancha prohibida
Carburo de silicio	SiC MOSFETs

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Acronyms

AGD	Active Gate Driver
AMP_1	Amplifier number 1
AMP_2	Amplifier number 2
BJT	Bipolar Junction Transistor
CGD	Conventional Gate Driver
CM	Common mode
$COMP_1$	Comparator 1
$COMP_2$	Comparator 2
EMI	Electromagnetic Interference
EV	Electric Vehicle
FFT	Fast Fourier Transform
GaN	Gallium Nitride
GIR	Gate impedance regulation
GVC	Gate voltage control
GD	Gate Driver
HF	High Frequency
IGBT	Isolated Gate Bipolar Transistor
I_C-driver	Integrated circuit - driver
JFET	Junction Field-Effect Transistor
LV	Low-voltage
MOSFET	Metal-oxide-semiconductor Field-effect transistor
MV	Medium-voltage
PCB	Printed Circuit Board
PHEV	Plug-in Hybrid Electric Vehicle
PWM	Pulse-Width Modulation
SAE	Society of Automotive Engineers
Si	Silicon
SiC	Silicon Carbide
SOA	Safe Operation Area
UVLO	Under voltage
WBG	Wide-Bandgap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Nomenclature

C_{D1}	Equivalent capacitance of the model SiC circuit	pF
C_{iss}	Small-signal input capacitance	pF
C_{oss}	Small-signal output capacitance	pF
C_{rss}	Small-signal reverse transfer capacitance	pF
di/dt	Current slope	A/s
dv/dt	Voltage slope	V/s
g_{fs}	Transconductance	S
I_d	Drain current	A
$I_{d,mod}$	Modified drain current	A
$I_{d,peak}$	Peak drain current	A
L	Inductance load	µH
L_d	Parasitic inductance of the drain leg of SiC MOSFET	nH
L_{loop}	Parasitic inductance on the DC-link	nH
L_g	Parasitic inductance of the gate leg of SiC MOSFET	nH
L_s	Parasitic inductance of the source leg of SiC MOSFET	nH
$R_{ds(on)}$	On resistance of the MOSFET	Ω
$R_{g,ext}$	External gate resistance	Ω
$R_{g,int}$	Internal gate resistance	Ω
$R_{g,off}$	Gate resistance for OFF path	Ω
$R_{g,on}$	Gate Resistance for ON path	Ω
R_{off}	Gate driver resistance for turn-off transition	Ω
R_{on}	Gate driver resistance for turn-on transition	Ω
S_1	Gate driver transistor number 1	---
S_2	Gate driver transistor number 2	---
$V_{1,high}$	Reference 1 of the gate-source voltage in turn-on transition	V
$V_{2,high}$	Reference 2 of the gate-source voltage in turn-on transition	V
$V_{1,low}$	Reference 1 of the gate-source voltage in turn-off transition	V
$V_{2,low}$	Reference 2 of the gate-source voltage in turn-off transition	V
$V_{ctrl,T1}$	Voltage control for T_1	V
$V_{ctrl,T2}$	Voltage control for T_2	V
V_{dc-bus}	DC-bus voltage	V
V_{ds}	Drain-source voltage	V
$V_{ds,mod}$	Modified drain-source voltage	V
$V_{ds,peak}$	Peak of drain-source voltage	V
V_{GG}	Voltage to gate transistors	V
v_{gs}	Gate-source voltage	V
V_{Miller}	Voltage of Miller	V
$t_{d,1}$	Delay time 1	s
$t_{d,2}$	Delay time 2	s
t_{fi}	Current fall time	s
t_{fv}	Voltage fall time	s
t_{ri}	Current rise time	s
t_{rv}	Voltage rise time	s

1

Introduction

This chapter outlines the main content of the thesis. Presents the research topic, research problem and the hypotheses, which are the basis of this Thesis. These three parts are followed by the identification of the research objectives and a description of the Thesis's structure.

CONTENTS:

1.1 Research topic

The trend in power electronic applications is to reach major power density, higher efficiency and reliability with low cost [1]–[3]. In this regard, the new power devices should be able to work at high frequency with lower total losses and work a higher temperature that its predecessors. The use of conventional silicon switching devices limits the development of converters with features that fulfil the requirements of current applications such as battery chargers [4].

The use of Wide-bandgap (WBG) devices is increasing in power converters for medium and high-power applications due to its greater benefices and characteristics than traditional silicon (Si) switching devices. These elements are widely studied and its advantages and drawbacks have been deeply discussed in the literature [5]–[8]. Hence, the silicon carbide (SiC) and gallium nitride (GaN) devices are outlined as the current best solution to cover the requirements for achieving highly efficient power converters [9]–[11].

Although the WBG devices have better features than silicon devices, both SiC and GaN semiconductors have different properties that need to be considered in their respective in converter designs. Although GaN devices present overall better characteristics than SiC devices, current market availability of GaN technology is limited and its costs of implementation are fairly high compared to their SiC counterparts. Moreover, the limited current and voltage (<650V), is a limitation when developing power converters in applications with power greater than 3 kW. In this regards, SiC devices are a more mature technology and have been already used in different industrial applications, such as renewable energy [2], [12], [13], induction heating [7], drives for electrical machines [14], [15], power converters and battery chargers for plug-in hybrid electric vehicles (PHEVs) and Electric Vehicles (EVs) [16]–[19].

One of the challenges for the new power converters based on SiC devices such as BJTs, JFETs, MOSFETs and even IGBTs, is reaching better performance and reliability for hard-switching and even soft-switching conditions. In the specific case of the SiC MOSFETs, several studies have shown the advantages for these devices [11], [19], [20], higher operation range of temperature around 150 ºC, low switching losses and the possibility for working at high frequencies (>40 kHz) and high levels of voltage (1200 V and 1700 V). However, despite its advantages, there are challenges that required to be addressed in the power converters design based on SiC MOSFETs. Protection of the device, EMI filters, thermal management and gate drivers are important issues to achieve complete integration of silicon carbide MOSFETs and reduce the problems presented in the power devices when they working at high-frequency.

This thesis presents the research about problems emerged from the use of SiC MOSFET devices. It is studied the solution for addressed the SiC MOSFETs issues and it is demonstrated the importance of gate driver circuits in power switching devices. Over the course of this Thesis, active gate driver techniques are proposed, designed and developed. The proposed AGDs are experimentally tested and are applied in a high-frequency power converter. An analysis of the power converter efficiency is developed by using the designed AGD. The next sections present a detail the description of the research and show the stages developed for designed and tested AGD.

1.2 Research problem

The silicon carbide (SiC) devices but in particular the SiC MOSFET, have been gaining interest for new applications due to its advantages in comparison to their silicon counterparts [5], [21]. The SiC MOSFETs have enough capability to work in high-speed switching, a higher voltage and high temperature [22]–[24]. However, reducing or eliminating the problems that arise when these devices work at high frequencies are some of the most important challenges when designing converters based on SiC devices. It has been shown that the SiC MOSFETs at high operation frequency lead to issues such as electrical oscillations and overshoots due to large *di/dt* and *dv/dt* that can generate electromagnetic interference (EMI) problems, stress and misbehaviour of the devices [2], [6], [25]–[29].

There are extensive solutions to face the high-frequency issues in the SiC MOSFETs. PCB layout optimization is a mandatory technique to reduce stray inductance and avoid oscillations [30]. However, the PCB layout optimization is not enough to decrease the oscillations in high-power applications due to the difficulty of stray inductance reduction after a certain point. Besides, snubber circuits are a basic method for improving the behaviour of the SiC MOSFETs transition [31], [32]. The caveat of using snubber networks is that can compromise the total efficiency because it requires additional components such as resistors, capacitors and inductors.

A conventional gate driver (CGD) based on fixed gate resistance and CGD with two resistances and diodes to control turn-on and turn-off individually is a simple solution to control *di/dt* and *dv/dt* slopes. The challenge, however, is the selection of the gate resistor values. Large R_g can decrease the high *di/dt* and *dv/dt*, and reduce the overshoot and oscillations, but this would cause large transitions time delays and to increase the switching losses [27], [33]. Accordingly, several studies have used optimization techniques to balance di/dt and dv/dt and, switching losses, but this compensation still has remained a challenge [34], [25].

The gate drivers (GD) circuits have been an alternative to address the issues in silicon MOSFETs and IGBTs. Comprehensive investigations about gate driving techniques and protection circuits are found in [35]–[37]. Most of them could be used for SiC MOSFETs, but these drivers must be adapted due to the differences between Si and SiC devices, for example, asymmetrical gate-source voltage. Therefore, various GDs for SiC devices have been presented in the literature [38]–[43]. Many of these gate drivers have only been tested at low frequencies; some others only at low power and the most complete are complex and were designed for specific load profiles. Therefore, despite numerous proposals for SiC MOSFETs have been presented, it is necessary to develop new drivers due to the demands of the current applications.

The purpose of this thesis is the study of the SiC MOSFETs and the solutions to improve the performance of these devices. In addition, it will propose GD solutions for controlling the turn-on *di/dt* and turn-off *dv/dt*, and reducing the over-voltage and over-current problems without harming the efficiency. Finally, apply the proposed new solutions of GDs in high-frequency power converters and study the impact of the efficiency.

1.3 Hypotheses

Regarding the previous discussion, the general hypothesis is that the silicon carbide MOSFET devices can cover the new requirements of power converters due to extended advantages. However, the application of the SiC MOSFET devices forces to research new solution to face the issues induced in the devices such as overshoots and EMI problems. Assuming this argument, the following hypotheses are formulated:

- The active gate drivers (AGDs) are necessary to improve the switching characteristics of SiC MOSFETs and to increase its performance at high-frequency operation.
- It is possible to achieve a simple AGD with high performance, capable of reducing overshoots and oscillations: source of electromagnetic interference (EMI).
- A feedback AGD able withstand parameter variations such a load, current and voltage, is better for improving the efficiency of the power converters.

In consequence,

> An AGD will improve the performance of the switching devices applied on power converters for high-frequency applications, and in consequence, will improve the total efficiency of the power converters.

1.4 Aim and objectives

In order to address the research problem and test the research hypotheses, the main objective of this Thesis is to design and develop active gate drivers capable of reducing the problems that arise in SiC MOSFET when used in converters working at high frequency (>40 kHz) and medium power.

The active gate drivers have to be able to reduce the overshoots and oscillations without compromising both; the performance of the SiC devices and the efficiency of the power converters. In addition, the active gate drivers have to withstand load variations and temperature changes in order to be considered robust.

Then, the following specific objectives are defined to accomplish successfully the thesis purpose:

a) First, the analysis of the SiC MOSFETs devices at high frequency. This study consist of characterizing the behaviour of the SiC MOSFETs at switching frequency >40 kHz by using conventional gate drivers. This objective includes the analysis of the aforesaid basic solutions to reduce the problems in SiC MOSFETs such as snubber circuits and gate resistance optimization.

b) A proper characterization of the SiC MOSFET, which allows the design of AGD and SiC MOSFET models able to be tested and compared through simulation and experimental tests. The purpose of the AGD is to reduce the overshoots and oscillations that can provoke EMI problems.

c) To check the temperature impact of driver designs, being operational temperature one of the common parameter which affects SiC MOSFETs behaviour. Then, design a feedback gate driver compatible with such variations. The AGD must be tested experimentally at high frequency and medium voltage.

d) Finally test and compare an AGD able to be used at high-frequency power converters. To achieve this goal, a high-frequency converter with SiC MOSFET devices will be designed and the purposed AGDs used and analysed. Finally, a study of the power converter efficiency will be developed and the impact of the AGD is discussed.

1.5 Thesis outline

To cover the exposed objectives, this thesis is organized as follows:

Chapter 2 consists of the description of the SiC MOSFETs, its main characteristics, advantages and drawbacks and solutions to improve their switching behaviour. It also discusses a method for calculating switching losses and a method for calculating gate resistance considering parasitic capacitances. Finally presents an analysis of the active gate drivers for SiC MOSFETs found in the state-of-the-art and the market.

C**hapter 3** presents a new proposal of the AGD, its design, parameters calculation, and optimization. A model and its simulation are presented and a prototype is manufactured and evaluated by experimental tests. In addition, this chapter presents a viability study, the costs of the gate driver and the study of the EMI reduction.

C**hapter 4** shows the design and evaluation of an AGD using feedback control. The design parameters and modelling of the control algorithm are developed. An experimental analysis is performed and the behaviour of the AGD and performance evaluation are presented in this chapter as well.

C**hapter 5** discusses the application of the AGD in power inverter for wireless charging system for electric vehicles. It also develops the experimental evaluation and the efficiency analysis.

C**hapter 6** presents the general conclusions and the future work of this investigation.

Chapter 7 presents the thesis disseminations and published papers as a result of the investigation collaborations around this Thesis.

2

Characteristics and gate drivers of SiC MOSFET devices

This chapter presents an analysis of the SiC MOSFET devices and their characteristics. Conduction and switching losses definition and a study at high-frequency operation of a SiC MOSFET. In addition, this chapter presents an analysis of the techniques to improve the switching behaviour of the SiC devices and a discussion of the gate driver techniques available in the literature and in the market. Finally, this chapter enlists the general characteristics, requirements and challenges to design gate driver circuits.

CONTENTS:

2.1 A brief analysis of SiC Power Semiconductors Devices

The switching power devices play an important role in the power electronic applications. Silicon devices have been the most widely used semiconductor in power converter applications for decades. However, with the new requirements for the design of power converters, silicon devices (Si) have been upcoming to its physical limits [44].

Although WBG devices such as SiC and GaN have been introduced for several years, the current improvement in the technology and accelerated growth in the market of these devices allows the integration of switching elements with better characteristics than silicon devices to meet the needs of power converters used in current applications [45], [46]. However, despite the advantages of WBG devices, there are some challenges to enjoy the full potential of these devices. Consequently, studies have been conducted on the advantages and disadvantages of these devices and the main challenges that need to be addressed for the power converters design based on WBG devices.

2.1.1 Comparison and status of power semiconductor devices

Many authors have used different technologies to cover the requirements concerning power efficiency in new power converter designs. In the literature, there are numerous studies and comparisons between different semiconductors technologies such as Si, SiC and GaN for different applications [18] [20], [47]–[59].

Conduction efficiency (low on-resistance), breakdown voltage, size, switching efficiency and cost are the most important characteristics of power semiconductors applied in power converters available today and these characteristics are related with the electrical properties shown in Table 2.1, which shows a comparison of semiconductor properties between different technologies.

Table 2.1. A comparison of power-semiconductors electrical properties [2] [17], [57], [46],

Parameter	Nomenclature	Units	Silicon	SiC	GaN	Characteristic
Band Gap	E_g	eV	1.2	3.26	3.39	Higher Junction temperature / small leakage current
Critical Field	E_{Crit}	MV/cm	0.23	2.2	3.3	High blocking voltage/ low ON state resistance
Electron Mobility	μ_n	$cm^2/V{\cdot}s$	1400	950	1500	High speed / high switching frequency
Permittivity	ε_r		11.8	9.7	9	High current levels
Thermal conductivity	λ	W/cm·K	1.5	3.8	1.3	Operation at high temperature / Low thermal resistance

As shown in the table, in general, WBG devices have better properties than conventional Si. GaN devices have greater electron mobility and electron saturation. These two properties allow GaN devices to operate at higher switching speeds. However, GaN devices have low permittivity, this limits GaN devices to achieve high current levels. SiC devices have a higher thermal conductivity while GaN has the lowest of the three technologies. Therefore, silicon carbide can work at very high temperatures. However, broadband

devices lack high temperature packaging techniques. Therefore, despite the advantage of SiC to work at high temperatures, in practice SiC devices operate at similar temperatures of conventional silicon [17], [45], [57].

In addition, the manufacturing processes of WBG devices are not fully mature. This drawback makes these devices more expensive. SiC devices are more expensive to manufacture than GaN devices. This will reduce the cost of GaN devices in the future and make them the most popular devices in the design and development of power converters [54].

For now, WBG devices are widely available in the market. However, GaN devices are limited in common distributors and manufactures. Table 2.2 shows a comparison of the characteristics available in market.

Table 2.2. Comparison of characteristics, availability and costs of switching power devices

Devices	Main characteristics	Cost p. u.	Availability
Si MOSFET	<900 V, <90 A	0.5	High
SiC MOSFET	<1200 V, <90 A	0.7	High
GaN devices	<650 V, <35 A	1	Low

The proper selection of WBG devices depends on the needs and characteristics of the application where they are integrated and continue to be a topic of discussion. However, the SiC devices, in the short term, are an alternative to Si devices for fulfilling the requirements of recent high-frequency power converters applied to low, medium power and even high power application by using SiC modules. Thus, this thesis is focused to study of the SiC devices but in particular, is focused on SiC MOSFETs analysis.

2.1.2 Challenges for SiC-based power conversion system

Previously, it was analysed the impact of the SiC devices for new power converter applications. The SiC MOSFETs are emerging as the alternative for achieving high-efficiency power converters for short, medium and even long term. Nevertheless, despite the advantages of SiC devices, some challenges arise that must be addressed to take advantage of the SiC technology and achieve better power converter designs [44], [60], [61]. Fig. 2.1 shows the relationship between the challenges that limit power converter design based on SiC. This thesis is focused on the study and design of the gate driving techniques to improve the performance of the SiC MOSFETs.

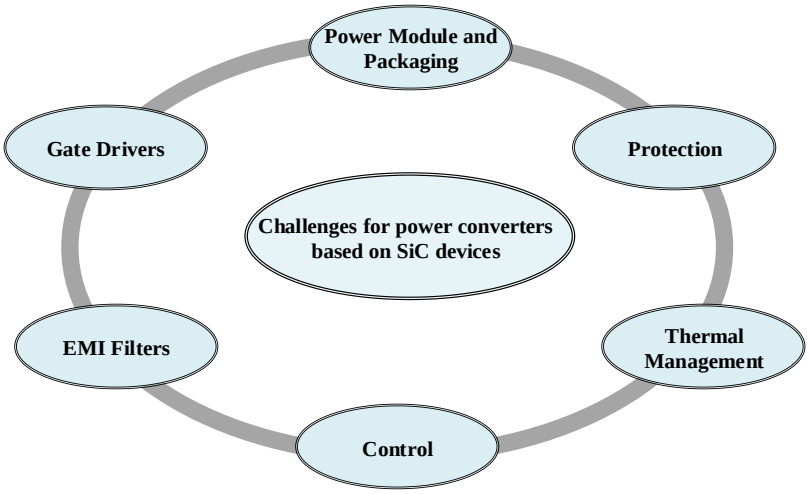

Figure 2.1. Challenges for developing power converters based on SiC devices.

Gate Driver

A gate driver is an important stage for power converters design. Basically, a GD is a circuit that amplifies the transmission signal coming from the control stage for ensuring the suitable switching of the power devices [38]. The transmission signal includes all the digital signal such as PWM, fault sensing signals and protections that are coupled through optocouplers, digital isolators and optical fibers. Besides, GD circuits connect the converter control unit and the power transmission stage [62]. According to [39], the power transmission stage should consider the following points for GD designs:

- Electrical isolation
- Low parasitic capacitance,
- Small footprints

These reasons are the main challenges to design power transmission. Then, in addition to the basic gate-driver design, to achieve a complete design of gate drivers for SiC devices it is required special consideration compared to silicon devices.

1) *Separation of power supplies*: The separation of the power supplies in the design of the power converters is fundamental to isolate the voltage and current levels within the stages of the converters. In addition, the power supplies separations limit the propagation of common-mode (CM) current that spreads in control circuits due to the presence of parasitic coupling capacitances of the optical isolators or transformers of the dc-dc converters used in power supplies for the gate drivers. The separation of CM current paths helps to reduce the peak CM current through signal isolation path and avoid the possible disruption in the gating signals [39].
   Besides, an isolated gate driver is crucial in application of MV and HV due to the voltage levels between stages.

2) *Layout design considerations:* the reduction of stray inductances principally present in the gate-source path it is important because large inductances lead overshoots in the gate voltage, which cause undesirable ringing in the gate-source supply when the switching devices are working at high frequency and might damage the gate isolation. Therefore, the design of the gate-source path must be designed carefully and should be as short as possible to minimize the stray inductance. Consequently, complete methodologies to reduce the stray inductance and optimize the PCB layout have been presented in the literature [63].

3) *Short circuit protection:* short circuit function can be applied in the GD structure with the purpose of protecting the power devices of shoot-through conditions. The integration of the short circuit protection guaranties the correct commutation off when there is excess current in the devices.

4) *Active gate driving:* the application of power semiconductors in high-frequency converters forces to control the high *di/dt* and *dv/dt* slopes. Large gate resistances can limit the *di/dt* and *dv/dt* and avoid overshoots and oscillations; however, this causes a slow transition and an increase in switching losses. An active gate-driving allows modulating the gate resistance dynamically during every switching instant or allows adjustment of the driving current/voltage to shape the switching trajectories. Therefore, with gate driving technique, it is possible to increase the switching trajectory of the power devices because it can manage the trade-off between energy losses, device stress, overshoots and ringing [39], [64].

2.2 SiC MOSFET power devices

The previous section discussed the importance of SiC devices and the advantages in comparison with silicon devices. Although there are different SiC devices such BJT, JFETs and IGBTs that have been applied in within the current applications of power converters, the SiC MOSFETs play an important role in the most of applications for LV (<3.3 kV) and MV (>3.3 kV). SiC MOSFETs are capable of supporting high power at high-switching frequencies as it combines the advantages of IGBTs and MOSFETs. SiC MOSFETs have low $R_{ds(on)}$ at high voltage levels similar to IGBTs and low switching losses compared to Si MOSFETs. This feature allows to the SiC MOSFETs to work at high switching-frequencies without affecting the efficiency of the converters [39].

2.2.1 Static characteristics of the SiC MOSFETs

The main static characteristics for SiC MOSFETs include on-resistance, device parasitic capacitance and gate threshold voltage and transconductance [24]. These parameters have been widely studied in the literature and the impact in power converter design have been discussed.

Miller voltage and Threshold voltage

Several studies have shown the variations of the Miller Plateau and thresholds voltages in SiC MOSFETs [21], [24], [65], [66]. In [65] and [66], studies about the behaviour of these parameters were developed, even for different SiC MOSFETS manufacturers. The presented results have shown that the threshold voltage in different SiC MOSFETs depend on the temperature and has a value around 2 V with a variation of ±0.5 V for a temperature range of 25 °C -150 °C, as shown in Fig. 2.2.

Besides, the Miller Plateau voltage has greater variations which depend on mainly of the current load and the SiC MOSFET transconductance [66]. The Fig. 2.3 shows a voltage Miller Plateau variation example for different SiC MOSFETs. Regarding the Fig. 2.3, the voltage plateau has a large variation.

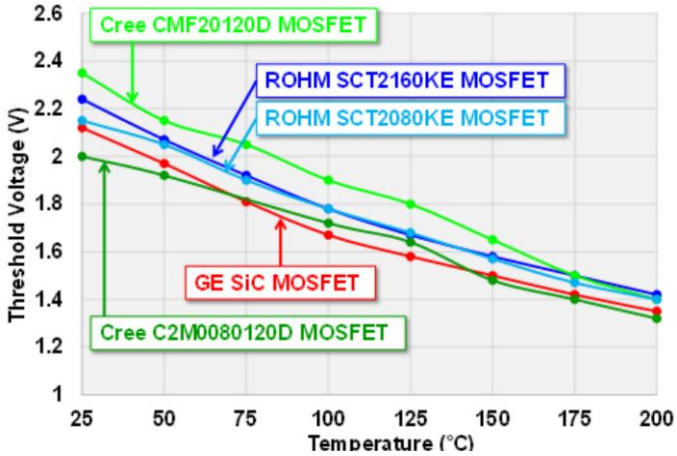

Figure 2.2. Threshold voltage comparison by [66]

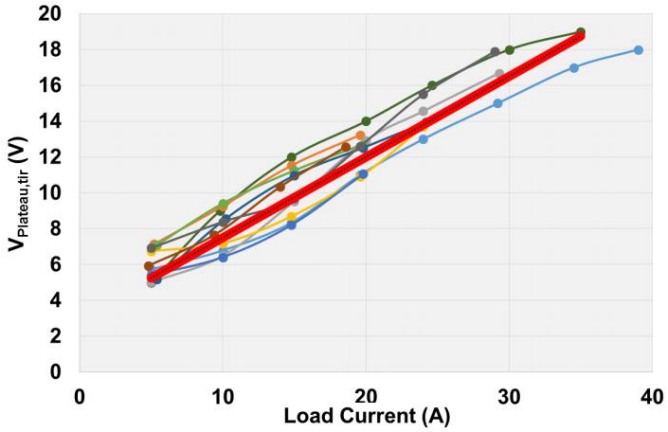

Figure 2.3. Plateau voltage versus load current for different SiC MOSFETs with different gate resistances for the current rise transition [66].

Device capacitances and inductances

Fig. 2.5 shows a typical testing circuit switching a clamped inductive load that is used for modelling the SiC MOSFETs and the parasitic representation of the capacitances e inductances. The parasitic elements

of the SiC MOSFETs that are considered include gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, drain-source capacitance C_{ds}, source inductance L_s, drain inductance L_d and gate inductance L_g. In addition, stray inductance L_{loop} and C_{D1} which is the parasitic capacitance of the diode. In this model the internal resistance R_{g_int} is also considered. The internal resistance in addition with external resistance R_{g_ext} are equal to the total gate resistance R_g, then, $R_g = R_{g\_int}+R_{g\_ext}$.

The parasitic elements behaviour as parasitic capacitances and parasitic inductances can be determined through the characterization of the defined system, of studies such as [21], [31], [33], [65], [66] and datasheets specifications [67]. Therefore, values range of parasitic elements can be defined or even it can be declared constants. Regarding the studies and datasheets, the parasitic capacitances in high voltages can be considered as constant, as depicted in Fig 2.4. Where C_{rss} is a small-signal reverse transfer capacitance and $C_{rss} = C_{gd}$. C_{iss} is a small-signal input capacitance with the drain and source terminal are shorted and $C_{iss} = C_{gs}+C_{rss}$. Finally, C_{oss} is a small-signal output capacitance with the gate and source terminals are shorted and $C_{oss}=C_{rss}+C_{ds}$.

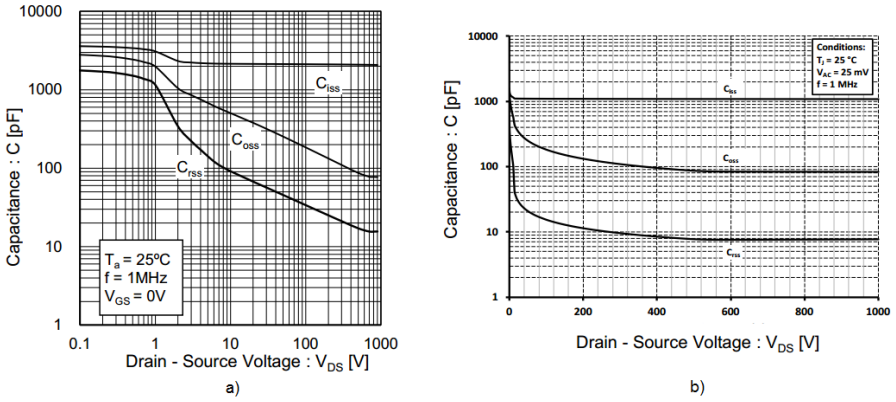

Figure 2.4. Capacitance versus drain-source voltage variation. a) SiC MOSFET SCT2080KE by Rohm semiconductor and b) SiC MOSFET C2M0080120D by Cree.

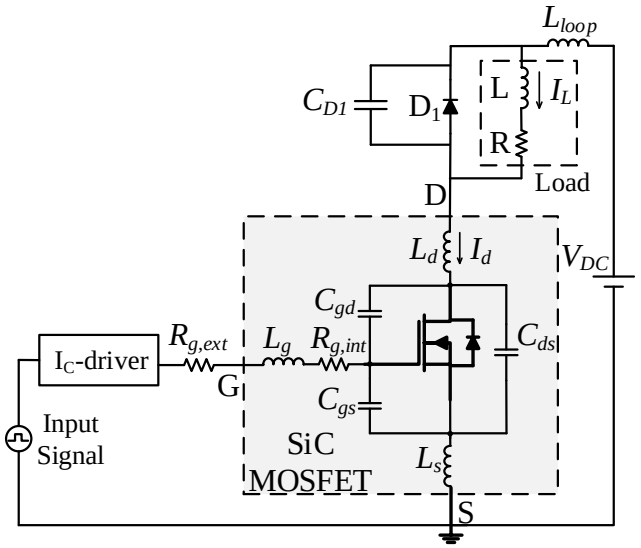

Figure 2.5. Equivalent testing circuit to evaluate and represent parasitic elements representation of the SiC MOSFET in turn-on conditions.

2.2.2 SiC MOSFETs dynamic characteristics and basic technics for reducing switching problems

The advantages of SiC MOSFETs have been discussed previously and the importance of the SiC MOSFETs have been presented as well. However, despite all benefits of SiC MOSFETs especially in high operating frequencies, it is necessary to develop solutions to reduce the problems caused by parasitic elements of the SiC MOSFETs. Many studies have demonstrated the effects of parasitic elements and have proposed models that help to determinate the behaviour of the devices in the power converter designs.

Several works have shown the effects of SiC MOSFETs taking considering the parasitic elements when the MOSFETs are working at frequencies greater than 20 kHz [24], [27], [33]. Fig. 2.6 shows an example of current and voltage behaviour of SiC MOSFETs working at 100 kHz.

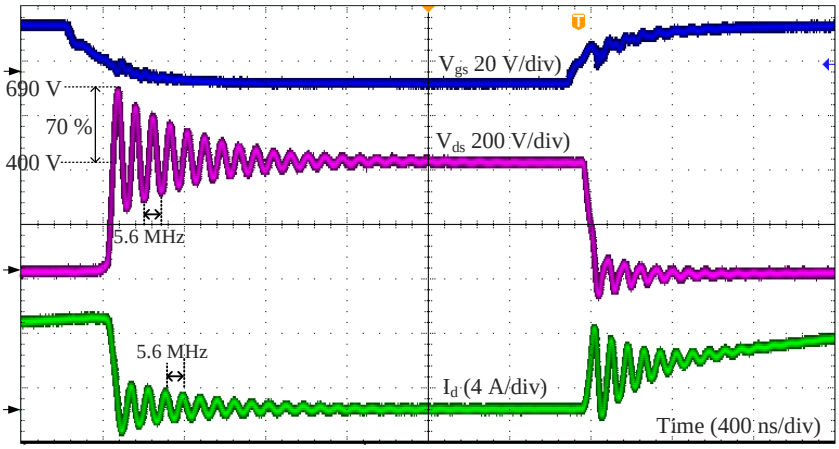

Figure 2.6. Current and voltages of a discrete SiC MOSFET by ROHM semiconductors applied on the power converter of Fig. 2.5 and working at 100 kHz of switching frequency, R_g=6.3 Ω and 400 V of DC-bus.

The figure shows the oscillations on the current and voltages. The voltage exceeds 70 % of the nominal value and the oscillations have a resonant frequency of 5.6 MHz.

The basic solution to reduce the oscillation caused by parasitic elements is to modify the gate resistance for controlling *di/dt* and *dv/dt* slopes. Notwithstanding, with a large gate resistor, the overshoots are reduced, but the losses are increased. Besides, if the gate resistor value is small, the losses can reduce but the current and voltage overshoots are increased, which could involve EMI problems and stress in the devices. Fig. 2.7 shows an evaluation of the behaviour of one SiC MOSFET by using different gate resistances. Fig. 2.8 shows the temperature of power MOSFET when the gate resistance increases. C_{gs} and C_{ds} optimization is another alternative for reducing the oscillations without increase the switching losses, however, a trade-off is the main challenge of this method as well. Additionally, when using a better design of PCB layout the stray inductances are reduced, and EMI problems can be eliminated [63].

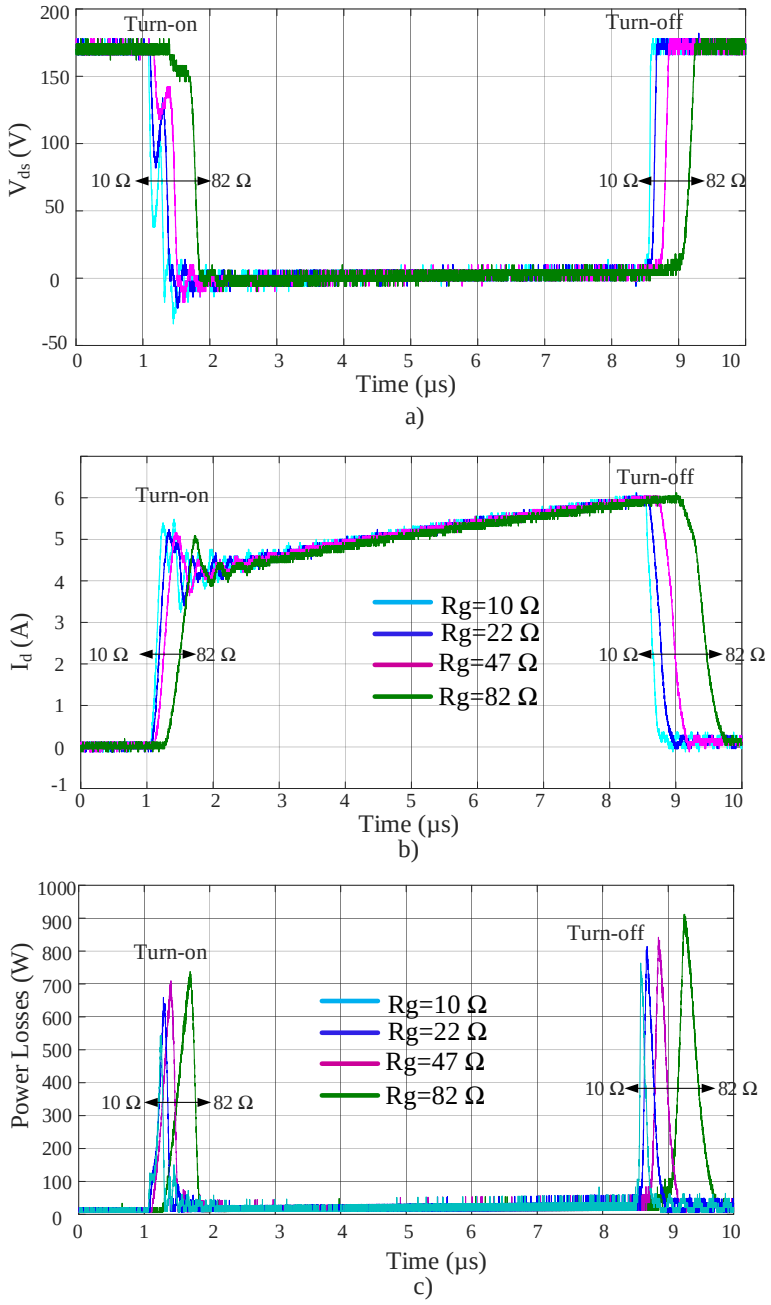

Figure 2.7. Gate resistance comparison of a discrete SiC MOSFET by ROHM semiconductors applied on a power converter of Fig. 2.4 at 100 kHz of switching frequency, R_g=6.3 Ω and 200 V of DC-bus.

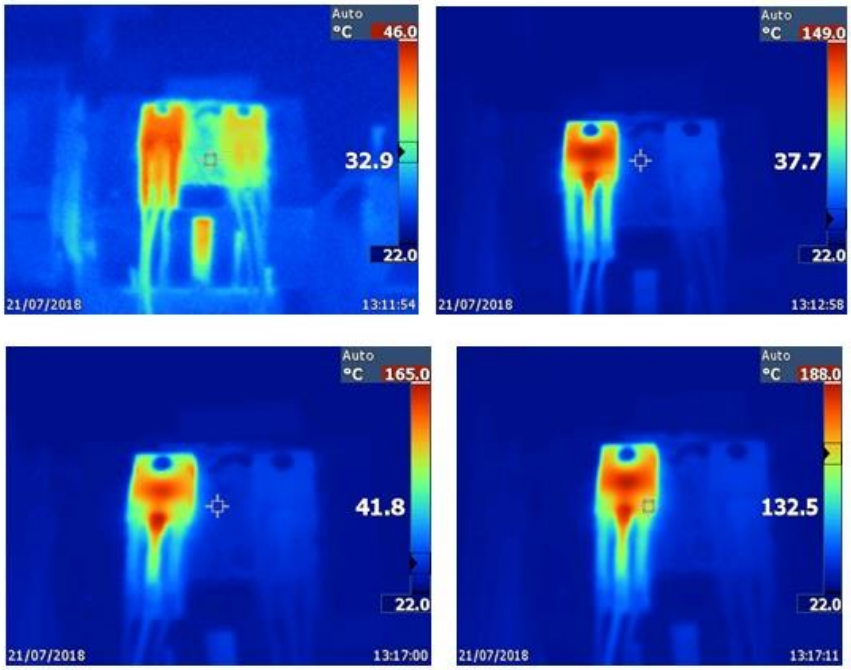

Figure 2.8. Temperature of the SiC MOSFET when the R_g increases.

Snubber circuits have been a solution for reducing the overshoots and oscillations in power devices. Many works have developed snubber circuits optimized for SiC devices with good results. However, despite the benefits of using snubber circuits, the elements used such as capacitors, inductors and resistors can be bulky and should withstand large amounts of energy can leave high stress in additional components. Fig. 2.9 shows an example of the snubber capacitor used in SiC MOSFET device applied on buck converter.

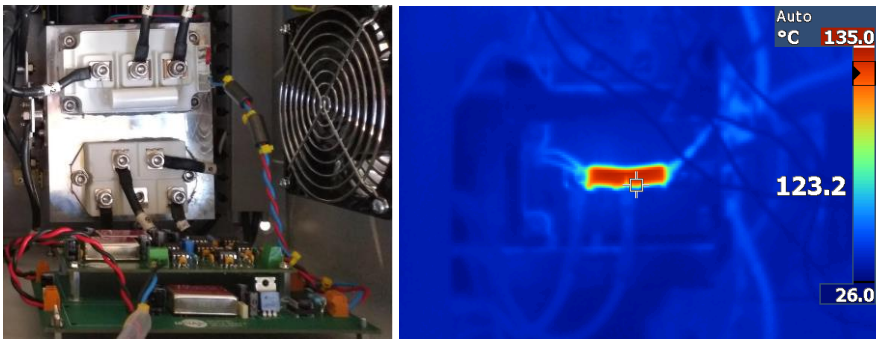

Figure 2.9. Snubber circuit example applied to SiC MOSFET module working at 100 kHz of switching frequency and 400 V of the DC-bus. Maximum temperature measured on the snubber component was 135 °C.

Previously it was discussed that the SiC MOSFET is being widely studied in power electronics systems due to its advantages. Nevertheless, SiC MOSFETs have low transconductance in comparison with silicon devices such as MOSFET or IGBT. Hence, higher gate-source voltage levels are required for turn-on. Moreover, the total pulse of the gate-source voltage is commonly asymmetrical (-10 V to 20 V). Therefore, different values of R_g to improve its performance in both turn-on and turn-off transitions are required. The conventional GD with two resistances is shown in Fig. 2.10, which is commonly used for controlling the

turn-on and turn-off path. Although this configuration controls the turn-on and turn-off path separately, it is limited with regarding to the trade-off between efficiency and EMI problems. The next section shows an optimization method for gate resistances.

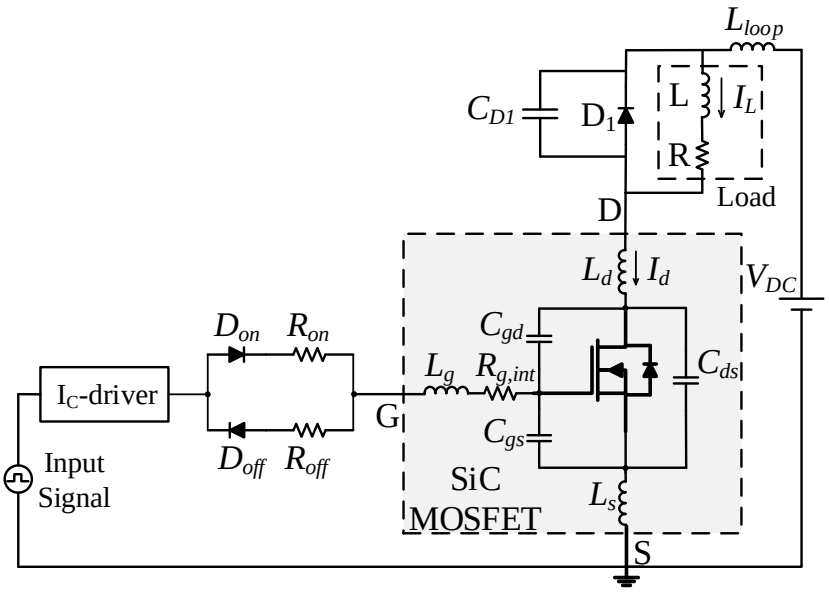

Figure 2.10. Gate driver for SiC MOSFET with different turn-on and turn-off gate resistances.

2.2.3 Gate resistances optimization method

As noted above, the R_g performs an important role in the switching behaviour of the SiC MOSFET. The common way for achieving a good switching performance of the power devices is conducting a calculation of the gate resistance (R_g) for each transistor; this resistance can be obtained by (2.1) [62], [68].

$$R_g \geq 2\xi\sqrt{\frac{L_g}{C_{gs}}}, \tag{2.1}$$

where ξ is the damping factor usually around 0.707. In addition, L_g is the parasitic inductance in the gate loop of MOSFET and this inductance can be calculated by using methodologies proposed in the literature[63], [65].

Nonetheless, for achieving better performance, the R_g should be calculated in relation to the parasitic elements of the system. Then, an alternative to calculate the gate resistances can be developed based on the presented and validated methods in [31] and [69]. The gate resistances are calculated through equivalent circuits of the total parasitic elements.

The circuit depicted in Fig. 2.11 (a) is commonly used to analyse the behaviour of the MOSFET parasitic elements together with the freewheeling diode and its parasitic capacitance C_{D1} for turn-on transition when the power device is in conduction mode. Whereas, Fig. 2.11 (b) depicts the equivalent circuit for turn-off conditions when the device is in blocking mode. It is important to mention that the load inductance L is

considered as a constant current source due to does not change during switching transients. On the other hand, the parasitic capacitance associated with L is neglected in the models because is commonly lower than the output capacitance and it does not intervene in the resonant effect [65].

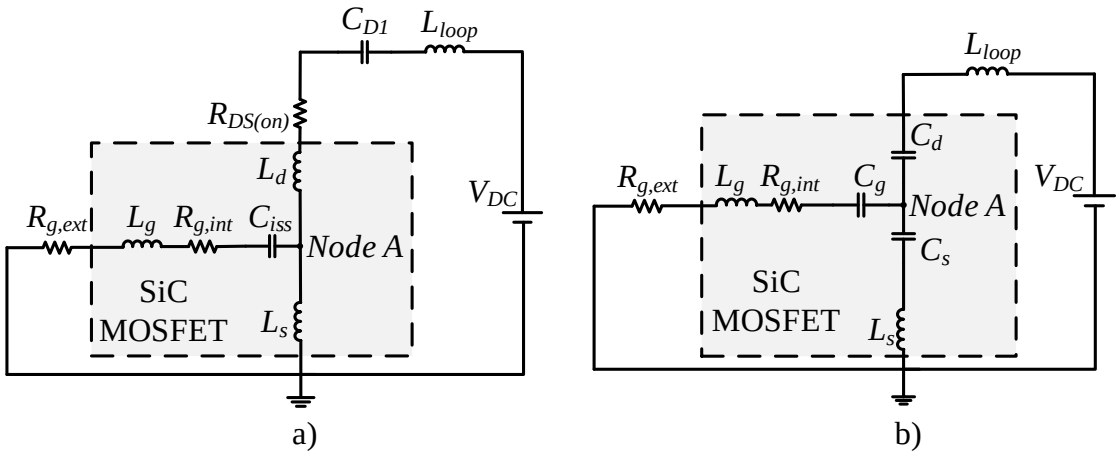

Figure 2.11. Parasitic elements representation of the SiC MOSFET in turn-on and turn-off transition conditions. a) Turn-on circuit, b) turn-off circuit.

Equivalent elements are defined as: $L_{eq} = L_{loop} + L_d$, $R_{g,on} = R_{on} + R_{ext} + R_{int}$, and $R_{g,off} = R_{off} + R_{ext} + R_{int}$. An impedance analysis is developed in the node A in both circuit and the final equivalent circuits are represented in Fig. 2.12.

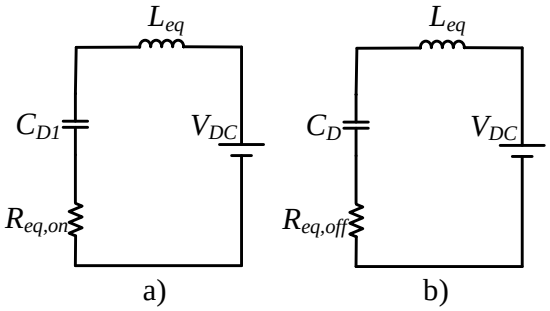

Figure 2.12. Final equivalent circuit of SiC MOSFET with parasitic elements. a) Turn-on equivalent circuit and, b) Turn-off equivalent circuit.

Regarding Fig. 2.12, the equivalent resistances $R_{eq,on}$ and $R_{eq,off}$ are obtained as [31]:

$$R_{eq,on} = \frac{(\omega_1 \cdot L_d)^2}{\frac{R_{g,on} + (\omega_1 \cdot L_g + \omega_1 \cdot L_s - \frac{1}{\omega_1 \cdot C_{iss}})}{R_{g,on}}} \tag{2.2}$$

$$R_{eq,off} = \frac{(\omega_2 \cdot L_s - \frac{1}{\omega_2 \cdot C_s})^2}{\frac{R_{g,off} + (\omega_2 \cdot L_g + \omega_2 \cdot L_s - \frac{1}{\omega_2 \cdot C_g} - \frac{1}{\omega_2 \cdot C_s})}{R_{g,off}}} \tag{2.3}$$

where ω_1 and ω_2 are the resonant frequencies of the resulting RLC circuits and are defined by equation (2.4) and equation (2.5).

$$\omega_1 = \frac{1}{\sqrt{(L_{eq}+L_s)\cdot C_{D1}}} \tag{2.4}$$

$$\omega_2 = \frac{1}{\sqrt{(L_{eq}+L_s)\cdot (C_{gd}+L_{ds})}} \tag{2.5}$$

The final circuits, as shown in Fig. 2.12, are second order systems and can be solved using Laplace domain to obtain the value of $R_{g,on}$ and $R_{g,off}$. However, according to studies in [69], equivalent resistances reach the maximum value when the equations (2.6) and (2.7) are fulfilled.

$$R_{g,on} = \left|\omega_1 \cdot L_g + \omega_1 \cdot L_s - \frac{1}{\omega_1 \cdot C_{iss}}\right| \tag{2.6}$$

$$R_{g,off} = \left|\omega_2 \cdot L_g + \omega_2 \cdot L_s - \frac{1}{\omega_2 C_g} - \frac{1}{\omega_2 \cdot C_s}\right| \tag{2.7}$$

2.2.4 Switching and conduction losses of the SiC MOSFETs

If the behaviour of the parasitic elements in the Fig. 2.5 is neglected and considered ideal, the switching and conduction power losses of the SiC MOSFET can be represented in Fig. 2.13.

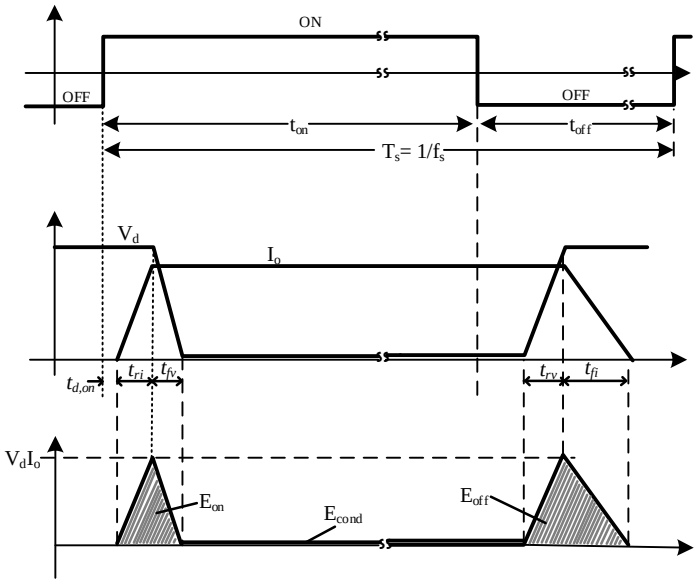

Figure 2.13. Representation of power losses of the SiC MOSFET

The energy dissipated in the device during the turn-on and turn-off transition can be approximated from the Fig. 2.13 as:

$$E_{on} = 0.5 \cdot (V_{ds} \cdot I_d \cdot t_{on}) = E_{ri} + E_{fv} \tag{2.8}$$

$$E_{off} = 0.5 \cdot \left(V_{ds} \cdot I_d \cdot t_{off}\right) = E_{rv} + E_{ri} \tag{2.9}$$

Where

$$t_{on} = t_{ri} + t_{fv}\,, \tag{2.10}$$

and

$$t_{off} = t_{rv} + t_{fi}\,, \tag{2.11}$$

On the other hand, a method to characterize the power losses in relation to the rise time and fall time of the current i_d was presented in [70]. This method is used for getting the optimal times for the points $V_{1,low}$ and $t_{d,2}$, when a relation between minimal losses E_{min} expressed in (2.12), and the energy losses E_{ri} and E_{fi}, is found. In addition, taking into account the overshoots and turn on and turn off delay times.

$$E_{min} = 0.5 \cdot (I_d)^2 \cdot L_{loop} \tag{2.12}$$

The rise time losses of the current are calculated by using the expression:

$$E_{ri} = 0.5 \cdot (I_d)^2 \cdot L_{loop} \cdot \left(\frac{1}{\alpha} - 1\right) \cdot (1 + \sigma_1)^3, \tag{2.13}$$

where α is the relation between $di=dt$ and $[di=dt]_{max}$ according to (2.14).

$$\alpha = \frac{di_d/dt}{(di_d/dt)_{max}} \tag{2.14}$$

The maximum *di/dt* is defined by equation (2.15). In general, the maximum *di/dt* slope is infinite, for this reason in this analysis the maximum value of di_d/dt is considered with the minimum value obtained with minimum R_g allowed.

$$(di_d/dt)_{max} = V_{dc}/L_{loop} \tag{2.15}$$

In addition, σ_1 is the relation between diode reverse recovery current and i_d as shown in equation (2.16).

$$\sigma_1 = I_{rr}/I_d \tag{2.16}$$

Equation (2.17) represents the ratio between the losses in t_{rise} and minimal losses.

$$\frac{E_{ri}}{E_{min}} = \left(\frac{1}{\alpha} - 1\right) \cdot (1 + \sigma_1)^3 \tag{2.17}$$

For the case of the losses for fall time of the current, the equation (2.18) is used

$$E_{fi} = 0.5 \cdot (I_d)^2 \cdot L_{loop} + 0.5 \cdot (I_d)^2 \cdot L_{loop} \cdot \frac{1}{\sigma_2} \tag{2.18}$$

where

$$\sigma_2 = \frac{V_{os}}{V_{ds}} = \frac{L_{loop} \cdot di_d/dt}{V_{dc}}, \tag{2.19}$$

If the minimal losses are defined by (2.12), the ratio between t_{fall} losses and minimal losses can be represented by (2.21).

$$\frac{E_{fi}}{E_{min}} = (1 - \sigma_1) \tag{2.20}$$

According to [59], [71], instantaneous value of the conduction losses for a SiC MOSFETs can be calculated using a model of MOSFET approximation with the drain source on-state resistance $R_{ds(on)}$:

$$V_{ds} \cdot i_d = R_{ds(on)} \cdot (i_d) \cdot (i_d), \tag{2.21}$$

where V_{ds} and i_d are drain source voltage and the drain current, respectively. For SiC MOSFETs the typical $R_{ds(on)}$ has values of 80mΩ - 1 Ω.

The instantaneous value of the conduction losses can be calculated by (2.22) as:

$$P_{Cond}(t) = V_{ds}(t) \cdot i_d(t) = R_{ds(on)} \cdot i_d^2(t) \tag{2.22}$$

Then, the average value of the conduction losses can be obtained by integration of the instantaneous power losses for each commutation cycle as:

$$P_{Cond}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} P_{Cond}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} \left(R_{ds(on)} \cdot i_d^2(t)\right)dt = R_{ds(on)} \cdot I_{drms}^2 \tag{2.23}$$

where I_{drms} is the rms value of the drain current i_d.

2.3 Gate drivers for SiC MOSFET devices

Previously sections discussed the importance of the gate drivers. This section presents a review of the GDs applied to SiC MOSFETs. It presents the GD characteristics and a comparison between their advantages and drawbacks. In addition, an analysis of commercial gate drivers is presented and their advantages and drawbacks are discussed as well.

2.3.1 State-of-the-art of GDs for SiC MOSFETs

The most GD techniques presented for silicon IGBTs and MOSFETs can be applied to SiC MOSFETs if the differences such as parasitic elements, power supplies, switching speeds, voltage threshold, Miller plateau zone and transconductance are considered. Several solutions applied to silicon devices have been adapted to SiC MOSFETs [37], [35], [41], and new solutions of GDs have been studied [41]. Based on the classification presented in [42], [43], [72]. AGDs for SiC MOSFETs can be categorized as open-loop, closed-loop, status feedback, overvoltage protection and crosstalk protection techniques. Fig. 2.14 shows a resume of the AGDs classification found in the literature.

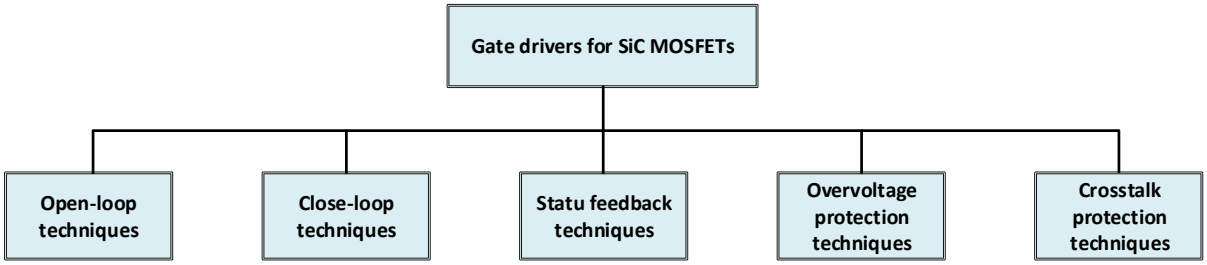

Figure 2.14. A classification of the GD circuits for SiC MOSFET devices.

Open-loop techniques

Several gate drivers solution based on open-loop control technique have been presented and discussed in the literature. In [73] a GD topology with circuits to control the gate-current of SiC MOSFETs was presented, this gate driver can control the slops and reduce the gate current, thus, reduce the oscillations and overshoots. Resonant gate drivers are commonly used for SiC MOSFETs devices and several works have discussed its advantages for different applications [74]. Most of the gate drivers are simple and can reduce the problems caused by the physical properties of SiC MOSFETs and resulting issues due to the fast switching of the devices. Nevertheless, in general, the open-loop techniques can only be used for specific applications or a fixed load profile. In addition, many of these techniques do not consider the effects caused by temperature.

Close-loop techniques

Alternatively, different active gate drivers (AGD) based on closed-loop control have been developed. In [75], a high-efficiency GD based on closed-loop control was showed, but, the GD only was designed for turn-off transition and the system to supply gate-current requires a laser that increases the cost and complexity of the gate driver.

Status feedback techniques

The main concept of the GD status is to read the door signal or the load signal and perform an action based on reference values. Most of these controllers are based on multiple stages that consist of varying the resistance levels to control the current in the door and thus control the voltage and current slopes of the SiC MOSFET [76]–[79]. The authors in [80] and [81] presented multistage gate drivers by using the status-feedback method to control independently *di/dt* and *dv/dt*. Results suggest that the gate drivers reduce the high-frequency problems without increasing the power losses. Nevertheless, the gate drivers use numerous resistances and switches, which could increase the losses of the GD and affect the transition times of the devices. In addition, the gate drivers could be complex and expensive for applications with more than one leg; due to the drivers would use many programmable devices or many isolating elements for the required input signals. A similar drawback is found in [82]. This gate driver is based on feedback control and its high performance and viability was evaluated in SiC MOSFET modules. However, this technique also required many programmable devices or many isolating elements for converters with more than one leg.

Overvoltage and overcurrent protection techniques

One of the important characteristics of a GD is to have a short circuit protection system. Most GDs use advanced and complex methods to protect themselves from an overvoltage and an overcurrent [83], [84]. The common technique for overcurrent protection is desaturation using a sensing diode to detect the drain source voltage under overcurrent faults as [83].

Crosstalk protection techniques

Unlike conventional silicon MOSFETs, SiC MOSFETs have lower threshold voltage and higher allowable negative gate voltage. These characteristics lead to crosstalk effect in phase-leg configuration, which limits the switching speed potential of SiC MOSFETs.

Thus, several GDs to increase the performance of the SiC MOSFETs and eliminate the crosstalk effect have been proposed [85]–[89]. According to [85], GDs for suppressing crosstalk effect can be classified into two categories: gate impedance regulation (GIR) and gate voltage control (GVC). GIR technique consists of to provide a small gate impedance during the switching transient to the complementary devices. On the other hand, GVC technique consists of providing a negative turn-off gate voltage for suppressing the positive gate voltage spikes of the switching devices when a complementary switch is deactivated.

Based on the previous description and classification of GDs for SiC MOSFETs the Table 2.3 shows a comparison of the advantages and drawbacks of the principal GDs solutions.

Table 2.3. Comparison of the AGDs found in state-of-the-art

Gate driver concept	Advantages	Drawbacks
Open-loop techniques	• Simple circuits • Easy to develop and apply	• Do not consider the load variation and temperature • Have a fixed profile of the load
Close-loop techniques	• Can reduce and eliminate effectively the overshoots and current • Are complete circuits that consider the load and temperature variation	• Complex • Are for specific applications • Are complex to program
Status feedback techniques	• Can be adaptive • Can reduce and eliminate the oscillations and overshoots • The most are efficient	• The load should be know • Can be complex
Overvoltage and over current protection techniques	• Can protect of short-circuits • Increase the viability of the devices	• Can be complex • Additional circuits are required to operate properly
Cross-talk protection techniques	• Are effective to control the crosstalk in two legs	• Complex systems • Are expensive

Although various gate driver solutions have been developed, there are many research challenges in the development of these systems. A complete driver that considers most of the points described above could be developed. Therefore the investigation of new GD solutions is required.

2.3.2 Commercial gate drivers

The previous sections presented the state-of-the-art of GDs for SiC MOSFETs. However, several power semiconductor manufacturers have developed GDs in integrated circuits, which can be found in the market. Many commercial gate drivers are complete systems that can improve the performance of the power semiconductors. Table 2.4 shows a comparison of commercial gate drivers applied in SiC MOSFETs.

Table 2.4. Gate driver for SiC MOSFETs available in the market

Manufactures	Model	Characteristics	Advantage	Drawbacks
Texas Instrument	UCC21710-Q1	• Single channel SiC/IGBT isolated gate driver • Small propagation delay • SiC MOSFET and IGBT up to 1700 V • Fast overcurrent and short circuit detection	• Galvanic Isolated • Advanced protections • Low cost • Easy to implement	• Low availability in the market
Texas Instrument	UCC21530	• Dual channel isolated gate driver • Separate source and sink outputs • For 600 V/650 V/1200 IGBs, MOSFETs and SiC MOSFETs	• Galvanic Isolated • Advanced Protections • Very fast • Suitable for operation at high temperature	• Only for SiC modules
Infineon	1EDCxxI12AH and 1EDCxxH12AH Family	• Single channel SiC/IGBT isolated gate driver • SiC MOSFET and IGBT up to 1700 V	• Fast overcurrent and short circuit detection • Small propagation delay	• Need several isolating power supplies

Power Integrations	SIC1182K Scale-iDriver Family	• Single channel SiC/IGBT isolated gate driver • SiC MOSFET and IGBT	• Fast overcurrent and short circuit detection • Small propagation delay	• Expensive
ROHM	BM61M41RFV-C	• Single channel SiC/IGBT isolated gate driver • SiC MOSFET and IGBT	• Fast overcurrent and short circuit detection • Small propagation delay	• Low viability
SILICON LABS	Si823x	• Two completely isolated drivers in one package Small propagation delay • SiC MOSFET and IGBT up to 1700 V • Fast overcurrent and short circuit detection	• Galvanic Isolated • Advanced Protections • Low Costs • Easy to implement	• Low viability • Expensive
AgileSwitch	EDEM3	• Single channel SiC/IGBT isolated gate driver • Small propagation delay • Up to 8MHz switching frequency	• High electromagnetic immunity Advanced Protections • Overlap protection and programmable dead time	• This GD is to specific applications
EBVElektronik	SIC1182K	• Suitable for 600 V/ 650 V/ 1200 V SiC MOSFETs • Up to 150 kHz switching frequency • typical 2us • +/-8 A peak output current	• Over-current detection • UVLO primary and secondary side • Overvoltage limitation (SiC advanced Active Clamping) • Short-circuit current fault detection and turn-off	• Needs additional components
Microsemi	MSCSICMDD and MSCSICSP3	• Adjustable -5 V to +20 V output gate driver • Galvanic isolation of more than 2000 V on both gate drivers • Capable of 6 W and 8W of gate driver power per side • Maximum switching frequency greater than 4000 kHz • Peak output current of up to 30 A	• Short circuit protection • Programmable dead time protection • Fault signalling • Under-voltage lockout protection	• Isolation
Cree/Wolfspeed	CDR-001	• Dual channel SiC isolated gate driver • 4000kHz maximum switching frequency • +/- 100 Kv/uS capability	• Galvanic Isolated • Advanced Protections • Low Costs • Easy to implement	• Expensive • Need additional components
Cree/Wolfspeed	CGD12HBXMP	• Dual channel SiC isolated gate driver • 4000kHz maximum switching frequency • +/- 100 Kv/uS capability	• Galvanic Isolated • Advanced Protections • Low Costs • Easy to implement	• Needs additional components
Cree/Wolfspeed	CGD15HB62P1	• Two output channels • Integrated power supply	• Short circuit protection • Under voltage protection	• Needs additional components

Commercial gate drivers are a good alternative for the design of power converters. Most of these devices are integrated circuits (I_c) and have all functions that are required efficient power converters UVLO,

isolation stages, short circuit protection, dead time integration and overcurrent and overvoltage protection. Most of these commercial drivers are integrated circuits and others are developed in evaluation boards. The main drawback is that most of these GDs is that the I_c GD needs additional components to operate properly. Additional components could limit the use of these integrated circuits and make complex circuits.

2.4 Conclusions

In this chapter an analysis of the state of the art of broadband devices has been carried out, the problems that arise when applied in high-frequency converters and the solutions that exist to counteract or eliminate over-voltages and oscillations in both voltage as in the current. According to the study, it has been observed that basic solutions such as gate resistance optimization, input capacitance optimization, PCB design optimization and snubber networks are simple and widely used due to their application advantages, results and cost. However, these solutions do not completely solve the problems caused by high switching frequencies (around 100 kHz) and do not allow you to take advantage of the SiC MOSFETs.

Consequently, various techniques of gate drivers and gate driving have been presented in the literature. GDs allow to reduce or eliminate problems caused not only by high switching frequencies but also, problems caused by the characteristics of the devices of SiC such as cross-talk. On the other hand, there are solutions on the market for gate drivers that are used to improve the switching behaviour of SiC MOSFET transistors.

Despite the various gate driver solutions, the design of these circuits remains key to improving the performance of MOSFETs in high-frequency applications. Therefore, the research and development of gate drivers is a topic that is currently highly researched to achieve high-efficiency converters and low power density.

3

An active gate driver for improving the switching performance of SiC MOSFET

The previous chapter discusses the state-of-the-art of AGDs and their importance. This chapter presents a proposal of AGD to improve the performance of the SiC MOSFET devices. The main concept, structure and operation are discussed. Simulations and experimental evaluations of AGD is addressed and its viability is analysed.

CONTENTS:

3.1 Description and operation principle of the proposed gate driver

The general schematic circuit of the proposed AGD is depicted in Fig. 3.1. The circuit consists of a conventional totem-pole drive supplied by an isolated power supply. The AGD has two switches T_1 and T_2 placed in the turn-on and turn-off path with two resistances in parallel. The switches are controlled by two window comparator configurations, which compares the gate-source voltage (v_{gs}) with four reference voltages. In addition, a simple control block is on the feedback path for coupling the output signals of the comparators and then to generate delays. Therefore, it produces the expected pulses and suitable voltages for switches T_1 and T_2.

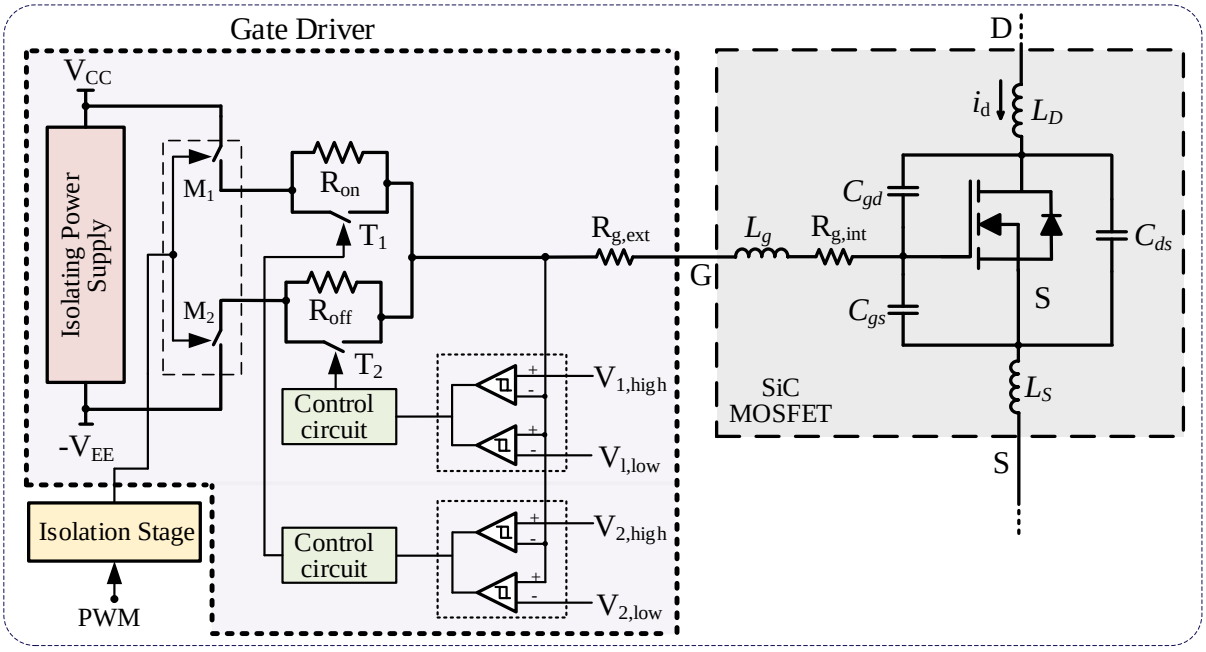

Figure 3.1. General scheme of the proposed AGD

In addition to internal resistance ($R_{g,int}$) of the device, an external gate resistance $R_{g,ext}$ is considered because the switches T_1 and T_2 could have a very low on-resistance ($R_{ds(on)}$) and consequently, the power MOSFET could be outside of the safe operation area (SOA) when T_1 and T_2 are carrying current. Therefore, $R_{g,ext}$ is connected in series with the driver. It should be worth mentioning that the minimum $R_{g,ext}$ is considered according to the recommended value in the datasheet which was considered of 6.3 Ω in this work for the main device studied. On the other hand, $R_{g,int}$ is usually very low and is found in the note application. For this study $R_{g,int}$ was less than 1 Ω.

The AGD principle is to increase the gate resistance value about the Miller Plateau zone of the voltage v_{gs}, in both turn-on and turn-off conditions. Thus, the current and consequently the energy are decreased in the interval where overshoots occur, as shown in Fig. 3.2. Taking into account Figure 3.1, the gate resistance is increased due to the switches T_1 and T_2 being off during $t_{1,1}$ - t_3 and t_7 - t_8 respectively. Therefore, only R_{on} and R_{off} are carrying current during these intervals.

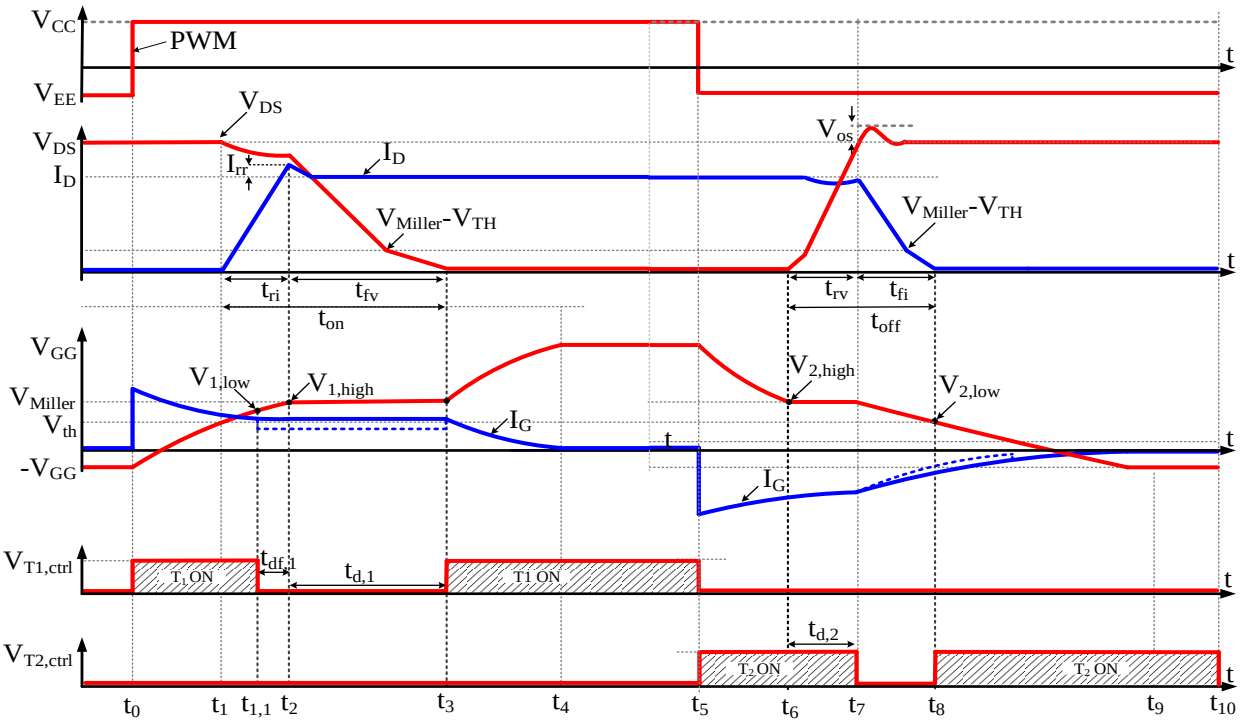

Figure 3.2. Turn-on and Turn-off SiC MOSFET waveforms and control signals for T_1 and T_2 of the AGD.

Switching off the S_1 and S_2 switches is reached through a comparison realized by windows comparators that compare four voltage references; $V_{1,high}$, $V_{1,low}$ and $V_{2,high}$, $V_{2,low}$, with v_{gs}. In addition, two delays $t_{d,1}$ and $t_{d,2}$ are applied to reach the expected control signal.

On the one hand, the reference voltage $V_{1,low}$ could be defined at time t_2, where v_{gs} voltage reaches the Miller Plateau voltage. However, the delay $t_{df,1}$ of T_1 control which is the total delay caused by MOSFET, the coupling circuit, and comparators, should be considered for ensuring the timely switching of T_1 and reach the optimal behaviour of the turn-on transition. On the other hand, $V_{2,high}$ is considered in t_6, where the Miller Plateau voltage is reached by v_{gs}, but the delay $t_{d,2}$ define the V_{ds} and I_{ds} slopes behaviour.

The voltages $V_{1,high}$ and $V_{2,low}$ should be properly defined. $V_{1,high}$ is defined as the Miller Plateau voltage, but the delay $t_{d,1}$ keeps the control signal high until the Miller Plateau zone has finished, because it is the point when v_{ds} reaches the minimum value as shown in Fig. 3.2. On the other hand, $V_{2,low}$ is considered equal to voltage threshold because it is the point where id current drops to zero, as shown in Fig. 3.2 The total delay caused by the T_2 MOSFET, the coupling circuit and the comparators for controlling the turn-off transition is considered, but it has no effect on the output signals.

3.1.1 Operating at turn-on transition

As depicted in Fig. 3.2, in t_0 the PWM signal rises to high, M_1 and T_1 switches are activated, and v_{gs} starts to rise. While a constant I_g is generated to charge C_{gs} capacitance with $R_{g,on} = R_{g,ext} + R_{g,int}$. Then, in t_1 v_{gs} reaches the threshold voltage ($V_{gs(th)}$) and the drain current (I_d) begins to rise. When v_{gs} reaches $V_{1,low}$ the switch T_1 is turned off and R_{on} conducts, therefore I_g decreases with $R_{g,on} = R_{on}+R_{g,ext}+R_{g,int}$. After the $t_{1,1}$,

v_{gs} goes beyond $V_{1,low}$ and reaches the Miller Plateau voltage. In this time, I_d current matches the nominal value and a peak of current arises due to the freewheeling diode effect. On the other hand, v_{ds} starts to fall, at that time the reference voltage $V_{1,low}$ is also reached and T_1 is turned off, when $t_{d,1}$ is over in t_3. The v_{gs} voltage starts to rise again in t_3. Finally, in t_4, v_{gs} reaches the V_{gg} and SiC MOSFET is in conduction mode. T_1 is active until the PWM signal rises again. The current slope of ids during turn-on transition is approximated from the following equation:

$$\frac{di_d}{dt} = gfs \cdot \frac{V_{gg+} - V_{gs(th)} - \frac{I_d}{2 \cdot gfs}}{C_{iss} \cdot R_{g,on}}, \tag{3.1}$$

where g_{fs} is the transconductance and $C_{iss} = C_{gs} + C_{gd}$ is the input capacitance of the SiC MOSFET. On the other hand, the expressions for the i_g current are:

$$i_{g,on} = \frac{V_{gg+} - V_{Miller}}{R_{g,on}}, \tag{3.2}$$

taking into account that $R_{g,on} = R_{on} + R_{g,ext} + R_{g,int}$ during the interval $t_2 - t_{1,1}$. Moreover, v_{ds} is:

$$\frac{dv_{ds}}{dt} = \frac{i_{g,on}}{C_{gd}} \tag{3.3}$$

Regarding the equations (3.1)-(3.3), the current and voltage slopes can be controlled varying the values of $R_{g,on}$.

3.1.2 Operating at turn-off transition

As shown in Fig 3.2, when PWM input drops to zero in t_5, M_2 and T_2 are turned on and V_{gs} starts to fall until it reaches the Miller Plateau voltage in t_6. The voltage V_{gs} is approximately constant in t_6 and in this time, V_{ds} starts to rise, $V_{2,high}$ is reached, and T_2 is turned off, after that the delay $t_{d,2}$ is over. Therefore, only R_{off} is carrying current and I_g magnitude decreases with $R_{g,off} = R_{on} + R_{g,ext} + R_{g,int}$. After in t_7 the v_{ds} voltage matches the Vdc-bus but an overshoot is created due to the parasitic inductance L_{loop}. At that time, also I_d starts to fall. When $V_{2,low}$ is reached in t_8, T_2 is turned on and it is carrying current until turn-off transition is completed. After t_8, the SiC MOSFET is in blocking mode. In addition, slope for v_{ds} during turn-on transition is approximated from the following equation:

$$\frac{dv_{ds}}{dt} = \frac{i_{g,off}}{C_{gd}} \tag{3.4}$$

On the other hand, the expressions for the i_g current are:

$$i_{g,off} = \frac{-V_{gg-} - V_{Miller}}{R_{g,off}}, \tag{3.5}$$

taking into account *that* $R_{g,off} = R_{off} + R_{g,ext} + R_{g,int}$ in the interval t_7 - t_8. In addition, v_{ds} slope approximation is:

$$\frac{di_d}{dt} = gfs \cdot \frac{-V_{gg-} - V_{gs(th)} - \frac{I_d}{2 \cdot gfs}}{C_{iss} \cdot R_{g,off}}, \tag{3.6}$$

Regarding the equations (3.4)-(3.6), the current and voltage slopes can be controlled by varying the values of $R_{g,off}$.

3.2 An Analysis of AGD by using simulations

With the purpose of evaluating the general behaviour of the AGD, simulations were performed using the model of the buck chopper circuit shown in Fig. 2.5 and the real parameters of semiconductor devices. There are many simulators that allow integrating transistor models. Matlab/Simulink Simscape is software that has many tools and libraries that contain models that can be adapted to characterize the behaviour of the transistors in detail. Figure 3.3 shows the model used for simulations in Simscape. The simulations are realised considering the physical model and parasitic elements, and the real parameters of the N-channel SiC MOSFET SCT2080KE by Rohm Semiconductor and the SiC Schottky diode C3D25170H by Cree. Besides, Table 3.1 shows the parameters and conditions used to evaluate the AGD.

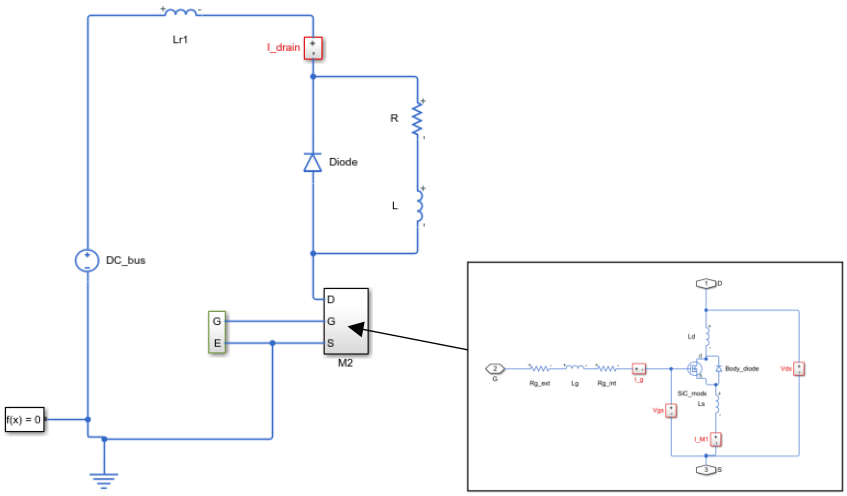

Figure 3.3. MOSFETs models used for simulations

Table 3.1. Parameters for AGD evaluation.

Parameter	Value
DC-bus	600 V
Maximum load current	20 A
Switching frequency	100 kHz
MOSFET power supply	-5/20 V
Load inductance	100 µH
Control signal for testing	50 % duty cycle

Gate-source voltage measurement

One of the main characteristics of AGD is to measure the v_{gs} voltage to operate. However, the $R_{g,ext}$ resistance can vary the results of the GD measurements. Then, taking into account the circuit of the Fig. 3.4 and considering that the $R_{g,in}$ value is commonly lower than $R_{g,ext}$, it is be concluded that the sensing is affected by the sensing point. An analysis with different $R_{g,ext}$ values and measurements the gate-source voltage (v_{gs}) on both sides of $R_{g,ext}$ was developed. The study was realised by using a $R_{g,ext} = 6.3\ \Omega$ (minimum

value recommended by datasheet), $R_{g,ext}$ = 22 Ω and a high resistance value, $R_{g,ext}$ = 50 Ω. The results depicted in Fig 3.5, shown that with the $R_{g,ext}$ increase, the $v_{gs,2}$ voltage delay for reaching the maximum and minimum v_{gs} value increases. Accordingly, if the resistance $R_{g,ext}$ is low, the v_{gs} voltage delay between the measures $v_{gs,1}$ and $v_{gs,2}$ is quite small.

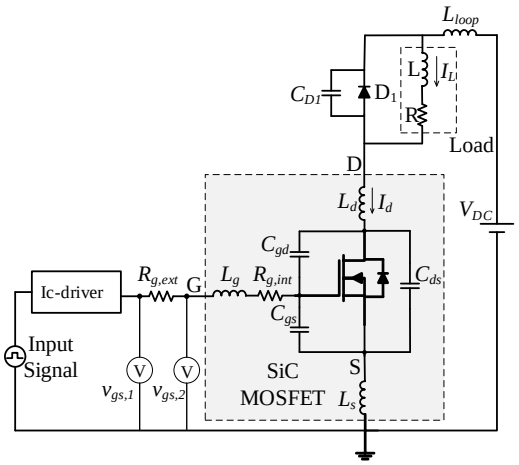

Figure 3.4. Test circuit representation for measuring v_{gs} voltage on both side of R_{g_ext}

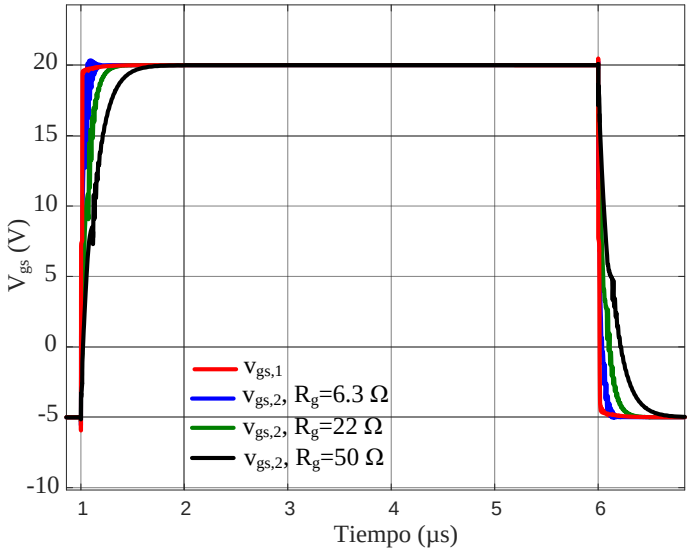

Figure 3.5. Test circuit representation for measuring V_{gs} voltage on both side of R_{g_ext}

Turn-on and turn-off behaviour analysis

In this section, an analysis between CGD and the proposed AGD is realized in turn-on and turn-off transition. First, the Miller plateau voltage is characterized taking into count the modelling and dynamics characteristics of the SiC MOSFET, to define the R_{on} and R_{off} resistances and the reference voltages. Because the purpose of the simulations was to evaluate the general behaviour of the SiC MOSFETs using

the AGD, the reference voltages and the gate resistances were determined qualitatively. In the following section, a more detailed study of the GD is carried out using the models presented in Chapter 2.

The obtained values for the study were R_{on}=10 Ω and R_{off} = 15 Ω. The value of the CGD is used considering the value recommended by the manufacturer, which is 6.3 Ω. After characterizing the dynamic behaviour of the SiC MOSFET, the references values were defined. For turn-on transition $V_{1,hihg}$=15 V and $V_{1,low}$ = 10 V. $V_{2,hihg}$ =10 V and $V_{2,low}$ = 0 V for turn-off. The Fig. 3.6 shows the drain current I_d waveforms for these conditions defined and Fig. 3.7 shows the V_{ds} waveforms.

As it is shown in Fig. 3.6 the active gate driver can reduce the magnitude of the ringing in the turn-on process. However, in turn-off transition, the delay is increased with the AGD. This effect in the delay switching transition can increase the switching losses. Regarding the Fig. 3.7, the drain-source voltage has better behaviour in turn-on transition but in turn-off transition can be seen that the delay is higher with the AGD. Nevertheless, the over-voltage is considerably reduced in comparison with $R_{g,ext}$ = 6.3 Ω. Also, this AGD can be improved for the trade-off between the delay and over-voltages.

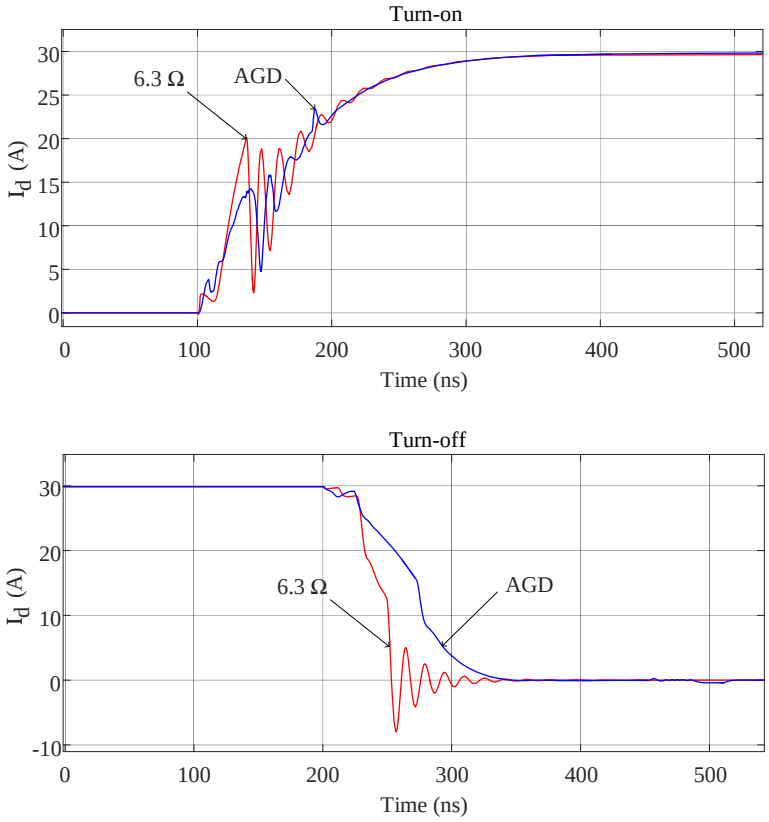

Figure 3.6. Turn-on and turn-off I_d with R_g = 6.3 Ω and AGD. $V_{1,high}$ =15 V and $V_{1,low}$ =10 V, and $V_{2,hihg}$ = 10 V and $V_{2,low}$ = 0 V for AGD

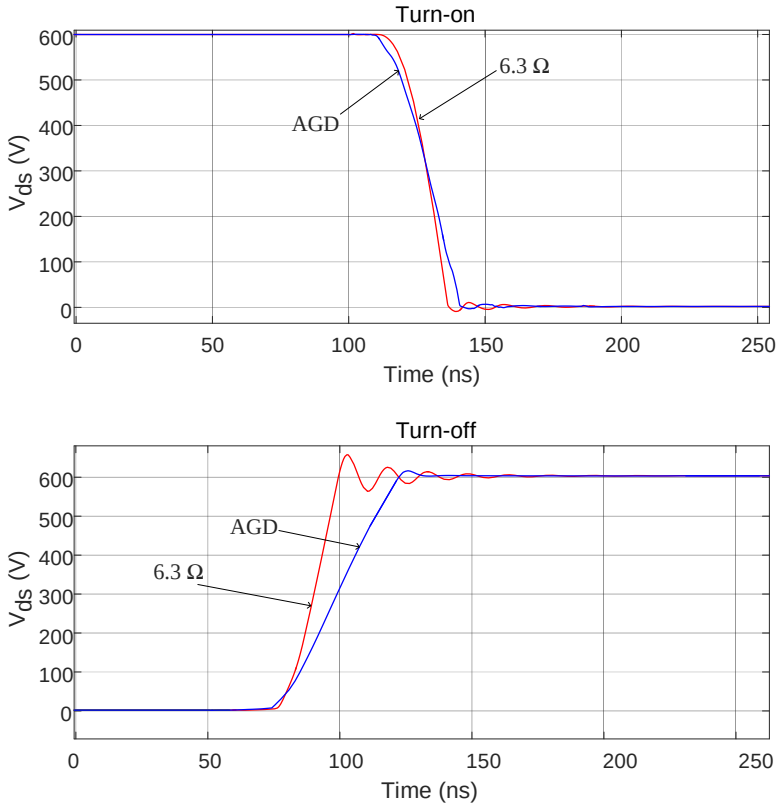

Figure 3.7. Turn-on and turn-off V_{ds} with R_g = 6.3 Ω and AGD. $V_{1,high}$ = 15 V and $V_{1,low}$ = 10 V, and $V_{2,high}$ = 10 V and $V_{2,low}$ = 0 V for AGD.

On the other hand Fig. 3.8 shows the behaviour of the gate-source voltage. In the turn-off transition can be seen clearly the effect of this AGD. The slope changes in the interval of 10 V and 0 V is as expected. It is important to mention that among larger is the window comparator interval the delay and losses can increase. On the other hand, if the R_{on} or R_{off} are very large, the losses and the switching delays can be affected.

The Fig. 3.9 offers a representation of the gate current in both turn-on and turn-off transitions. According to corresponding figures, the I_g changes with the AGD. Also, in turn-on the I_g has more oscillations, this due to the behaviour of T_1 and T_2.

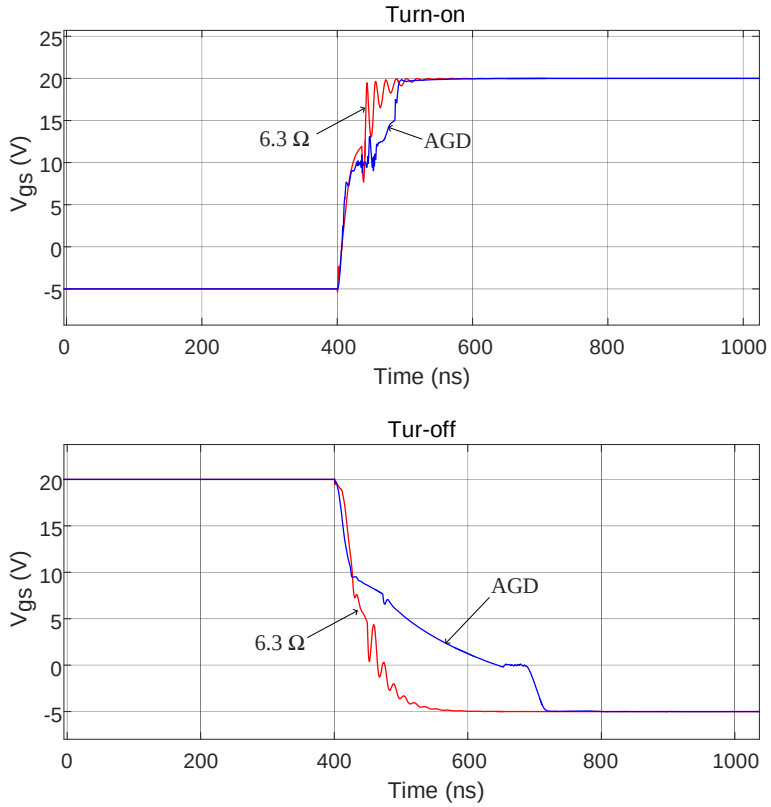

Figure 3.8. Turn-on and turn-off V_{gs} with R_g = 6.3 Ω and AGD. $V_{1,high}$ =15 V and $V_{1,low}$ = 10 V, and $V_{2,high}$ = 10 V and $V_{2,low}$ = 0 V for AGD

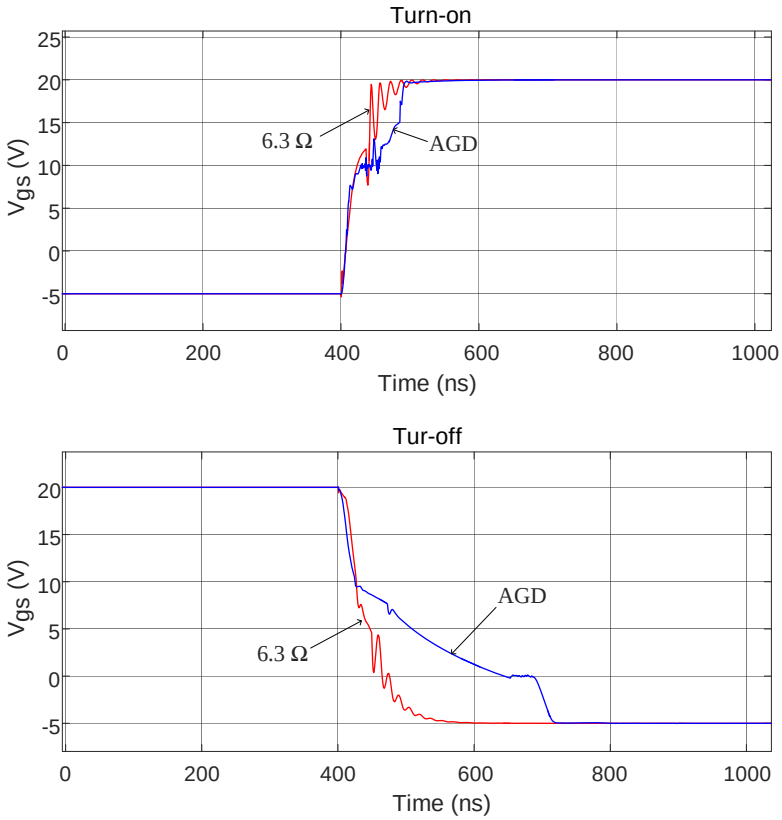

Figure 3.9. Turn-on and Turn-off I_g with R_g = 6.3 Ω and AGD. $V_{1,high}$ = 15 V and $V_{1,low}$ = 10 V, and $V_{2,high}$ = 10 V and $V_{2,low}$ = 0 V for AGD

Switching losses analysis

In order to evaluate the performance of the proposed AGD, a comparison of switching total losses is developed. Fig. 3.10 shows that the total switching losses of the AGD are higher than CGD with 6.3 Ω. However, the difference is small and the over-current and over-voltage problems are reduce. Furthermore, the proposed AGD can be improved and achieve better results.

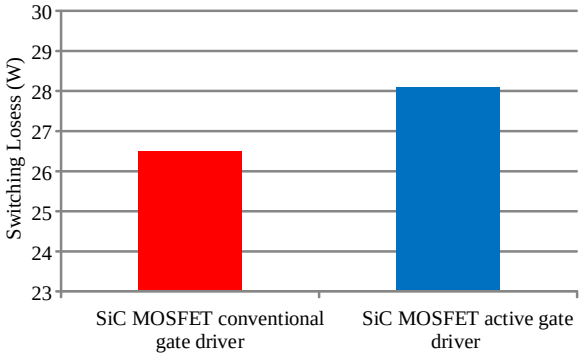

Figure 3.10. Prototype of the open loop AGD for one device

Regarding the results, the AGD reduces the over-voltage and ringing as was expected, which leads to decrease the EMI and the stress in the power MOSFET. It is important to consider that the resistance values of the R_{on} and R_{off} are higher than the simulations. This is due to the elements considerate in the modelling in Simscape. Although the experimental test was developed in low voltage, this driver is a new solution for applications in high power and high frequency due to analysis realized. Additionally, the results can be improved using faster devices.

3.3 AGD experimental validation

3.3.1 AGD design and parameter calculation for experimental studio

This section present the main parameters calculation, voltage calculation, time intervals and optimization of these values. Based on method to calculate the gate resistance presented in chapter 2 and taking into account the equations (2.6) and (2.7), gate resistance values of R_{on} and R_{off} were calculated and are 28.3 Ω and 32.1 Ω respectively.

3.3.2 Time intervals calculation

If conventional gate driver (CGD) with fixed resistance is used, the time intervals to define the behaviour of the AGD can be calculated. Regarding the Fig. 2, the time $t_{1,1}$ is calculated as $t_2 - t_{df,1}$ and t_2 is expressed in equation (3.7), where $t_{df,1}$ is considered constant.

$$t_2 \cong R_{g,on} \cdot C_{iss} \cdot ln\left(\frac{V_{gg}-v_{gs(th)}}{V_{gg}-\left(\frac{2 \cdot I_d}{g_{fs}}\right)+v_{gs(th)}}\right). \quad (3.7)$$

On the other hand, the delay t_{d1} is the interval $t_3 - t_2$ and the time t_3 is expressed as:

$$t_3 \cong \frac{Q_{gd} \cdot R_{g,on}}{\left(V_{gg} - \left(\frac{2 \cdot I_d}{g_{fs}} + v_{gs(th)}\right)\right)} \tag{3.8}$$

where the Q_{gd} is gain-drain charge. For turn-on transition, the delay $t_{d,2}$ is the interval $t_7 - t_6$ where t_6 and t_7 are determined as:

$$t_6 \cong R_{g,off} \cdot C_{iss} \cdot ln\left(\frac{V_{gg}}{\left(\frac{2 \cdot I_d}{g_{fs}}\right) + v_{gs(th)}}\right), \tag{3.9}$$

$$t_7 \cong \frac{Q_{gd} \cdot R_{g,off}}{\left(V_{gg} - \left(\frac{2 \cdot I_d}{g_{fs}} + v_{gs(th)}\right)\right)}. \tag{3.10}$$

3.3.3 Optimal values for reference voltage $V_{1,low}$ and optimal delay $t_{d,2}$

As previously mentioned, $V_{1,low}$ and $t_{d,2}$ are the parameters that influence the optimal behaviour of the current i_d and voltage v_{ds}. Accordingly, to reach a better design, $V_{1,low}$ and $t_{d,2}$ are calculated realizing the optimization between losses and switching times.

Taking into account the method to calculated the switching losses and using the equations (2.8) and (2.9), the E_{on} and E_{off} losses were calculated and the optimal t_{rise} and t_{fall} were obtained. Then, times obtained by the equations (3.7)-(3.10) were used to calculated $V_{1,low}$ and $t_{d,2}$. Tables 3.2 and 3.3 show the variation values when the $V_{1,low}$ and $t_{d,2}$ were finally calculated. In addition, the delay $t_{df,1}$ of 28 ns and minimal losses E_{min} = 350.4 µJ (for R_g = 6 Ω) were considered.

Table 3.2. Turn-on energy losses and current peaks.

$V_{1,low}$ (V)	di/dt (A/µs)	α	I_{rr} (A)	σ_1	E_{on} (µJ)	E_{on}/E_{min}
5	14.5	0.47	1.8	0.63	195	2.43
6	15.8	0.50	2.3	0.74	182.3	2.27
7	16.8	0.58	2.7	0.88	163.6	2.03
8	22.4	0.59	3.2	1.05	134.3	1.67
9	27.1	0.63	3.8	1.16	128.2	1.59
10	37.3	0.11	4.2	1.29	115.3	1.43
11	36.8	0.81	4.7	140	95.6	1.19
12	47.2	0.92	5.1	146	88.2	1.1

Table 3.3. Turn-on energy losses and voltage overshoots.

t_d (ns)	V_{os}	σ_2	E_{off} (µJ)	E_{off}/E_{min}
200	2	1	195	2.43
197	15	1.04	182.3	2.27
156	79	1.19	163.6	2.03
130	88	1.22	134.3	1.67
114	135	1.33	128.2	1.59
96	162	1.145	115.3	1.43
92	189	1.47	95.6	1.19
88	198	1.49	88.2	1.1

3.4 AGD evaluation

To evaluate the proposed AGD concept an experimental study has been carried out by using the standard clamped inductive circuit depicted in Fig. 2.5. The circuit consists of an inductive load, clamped diode with its parasitic capacitance (C_{D1}), and the SiC power MOSFET with parasitic elements. The L_{loop} represents the parasitic inductance, which is created in the loop of the PCB and power devices. Besides, the gate driver circuit for one device was designed and implemented and is shown in Fig. 3.11.

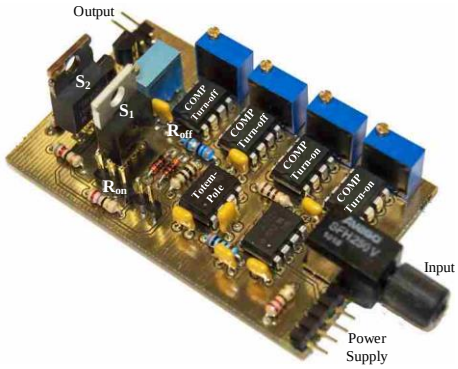

Figure 3.11. Prototype of the open loop AGD for one device

The main experimental tests have been realized by using the N-channel SiC MOSFET SCT2080KE by Rohm Semiconductor and the SiC Schottky diode C3D25170H in hard switching conditions. The load current was 6 A, and the value of L was 87.7 µH. A square signal with 50% of duty cycle and frequency at 100 kHz was applied in the input. The Voltage dc-bus was 400 V and the V_{gg} supply was -5/20 V. The parasitic capacitances were taken from the datasheet and parasitic inductances were measured by considering previous methodologies [36], [65]. The final values for parasitic elements are listed in Table 3.4.

An inductance L_{loop} was connected on the circuit to emulate the oscillations and overshoots. In addition, the maximum values of R_{on} and R_{off} were calculated and the selection of the voltage references were realized.

Table 3.4. Comparison of characteristics, availability and cost of devices for WCS.

Parameters	Value	Unit
C_{d1}	187.5	pF
C_{gd}	16	pF
C_{gs}	2064	pF
C_{ds}	61	pF
L_d	6	nH
L_g	7	nH
L_S	9	nH
L_{loop}	190.5	nH

3.4.1 Experimental validation analysis of the AGD

With the calculated values in the previous subsection, experimental setup of the AGD for both turn-on and turn-off transitions were developed. Firstly, an evaluation test between AGD and CGD with the minimum fixed $R_{g,ext}$ of 6.3 Ω was carried out. The purpose of this comparison was to analyse the overshoots and oscillations behaviour of the AGD and the CGD with minimal resistance. In addition, for the AGD the initial values of R_g and reference voltages were used according to the values calculated previously. The commercial values R_{on} = 27 Ω and R_{off} = 33 Ω were used finally.

The value references considered for the study taking into account the results listed in Tables 3.2-3.3, were $V_{1,hihg}$ = 14 V and $V_{1,low}$ = 7 V for turn-on transition and $V_{2,hihg}$ = 8 V and $V_{2,low}$ = 2 V for turn-off transition. On the one hand, Fig. 3.12 shows the experimental results of v_{gs} and the Ig respectively. On the other hand, the v_{ds} and I_d impact when the driver is applied are shown in Fig. 3.13 and Fig. 3.14 for turn-on and turn-off transition.

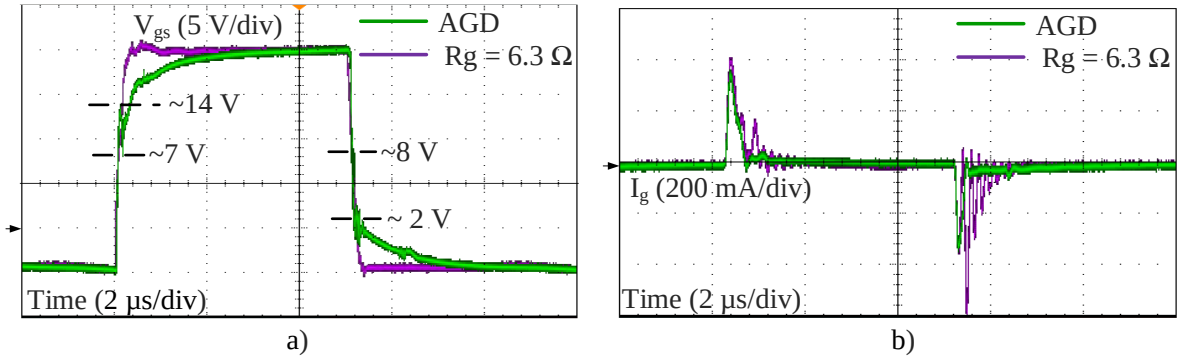

Figure 3.12. Experimental results for voltage V_{gs} transitions. R_g= 6.3 Ω and AGD with $V_{1,high}$ =14 V and $V_{1,low}$=7 V and $V_{2,high}$ =8 V and $V_{2,low}$= 2 V. a) voltage-source voltage, b) gate current.

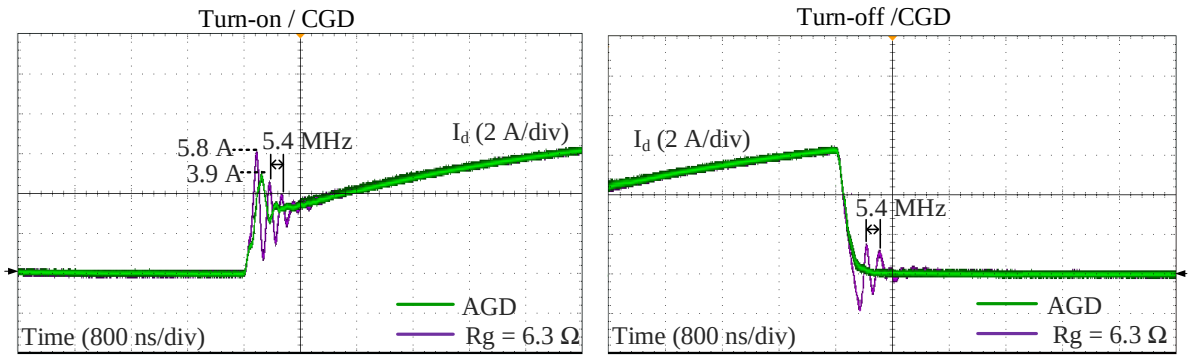

Figure 3.13. Experimental results of I_d for tur-on and turn-off transition. R_g = 6.3 Ω and AGD with $V_{1,high}$ = 14 V and $V_{1,low}$ = 7 V and $V_{2,high}$ =8 V and $V_{2,low}$ = 2 V.

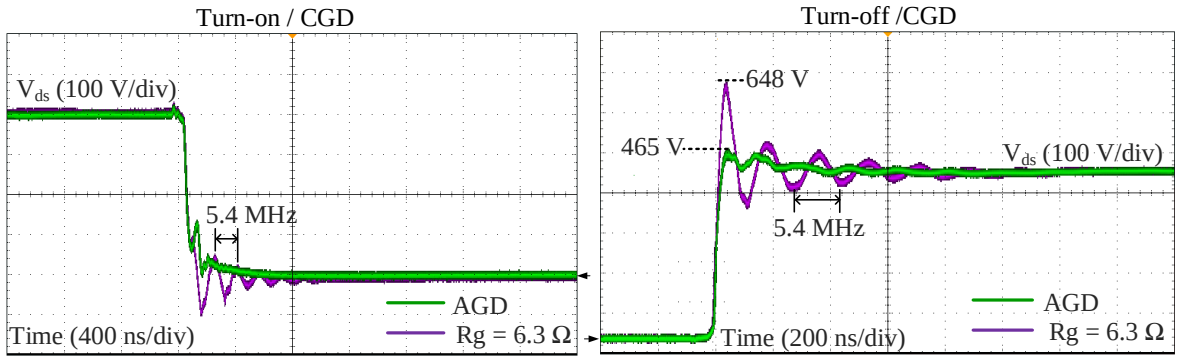

Figure 3.14. Experimental results of V_{ds} for tur-on and turn-off transition. R_g = 6.3 Ω and AGD with $V_{1,high}$ = 14 V and $V_{1,low}$ = 7 V and $V_{2,high}$ =8 V and $V_{2,low}$ = 2 V.

3.4.2 Experimental studio of the AGD with different SiC MOSFET models

To strengthen the experimental validation of the proposed AGD, an analysis with another SiC MOSFET was performed. Accordingly, the SiC MOSFET C2M0080120D by Cree was evaluated by using the AGD and CGD with the minimum fixed $R_{g,ext}$ of 2.5 Ω. For realising the analysis with the AGD, the presented method to determinate the gate resistances and reference voltages was used.

Regarding the calculation obtained, the gate resistance values for this SiC MOSFET were R_{on} = 33 Ω and R_{off} = 39 Ω. In addition, the voltage references were $V_{1,hihg}$ = 16 V and $V_{1,low}$ = 9 V for turn-on transition and $V_{2,hihg}$ = 10 V and $V_{2,low}$ = 3 V for turn-off transition. The test setup parameters were DC-bus = 400 V, switching frequency at 100 kHz, a load of 6 A and L = 120 µH. Whereas the parasitic elements were considered from the datasheet and previous experiments. The obtained data were compared with the results of a developed study with the SiC MOSFET SCT2080KE under the same operation conditions and AGD parameters used previously for this device. The voltage and current waveforms comparison is shown in Fig. 3.15.

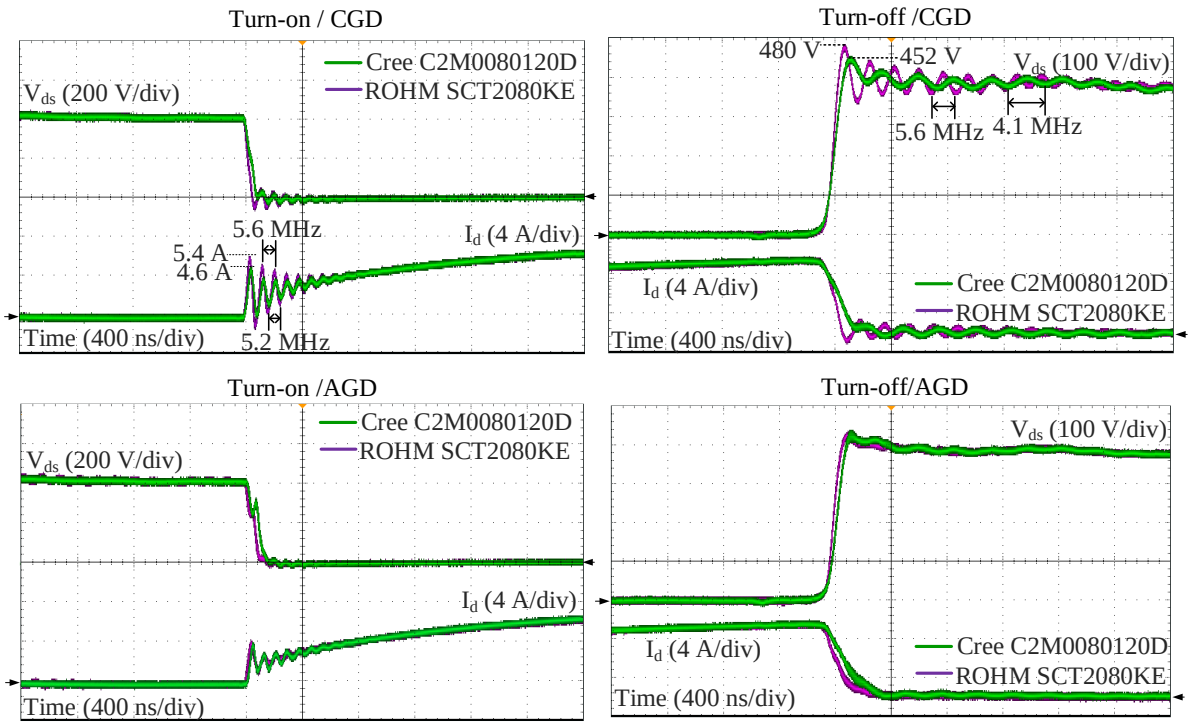

Figure 3.15. Experimental results of I_d and V_{ds} for turn-on transition between two SiC MOSFETS.

In the figures can be seen that the behaviour in both power devices is similar with CGD. Whereas the overshoots in Cree MOSFET are low, the switching delay times are better in Rhom MOSFET. In addition, the frequency oscillations are bigger in the latter. Furthermore, with AGD the oscillations and overshoots are reduced in both devices, despite of the switching time in SiC MOSFET C2M0080120D is longer. Therefore, it can be concluded that the AGD is valid for different MOSFETs and its performance depend on the characteristics of each device and the proper parameters calculation.

3.5 AGD viability study

This section studies the viability of the AGD, performance; EMI and cost.

3.5.1 SiC MOSFET performance analysis with AGD

The aim of the proposed AGD is to reduce the oscillations in both current and voltage but also to reduce total losses. Accordingly, the performance of the AGD was analysed for the SiC MOSFET SCT2080KE, realising a comparison between losses with the AGD and losses with the CGD. The total losses were calculated as:

$$P_{total} = P_{conduction} + P_{switching} + P_{gate}, \tag{3.11}$$

where

$$P_{conduction} = R_{ds(on)} \cdot (I_{d,rms})^2, \tag{3.12}$$

and

$$P_{gate} = \left(V_{gg,on} + \left|V_{gg,off}\right|\right) \cdot Q_{gate} \cdot f_{sw}. \quad (3.13)$$

Table 3.5 shows the experimental results of switching losses by cycle, with operation conditions of 400 Vdc-bus, 6 A on the load, f_{sw}=100 kHz, Q_g =106 nC and $R_{ds(on)}$=125 mΩ (Tj=125◦C).

Table 3.5. Numerical comparison of power losses.

Gate drivers	P_{gate} (W)	P_{cond} (W)	P_{sw} (W)	Total losses (W)
CGD with minimum R_g	0.233	1.25	35.04	36.5
CGD with large R_g	0.254	2.03	85.4	87.6
Proposed AGD	0.252	1.66	39.1	40.9

On the one hand, the performance of proposed AGD has been compared with CGD and fixed resistance of 6.3 Ω justified previously. The complete analysis has been realized with the purpose of obtaining the approximation of minimal losses with the minimal considered resistance. On the other hand, an analysis of CGD with large fixed resistance and different values for turn-on and turn-off path has been performed.

The considered resistances for this evaluation have been the maximum values calculated and selected previously, which were 27 Ω for turn-on and 33 Ω for turn-off paths.

According to results, the conduction losses are low due to them being dependent on statics characteristics of the SiC MOSFET such as $R_{ds(on)}$ and blocking capabilities. Despite this, the conduction losses have an important variation between the AGD and the CGD with different resistance values. This variation is because of the $i_{d,rms}$ current changes with respect to the maximum and minimum drain current that can have significant differences for each driver.

Besides, in Table 3.4 it can be seen that the conduction losses and losses in the gate are less than the switching losses. Therefore, only the switching losses play an important role. With AGD the switching losses are 4.4 W more than CGD with minimum fixed resistance. However, the switching losses are 40.9 W and are less than CGD with fixed large resistance.

3.5.2 Electromagnetic interference analysis

The proposed AGD has the capability of reducing the ringing and oscillations in both drain current and drain-source voltage, as shown in Fig. 3.14. In general, the high *dv/dt* is the main parameter of conduced EMI production in power converters. Therefore, although the proposed AGD only reduces the overshoot voltage in 28.2%, the oscillation are eliminated.

The purpose of this EMI study is to have an understanding of the noise provoked mainly by high *di/dt* and *dv/dt*. Therefore, this analysis does not include the total noise but also the main oscillation in the current and voltage waveforms.

Accordingly, the effect of oscillations can be characterized considering the current or voltage source as a periodic trapezoidal pulse and FFT analysis. In addition, it is important to consider that the id and v_{ds} measures were in common mode (CM) conditions.

Fig. 3.16 shows an approximation of the spectrum for both v_{ds} voltage and id current. These results were obtained from experimental measurement by means of an oscilloscope Tektronix MDO3024 and the spectrum was obtained applying the FFT in MATLAB software after the data were processed. The results show that the AGD can eliminate the noise in v_{ds} voltage and reduce the noise in id current with a resonant frequency of 5.4 MHz.

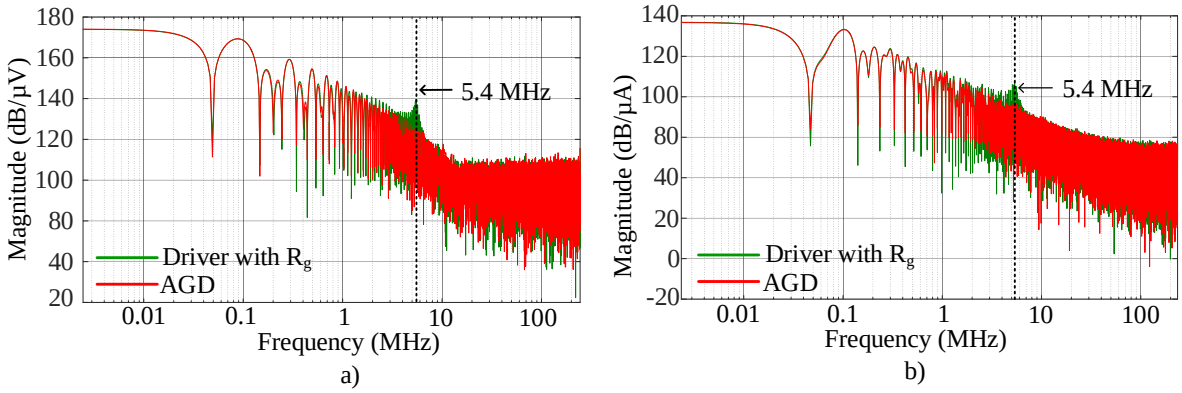

Figure 3.16. Spectrum comparison between CGD with R_g=6.3 Ω and AGD for I_d and V_{ds} experimental results. a) Spectrum approximation of V_{ds} and b) spectrum approximation of I_d.

3.5.3 Cost study

As noted above, the SiC MOSFET requires a driver to supply the device, achieve better performance, reliability and even reduce EMI problems. In power converters with a simple gate driver, the snubber circuits are necessary to reduce the EMI problems and overshoots. However, the snubber circuits could reduce the system efficiency.

As an example, the total cost of the driver plus snubber circuit can be considered 100 % and it is obtained regarding the driver components cost. One optocoupler driver HCPL-3120 with 10 % price, one isolated power supply with 54 % of the cost and a snubber network with of 36 % of total cost.

Mainly the high-speed comparators and MOSFETs increase the cost of the proposed gate driver. Regarding Fig. 1 four high-speed comparators and four MOSFETS are required.

For the implementation of the proposed AGD, four ANALOG DEVICES AD8561ANZ comparators were used with a 16 % price per unit. In addition, two N-channel MOSFETS IRF520NPBF and two P-channel MOSFETs IRF9520PBF were used with a price of 3 % per unit. Assuming, that the rest of components have an approximately cost of 36 %, and one isolated power supply of 54 % value; the AGD approximated total cost is 166 %. It is also important to mention that the components cost of this study was

consulted for a few components, not for large series. In addition, this type of solutions could be integrated into specific gate drivers, reducing, even more, the final cost compared to bulky snubber.

In Table 3.6 a comparison of approximated costs and main characteristics between CGD plus snubber network and proposed gate driver is developed. The comparison shows that the AGD is a good solution and in spite of its cost it has advantages in terms of efficiency, EMI and overshoots reduction.

Table 3.6. Comparison of characteristics, availability and cost of devices for WCS.

Drivers	Cost (%)	Efficiency	EMI reduction	Overshoots reduction
GD + Snubber	100	Medium	High	High
Proposed AGD	166	High	High	High

3.6 Conclusions

A new AGD has been presented under hard-switching conditions. The concept of the controller was defined and the main parameters were calculated and optimized. The new gate driver can control the *di/dt* turn-on and the *dv/dt* turn-off individually with low switching losses. The proposed AGD has been validated in two parts. First part shows a study of the AGD by using simulations in Matlab/Simulink applying models which was developing taking into account the real parameter of the devices. The simulations showed that the driver can reduce the over-voltage and ringing caused by high frequency and high voltage. Whereas, the power losses were higher in comparison with CGD but a small difference.

The second part consisted of realizing an experimental evaluation at 100 kHz of switching frequency and 400 V of dc-bus. The results showed that the AGD can reduce the overshoot voltages until 28.2% and until 31.6% of the current peak. The reduction of the overshoots leads total switching losses until about 53.3% less than conventional gate driver with high gate resistance fixed. On the other hand, the AGD cannot only attenuate the current oscillations, but also eliminated the voltage oscillations, which are caused by parasitic elements in 5.4 MHz for conditions of this study. In addition, an experimental validation for two different SiC MOSFET has been developed. The two devices evaluation show that the active gate driver can work for any SiC MOSFET. Taking into account all of the above, it has been demonstrated that if the energy on gate-voltage trajectory of the SiC MOSFET is reduced, varying the R_g on a specific interval of v_{gs} around the Miller Plateau zone, the overshoots problems are reduced without compromising performance. Although this driver needs two switching devices and high-speed comparators, it is a good solution due to its control simplicity. In addition, the AGD can be implemented as a closed-loop control with the output signals, just by adding simple analogy circuits connected to the load. Therefore, this AGD is a good alternative to snubber circuits and even complex gate circuits presented so far.

4

Advanced gate driver for SiC MOSFET based on feedback circuits

Chapter 3 showed a gate driver solution based on open-loop control. Even the AGD presented good results there are several considerations that should be addressed to improve the solution. Load variation and temperature variation are the main considerations during the AGD driver designs.

In this chapter, an active gate driver based on the multi-stage concept is presented. The gate driver includes a feedback circuit which measures the drain current and drain-source voltage for modulating the gate resistance and then, to reduce the oscillations and overshoots. This chapter also presents the AGD design and an analysis of the AGD by means of experimental tests.

CONTENTS:

4.1 Concept and operating principle of the AGD

4.1.1 Operating principle

Fig. 4.1 shows the general schematic circuit of the proposed AGD. The basic architecture of the AGD was presented in chapter 2. The AGD has a typical totem-pole configuration and two circuits placed on the turn-on and turn-off transition path. Each circuit consists of one switch in parallel with one resistance, T_1 in parallel with R_{on} between the nodes AB and T_2 in parallel with R_{off} between the nodes BC. T_1 and T_2 are controlled by a feedback loop that has a control circuit, a conditioning circuit and sensors for measuring the status of current I_d and voltage V_{ds}.

It is important to mention that an external gate resistance ($R_{g,ext}$) is connected because the switches M_1, M_2, T_1 and T_2 could have a very low on-resistance ($R_{ds,on}$). Therefore, the power SiC MOSFET would be outside of the SOA when the gate current i_g is only driven through M_1 and T_1 or M_2 and T_2. The minimum $R_{g,ext}$ to ensure SOA of the MOSFET can be calculated or considered according to the recommended value in the datasheet. In this gate circuit $R_{g,ext}$ value used was 6.3 Ω obtained from the datasheet.

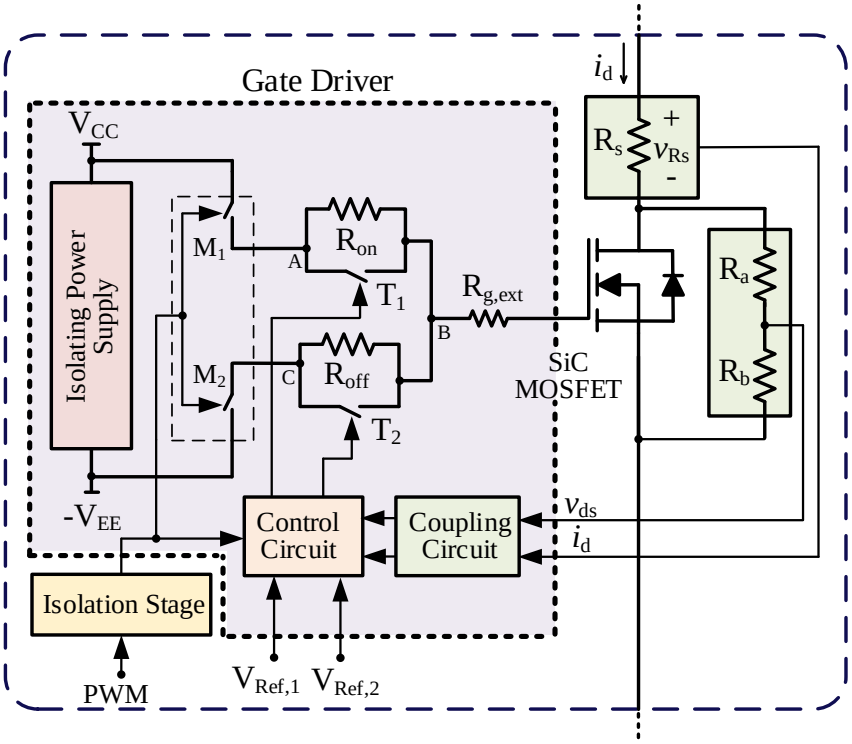

Figure 4.1. General scheme of the proposed gate driver based on feedback circuits for one device

The principle of the proposed AGD consists of adapting the total R_g values during the turn-on and turn-off transitions stages of the SiC MOSFET as is shown in Fig. 4.2. R_g is adapted in such a way that is increased its value in the stage where the oscillations and overshoots occur, that is, in Miller Plateau zone of the gate-source voltage in both turn-on and turn-off transition. Meanwhile, R_g has a smaller value in the rest of the transition stages. The transition times of the SiC MOSFET are divided into six stages as shown Fig. 4.2.

The control of the transistors T_1 and T_2 define the duration stages through of a feedback circuit that measures the status of the current I_d and the voltage V_{ds}, and two delays t_{d1} and t_{d2}. The voltage and current measured are properly conditioned and compared with a reference voltages $V_{ref,1}$ and $V_{ref,2}$. Whereas, $V_{ref,1}$ is the equivalent voltage of I_d measured by a sensor current, $V_{ref,2}$ is a conditioned signal of a voltage sensor.

On the one hand, $V_{ref,1}$ should be calculated in the point where I_d reaches the nominal value. However, due to the delay $t_{d,1}$ caused by the feedback circuits in the turn-on path, the $V_{ref,1}$ is selected before reaching the nominal value of the current taking into account the delay $t_{d,1}$. Similarly, $V_{ref,2}$ would be defined before maximum V_{ds} due to the delay t_{d2} caused by the feedback circuit in the turn-off path.

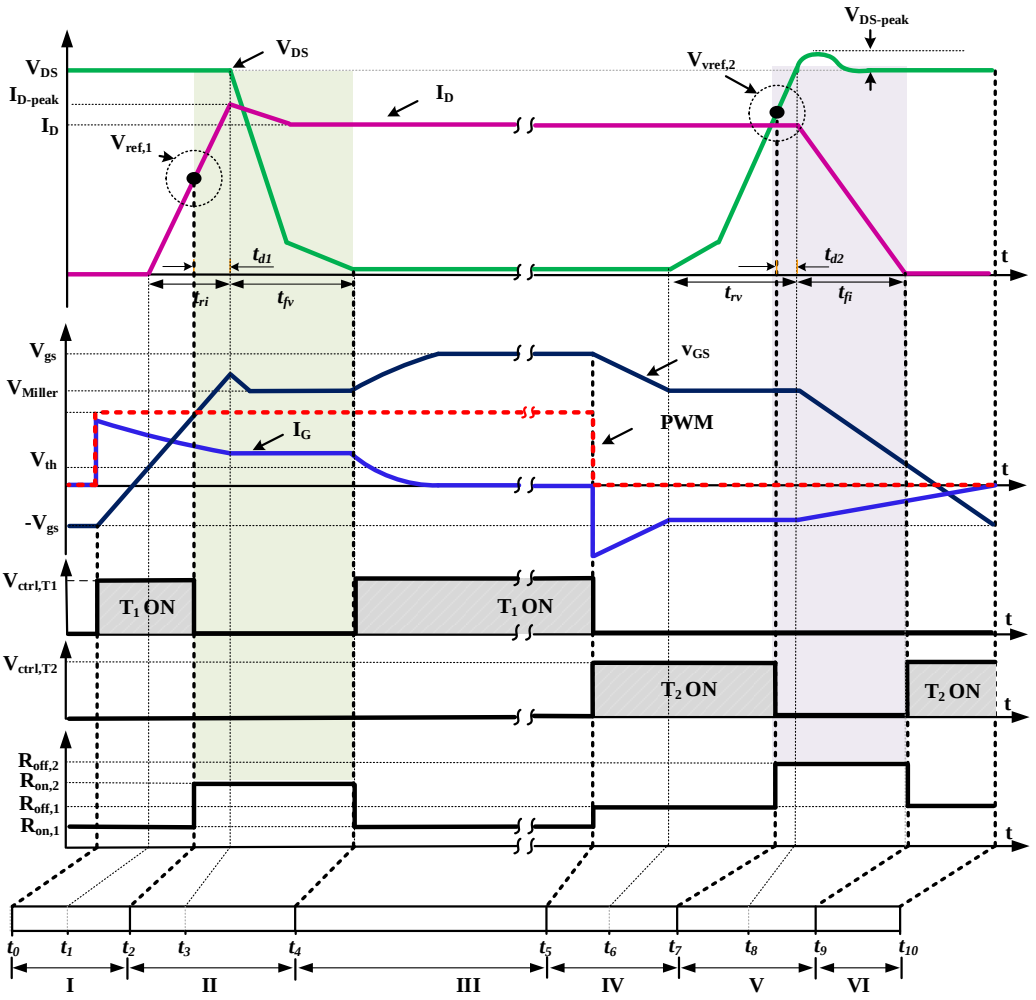

Figure 4.2. Turn-on and turn-off SiC MOSFET waveforms and control signals for S1 of the AGD.

4.1.2 Operating principle at turn-on

Regarding the Fig. 4.1 and Fig. 4.2, in the turn-on transition, stage I starts when the PWM signal is high and M_1 is ON; then the switch T_1 is closed and the voltage v_{gs} starts to rise and the gate-current is driven through the resistance R_{on} and T_1. When v_{gs} reaches the voltage threshold (V_{th}), the I_d current rises toward its maximum value. When I_d current exceeds the current reference $V_{ref,1}$, T_1 is opened and the gate resistance value changes to stage II. Consequently, the gate current I_g is only through R_{on}. T_1 continues OFF until v_{gs}

reaches the maximum value and the gate resistance changes again to a minimum value and so, III is achieved. T_1 remains ON until turn-on transition ends.

4.1.3 Operating principle at turn-off

As in the previous case, during turn-off transition, the stage IV starts when the PWM signal changes from high level to low level and T_2 is then closed. At that time, the v_{gs} voltage starts to falls toward the minimum value and the negative gate-current I_g is driving through the resistance R_{off} and T_2. After that, V_{ds} rises toward the dc-bus value. When V_{ds} exceeds the voltage reference $V_{ref,2}$, then T_2 is opened and only R_{off} is carrying current. This stage ends when v_{gs} falls to its minimum value, consequently, the gate-resistance value changes to stage V. Finally, the gate resistance changes again to a lower value and VI is achieved. The VI stage resistance value remains turn-off transition finishes.

4.2 AGD design

4.2.1 General consideration for the gate driver

The AGD driver should be a robust system not only to the effect of the parasitic elements but also to temperature and load variations. Thus, the parasitic elements such as capacitances and inductances and variations caused by temperature as voltage threshold V_{th}, as well as, load current variation are considered in the AGD design:

1) *Parasitic inductances:* the parasitic inductances can affect the behaviour of the switching devices in high-frequency operation. For this AGD design, the values are selected by using the values in Table 3.4.
2) *Parasitic capacitances:* the parasitic capacitances affect the behaviour of the switching transitions of the MOSFETs. Parasitic capacitances can be considered constant for specific drain-source voltage range as described in chapter 2.
3) *Voltage threshold variation:* the voltage threshold variation depend not only of the temperature changes but else the load variation. The threshold voltage plays an important role in gate driver design because for low values crosstalk effect happens. Then, this parameter should be considered in the gate driver designs. Section 2.2 analyses the threshold voltage effects.
4) *Temperature effect:* temperature variations can affect the design of this AGD because the voltage reference can change substantially. Then, the temperature should be analyzed in the AGD evaluation.
5) *Load variation:* load variations affect the voltage threshold and the current flowing in the transistors. Large load variations can affect the reference voltages of the AGD and affect its operation. Therefore, a load variation with the AGD should be studied.

4.2.2 Gate driver parameters design

Gate resistances, transition times and voltage references are the fundamental parameters of the AGD. In this section, these parameters are defined as the following:

1) *Gate resistances calculation:* the gate resistances are key parameters in the proposed AGD. The method previously presented in chapter 2 was used for calculating the gate resistances R_{on} and R_{off}. Based on this method R_{on} and R_{off} were calculated and the values used were R_{on}= 23Ω and R_{off} = 27Ω.
2) *Transition times:* transition times shown in Fig. 4.1 are obtained considering the overshoots and over current caused by *di/dt* and *dv/dt* slopes and considering the power switching losses in the ON and OFF times. For this AGD design, the delay times were obtained from the datasheets of the SiC MOSFETs used and by means experimental tests
3) *Voltage and current references:* in [75], the authors presented a method to choose the optimal value of the voltage reference. Then, by (4.1) an (4.2), the voltage reference can be calculated.

$$V_{ref,1} = v_{ds,1} = V_{bus} - \left(\frac{dv_{ds}}{dt}\right) \cdot t_{d1}, \tag{4.1}$$

$$V_{ref,2} = v_{Rs} = I_{d,1} \cdot R_s = \left(I_d - \left(\frac{di_d}{dt}\right) \cdot t_{d2}\right) \cdot R_s \tag{4.2}$$

4.2.3 Current and voltage sensors

Current sensors have been a topic to discuss for a long time. In [90] was realized a study of advantages and drawbacks of current sensors applied to power converters and the main challenges to measuring the current for high-speed switching devices [91]. The basic technique to measure the current is based on a shunt resistor. This technique is simple and cheaper, but the shunt resistor can represent high losses and instability in high current applications. Current sensor by using Rogowski coil is an alternative that has been used in design of GDs. This current method offers precision and isolating but its drawback is the use of an integrator, which increases the time in the loop. Generally, the current sensors used in GDs are based on the measurement of the voltage drop in the Kelvin inductor of the device. Nevertheless, this method is highly dependent on *di/dt* [92]. The current sensor used for this GD is based on a shunt resistor as shown in Fig. 4.1. The shunt resistance used was 20 mΩ and the voltage was amplified to get the desired equivalent current.

Besides, the voltage sensor consists of a voltage divider configuration connected in the SiC MOSFET drain and source terminal as shown in Fig. 4.1 and Fig. 4.3. The gate resistances used was proposed taking into account the parasitic inductance, temperature influence and tolerance.

4.2.4 Coupling stage and control circuit architecture

The control circuit was designed using high-speed operational amplifiers, comparators, and digital components. Fig. 4.3 shows the general circuits to condition and control T_1 and T_2. The V_{ds} voltage is measured with a voltage sensor and the signal is conditioned and compared with $V_{ref,1}$ through C_{OMP1}. In addition, a current sensor consists of the voltage measurement of a resistor (R_s) connected in series on the drain terminal of the SiC MOSFET to determinate the equivalent I_d. This voltage is conditioned and amplified by AMP_1 and it is compared with the equivalent voltage to the current reference $V_{ref,2}$ through $COMP_2$. In addition, for achieving the expected stages shown in Fig. 4.1, a Flip-Flops configuration and logic gates are used. Finally, the output signals are connected with the switches T_1 and T_2.

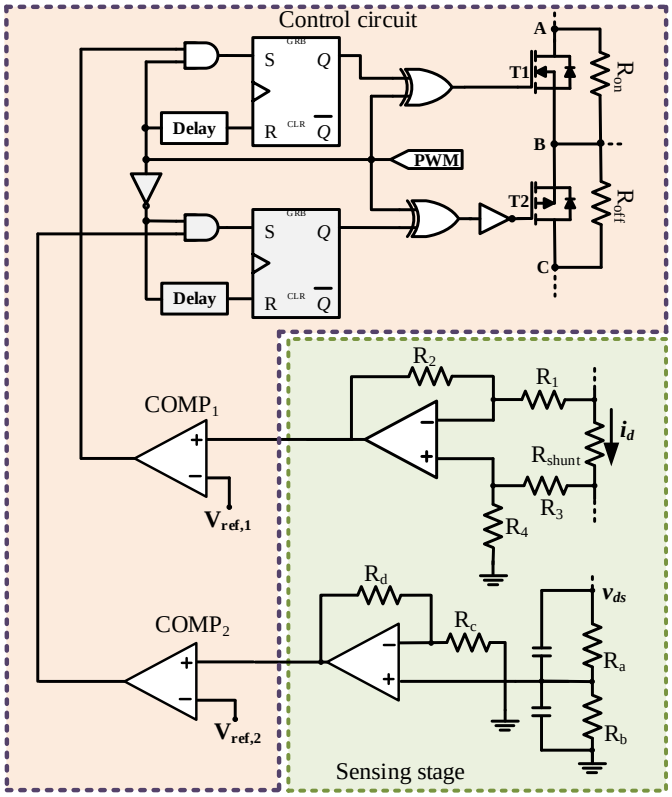

Figure 4.3. Circuit control of the feedback AGD

Fig. 4.4 shows the algorithm to control the switches and Table 4.1 and 4.2 is the truth table of the control circuit during the six stages.

Table 4.1. Logic states for turn-on

PWM	PWM+delay	Comp1	S	R	Q	T1
1	0	0	0	0	0	1
1	0	1	1	0	1	0
1	1	1	1	1	0	1
0	0	1	0	0	0	0
0	0	0	0	0	0	0
0	0	0	0	0	0	0

Table 4.2. Logic states for turn-off

$\overline{PWM}$	PWM+delay	$Comp_2$	S	R	Q	O_1	T_2
0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	0
1	0	1	1	0	1	0	1
1	1	1	1	1	0	1	0

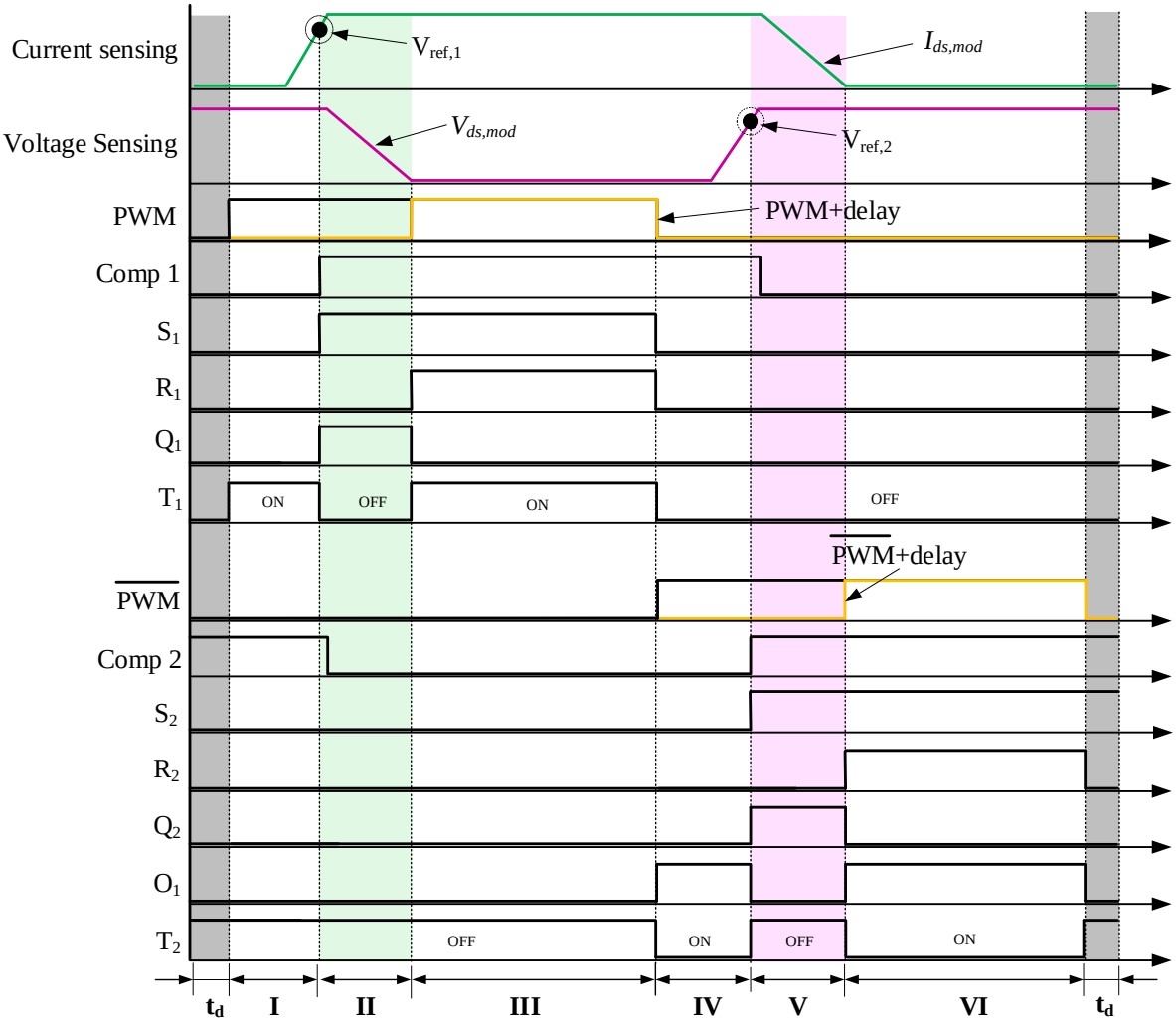

Figure 4.4. Control algorithm of the feedback AGD

4.3 Active gate driver development and experimental validation

The proposed AGD was evaluated in two steps. It was developed an experimental test for one device in hard switching conditions through the standard inductive clamped circuit shown in Fig. 4.5. The test bench and prototype para evaluation are presented in Fig. 4.6. and Fig. 4.7. Meanwhile, Tables 4.3 and 4.4 show

the components used for the AGD and the parameters for evaluation. In this step was also realized the optimization of delays and reference voltages. In addition, it is realized a study of variation load and its effects in the AGD. The analysis with temperature variation also was developed and a study of the performance was completed.

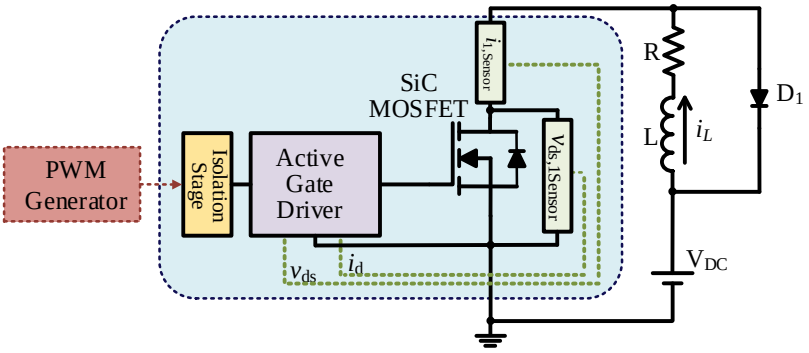

Figure 4.5. Power converter representation to evaluate the AGD.

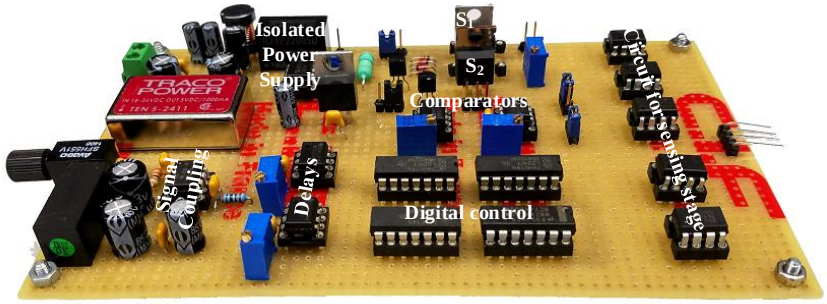

Figure 4.6. Active Gate driver prototype based on feedback control for one device

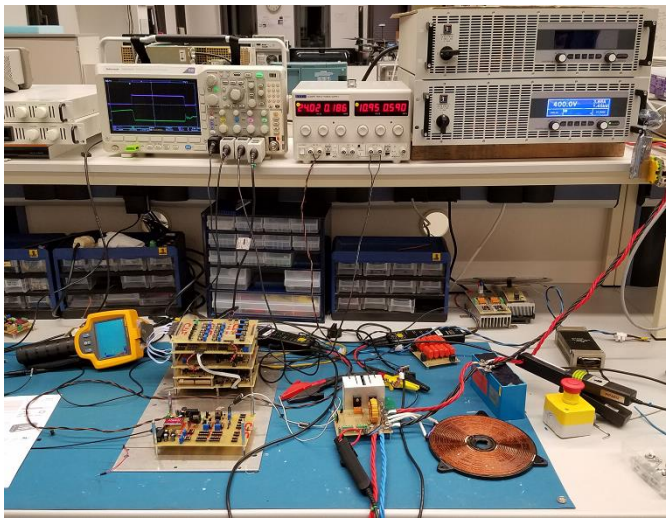

Figure 4.7. Experimental workbench for AGD evaluation

Table 4.3. Devices and elements used for the AGD

Device	Model	Characteristics		
		Parameter	Name	Value
NPN MOSFET	International Rectifier IRF520NPbF	-Vdss	Drain-Source Voltage	100 V
		-Id@ 100 °C	Drain Current	6.8 A
		-Vgs	Gate-Source Voltage	±20 V
		-Rds(on)	Drain-Source On-State Resistance	200 mΩ
		-PD	Power Dissipation	48 W
		-TJ	Operation Junction Temperature	-55 to +175 °C
PNP MOSFET	VISHAY IRF9520	-Vdss	Drain-Source Voltage	-100 V
		-Id@ 100 °C	Drain Current	-4.8 A
		-Vgs	Gate-Source Voltage	-10 V
		-Rds(on)	Drain-Source On-State Resistance	600 mΩ
		-PD	Power Dissipation	60 W
		-TJ	Operation Junction Temperature	-55 to +175 °C
Isolated Power Supply	RECOM R24P22005D	-Vdc-in	Input voltage Range	24 V
		-Vdc_out	Output voltage	+20/-5
		-Iout	Output Current	50/-200 mA
Isolated Power Supply	TRACO POWER TEN 5-2411	-Vdc-in	Input Voltage	24 V
		-Vdc_out	Output Voltage	+5 V
		-Iout	Output Current	1000 mA
High-speed comparator	AD8561	-tp	Propagation delay	9.8 ns
		-Vo	Output Voltage	3.5 V
		-Ps	Power Supply	5 V
High-speed Operational amplifier	AD8001	-St	Rise and fall time	1.4 ns
		-Sr	Slew rate	1200 V/µs
Shunt resistor		R	Resistance	20 mΩ

Table 4.4. Parameters for experimental validation of the feedback AGD

Parameter	Value
DC-bus	200 V
Maximum load current	10 A
Switching frequency	100 kHz
MOSFET power supply	-5/20 V
Load inductance	500 uH

4.3.1 Time transition and voltage reference optimization

As described earlier, the voltage references $V_{ref,1}$ and $V_{ref,2}$ are a function of *di/dt* and *dv/dt* and the transition times t_{ri} and t_{rv}. The voltages and times were determined by experimental evaluation and datasheets of the devices and an optimization analysis was developed. The results are depicted in Table 4.5 and Table 4.6. The values of the gate resistances $R_{g,on}$ and $R_{g,off}$ for this study were 33 Ω and 27 Ω respectively, whereas,

$R_{g,ext}$ was 6.3 Ω. The delays t_{d1} and t_{d2} were measured and the resulting values were 20 ns and 30 ns respectively. Then, $V_{ref,1}$ and $V_{ref,2}$ were calculated by (4.1) and (4.2) and the values obtained was 2.1 V and 2.5 V respectively. In addition, the control circuit was analyzed and Fig. 4.8 shows the signals obtained for each transistor.

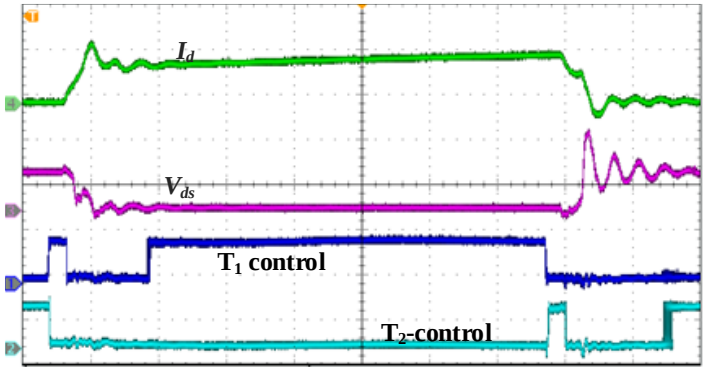

Figure 4.8. Control signals ofor T_1 and T_2

4.3.2 Study of the AGD under hard switching conditions

Taking into account the values of voltage references $V_{ref,1}$ and $V_{ref,2}$ and Fig.4.1, it was developed an evaluation between AGD and CGD with only the fixed resistance $R_{g,ext}$ of 6.3 Ω under hard switching conditions. The purpose of this comparison is to analyze the effect of the CGD with minimum R_g and the advantages of the proposed AGD. Fig. 4.9 and Fig. 4.10 show the I_d current and V_{ds} voltage. The signals were obtained by using the Oscilloscope Tektronix MD03024 by using the current probes Tektronix TCP0030A and voltage probes Tektronix THDP0200.

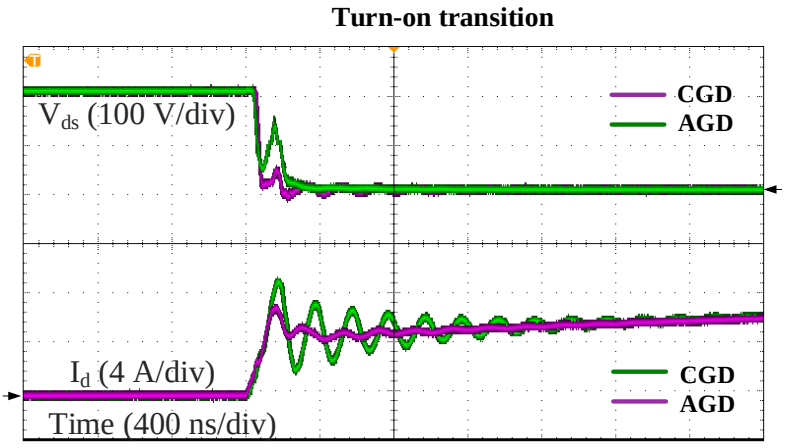

Figure 4.9. Comparison between CGD with R_g=6 Ω and AGD. Switching frequency 100 kHz, 200 V of DC-bus and $V_{ref,1}$=2.1 V.

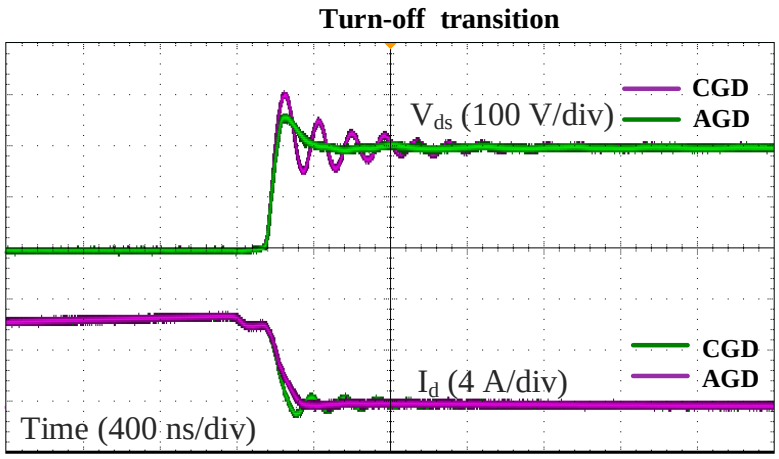

Figure 4.10. Comparison between CGD with R_g=6 Ω and AGD. Switching frequency 100 kHz, 200 V of DC-busand $V_{ref,2}$=2.5 V.

The results show that by using the CGD with small gate resistor the current oscillations are remarkable with resonant frequency at 5.4 MHz, maximum amplitude 8.2 A and switching speed *di/dt* of 94.4 A/µs. However, the AGD reduces the current oscillations 40% of the maximum amplitude leading a *di/dt* of 37.76 A/µs. For turn-off transition voltage oscillations with 5.4 MHz of resonant frequency, an overshoot of 310 V and *dv/dt* of 4.1 kV/µs by using the CGD. Nevertheless, the AGD damps the t oscillations and reduces 28.2 % of the voltage overshoot with *dv/dt* of 3.2 kV/µs.

An objective of the AGD is to analyse the temperature effect to verify its performance and its sturdiness in respect of temperature increase. A study of the AGD behaviour with the temperature was developed. Fig. 4.11 shows the comparison between different temperatures.

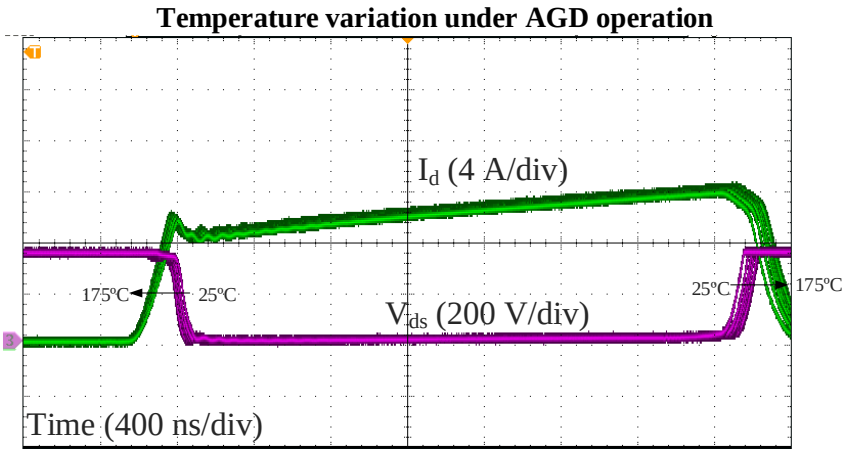

Figure 4.11. Behavior of the current and voltage with the temperature variation applying AGD. 100 kHz of switching frequency

Regarding the results, the current and voltage slopes have low variation for turn-on, but a representative variation in turn off. However, regarding the figure, AGD continues removing the oscillations and overshoots.

As was previously mentioned, the purpose of the AGD is to work under load variation conditions with high performance. Then, it developed an analysis with different loads and the results are shown in Fig. 412

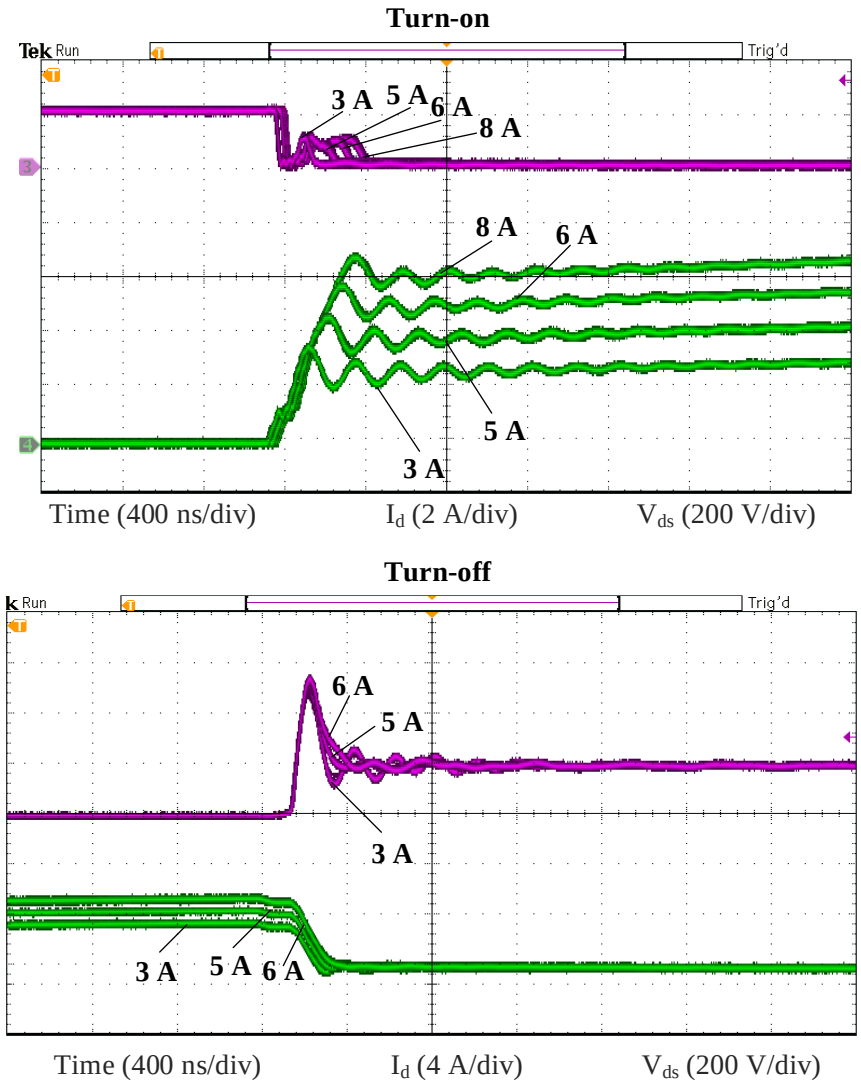

Figure 4.12. Load variation analysis applying AGD.

According to the results, the AGD remains effective while the charging current changes. This is because the AGD can independently control the slopes *di/dt* and *dv/dt*. However, it is important to note that for a very large variation, the reference values could change and therefore the AGD would stop acting.

The switching losses were calculated by using (3.11)- (3.13) and a comparison with the CGD was developed. The CGD was considered with two fixed resistances of 27 Ω and 22 Ω in both turn-on and turn-of transition path respectively. In Fig. 4.13, the comparison of the switching losses with load currents variation of 3-8 A between CGD and the proposed GD are shown. The comparison shows that the AGD is better solution than conventional GD.

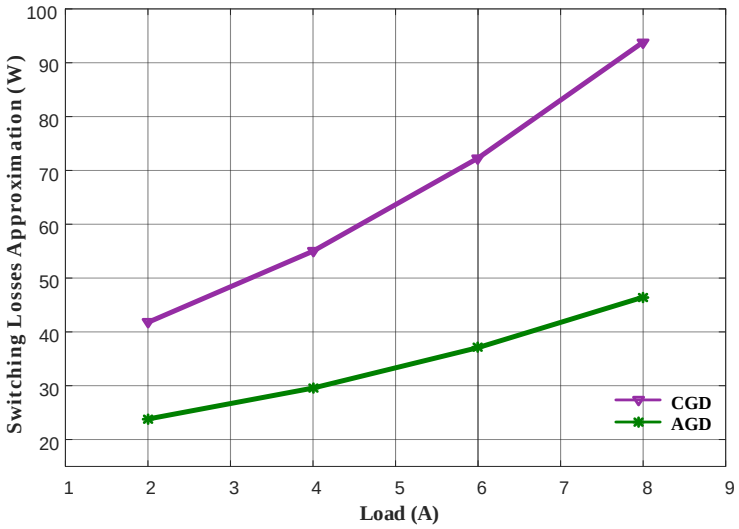

Figure 4.13. Power losses comparison between CGD and proposed AGD under different load current. Switching frequency 100 kHz, 200 V dc-bus, 27 Ω and 22 Ω for turn-on and turn-off respectively for the CGD resistances.

4.3.3 Results discussion

One of the main problems encountered in the design of this GD was the response times that the components need. Most of the components that were used have very short response times in the order of ns. However, the delays caused by the entire feedback loop mean that the proposed AGD is not very effective if these parameters are not considered. Nowadays, there are faster components which can be integrated this type of application and then achieve a driver with better performance. Besides, a method to calculate the time transitions and voltage references should be investigated. In the design of this AGD, the transition times were obtenid by experimentl test and datasheets of the SiC MOSFETs.

4.1 Conclusions

This paper presents an AGD based on multi-stage concept and feedback structure. The study validates the AGD was under experimental tests. The AGD presented is able to reduce the overshoots problems and current and voltage oscillation that can cause EMI problems. The gate driver can reduce the oscillations and the overvoltages and overcurrents. However, the components used by this device have to be very fast to integrate a more efficient system. Another problem that arose during the design of this gate drive is the measurement of the current. Although a very low power resistor was used, the noise that appears in the current measurement signal complicates the design of the gate driver. On the other hand, conventional gates were used for digital devices. Although the algorithm for resistance control is simple, the elements that were used for digital control are very slow, so alternatives are required to program these systems. Then a future work is to develop a digital gate driver applying the developed algorithm and test in different applications.

5

Analysis of the AGD applied on power inverter for Wireless EV charging systems applications

This chapter presents a qualitative evaluation of the AGD proposed in chapter 4. First, a brief analysis of the wireless charging systems and the opportunity to use AGDs in this application is presented. After, the application of the AGD driver in a power inverter with characteristics of wireless charging and qualitative analysis is presented.

CONTENTS:

5.1 A brief analysis of Wireless EV charging systems

The wireless charging systems (WCS) have been widely studied and its advantages and drawbacks have been discussed in the literature for different charging applications [93]–[97]. In spite of the advances and works presented, the costs, the efficiency, power density and reliability remain as challenges in the design and development of WCS [93],[98]. These factors imply the used of new technologies or methods to optimize the systems for covering the requirements concerning the proposed standards, large distances of energy transmission and the energy demanded to achieve short charging times. Consequently, studies and methodologies design have been shown [99]–[103], but the investigations and developments presented are focused on specific charging applications. Moreover, the studies are different due to the requirements between applications, i.e. the power levels, the frequency operation and the type of transmission variate during the WCS design.

Inside the charging systems for electric vehicles (EV), many articles have been presented, but in most of these works, it is developed the analysis and optimization greatly in the transmission coils modelling [104], [103]. Then, the power electronic semiconductor devices even others passive elements are considered superficially in the designs and optimization of charging systems. Few authors have analysed and optimized the WCS considering the power semiconductors effects at high frequency operation and high power.

The importance of considering the power semiconductor devices, its behaviour and techniques such an AGD for improving its performance at high frequency is because the parameters such as power losses and switching frequency are also keys to achieving WCS with high-performance, low cost and high power density. Therefore, the use of WBG semiconductor technologies can improve the design of these systems. Though different semiconductor technologies have been explored for WCS [105]–[107] and GDs circuits have been used in WCS [106], it is important to explore new solutions of gate driver for achieve high efficiency EV charging systems under standard conditions.

5.1.1 Converter topologies for wireless charging systems

All types of topologies have been investigated not only for WCS but else for conductive charging systems [108]. Within the chain of WCS, DC-DC converter is currently the most studied. This converter consists of a full-bridge power inverter, a resonant circuit that has a transformer or transmission coils and compensation capacitors, and also a bridge rectifier. Studies have shown that DC-DC converter topology is the more used structure in WCS for electric vehicles due to advantages such as power output, the number of elements and the cost of its development. Furthermore, because of advantages of the series-series resonant circuit in comparison with other topologies [109]–[111].

In this part, a full-bridge series resonant converter is designed and implemented by using silicon carbide MOSFETs and the AGD presented in chapter 4 is used.

5.1.2 Power devices and technologies for WCS

Power electronics switching devices play an important role in the WCS. The performance of these elements affect the total efficiency of the system and its good operation can guarantee a better design of the wireless chargers. Then, the power devices should be selected considering the characteristics of the system.

Many authors have used different technologies to cover the requirements concerning power and efficiency in WCS for EV. Therefore, several studies and comparisons between different semiconductor technologies such as silicon, silicon carbide (SiC) and gallium nitride (GaN) have been presented [106], [107], [112], [113]. The Fig. 5.1 shows the distribution of the semiconductors used in several works presented about WCS for EV.

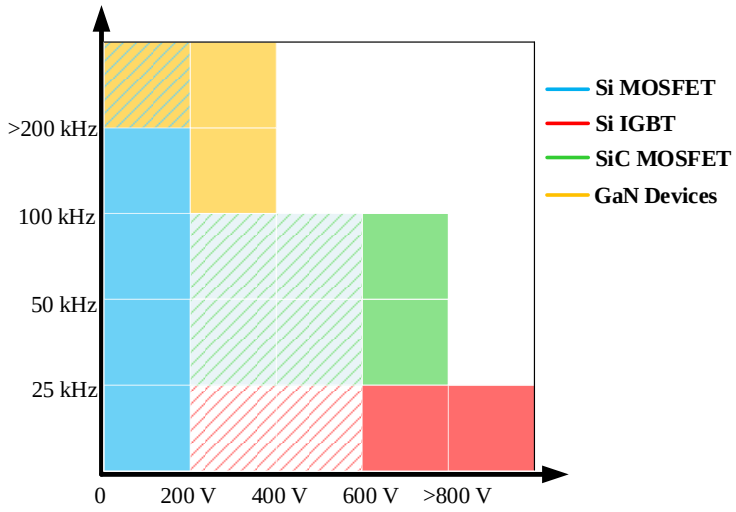

Figure 5.1. Power electronics devices comparison applied in wireless EV charging system.

The distribution shown in Fig. 5.1 was obtained through a comparison between dc-bus voltage and operating frequency used in the designs investigated. The power levels found in the prototypes are around 600 W to 50 kW, meanwhile, the efficiency reached in the prototypes is a range of 80 to 97.4 %. In addition, the Fig. 5.1 shows that the silicon MOSFETs and SiC MOSFETs are the most used in EV chargers conditions so far. It should be noted that the IGBTs are used in high power systems but the frequency is less than 25 kHz. Furthermore, the GaN devices have been used in high-frequency and medium power levels, but these still have been little studied in this application.

Keeping the above in mind, an important consideration is that the power silicon semiconductors can be soon displaced by wide-ban gab devices. Although the silicon MOSFETs are still used in WCS applications, these could not cover the new requirements of WCS designs in EVs, i.e. the operating frequency standard which has been proposed at 85 kHz and power levels required for short charging times in this frequency [93]. Besides, the GaN devices are outlined as the best solution, however, these type of devices continue to be expensive and limited in the marked so far.

5.1.3 Power losses and the importance for using AGDs

The converter efficiency is related to the power losses in components, thermal performance of the integrated circuit, and printed circuit boards, which determines the power effectiveness of the system.

Resonant converters have the advantage of working in soft-switching and these converters can be work in zero-voltage switching (ZVS) or zero-current switching (ZCS), then, the switching losses can be reduced. The soft-switching condition can be achieved either above or below the resonant frequency. However, in WCS the resonant frequency is required to increase the efficiency of the transmission coils and the soft-switching conditions could be not considered. In consequence, the switching losses could be affected by hard-switching conditions[106].

5.2 Power inverter development

The power inverter used for this study is shown in Fig. 3. Based on the models presented in [114] the main parameters of the converter design are presented in Table 5.1.

Table 5.1. Main equation for the resonant inverter used to the evaluation of the AGD

Device	Model
Resonant frequency	$\omega_0 = 1/\sqrt{LC}$
Load quality factor	$Q_L = \omega_0 \cdot L$
Input impedance	$Z_{in} = R_{eq} + j\left(\omega \cdot L_1 - \frac{1}{\omega \cdot C}\right)$
Characteristic impedance	$Z_0 = \sqrt{LC}$
Equivalent resistance	$R_{eq} = 8 \cdot \frac{R_{out}}{\pi^2}$
Resonant thank capacitor	$C_1 = 1/(\omega_0 \cdot Q_L \cdot R)$
Resonant thank inductor	$L_1 = Q_L \cdot R_{eq}/\omega_0$
Output voltage thank	$v_1 = (4 \cdot Vdc/\pi) \cdot \sin \omega t$
Output current thank	$i_1 = v_1/Z_{in}$
Peak current	$I_P = 2 \cdot V_{dc}/R_{eq} \cdot \pi$

The total power losses for the power inverter ($P_{T,inverter}$) can be estimated by (5.1) and the efficiency can be calculated by (5.6).

$$P_{T,inverter} = P_{cond} + P_{sw} + P_{gate} + P_{cond,D} \tag{5.1}$$

where

$$P_{conduction} = 2 \cdot R_{ds,(on)} \cdot I_{p,rms}^2 + \frac{(r_L + r_C) \cdot i_{1,rms}^2}{2}, \tag{5.2}$$

$$P_{switching} = 2 \cdot \left(V_{dc} \cdot I_p \cdot f_{sw} \cdot t_{on}\right) + 2 \cdot \left(V_{dc} \cdot I_p \cdot f_{sw} \cdot t_{off}\right), \tag{5.3}$$

$$P_{gate} = 4 \cdot Q_{g,total} \cdot \left(V_{gg,on} + \left|V_{gg,of}\right|\right) \cdot f_{sw} \tag{5.4}$$

$$P_{conduction,diode} = V_d \cdot I_{p,average} + R_{diode} \cdot I_{p,rms}^2. \tag{5.5}$$

If the output power (P_{out}) is defined, then, considering (5.1), the inverter efficiency can be approximated by (6).

$$\eta_{Inverter} = \frac{P_{out}}{P_{out} + P_{T,inverter}} \tag{5.6}$$

5.3 Experimental analysis of the wireless charging system by using AGD

In consideration of Fig. 5.2 and 5.3 a power losses and efficiency analysis of the power inverter under EV chargers conditions was designed and developed by experimental tests. The parameters used are shown in Table 5.2. In addition, power inverter was configured and a control frequency was used.

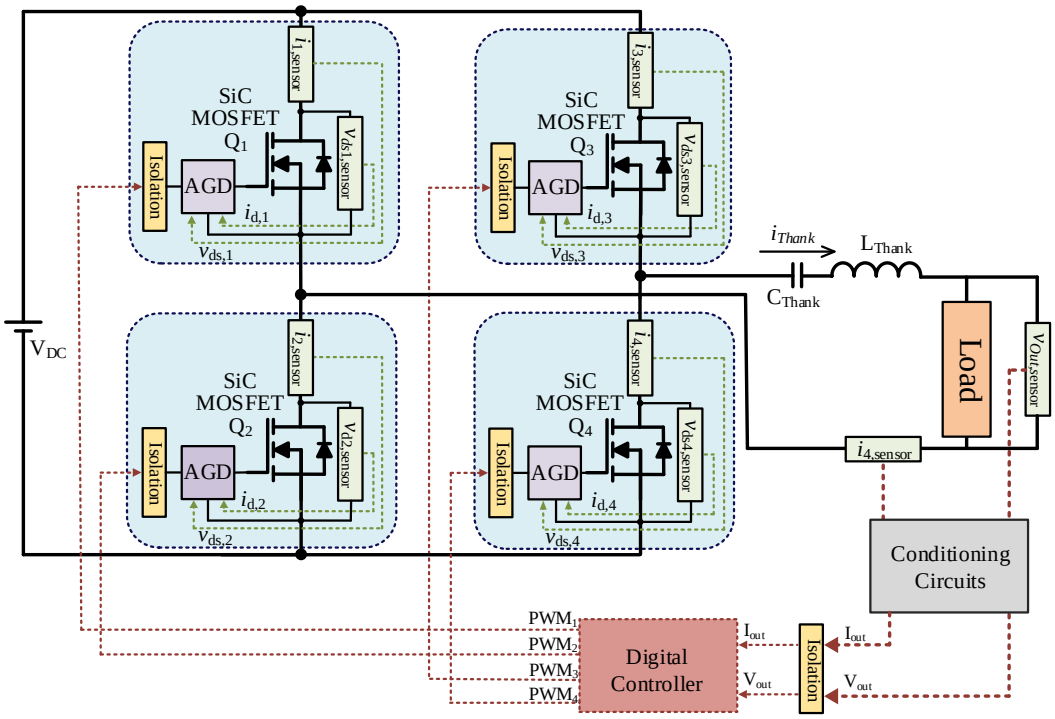

Figure 5.2. Schematic representation of power inverter used to evaluate the AGD.

Table 5.2. General parameter of the system for evaluations

Parameter	Name of parameter	Value
V_{dc}	DC-Bus	200 V
P_N	Nominal power	2 kW
Fr	Resonant frequency	85 kHz
L1	Resonant thank inductor	92 µH
C_1	Resonant thank capacitor	20 nF

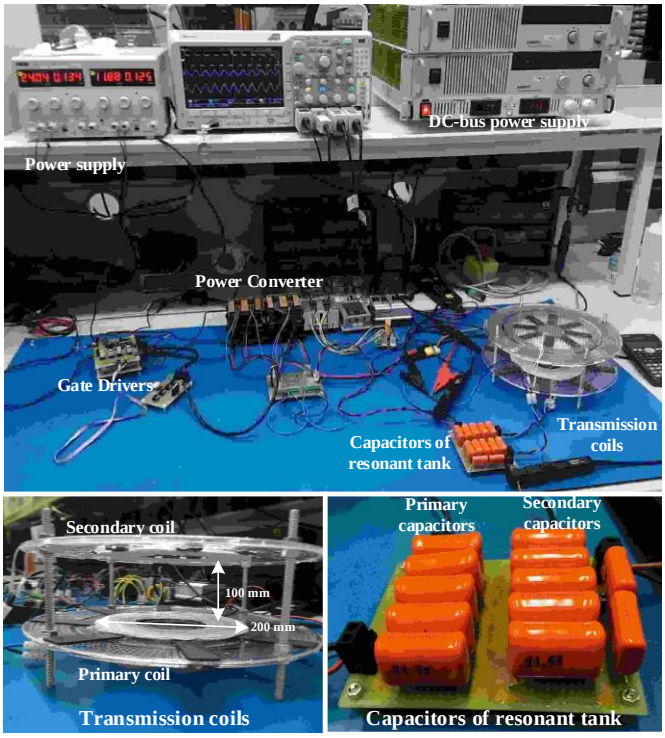

Figure 5.3. Test bench and prototypes, only primary coil was used in this evaluation.

5.3.1 General study of the behaviour of the system

In the first stage of the experimental analysis using the AGD, a comparison of the output signals with different gate resistances was developed. The purpose of this comparison is for demonstrating the effects of switching devices on operating frequency proposed in WCS for EVs. In addition, to exhibiting the contrast of the efficiency for small and large values. Therefore, a SiC MOSFET SCT2080KE by Rhom semiconductor was selected and the results are shown in Fig. 5.4 and Fig. 5.5. On the one side, the gate resistance was considered in a minimum value of 6.3 Ω which was taken from the datasheet. In the other part, the second gate resistance was selected considering the model of the chapter 2.

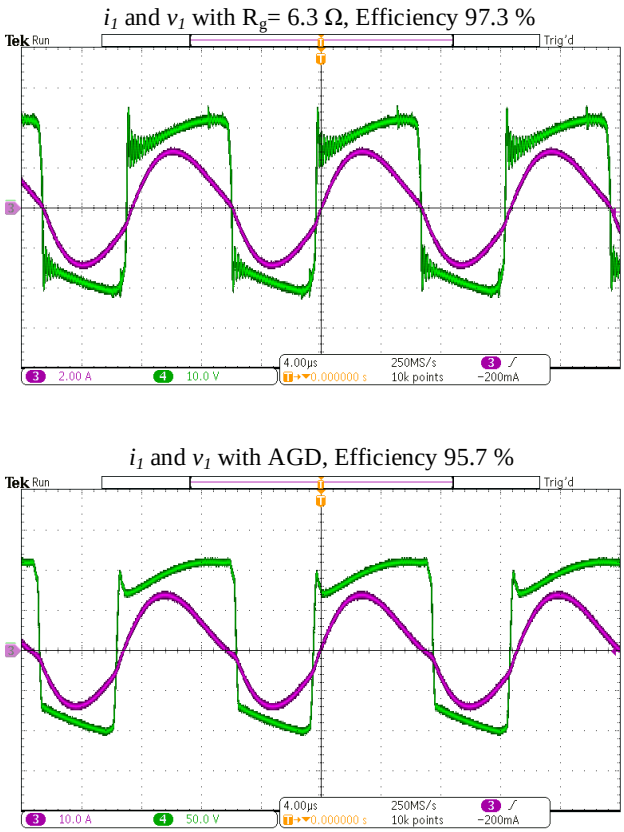

Figure 5.4. Current and voltage output waveforms of the resonant inverter with R_g=6.3 Ω and R_g=33 Ω at 85 kHz, 200 V of DC-bus and power 2 kW.

The results showed that the efficiency changes of 97.9 % to 93.5% with large gate resistor, but, the voltage and current waveforms have less noise and fewer overshoots. Hence, the adequate calculation of the gate resistance is necessary for the power semiconductor selection.

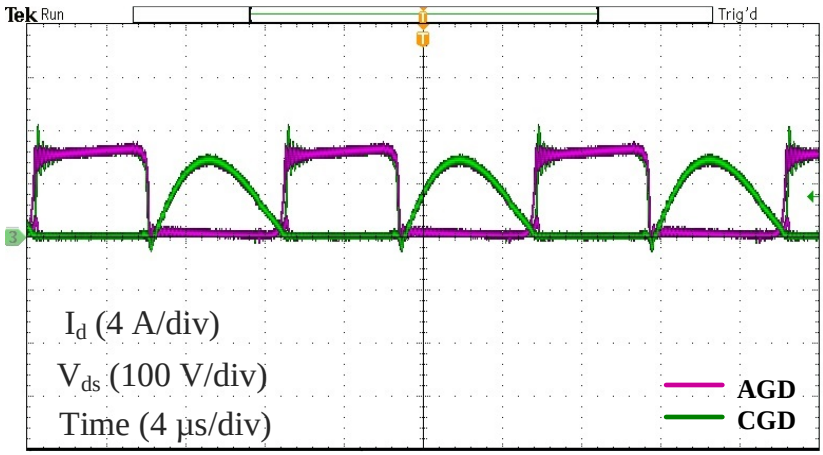

Figure 5.5. Current and voltage output waveforms of the resonant inverter with AGD and CGD with R_g=6 Ω at 85 kHz, 200 V of DC-bus and power 2 kW. Resonant converter working for above of the resonant frequency.

5.3.2 Power losses analysis

Resonant inverters have the property to work in soft-switching conditions. This characteristics help to increase the efficiency of the system because allows reduce the switching losses in power devices. Soft-switching can be achieved either above or below of the resonant frequency. For the operation for above resonance, turn-on switching loss is zero, but there is a turn-off switching loss. Fig. 5.6 shows a comparison of power losses in a SiC MOSFET between CGD and GD when the power inverter is operating above the frequency resonance. Fig 5.7 shows a power losses shows a comparison of the total power losses.

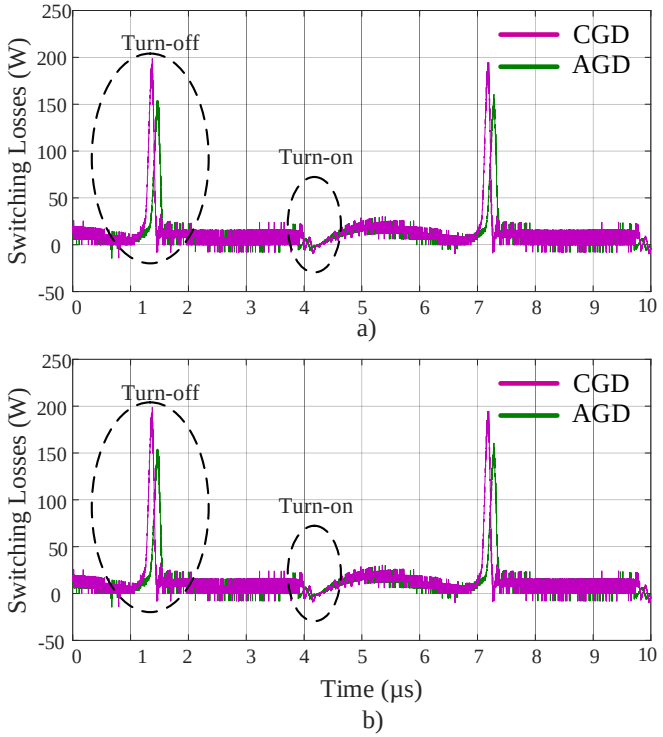

Figure 5.6. A comparison example of power losses for one SiC MOSFETs by using AGD and conventional GD with large gate resistance of 33 Ω.

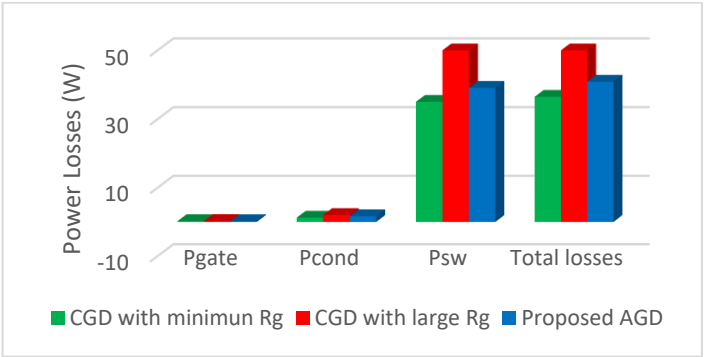

Figure 5.7. Power losses comparison of the SiC MOSFETS between AGD and conventional gate driver applied in the resonant power inverter 2 kW.

5.4 Conclusions

An inverter was designed for wireless charging conditions and the gate driver designed in Chapter 4 was used. As you can see, the gate driver can reduce the occlusions in the transient lines and can increase the efficiency of the converter in conjunction with soft-switching. . The purpose of this work was only to determine the behaviour of the AGD and observe how it affects efficiency. A subsequent work will be to implement the entire wireless charging system and conduct a study of the behaviour of the WCS using different types of control.

6

Overall conclusions and future works

General conclusions about the thesis project are presented in this section according to the approach the problem, hypotheses and objectives. In addition, future works are presented as well.

CONTENTS:

6.1 Thesis conclusions

With the project investigation realized, some global conclusions can be listed regarding the results obtained as follow:

- An analysis of WBG devices has been carried out. According to the literature, silicon carbide is a mature technology that has taken an interest in the development of power efficiency systems. On the other hand, the GaN is a technology that is gaining popularity but especially for low power and low voltage applications. In this sense, silicon carbide is profiled to meet the requirements of power converter designs in current applications.

- Although silicon carbide has advantages that allow high power density and high-efficiency power, there are challenges that need to be faced to take advantage of silicon carbide. One of the main problems of silicon carbide, when it works in high frequency, is the generation of overshoots and oscillations that can cause EMIs. In this sense, it was demonstrated that active gate drivers are fundamental for the design of silicon carbide-based converters.

- Based on studies of the state-of-the-art, two-stage gate drivers were designed. In the first stage, a multi-stage gate driver was designed based on the status feedback concept. The results showed that AGDs can reduce and eliminate oscillatory currents and even eliminate over-voltages. The main drawback of the first designed driver is that it does not consider load variations or temperature variations. In addition, it must be used for a specific application and load.

- In a second stage, a gate drive based on status feedback was designed but measuring the voltages and currents of the SiC MOSFET. The designed gate driver can reduce high-frequency oscillations and can reduce voltage overshoots. Although the gate driver has shown good results, the main drawback is the used of elements to the control. The majority of the circuits have a very fast response, however, when considering the delays of all of them, the driver may not be efficient.

- Finally, an inverter for wireless charging system was designed and the AGD designed in Chapter 4 was connected and system evaluations were carried out. The driver can eliminate oscillations and over-voltages and helps increase the efficiency of the entire system.

6.2 Future works

High-performance gate driver has been developed and it has been shown that they can eliminate the main problems that occur when SiC devices work at high speeds. However, future works derived from this thesis can be carried out and are described below:

- The designed drivers have good performance and do not affect the efficiency of the systems. However, future work is to improve the digital control of the AGD. It is also essential to improve and study the current and voltage sensing since high switching speeds limit current measurements and cause delays and noise.

- Designed drivers do not include protections. Therefore, it is interesting to create a system that integrates overvoltage and overcurrent protection.

- The gate driver has been tested on a resonant inverter for wireless charging applications. However, as future work, it is really interesting to study how the wireless charging system acts under different conditions and control.

- In addition, a comparison of different technologies can be realized and the impact of WBG devices and AGDs could be studied.

7

Thesis results disseminations

This chapter presents the international journals publications and international conferences resulting directly of this research investigation. In addition, publications in international conferences and international journals resulting in collaboration with investigations related to this work.

CONTENTS:

7.1 Derived publications from this thesis work

7.1.1 Journal papers

Alejandro Paredes, V. Sala, H. Ghorbani and J. L. R. Martinez, "A Novel Active Gate Driver for Improving SiC MOSFET Switching Trajectory," in IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 9032-9042, Nov. 2017. doi: 10.1109/TIE.2017.2719603

Impact factor: 7.503

Alejandro Paredes, V. Sala and L. Romeral, "Advanced Gate Driver for Switching Performance Enhancement of SiC MOSFET devices," **In preparation**.

Alejandro Paredes, V. Sala, L. Romeral, "Analysis of a simple active gate driver and simple control for improving the efficiency of high-frequency power converters" **In preparation**.

7.1.2 Conference papers

A. Paredes, V. Sala, H. Ghorbani and L. Romeral, "A novel active gate driver for silicon carbide MOSFET," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, Italy, 23-26 Oct. 2016, pp. 3172-3177. doi: 10.1109/IECON.2016.7793222

A. Paredes, H. Ghorbani, V. Sala, E. Fernandez and L. Romeral, "A new active gate driver for improving the switching performance of SiC MOSFET," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 3557-3563. doi: 10.1109/APEC.2017.7931208

A. Paredes, V. Sala, E. Fernández and L. Romeral, "Performance analysis of switching devices for wireless EV charging systems," 19th IEEE International Conference on Industrial Technology (ICIT), Lyon, Francia, 2018, pp. 794-799. doi: 10.1109/ICIT.2018.8352279

A. Paredes, E. Fernández, V. Sala and L. Romeral, "Switching trajectory improvement of SiC MOSFET devices using a feedback gate driver," 19th IEEE International Conference on Industrial Technology (ICIT), Lyon, Francia, 2018, pp. 847-852. doi: 10.1109/ICIT.2018.8352288

7.2 Resulting publications from additional collaboration related with this work

7.2.1 Journal papers

H. Ghorbani, V. Sala, **A. Paredes**, and L. Romeral, “A Simple Closed-Loop Active Gate Driver for controlling di/dt and dvCE/dt in IGBTs,” Energies, Method for Reducing THD and Improving the Efficiency in CSI Topology Based on SiC Power Devices,” Electronics, vol. 8, no. 2. 2019. doi: 10.3390/electronics8020144

E. Fernández, **A. Paredes**, V. Sala, and L. Romeral, “A Simple Method for Reducing THD and Improving the Efficiency in CSI Topology Based on SiC Power Devices,” Energies, vol. 11, no. 10. 2018. doi: 10.3390/en11102798

H. Ghorbani, V. Sala, **A. Paredes**, L. Romeral, Embedding a feedforward controller into the IGBT gate driver for turn-on transient improvement, Microelectronics Reliability, Volume 80, 2018, Pages 230-240. https://doi.org/10.1016/j.microrel.2017.12.008.

E. Fernandez, **A. Paredes**, V. Sala and L. Romeral, "Control and Modulation Techniques Applied to converters with impedances networks for traction systems," in IEEE Latin America Transactions, vol. 15, no. 1, pp. 21-30, Jan. 2017. ISSN: 1548-0992, ISSN: 1548-0992, doi: 10.1109/TLA.2017.7827884

7.2.2 Conference papers

E. Fernández, V. Sala, **A. Paredes** and L. Romeral, "Method to reduce THD and improve efficiency in SiC power converter," 19th IEEE International Conference on Industrial Technology (ICIT), Lyon, Francia, 2018, pp. 753-758. doi: 10.1109/ICIT.2018.8352272

H. Ghorbani, V. Sala, **A. Paredes** and J. L. Romeral, "A simple gate drive for SiC MOSFET with switching transient improvement," 2017 IEEE Industry Applications Society Annual Meeting, Cincinnati, OH, 2017, pp. 1-6. doi: 10.1109/IAS.2017.8101762

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