Cell drop threshold architecture for multi-class shared buffer with finite memory size

ABSTRACT

Shared buffer is commonly used to utilize the buffer in the switch. In order to minimize the cell lost of high class traffic in multi-class switch, the threshold is set to drop the low class cells in the shared buffer. This will give more space to accommodate the high class traffic cells. In this paper, we analyse the performance of shared buffer with different threshold settings. The multi-class shared buffer architecture is developed for 16x16 ports switch, which is targeted for Xilinx FPGA implementation. The performance of the multi-class shared buffer switch is analysed in term of the achievable throughput as well as the drop probability. Based on the simulation with different threshold settings, it is observed that the optimum selection of cell drop threshold depends on the size of the shared buffer that triggers the RAM threshold.

Keyword: Shared buffer; Multi-class; Cell drop threshold; Architecture design