THERMAL AND FLICKER NOISE ANALYSIS IN SAMPLE AND HOLD CIRCUIT

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By

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LIST OF ABBEREVIATIONS

AC	Alternative Currrent
ADC	Analog Digital Conveter
BJT	Bipolar Junction Transistor
CDS	Correlated-Double Sample-And-Hold
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide Semiconductor
CSA	Pre-Amplifier
DC	Direct Current
EDA	Electronic Design Automation
EMI	Radiated Emission
FC	Folded Cascode
JFET	Junction Field Effect Transistor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
OTA	Operational Transconductance Amplifier
RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal To Noise Ratio

LIST OF SYMBOLS

A_v	Total Gain
C	Capacitor Value
C_f	Frequency Capacitance
Cf	Feedback Capacitor
C_{ox}	Gate Oxide Capacitance Per Unit Area
Cs	Sampling Capacitance
E_n	Pwer Desity Voltage
f	Frequency
f_{max}	Maximum Frequency
f_{min}	Minimum Frequency
g_m	Transconductance Parameter
I_n	Power Density Current
Ipp	Current Peak-To-Peak
k	Boltzman Constant
K_e	Constant Voltage
K_f	Flicker Noise Coefficient
K_i	Constant Current
L	Lenth
q	Charge
R	Resistor Value
R_{on}	Resistance Of Sampling Switch
R_{out}	Output Resistor Value

$R_{thermal}$	Thermal Resistor
S	Switch
T	Temperature
Vc	Capacitance Voltage
Vpp	Voltage Peak-To-Peak
W	Width
Δf	Bandwidth

HINGAR HABA DAN HINGAR KERLIPAN ANALYSIS DALAM LITAR SAMPEL DAN PEGANG

ABSTRAK

Dalam aplikasi frekuensi rendah, hingar menjadi isu apabila saiz MOS dikurangkan. Oleh itu, hingar kerlipan dan hingar haba adalah salah satu isu yang terdapat dalam aplikasi frekuensi rendah . Dalam projek ini, hingar kerlipan dan hingar haba diukur pada litar sampel-dan-pegang, yang direka berdasarkan sepenuhnya dengan litar Cascode Pengamiran Sepenuh dengan Mod Suapbalik. Analysis hingar haba dan hingar kerlipan juga dijalankan dengan mengubah nilai kapasitor dan saiz transistor dalam litar sampel-dan-pegang. Dalam analisis hingar haba, SNR maksimum yang diukur adalah -120.28dB dengan 0.642uV/√Hz hingar haba masuk dan saiz transistor yang digunakan pada NMOS adalah 8µm . Selain itu, SNR maksimum yang diperolehi bagi hingar kerlipan adalah -83.27dB untuk hingar masuk 1uA dengan kapasitor nilai 0.5pF yang diukur pada frekuensi 1Hz dalam litar sampel-dan tegang.

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ABSTRACT

In low-frequency applications, noise is becoming more of an issue as the MOS size reduced. Therefore, the flicker noise and thermal noise are one of the issues found in low-frequency applications. In this work, the thermal noise and flicker noise are modelled and measured on the sample-and-hold circuit, based on Fully Differential Folded Cascode with Common Mode Feedback. The thermal noise analysis and flicker noise analysis are performed by varying the capacitance value and transistor sizes in the sample-and-hold circuit. In thermal noise analysis, the maximum output SNR measured is -120.28dB with 0.642uV/√Hz input thermal noise and transistor size for NMOS is set to 8µm. The maximum output SNR obtained for flicker noise is -83.27dB for 1uA input noise with low capacitance value 0.5pF and is measured at 1Hz frequency in sample-and-hold circuit.

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Nowadays, many electronic applications are using digital signal processing for high frequency example like sensors circuit, amplifier circuit, etc. In order to operate in digital domain, the analog signals are converted using analog to digital converter (ADC). Since, the ADC circuits used in many applications, the circuits are demanding to obtain for low power and low noise. To achieve low power and low noise in ADC circuit, one of the block contributes was the sample-and-hold circuit. To perform the ADC conversion, the sample-and-hold circuit function is to hold the analog signals for some periods. To get very accurate ADC output, the sample-and-hold circuit must be a high performance circuit.

The challenges faced to obtain high performance sample-and-hold circuit are linearity, gain, power, and noise. Therefore, the architecture of circuit is one of the main reason to achieve the high performance in sample-and-hold circuit. Most commonly architectures used to design the sample-and-hold circuit were charged-transferring design and flip-around design. Therefore, the designs have disadvantage and advantage, but for this work the sample and hold circuit was design based on mixture of two structure of sample-and-hold circuit. This architecture helped to reduce the linearity, power and the internal noise.

Furthermore, another circuit was used know as Fully Differential Folded Cascode with Common Mode Feedback operational amplifier (FC OTA with CMFB) to design the sample-and-hold circuit. Fully Differential Folded Cascode is a transconductance amplifier (OTA) design. To maintain the output voltage of this OTA circuit, another circuit helped was Common Mode Feedback circuit. In the OTA design there are several problem expected especially in gain bandwidth and the power. However, this problem solved by designed by stable OTA with expected gain and phase margin. The performance for OTA design measured at settling time, gain-bandwidth, and slew rate. Since, the OTA designed focused on the linearity and settling time, gain-bandwidth, the slew rate are not consider [15]

The sample-and-hold circuit can design as low power circuit but not for low noise. The representations of the noise in the sample-and-hold circuit are the electrical noise and current noise. There are few type of noises can be evaluated from the sample-and-hold circuits which is noise generated by the random variation of charges in the wire and device (thermal noise, flicker noise or shot noise). Another type of noise is quantization noise also produce from the signal are converted from analog to digital and another type of noise is coupled noise due to device signals feeding into each other and interfacing [16]. In this work, the noise analysis were focused on noise resulting from random movement charges on device and wires, known as thermal noise and flicker noise . The purpose of this work was identified the thermal and flickers noise in sample-and-hold circuit.

Thermal noise is an effect of random movement of electron due to temperature, also known as Johnson noise. This thermal noise produced from the internal device CMOS or the external inputs signal to the circuit. Besides, flicker noise known as 1/f noise produced when low frequency input and the internal devices in circuit. In addition, noise source from the output signal known as white noise also contributes to the flicker noise measurement in sample-and-hold circuit. In this work, there are two noise model were designed using Verilog-A. The noise models designed are white noise model used to measure the flicker noise in sample-and-hold circuit, and another noise model was thermal noise model used to measure the thermal noise in circuit.

1.2 PROBLEM STATEMENT

Sample-and-hold circuit is commonly use in ADC circuit. There are several disadvantages are found in ADC circuit, which are convert the low voltage signal and low frequency example like used in sensor application etc. The low voltage signals and low frequency produce two types of noises in circuit, which are thermal noise and flicker noise. These two types of noise effect the quality of the ADC. The thermal noise produced from the thermal effect on input signal and devices in the circuit. The flicker noise produced due to unstable signal flow with noise into the circuit. Since the sample-and-hold circuit used in ADC, the noise analysis was conducted on the sample-and-hold circuit, and measure the effect.

1.3 OBJECTIVE OF RESEARCH

i. To build thermal noise model and flicker noise model using Verilog-A.

ii. Analyze and measure the effect of the thermal and flicker noise on the sample-and-hold circuit.

iii. To measure the thermal noise and flicker noise effect by varying the capacitance value on the sample and hold circuit.

iv. To analyze the thermal noise and flicker noise effect by varying the transistor width size on the sample and hold circuit.

1.4 SCOPE OF RESEARCH

The scope of research was to analyze the thermal noise and flicker noise effect on the sample-and-hold circuit. As a preliminary study, the characteristic of thermal noise and flicker noise was identified from the noise impact on circuit. Besides, the noise analysis also conducted by varying the transistor size width and capacitance value in the sample-and-hold circuit. Furthermore, the proposed the sample-and-hold circuit was designed using 0.13um Silterra technology in Cadence IC 5 schematic editor.

1.5 RESEARCH CONTRIBUTION

From the research the contributions are:

i. Methods to analyze the flicker noise and thermal noise circuit by using the designed input noise models.
ii. Study on design of thermal noise and flicker noise model
iii. Determine impact based on the noise models in sample-and-hold circuit.

1.6 THESIS OVERVIEW

Chapter 2 discussed on the past year publications paper also known as literature study. This chapter also explained more on the characteristic of flicker noise and thermal noise and the method used to design the noise analysis research. Besides, this chapter also discussed on the different type of sample-and-hold circuit and the noise analysis.

Chapter 3 was described the methods used to noise model and design of sample-and-hold circuit. This chapter also discussed on the OTA design, which is the Fully Differential Folded Cascode Operational Amplifier with Common Mode Feedback circuit.

Chapter 4 shows the results and discussion based on the flicker noise and thermal noise analysis on the sample-and-hold circuit. Furthermore, also discussed the effect of the flicker noise and thermal noise on the circuit.

Chapter 5 has summary of the studies on the flicker noise and thermal noise effect on the sample-and-hold circuit. Moreover, the improvement and suggestion for further study on noise also included in this chapter.

1.7 SUMMARY

This chapter has discussed about the overview of this work on the analysis of the thermal noise and flicker noise and the sample-and-hold circuit, main four objectives of this project, problems intended to do this research and contribution from this project. Lastly, this chapter has a conclusion of the first four chapters to summarize this thesis.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

This this chapter discussed the flicker and thermal noise analysis on the circuit that have used by researchers. Besides, this chapter also discussed the methodologies used by other paper to design the sample-and-hold circuit. This chapter also explained the problem and challenges from previous journals on designing the sample-and-hold circuit. There is three topics were discussed which is flicker noise, thermal noise, and sample-and-hold circuit.

2.2 FLICKER NOISE

Most of the electronic circuits produce noises either in voltage noise or in current noise. Usually, the noise measured in frequency domain signals because the input signals are in the sinusoidal waveform. The sinusoidal signals cause noise inside the circuit and it is difficult to measure in current signal form or in the voltage signal. This is also known as random electrical noise across the circuitry however, those random noises generated by the component of the circuit, hence the effect of random noise is smaller than other type noise. Besides, the random noise causes other types of noise, which neglected in the design of electronic circuit. The other types of noise are micro-phonic effect due to system vibration, various source of radiated emission pickup (EMI), high narrowband noise due to parasitic oscillation, and noise through power supply.