NUMERICAL ANALYSIS DURING ENCAPSULATION PROCESS OF MOLDED UNDERFILL WITH MULTI FLIP CHIP PACKAGE

MUHAMMAD AFIQ BIN AZMI

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by

MUHAMMAD AFIQ BIN AZMI

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MUF	Molded Underfill	xiii
VOF	Volume of Fluid	xiii
EMC	Epoxy Molding Comppound	xiii
THM	Through-Hole Mount package	1
SMT	Surface Mount Package	1
FCBGA	Flip Chip Ball Grid Arrays	2
WBGA	Wire Bond Ball Grid Arrays	2
CUF	Capillary Underfill	3
NUF	No-flow Underfill	3
CAE	Computer-Aided Engineering	6
FEA	Finite Element Analysis	6
CFD	Computational Fluid Dynamics	6
MBD	Multibody Dynamics	6
FDM	Finite Different Method	6
FEM	Finite Element Method	6
FVM	Finite Volume Method	6
TQFP	Thin Quad Flat Package	10
TSOP	Thin Profile Small Outline Package	10

MAP	Mold array Package	10
S-CSP	Stacked-Chip Scale Package	10
CTE	Coefficient of Thermal Expansion	11
PUF	Pressurize Underfill	12
GNF	Generalized Newtonian Fluid	18
ICM	Injection Compression Molding	20
CIM	Conventioanal Injection Molding	20
EWLP	Embedded Wafer Level Package	20
PBGA	Plastic Ball Grid Array	21
TSV	Through Silicon Via	21
FSI	Fluid/Structure Interaction	22
DMA	Dynamic Mechanical Analysis	23
RTM	Resin Transfer Molding	23
CAD	Computer Assisted Design	24
PP	Polypropene	28
FCR	Flip Chip Region	64
FPR	Flip Passage Region	64
FCP	First Collision Point	102

LIST OF SYMBOLS

T_g	Glass transition temperature
V	Velocity vector
u	Fluid velocity component in x-direction
v	Fluid velocity component in y-direction
w	Fluid velocity component in z-direction
P	Pressure
T	Temperature
c_p	Specific Heat
k	Thermal Conductivity
ΔH	Exothermic heat
K	Flow consistency index
n	Power Law index
B	Exponential fitted constant
T_b	Temperature fitted constant
c_1	Fitting Constant
c_2	Fitting Constant
F	Front advancement parameter
T_{m}	Mold Temperature
T_{in}	Temperature at inlet
(x, y, z)	Cartesian coordinates

ρ	Density
η	Viscosity
$\dot{\gamma}$	Shear rate
$\dot{\alpha}$	Conversion rate
η_o	Zero shear rate viscosity
τ^*	A parameter that describes the transition region between power law region and zero shear rate of the viscosity curve
α	Degree of Conversion

ANALISIS BERANGKA SEMASA PROSES PENGKAPSULAN DALAM ACUAN ISIAN BAWAH DENGAN PEMPAKEJAN FLIP CIP BERGANDA

ABSTRAK

Pada masa kini, teknologi pembungkusan litar bersepadu (IC) menjadi reka bentuk yang canggih di samping dapat mengekalkan kebolehpercayaan dan kualiti. Pakej skala cip flip (CSP) adalah salah satu daripada cip IC yang mempunyai wafer-tingkat yang dibungkus dengan bebola pateri sfera yang terletak di atas grid yang mana jaraknya telah ditentukan di antara cip. Untuk membungkusnya, acuan isian bawah (MUF) telah digunakan dan ia merupakan proses yang lebih mudah dan lebih cepat. Walau bagaimanapun, aliran sebatian acuan epoksi (EMC) yang tidak konsisten semasa pengkapsulan yang lebih mudah terdedah kepada corak pengisian yang tidak seimbang, pengisian tidak lengkap dan kekosongan dalaman. Kerana itu, proses pengisian dan aliran EMC melalui flip cip sangat sukar untuk digambarkan dengan eksperimen sebenar. Dalam kajian ini, pendekatan berangka telah digunakan untuk mengkaji proses pembungkusan flip cip dalam rerongga. Oleh itu, analisis berangka adalah pendekatan yang sesuai untuk digambarkan semasa proses pembungkusannya. Perisisan ANSYS FLUENT pula telah digunakan untuk mensimulasi dan menganalisis fenomena aliran cecair dan akibatnya. Teknik jumlah cecair (VOF) telah digunakan untuk menvisualisasi aliran MUF di rongga kosong dan cip flip yg berganda telah dibentangkan. Kajian terhadap tingkah laku aliran EMC dalam model rheologi yang berbeza juga telah dijalankan. Model Castro Macosko telah dikenal pasti sebagai model reologi yang terbaik untuk mempelajari perilaku aliran kerana ia telah mempertimbangkan kesan pengawetan dan tahap penukaran. Analisis berangka diteruskan pada kesan susunan flip cip. Susunan

berganda tiga cip flip mempunyai aliran pengurangan yang lebih tinggi dan peratusan jumlah udara terbentuk terbesar semasa pembungkusan. Hubungan kesan rheologi ke atas reka bentuk flip cip telah dikaji dengan sewajarnya. Perubahan kesan rheologi dan reka bentuk susun telah mempengaruhi sifat-sifat EMC seperti halaju, kadar ricih dan kelikatan.

NUMERICAL ANALYSIS DURING ECAPSULATION PROCESS OF MOLDED UNDERFILL WITH MULTI FLIP CHIP PACKAGE

ABSTRACT

Nowadays, the technology of Integrated Circuit (IC) packaging has become a sophisticated design in addition to maintaining reliability and quality. Flip Chip Scale Package (CSP) is one of the IC chips which has a wafer-level packaged with spherical solder bump located on a grid with a pre-defined pitch between chip. In order to package it, Molded Underfill (MUF) was used which was an easier and faster process. However, the inconsistent flow of Epoxy Molding Compound (EMC) during encapsulation was more susceptible to unbalanced filling pattern, incomplete filling and internal void. Therefore, the EMC filling and flow through flip chip is very hard to visualize with actual experiment. In this study, the numerical approaches were used to study the encapsulation process of multi flip chip in the cavity. Thus, the numerical analysis is an appropriate approach to visualize during the encapsulation process. ANSYS FLUENT was used to simulate and analyze the fluid flow phenomena and consequences. The volume of fluid (VOF) technique was used for visualization of flow front. The flow visualization of MUF in the empty cavity and multi flip chip were presented. The flow behavior of EMC in different rheology models have been conducted. The Castro Macosko model has been identified as the best model to study flow behavior since it has considered the curing effect and degree of conversion. The numerical analysis is continued on stacking effect of flip chip. Triple stacked multi flip chip was found to have high retardation flow and large volume percentage during encapsulation. The relationship of rheological effect on stacking design of flip chip were studied accordingly. Changes in rheological effect

and stacking design have influenced the EMC properties such as velocity, shear rate and viscosity.

CHAPTER ONE

INTRODUCTION

1.1 Overview of Integrated Circuit Packaging

Integrated Circuit (IC) packaging is a final manufacturing process of semiconductor device which encapsulated with semiconducting material in order to prevent from physical damage. Higher demand by electronic industries for IC package in order to get high performance required a great design to maintain its reliability and quality of electronic devices (Wan et al., 2007). Development of IC package is dynamic technology that always need an improvement in design and has multi function. There are many types of IC package have been produce to fill the industrial needs.

IC package can be categorised into three type of packages, which are through-hole mount package (THM), surface mount package (SMT) and chip scale package (CSP). Figure 1.1 shows the trend of IC package change from through-hole mount package to chip scale package (Anon, 2001). The design of IC package evolve from large design to smaller design and the evolution of their trend also grow same as the technology devices nowadays. Recently, CSP become one of the popular IC package because of its trend toward smaller, lighter and thinner where it meets application's demand (Khor & Abdullah, 2013). The combination of its performance and its small size make it become ideal solution for electronic manufacturing.

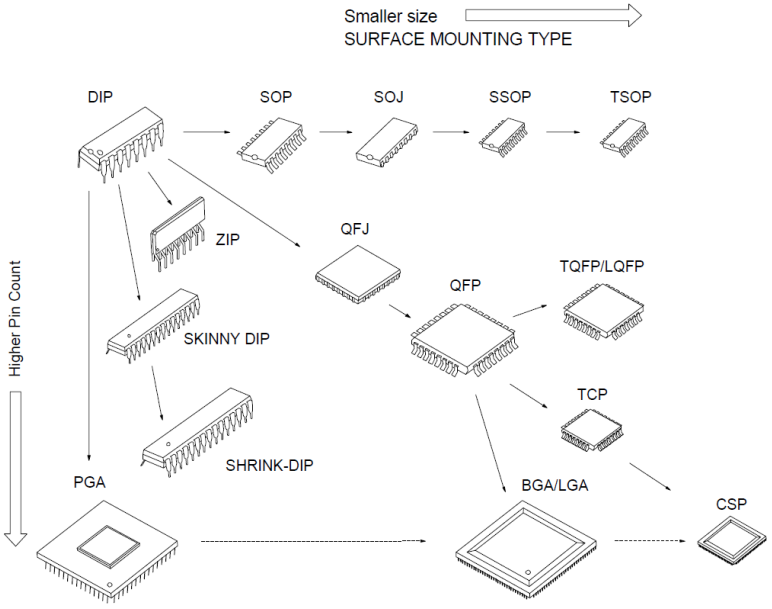


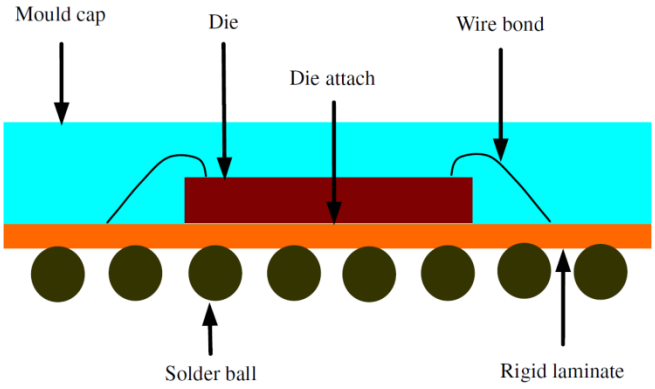
Figure 1.1 : Trend of IC Package (Anon, 2001)

CSP is a single die which its package is 1.2 times the size of the die and it is is an evolution of surface mount package. There are many types of CSP and the most popular in CSP are flip chip ball grid arrays (FCBGA) and wire bond ball grid arrays (WBGA). Figure 1.2 (a) shows the cross section of WBGA and it consist of the interconnection between substrate and die using wire. The die attach directly to the substrate and the active surface of the die face upward, then its looped and bonded to the substrate. Since the current trend to get smaller and higher input/output, it can be one of the challenging to the electronic industry. It needs more wire to be bond in the package. Hence, the industry will face a production problem and increase the cost.

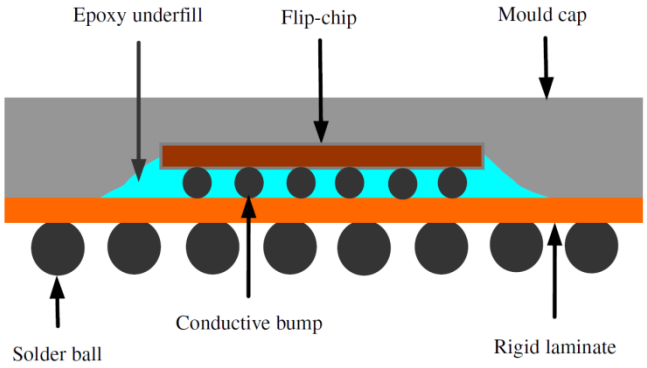
The flip chip technology is introduced to tackle this problem by the die is connected to subtrate with conductive bump (Wan et al., 2007). Figure 1.2 (b) shows the cross section of FCBGA package where the interconnection between chip and

subtrate by solder bump. The active surface of chip is flipped and attached to the solder bump, which is attached to the subtrate.

In flip chip technology, the gap between substrate and chip is underfilled with highly filled epoxy system. Underfill is one of important part in flip chip package where it provides a good reliability and quality. It can be classified into capillary underfill (CUF), no-flow underfill (NUF) and molded underfill (MUF) (Wong & Wong, 1999; Joshi et al., 2010).



(a)



(b)

Figure 1.2: (a) WBGA (b) FCBGA (Wan et al., 2007)

1.2 Molded Underfill of Flip Chip Package

Molded underfill (MUF) is a process used in IC packaging to fill the gap between the chip and subtrate, and encapsulate the whole chip (over molding). Figure 1.3 shows the cross section of single MUF of flip chip package. Increased functionality requirement and advance in packaging technology made MUF is the right choice for alteration of flip chip design. The advantages of using MUF are lower material cost, save time production and provide excellent reliability for advanced electronic application (Chen et al., 2013). Besides that, MUF process is simple and faster compared to CUF (Joshi et al., 2010). Epoxy Mold Compound (EMC) is a solid epoxy based resin with fillers that has been used as a molded underfill material for encapsulation in order to protect the die and the solder bump from the stress and temperature effect (Khor et al., 2011). Figure 1.4 show EMC flow through the flip chip package during encapsulation process.

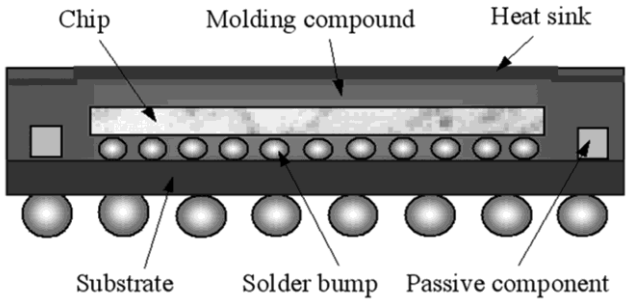


Figure 1.3: Cross section of Single Molded Underfill of Flip Chip Package (Chen, 2008)